mosaic

Mosaic Semiconductor Inc.

1M x 1 Monolithic CMOS DRAM

MDM11001-T/V/VX/G/J

Issue 2.0 : September 1992

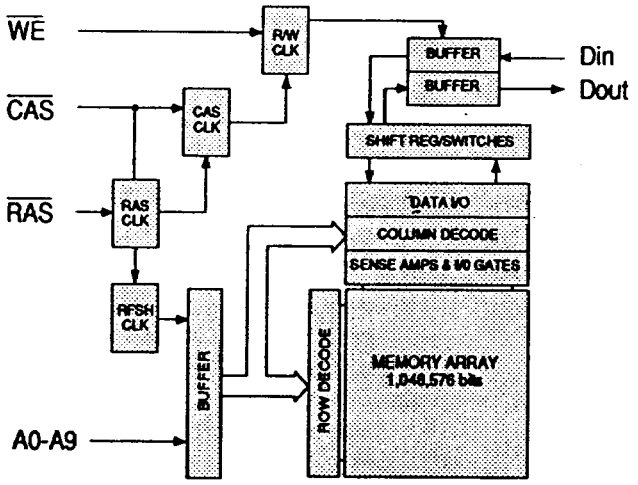
PRELIMINARY

1,048,576 x 1 CMOS High Speed Dynamic RAM

Features

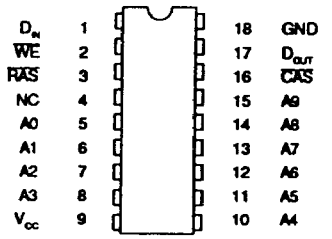
- Row Access Times of 80/100/120 ns
- High Density 300mil DIP and 100mil VIL
- Surface Mount 20 pin SOJ & 20 pin FlatPack
- 5 Volt Supply ± 10%
- 512 Refresh Cycles (8 ms)
- $\overline{CAS}$ before $\overline{RAS}$ Refresh
- $\overline{RAS}$ only Refresh
- Hidden Refresh
- Nibble Mode Capability
- Can Be Processed to MIL-STD 883D

Block Diagram

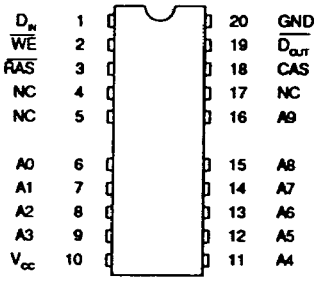


Pin Definition

Package Type: 'T','V','G'



Package Type: 'J'



Pin Functions

A0-A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
Din	Data Input
Dout	Data Output
V_{CC}	Power (+5V)
GND	Ground
NC	No Connect

Package Details

Pin Count	Description	Package Type	Material	Pin Out
18	300 mil Dual-in-line (DIP)	T	Ceramic	JEDEC
18	100 mil Vertical-in-Line (VIL)	V	Ceramic	JEDEC
24	100 mil Vertical-in-Line (VIL)	VX	Ceramic	ASIC
20	Bottom Brazed Flat Pack	G	Ceramic	JEDEC
20	Small Outline 'J' Lead (SOJ)	J	Ceramic	JEDEC

Package Dimensions and details on page 9,10.

Absolute Maximum Ratings

Voltage on any pin relative to V_{ss}	V_t	-1 V to +7	V
Power Dissipation	P_t	1.0	W
Storage Temperature	T_{STG}	-55 to +125	°C
Short circuit output current	I_{OSC}	50	mA

Recommended Operating Conditions

		min	typ	max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	-	6.5	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V
Operating Temperature	T_a	0	-	70	°C
	T_{ai}	-40	-	85	°C (I)
	T_{ai}	-55	-	125	°C (M/MB)

Capacitance (V_{cc}=5V±10%,T_a=25°C)

Parameter		*Symbol*	*typ*	*max*	*Unit*	*Notes*
Input Capacitance:	Address,	C_{IN1}	-	6	pF	1
	$\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$	C_{IN2}	-	8	pF	1,2
Output Capacitance:	Data Out	C_{OUT}	-	7	pF	1,2

Notes: 1. Capacitance calculated, not measured.
2. CAS=V_{IH} to disable D_{OUT}.

DC Electrical Characteristics

Parameter	*Symbol*	*Test Condition*	*-80* min	*-80* max	*-10* min	*-10* max	*-12* min	*-12* max	*Unit*
Operating Current	I_{cc1}	$\overline{RAS}$,$\overline{CAS}$ Cycling:							
Refresh Current	I_{cc3}	t_{RC}=min.(See Note 1) $\overline{RAS}$ only Refresh,	-	70	-	60	-	50	mA
Refresh Current	I_{cc6}	t_{RC}=min. $\overline{CAS}$ before $\overline{RAS}$ Refresh,	-	70	-	60	-	50	mA
Nibble Mode Current	I_{cc4}	t_{RC}=min. $\overline{RAS}$=V_{IL},$\overline{CAS}$ Cycling,	-	70	-	60	-	50	mA
		t_{PC}=min.	-	60	-	50	-	40	mA
Standby Current	I_{cc2}	$\overline{RAS}$,$\overline{CAS}$=V_{IH},	-	2	-	2	-	2	mA
	I_{cc5}	$\overline{RAS}$,$\overline{CAS}$ = V_{CC}-0.2V	-	1	-	1	-	1	mA
Input Leakage	I_{LI}	V_{IN}=0 to +7V	-10	10	-10	10	-10	10	µA
Output Leakage	I_{LO}	V_{OUT}=0 to +7V, D_{OUT} is disabled.	-10	10	-10	10	-10	10	µA
Output Levels	V_{OH}	I_{OUT}=-5mA	2.4	-	2.4	-	2.4	-	V
	V_{OL}	I_{OUT}=4.2mA	-	0.4	-	0.4	-	0.4	V

Note 1: I_{CC} depends on output loading condition when the device is selected, I_{CC} max. is specified at the outputopencondition.

AC Test Conditions

* Input pulse levels: 0.8 to 2.4V
* Input rise and fall times: 5nS
* Input and Output timing reference levels: 1.5V
* Output load: 2TTL loads + 100pF

Electrical Characteristics & Recommended AC Operating Conditions [1,9]

Parameter	Symbol	-80 min	-80 max	-10 min	-10 max	-12 min	-12 max	Unit	Note
Access Time from $\overline{RAS}$	t_{RAC}	-	80	-	100	-	120	ns	2,3
Access Time from $\overline{CAS}$	t_{CAC}	-	28	-	30	-	30	ns	3,4
Output Buffer Turn-off Delay	t_{OFF}	0	20	0	25	0	30	ns	5
Transition Time (Rise & Fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	160	-	190	-	220	-	ns	
R-M-W Cycle Time	t_{RWC}	190	-	225	-	260	-	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70	-	80	-	90	-	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{RAS}$ Pulse Width(Nibble Cycle)	t_{RASP}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	25	10000	30	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	25	90	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	20	-	25	-	30	-	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	-	100	-	120	-	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	-	10	-	10	-	ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	10	-	10	-	15	-	ns	
Row Address Setup Time	t_{ASR}	0	-	0	-	0	-	ns	
Row Address Hold Time	t_{RAH}	12	-	12	-	15	-	ns	
Column Address Setup Time	t_{ASC}	0	20	0	20	0	25	ns	
Column Address Hold Time	t_{CAH}	20	-	20	-	25	-	ns	
Read Command Setup Time	t_{RCS}	0	-	0	-	0	-	ns	12
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	-	0	-	0	-	ns	10,12
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	-	10	-	10	-	ns	10,12
Write Command Setup Time	t_{WCS}	0	-	0	-	0	-	ns	8
Write Command Hold Time	t_{WCH}	15	-	20	-	25	-	ns	
Write Command Pulse Width	t_{WP}	15	-	20	-	25	-	ns	11
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	-	30	-	35	-	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	-	20	-	25	-	ns	
Data in Setup Time	t_{DS}	0	-	0	-	0	-	ns	
Data in Hold Time	t_{DH}	20	-	20	-	25	-	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	80	-	100	-	120	-	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	20	-	25	-	30	-	ns	
Refresh Period (512 Cycles)	t_{REF}	-	8	-	8	-	8	ms	
$\overline{CAS}$ Setup Time	t_{CSR}	10	-	10	-	10	-	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	15	-	20	-	25	-	ns	12
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	-	0	-	0	-	ns	

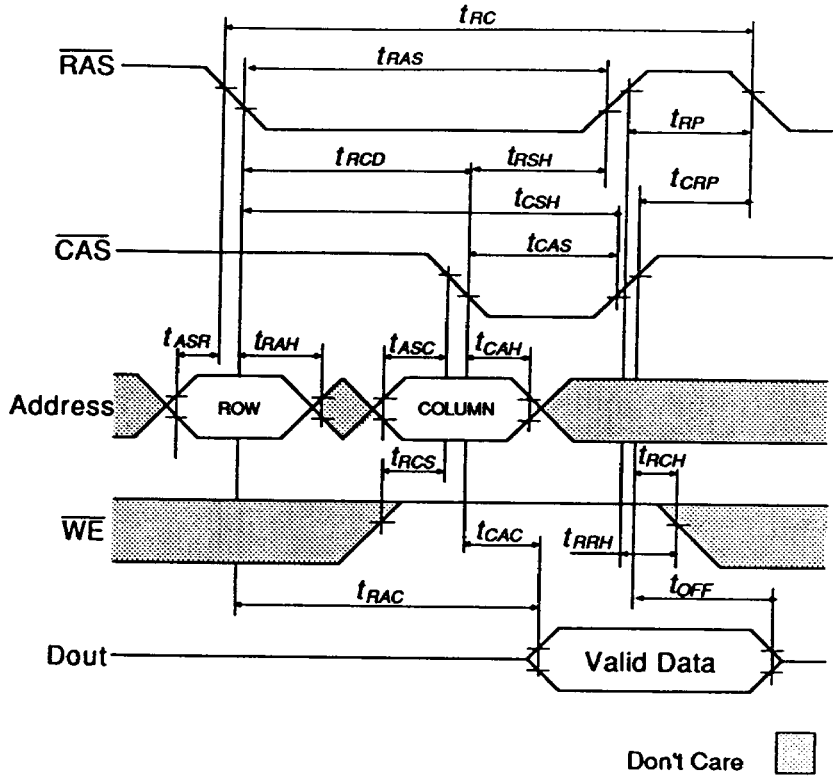
Nibble Mode Characteristics

Parameter	Symbol	-80 min	-80 max	-10 min	-10 max	-12 min	-12 max	Unit	Note
Nibble Cycle Time	t_{NC}	40	-	45	-	55	-	ns	12
Nibble Acces Time	t_{NAC}	-	20	-	25	-	30	ns	3
$\overline{CAS}$ Precharge Time,Nibble Cycle	t_{NP}	10	-	10	-	15	-	ns	12
$\overline{CAS}$ Pulse Width(Nibble Cycle)	t_{NAS}	20	10000	25	10000	30	10000	ns	3
$\overline{RAS}$ Hold Time(Nibble Read Cycle)	t_{NRRSH}	20	-	25	-	30	-	ns	12
$\overline{RAS}$ Hold Time (Nibble Write Cycle)	t_{NWRSH}	20	-	25	-	30	-	ns	12
$\overline{CAS}$ to $\overline{WE}$ Delay (Nibble Cycle)	t_{NCWD}	20	-	25	-	30	-	ns	12
Write Command to $\overline{CAS}$ Leadtime (Nibble Cycle)	t_{NCWL}	20	-	25	-	30	-	ns	12

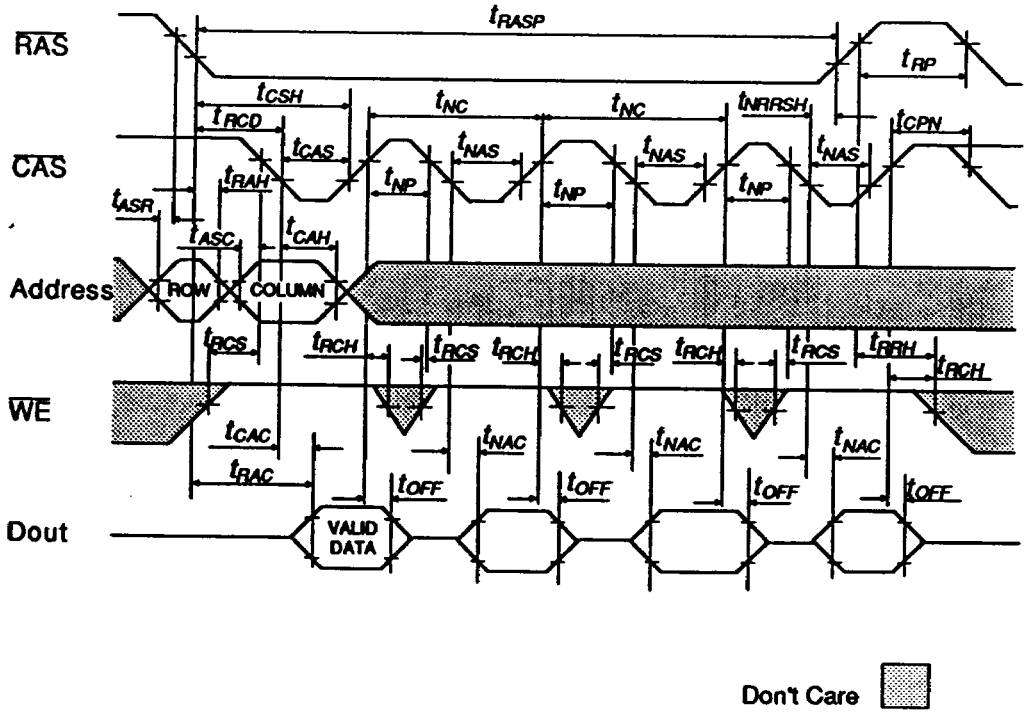
Notes:

1. AC measurements assume t_T=5ns.
2. Assumes that t_{RCD} is less than or equal to t_{RCD} (max.).If t_{RCD} is greater than the max. recommended value shown in this table,t_{RAC} exceeds the value shown.
3. Measured with a load current equivalent to two TTL loads and 100pF.
4. Assumes that t_{RCD} is greater than or equal to t_{RCD} (max.).
5. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals.Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RCD} (max.) is specified as a reference point only, if t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS} is not a restrictive operating parameter. It is included in the Data Sheet as Electrical Characteristics only.
9. An initial pause of 100µs is required after power-up. Then execute at least 8 initialization ($\overline{RAS}$) cycles.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. Parameter t_{WP} is applicable for a delayed write cycle. For early write cycle, both t_{WCS} and t_{WCH} must be met.
12. This parameter is not tested.

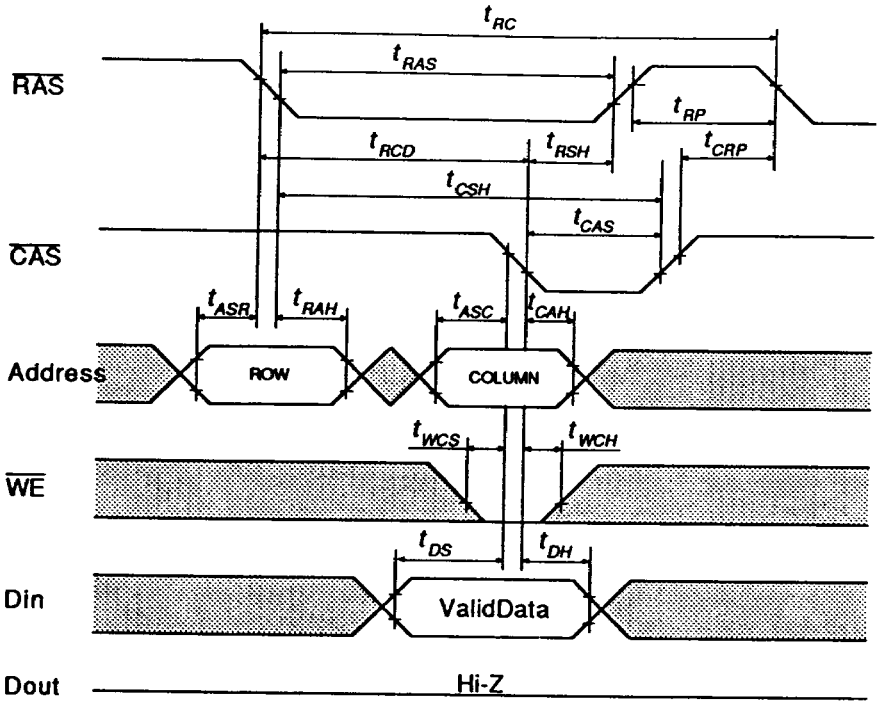
Read Cycle Timing Waveform



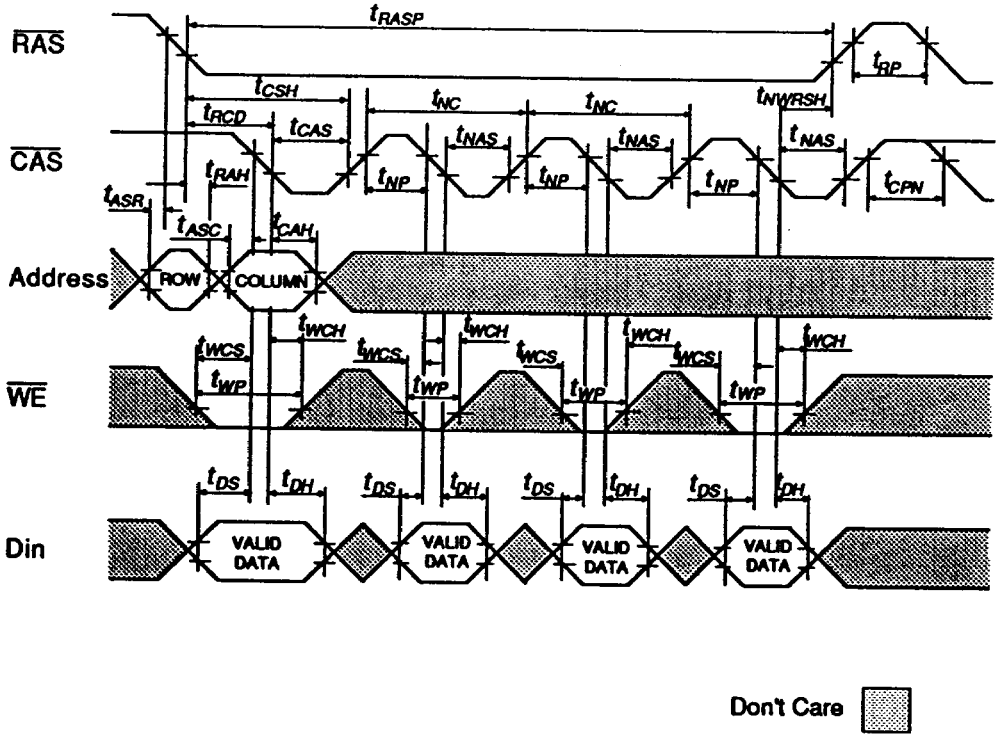
Nibble Mode Read Cycle



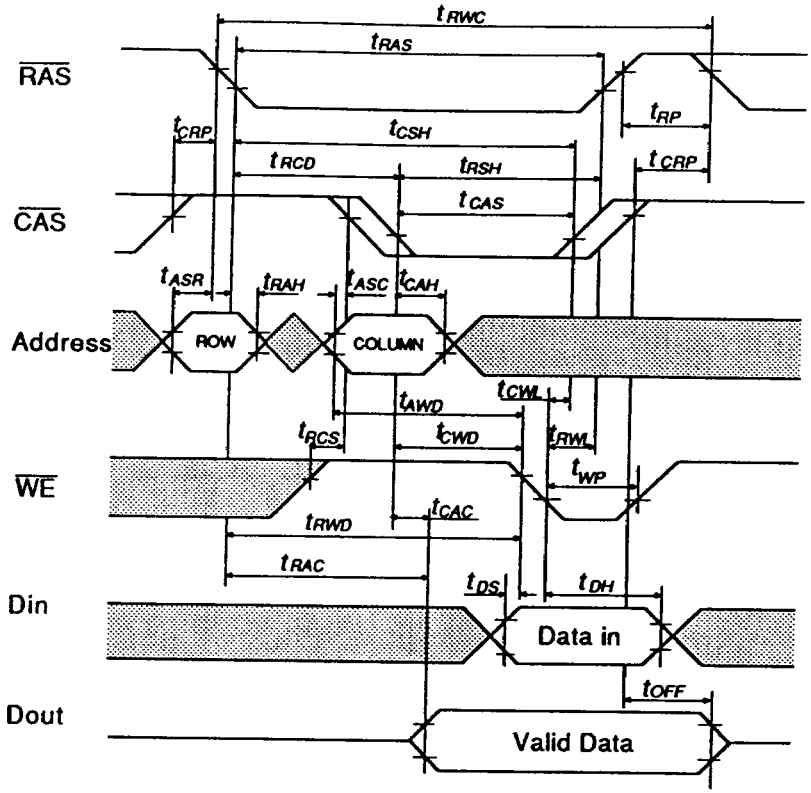
Early Write Cycle Timing Waveform



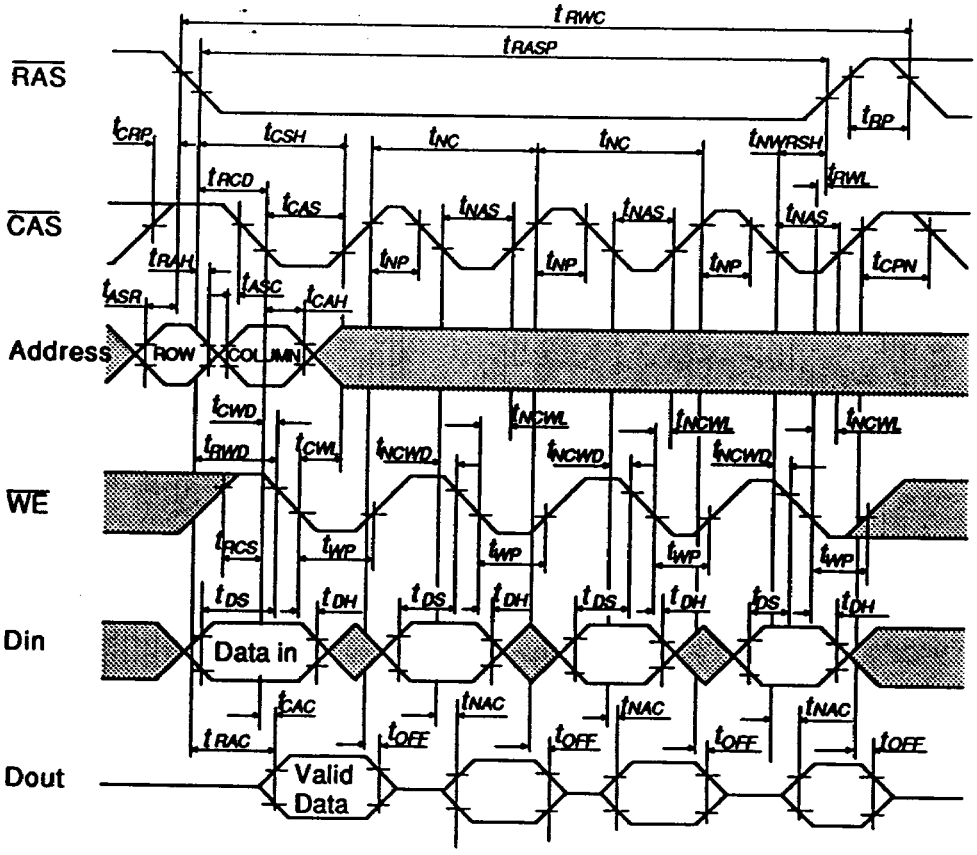
Nibble Mode Write Cycle Timing Waveform



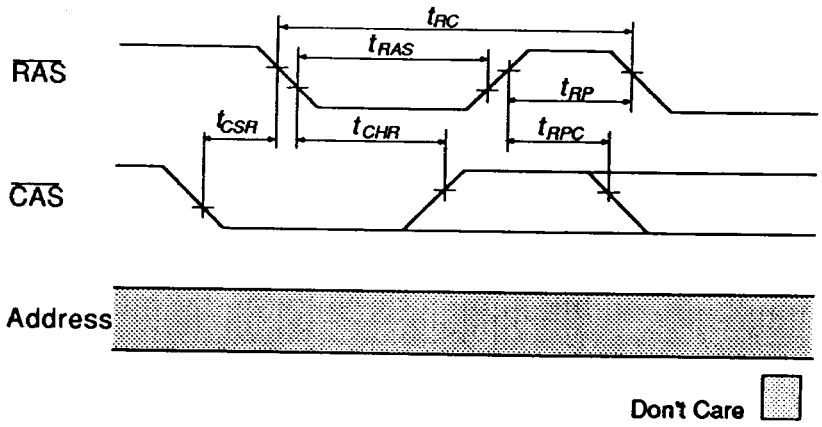
Read-Modify-Write Cycle Timing Waveform



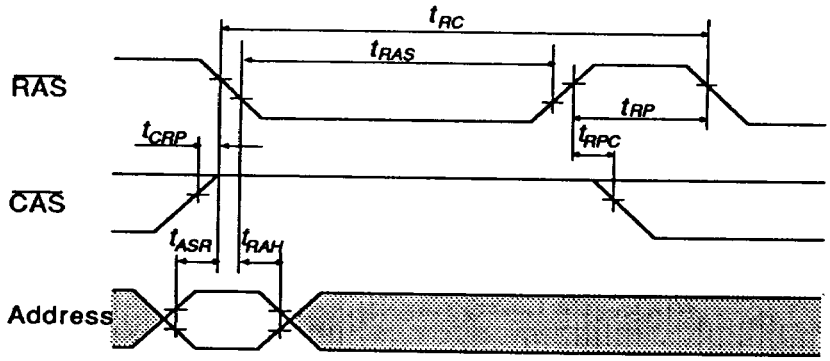
Nibble Mode Read-Modify-Write Cycle Timing Waveform



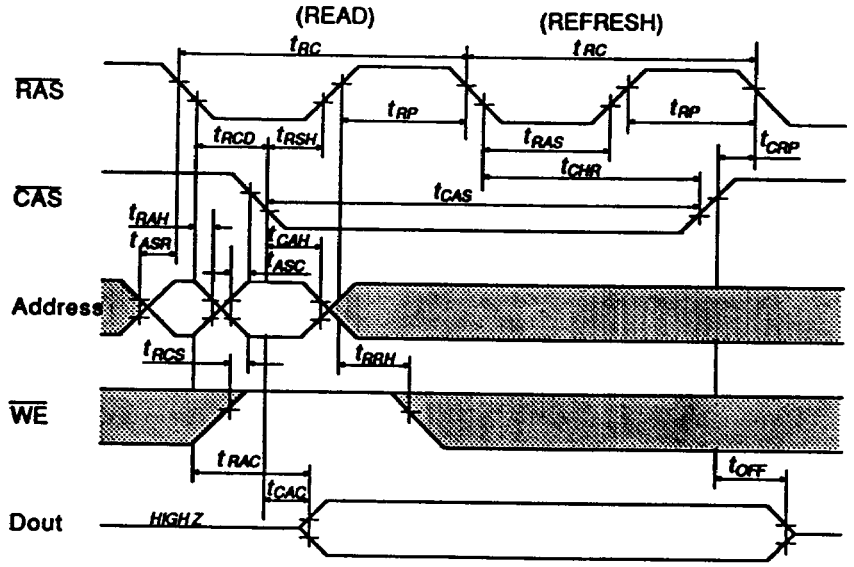
CAS Before RAS Refresh Cycle



RAS Only Refresh Cycle

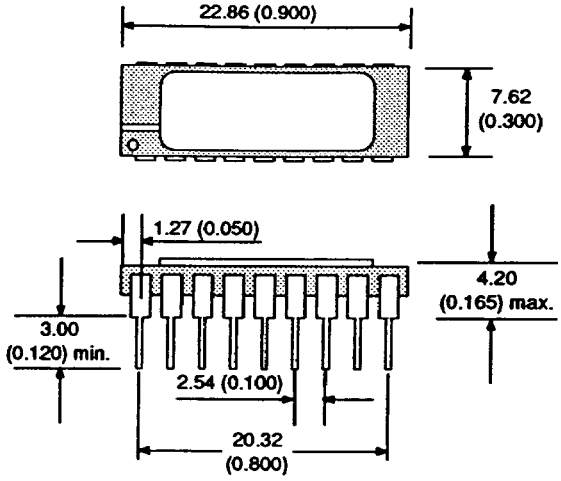


Hidden Refresh Cycle

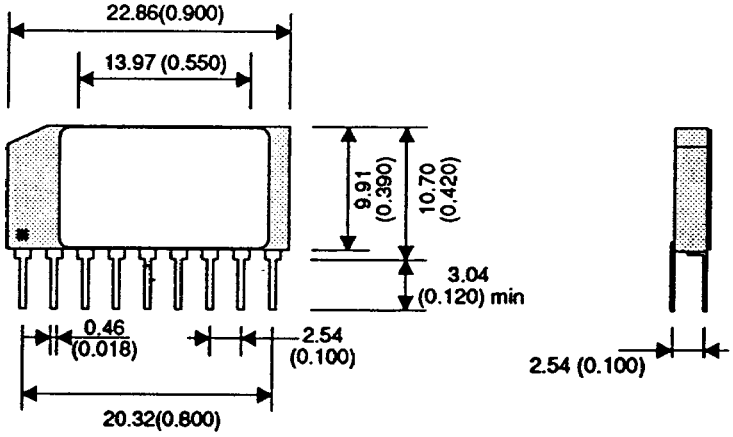


Package Details Dimensions in mm (inches)Tolerance on all dimensions ± .254 (0.010)

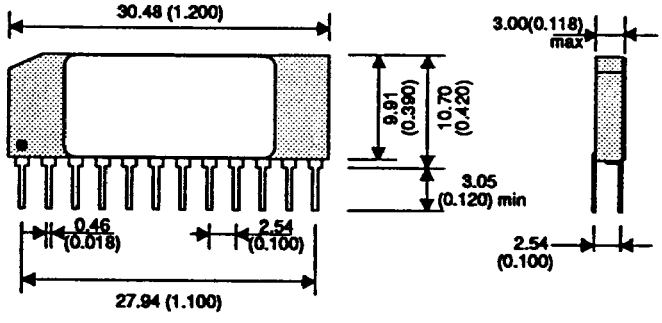
18 Pin DIP ('T' Package)



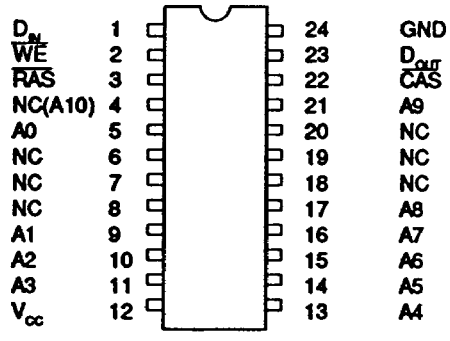
18 Pin Vertical-In-Line (VIL) ('V' Package)



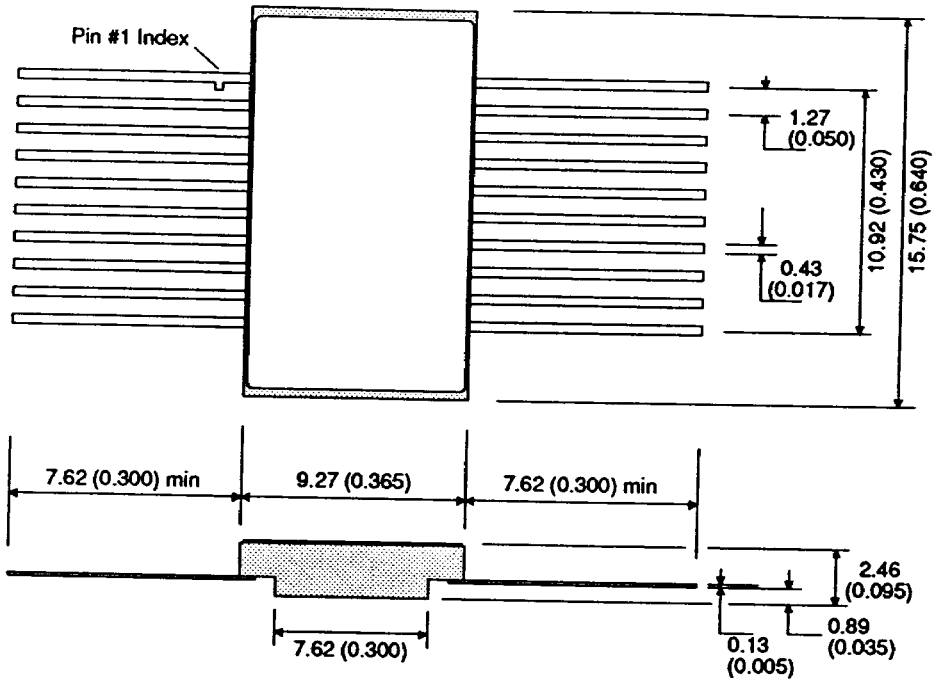
24 Pin Vertical-In-Line (VIL) ('V' Package)



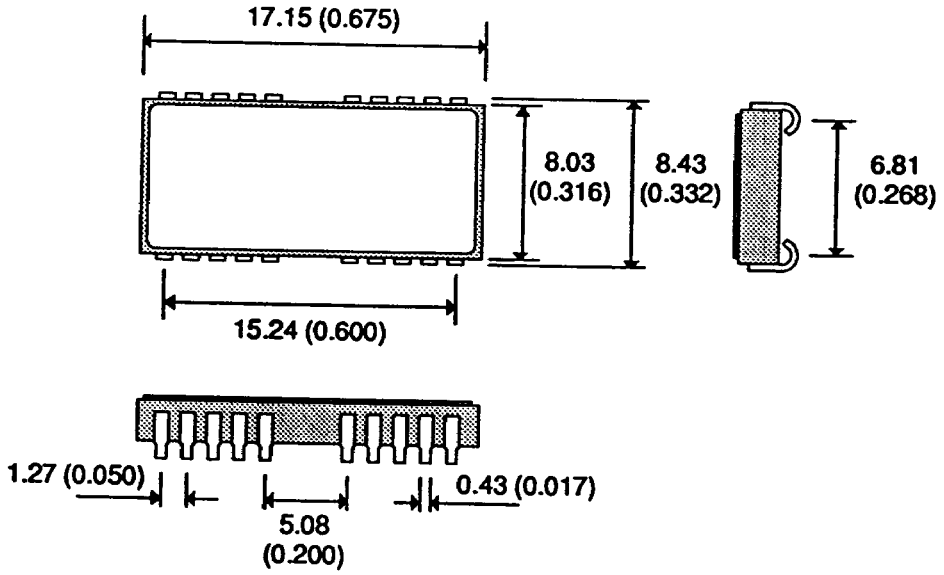
Pin Out Diagram



20 Pin Flat Pack ('G' Package)

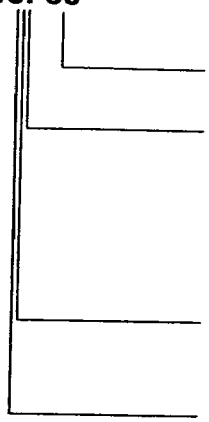


20 Pin CSOJ ('J' Package)



Ordering Information

MDM11001JI-80



Speed	80,100,120 ns	
Temp. range/screening	Blank	= Commercial Temp.
	I	= Industrial Temp.
	M	= Military Temp.
	MB	= Processed to MIL-STD-883 Method 5004, non-compliant
Pinout	Blank	= JEDEC
	X	= ASIC
Package	T	= 18 Pin 300 mil DIP
	V	= 18 Pin 100 mil VIL
	VX	= 24 Pin 100 mil VIL
	G	= 20 Pin Flat Pack
	J	= 20 Pin Small-Outline J-Lead (SOJ)

Note: For more information regarding screening levels, contact Mosaic Semiconductor for a 'Screening Level Applications Note.'

The policy of the company is one of continuous development and while the information presented in this data sheet is believed to be accurate, no liability is assumed for any data contained within. The company reserves the right to make changes without notice at any time.

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