

**FEATURES**

- Max. propagation delay of 1200ps
- IEE min. of -92mA
- Industry standard 100K ECL levels
- Extended supply voltage option:  
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 60% faster than National or Signetics
- Approximately 40% lower power than National or Signetics
- Function and pinout compatible with National and Signetics F100K
- ESD protection of 2000V
- Available in 24-pin CERDIP, 24-pin CERPACK and 28-pin PLCC packages

**DESCRIPTION**

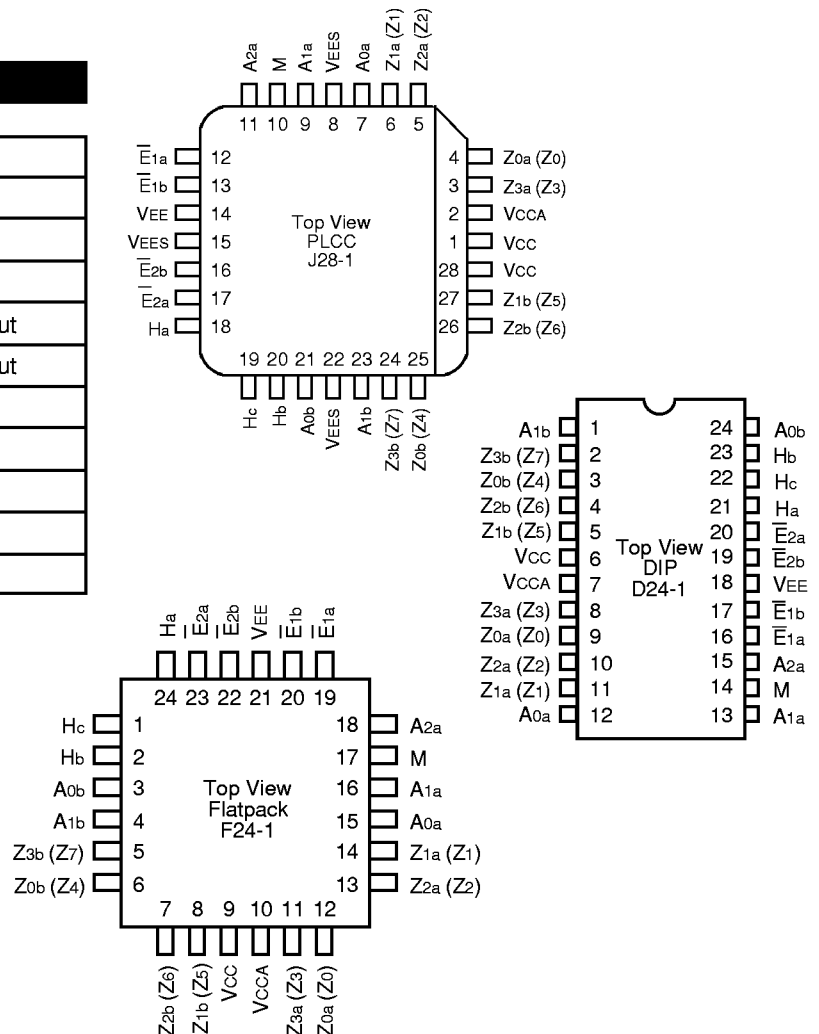
The SY100S370 is a universal demultiplexer/decoder that can be used as either a dual 1-of-4 decoder or as a single 1-of-8 decoder and is designed for use in high-performance ECL systems. The Mode control (M) input determines the function. In the dual 1-of-4 mode, each 4-input group has a pair of active-LOW Enable ( $\bar{E}$ ) inputs. The Enable pins are assigned such that in the single 1-of-8 mode they can be tied together in pairs to result in two active-LOW Enable inputs.  $\bar{E}_{1a}$  will be tied to  $\bar{E}_{1b}$  and  $\bar{E}_{2a}$  to  $\bar{E}_{2b}$ .

The auxiliary inputs ( $H_n$ ) are used to determine whether the outputs are active-HIGH or active-LOW. The address inputs for the dual 1-of-4 mode are  $A_{0a}$ ,  $A_{1a}$ ,  $A_{0b}$ .  $A_{2a}$  is unused. In the 1-of-8 mode, the address inputs are  $A_{0a}$ ,  $A_{1a}$ ,  $A_{2a}$ . The inputs on the device have 75KΩ pull-down resistors.

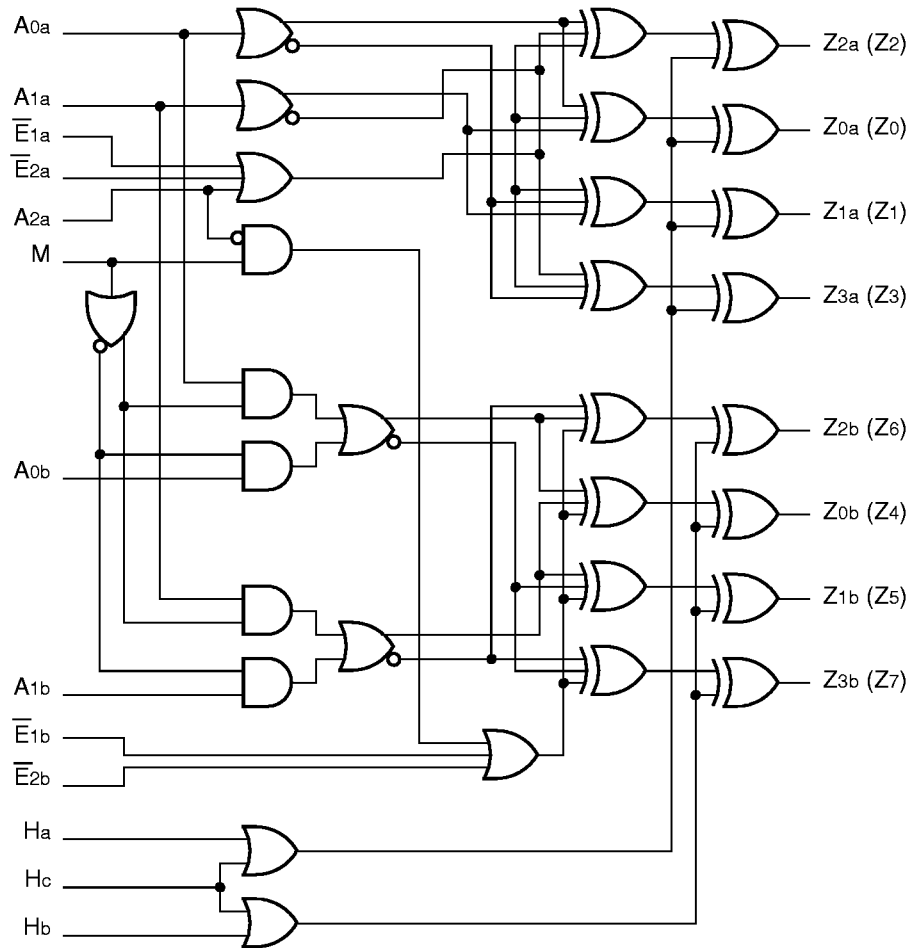
**PIN NAMES**

Pin	Function
$A_{na}$ , $A_{nb}$	Address Inputs ( $n = 0,1,2$ )
$\bar{E}_{na}$ , $\bar{E}_{nb}$	Enable Inputs ( $n = 1,2$ )
M	Mode Control Input
$H_a$	$Z_0 - Z_3$ ( $\bar{Z}_{0a} - \bar{Z}_{3a}$ ) Polarity Select Input
$H_b$	$Z_4 - Z_7$ ( $\bar{Z}_{0b} - \bar{Z}_{3b}$ ) Polarity Select Input
$H_c$	Common Polarity Select Input
$Z_0 - Z_7$	Single 1-of-8 Data Outputs
$Z_{na}$ , $Z_{nb}$	Dual 1-of-4 Data Outputs ( $n = 1...4$ )
VEES	VEE Substrate
VCCA	VCCO for ECL Outputs

**PIN CONFIGURATIONS**



**BLOCK DIAGRAM**



**TRUTH TABLES<sup>(1)</sup>**

Dual 1-of-4 Mode (M = A2a = Hc = LOW)											
Inputs				Active HIGH Outputs (Ha and Hb Inputs HIGH)				Active LOW Outputs (Ha and Hb Inputs LOW)			
$\bar{E}1a, \bar{E}1b$	$\bar{E}2a, \bar{E}2b$	A1a, A1b	A0a, A0b	Z0a, Z0b	Z1a, Z1b	Z2a, Z2b	Z3a, Z3b	Z0a, Z0b	Z1a, Z1b	Z2a, Z2b	Z3a, Z3b
H	X	X	X	L	L	L	L	H	H	H	H
X	H	X	X	L	L	L	L	H	H	H	H
L	L	L	L	H	L	L	L	L	H	H	H
L	L	L	H	L	H	L	L	H	L	H	H
L	L	H	L	L	L	H	L	H	H	L	H
L	L	H	H	L	L	L	H	H	H	H	L

Single 1-of-8 Mode (M = HIGH; A0b = A1b = Ha = Hb = LOW)												
Inputs					Active HIGH Outputs* (Hc Input HIGH)							
$\bar{E}1$	$\bar{E}2$	A2a	A1a	A0a	Z0	Z1	Z2	Z3	Z4	Z5	Z6	Z7
H	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H

**NOTE:**

1. H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

\* for Hc = LOW, output states are complemented

 $\bar{E}1 = \bar{E}1a$  and  $\bar{E}1b$  wired;  $\bar{E}2 = \bar{E}2a$  and  $\bar{E}2b$  wired

**DC ELECTRICAL CHARACTERISTICS**
 $V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified;  $V_{CC} = V_{CCA} = GND$ 

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
$I_{IH}$	Input HIGH Current Hc, A0a, A1a, A2a All Others	—	—	310 250	$\mu A$	$V_{IN} = V_{IH} (Max.)$
$I_{EE}$	Power Supply Current	-92	-73	-46	mA	Inputs Open

## AC ELECTRICAL CHARACTERISTICS

### CERDIP

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified;  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay $\bar{E}_{na}, \bar{E}_{nb}$ to Output	300	1400	300	1400	300	1400	ps	
tPLH tPHL	Propagation Delay $A_{na}, A_{nb}$ to Output	500	1700	500	1700	500	1700	ps	
tPLH tPHL	Propagation Delay $H_a, H_b, H_c$ to Output	500	1700	500	1700	500	1700	ps	
tPLH tPHL	Propagation Delay M to Output	600	2200	600	2200	600	2200	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

### CERPACK

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified;  $V_{CC} = V_{CCA} = GND$

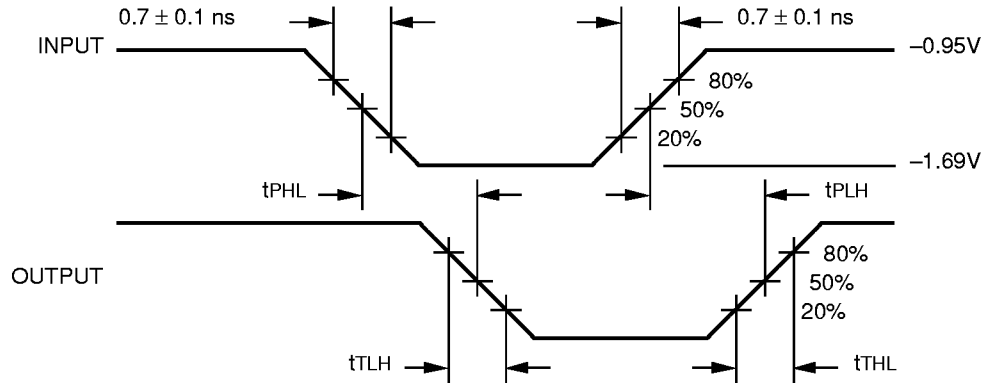
Symbol	Parameter	$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay $\bar{E}_{na}, \bar{E}_{nb}$ to Output	300	1300	300	1300	300	1300	ps	
tPLH tPHL	Propagation Delay $A_{na}, A_{nb}$ to Output	500	1600	500	1600	500	1600	ps	
tPLH tPHL	Propagation Delay $H_a, H_b, H_c$ to Output	500	1600	500	1600	500	1600	ps	
tPLH tPHL	Propagation Delay M to Output	600	2100	600	2100	600	2100	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

### PLCC

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified;  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay $\bar{E}_{na}, \bar{E}_{nb}$ to Output	300	1200	300	1200	300	1200	ps	
tPLH tPHL	Propagation Delay $A_{na}, A_{nb}$ to Output	500	1500	500	1500	500	1500	ps	
tPLH tPHL	Propagation Delay $H_a, H_b, H_c$ to Output	500	1500	500	1500	500	1500	ps	
tPLH tPHL	Propagation Delay M to Output	600	2100	600	2100	600	2100	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

**TIMING DIAGRAM**



**Propagation Delay and Transition Times**

**NOTE:**

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified;  $V_{CC} = V_{CCA} = GND$

**PRODUCT ORDERING CODE**

Ordering Code	Package Type	Operating Range
SY100S370DC	D24-1	Commercial
SY100S370FC	F24-1	Commercial
SY100S370JC	J28-1	Commercial
SY100S370JCTR	J28-1	Commercial

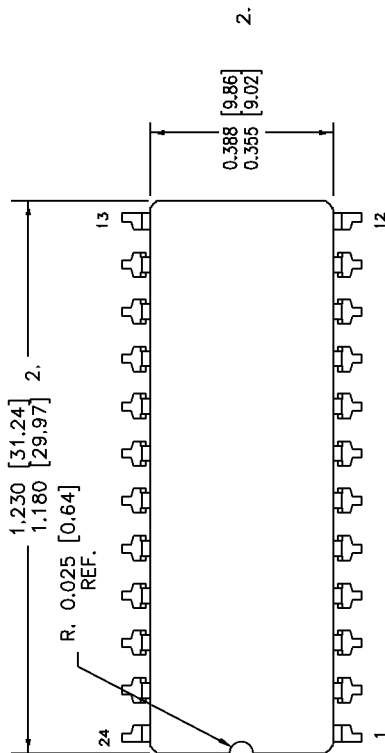
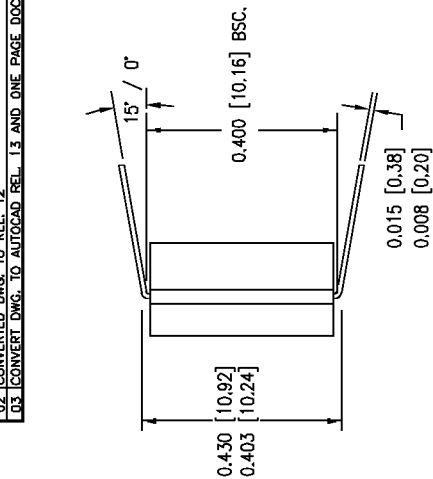
**24 LEAD CERDIP (D24-1)**

FILE/REV #: PD0003A03

PD/0003/ASCORP

PAGE 1 OF 1

REV.	REVISION DESCRIPTION	DATE
01	CONVERT DWG. TO DESIGNER VERSION 4.0 FORMAT.	12/30/93
02	CONVERTED DWG. TO REL. 12	03/15/96
03	CONVERT DWG. TO AUTOCAD REL. 1.3 AND ONE PAGE DOCUMENT.	02/18/98



**NOTES:**

1. DIMENSIONS ARE IN INCHES[MM].
- THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.



3250 SCOTT BOULEVARD  
SANTA CLARA CA 95054  
TEL: 408-980-9191  
FAX: 408-567-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	24 LEAD CERDIP (400" WIDE) PACKAGE OUTLINE	SCALE
ORIGINATOR: FERMIN G. LURRITA	02/23/98	QUALITY: MARSHALL WILDER		A		N/A
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO				REVISION
RELEASE DATE:						03

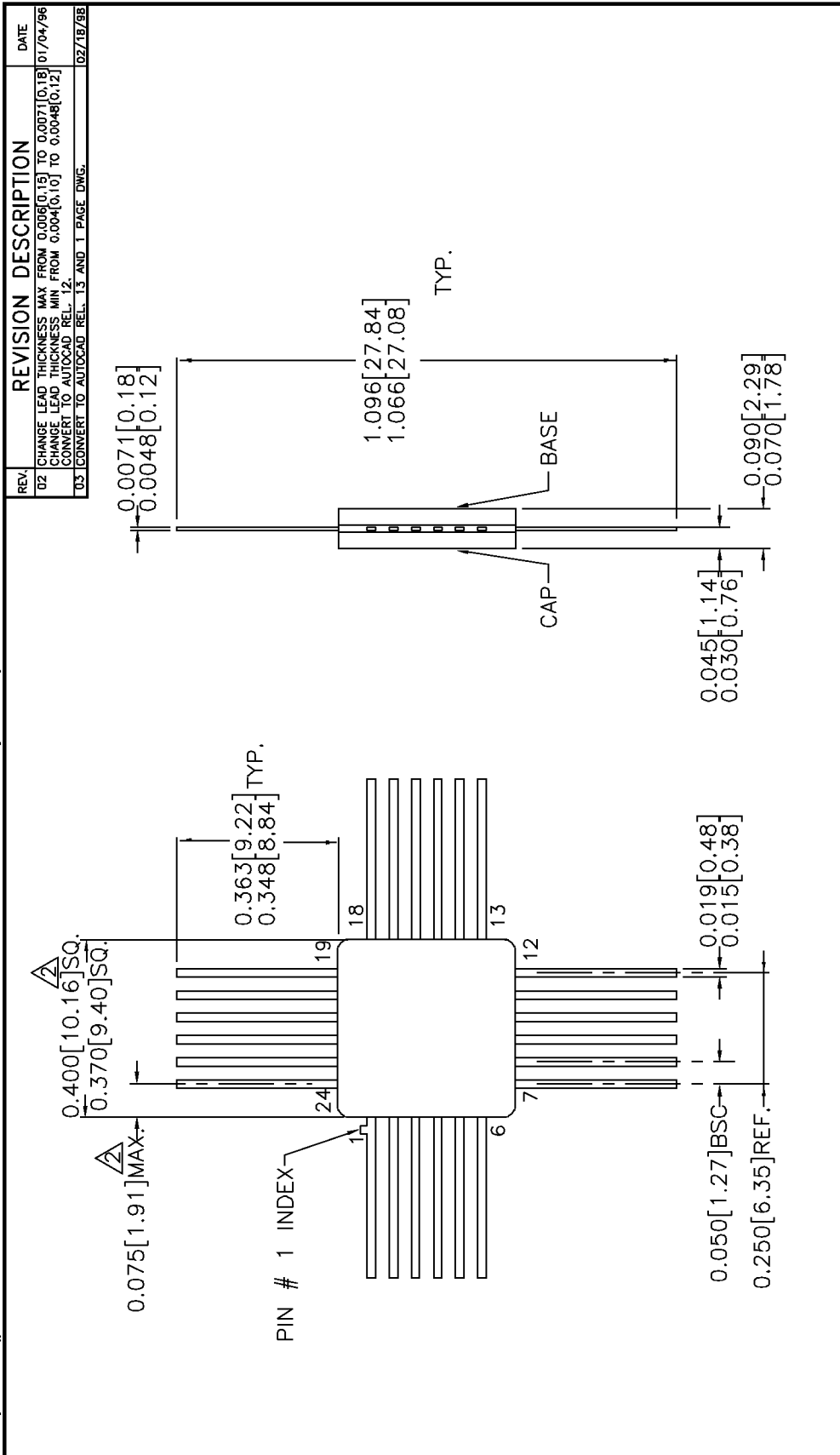
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**24 LEAD CERPACK (F24-1)**

FILE/REV #: PD0006A03

PD/0006/ASCORP

PAGE 1 OF 1



REV.	REVISION DESCRIPTION	DATE
02	CHANGE LEAD THICKNESS MAX FROM 0.006 [0.15] TO 0.0071 [0.18] CHANGE LEAD THICKNESS MIN FROM 0.004 [0.10] TO 0.0048 [0.12] (CONVERT TO AUTOCAD REL. 12)	01/04/96
03	CONVERT TO AUTOCAD REL. 13 AND 1 PAGE DWG.	02/18/98

**SYNERGY**  
SEMICONDUCTOR

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SANTA CLARA CA 95054  
TEL: 408-980-9191  
FAX: 408-587-7878

24 LEAD CERPACK  
PACKAGE OUTLINE

APPROVALS	DATE	APPROVALS	DATE	SIZE
ORIGINATOR: FERNUN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO		
RELEASE DATE:				

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SCALE: N/A  
REVISION: 03

- NOTES:
1. DIMENSIONS ARE IN INCHES [MM].
  2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
  3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

**28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)**

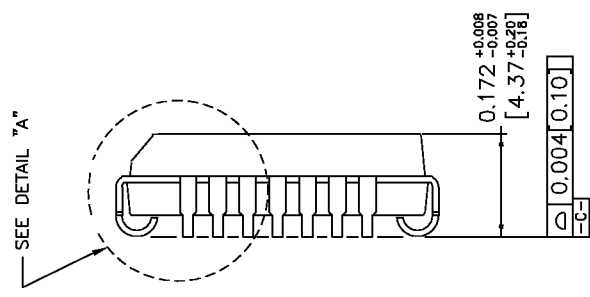
FILE/REV #: PD0008A03

PD/0008/ASCORP

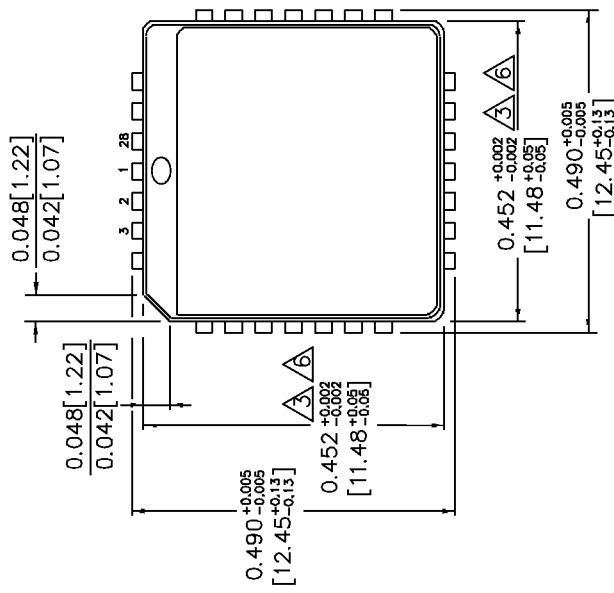
PAGE 1 OF 1

REV.	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER VERSION A.0. FORMAT AND COVER PAGE TO SPEC. CHANGE BODY WIDTH DIMENSION FROM 0.450[11.43] TO 0.443[11.25]. TYPOGRAPHICAL ERROR.	08/18/94
02	CONVERT DWG FROM DESIGNER TO AUTOCAD REL. 12. REFERENCE AMIKOR DWG. NO. 34653 REV. 00.	02/22/96
03	CONVERT DWG TO REL. 15 AND ONE PAGE DOCUMENT.	02/18/98

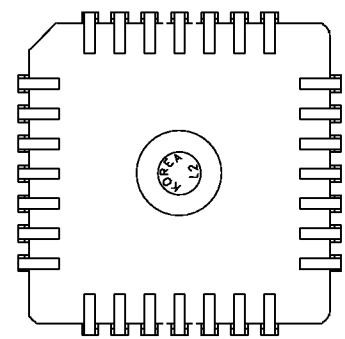
**SIDE VIEW**



**TOP VIEW**

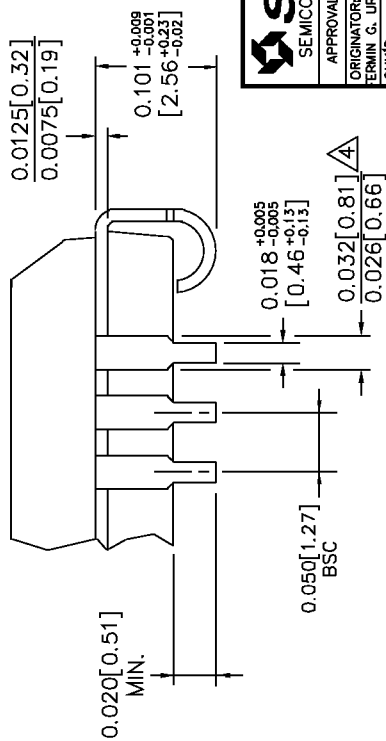


**BOTTOM VIEW**



**NOTES:**

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.



**DETAIL "A"**

**SYNERGY**  
SEMICONDUCTOR

3250 SCOTT BOULEVARD  
SANTA CLARA, CA. 95054  
TEL: 408-960-9191  
FAX: 408-367-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	28 LEAD PLCC
ORIGINATOR: ERMIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	PACKAGE OUTLINE
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			
RELEASE DATE:					

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SCALE: N/A  
REVISION: 03