Codirectional Digital Data Processor

GENERAL DESCRIPTION

The XR-T6165 is a digital CMOS circuit which performs the interface function between a 64Kbit/s data stream and a 2048Kbit/s PCM timeslot data channel. When used in conjunction with the XR-T6164, the XR-T6165 conforms to CCITT G.703 specification requirements for a 64Kbit/s codirectional interface.

The XR-T6165 is composed of a transmitter which transforms 8 bit 2048Kbit/s timeslot data packets into a coded 64Kbit/s data stream, and a receiver which performs the reverse operation. Repetition or deletion of received or transmitted data when clock skews or transients occur is automatic, allowing continuous synchronized data transmission or reception.

FEATURES

Low Power CMOS Technology
All Receiver and Transmitter Inputs and Outputs are TTL Compatible

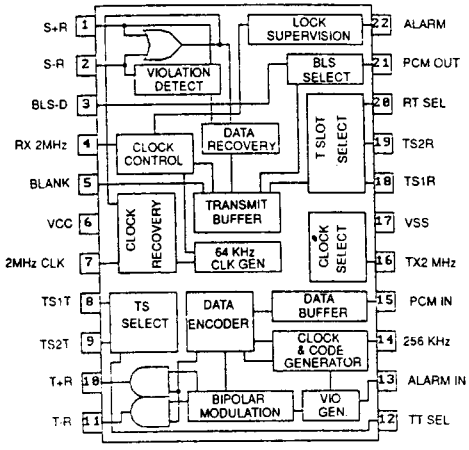
Receiver

Converts Received Encoded 64kbit/s Data to 2048Kbit/s Binary Data For Insertion Into a Timeslot of a PCM Frame
Recovers Both Clock and Octet Timing
Performs Byte Insertion or Deletion in Response to Local Clock Slips
Programmable Loss of Lock Alarm (Output Inhibit/ non-Inhibit)
Glitch Free Output Data Completely Available Within Supplied Timeslot Envelope
Up to 125µs Variance of Data Transfer Timing in Both Transmit and Receive Paths, Allowing Operation in Plesiochronous Networks

Transmitter

Extract 2048Kbit/s Data From a PCM Frame Timeslot and Encodes it as 64Kbit/s Data According to CCITT G.703 Requirements
Performs AMI Coding and Bipolar Violation Insertion for Octet Timing
Allows Inhibit of Bipolar Violation Insertion for Transmission of Alarm Conditions
Performs Byte Insertion or Deletion in Response to Local Clock Slips and Timeslot Changes

PIN ASSIGNMENT



APPLICATIONS

Data Adaptation Unit (DAU)
General 64Kbit/sec Interfaces

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to 150°C
Supply Voltage	4.5V to 5.5V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T6165 CN	Ceramic DIP	0°C to 70°C
XR-T6165 CP	Plastic DIP	0°C to 70°C

PIN DESCRIPTIONS

Name	I/O	Pin	Description
S+R	I	1	Positive AMI data to receiver (Active Low).
S-R	I	2	Negative AMI data to receiver (Active Low).
BLS	I	3	Byte Locking Supervision (Active Low). When active causes blanking of PCMOUT under received alarm conditions.
RX2MHZ	I	4	Receiver 2048kHz clock.
BLANK	I	5	PCMOUT data blanking (Active High), When active, forces PCMOUT data to all ones(AIS)
VCC	I	6	+5V ± 10% power supply.
RXCK2	I	7	2048kHz clock recovery MHz signal.
TS1T	I	8	Timeslot input 1 for transmitter.
TS2T	I	9	Timeslot input 2 for transmitter.
T+R	O	10	Transmit positive output AMI data (Active Low).
T-R	O	11	Transmit negative output AMI data (Active Low).
TTSEL	I	12	Transmit timeslot select. When high pin 8 selected. When low pin 9 selected.
ALARMIN	I	13	Alarm input (Active High). When active inhibits insertion of violation in transmitted data.
TX256KHZ	I	14	Transmitter 256kHz clock.
PCMIN	I	15	Transmitter PCM input.
TX2MHZ	I	16	Transmitter 2048kHz clock.
VSS	I	17	0V power supply.
TS1R	I	18	Timeslot input 1 for receiver.
TS2R	I	19	Timeslot input 2 for receiver.
RTSEL	I	20	Receive timeslot select. When high pin 18 selected; when low pin 19 selected.
PCMOUT	O	21	Received PCM output data.
ALARM	O	22	Alarm (Active High), When active, indicates loss of received bipolar violations.

SYSTEM DESCRIPTION

When used in conjunction with the XR-T6164, the XR-T6165 will form a CCITT G.703 compatible 64Kbit/s data adaption unit (DAU), interfacing between a 2048Kbit/s PCM highway and a variable length twisted pair cable.

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Transmitter

Operation of the transmit circuit is to convert eight bit 2048Kbit/s PCM timeslot data packets into coded continuous 64Kbit/s data. PCM data is read into the transmitter using a 2048kHz local clock and timeslot signal. Transmission is controlled by a 256kHz local clock. Four periods are dedicated to each bit in order to code "0" (0101) and "1" (0011). Timeslot is an envelope derived externally from the 2048kHz clock. and covers eight clock pulses. A two input selector at the timeslot input allows the transmitter to be hard wired to two timeslot positions, selectable using TTSEL. Data is loaded to a storage buffer and transferred to an output shift register, controlled by the external 256kHz signal, only after complete transmission of previously received data. Circuitry is included to delete or repeat complete words of data should skew between the clock signals occur, or during an adjustment of the timing of the timeslot signal, for example when changing from one timeslot position to another. A byte repetition just occurs once; if no new PCM data is received, the transmitter outputs stay high. Octet timing is maintained during these operations. Coded data is alternately fed to two output pins to realize AMI coding, using an external transformer and two line drivers. Transmission of octet timing is performed by feeding the seventh and eighth data bits in each word to the same output. This function may be inhibited by setting ALARMIN active.

Receiver

Operation is to receive coded continuous 64kbit/s input and extract data in the form required for insertion into a 2048kbit/s PCM timeslot. A 128kHz clock is derived from the received data and used to perform decoding of the input signal. If lock is lost with received data the clock circuit enters a seek mode, increasing the speed of the internal clock and reducing the time required to regain lock. Bipolar violations, used to identify bit 1 in the input signal are used to synchronize circuit operation for octet timing. In the absence of violations, for example when receiving a transmitted alarm condition, the circuit will continue to operate in synchronization with respect to the last received violation, Under this condition the received signal PCMOUT (Received PCM output data) is held high indicating AIS. This function may be inhibited using BLS, and the output

set to all ones if required using the BLANK input. ALARM goes high after eight consecutive violations are missed. To accommodate differences between the remote (transmitting) and local clock rate, slip control logic is included in the receiver design. Under slow local clock conditions data will be deleted periodically, while under fast conditions the last output PCM data will be repeated. Octet timing is maintained during these operations. Data appearing at PCMOUT is arranged to be completely framed by the read timeslot signal and is glitch free. A two input selector at the timeslot input allows the receiver to be hard wired to two time slot positions, selectable using RTSEL.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IH}	Logic 1	2.4			V	
V_{IL}	Logic 0			0.4	V	
V_{DD}	Supply	4.5		5.5	V	

DC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5V ± 10%, T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
I_{DD}	Supply Current		500		µA	
I_{IL}	Input Leakage			1	µA	
I_{OL}	O/P Low Current		2		mA	V_{OL} < 0.4V
I_{OH}	O/P High Current		2		mA	V_{OH} > 2.4V

AC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5V ± 10%, T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
GENERAL						
tr, tf	Output Rise/Fall Time		20		nS	
RECEIVER						
t_{RS}	TS Rising Edge to RX2MHZ Set up	0		TRXL −100	nS	Figure 1
t_{RH}	TS Falling Edge to RX2MHZ Hold	0		TRXL −100	nS	Figure 1
t_{DRS}	PCMOUT Edge to RX2MHz Set up		10		nS	Figure 1
t_{DRH}	PCMOUT Edge to RX2MHz Hold		10		nS	Figure 1
t_{PW}	PCMOUT Pulse Width		488		nS	Figure 1
t_{RXH}	RX2MHz High Time		244		nS	±100ppm
t_{RXL}	RX2MHz Low Time		244		nS	±100ppm
TRANSMITTER						
t_{TS}	TS Rising Edge to TX2MHZ Set Up	20		TTXL −100	nS	Figure 2
t_{TH}	TS Falling Edge to TX2MHz Hold	0		TTXL −100	nS	Figure 2
t_{DS}	PCMIN Edge to TX2MHz Set Up	100			nS	Figure 2
t_{DH}	PCMIN Edge to TX2MHz Hold	100			nS	Figure 2
t_{TXH}	TX2MHz High Time		244		nS	±100ppm Figure 2
t_{TXL}	TX2MHz Low Time		244		nS	±100ppm Figure 2
t_{KXH}	TX256kHz High Time		1.95		µS	±100ppm
t_{KXL}	TX256kHz Low Time		1.95		µS	±100ppm

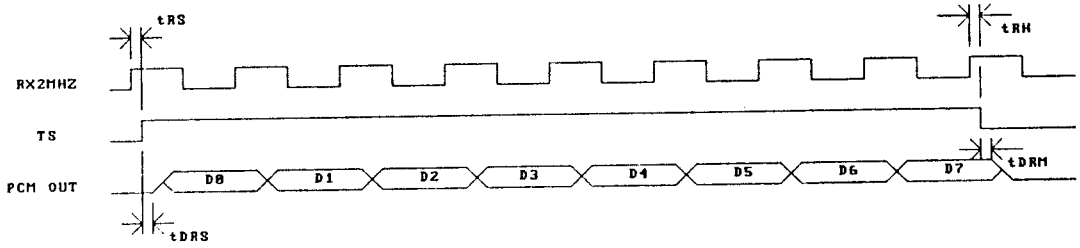

Figure 1. Receiver Time Slot Detail

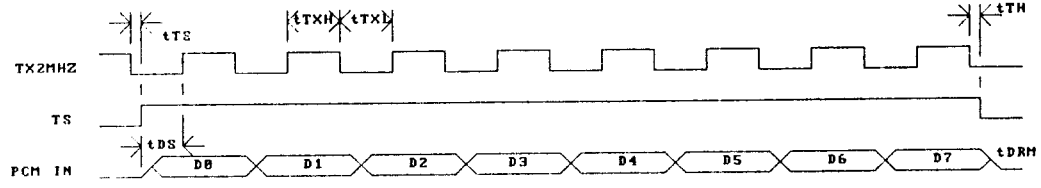

Figure 2. Transmit Time Slot

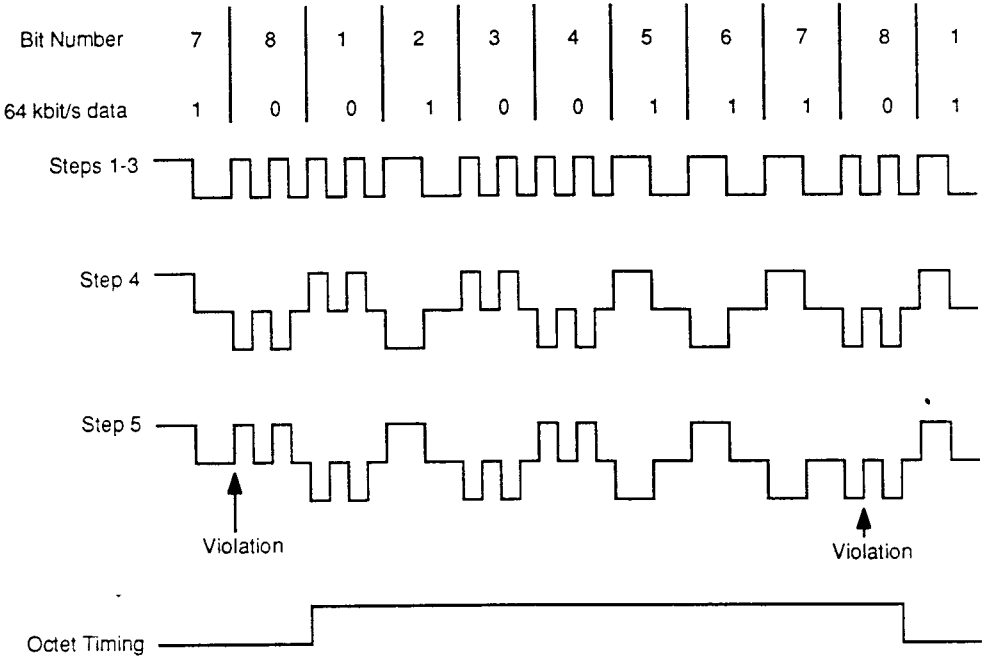

Figure 3. Transmitter Code Conversion for 64 Kbit/s Bipolar Line Signal

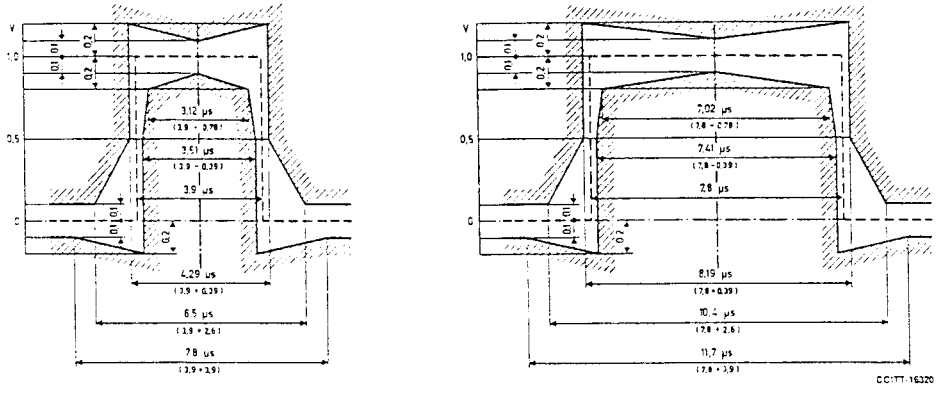

Figure 4. Pulse Masks of the 64kbit/s Codirectional Interface

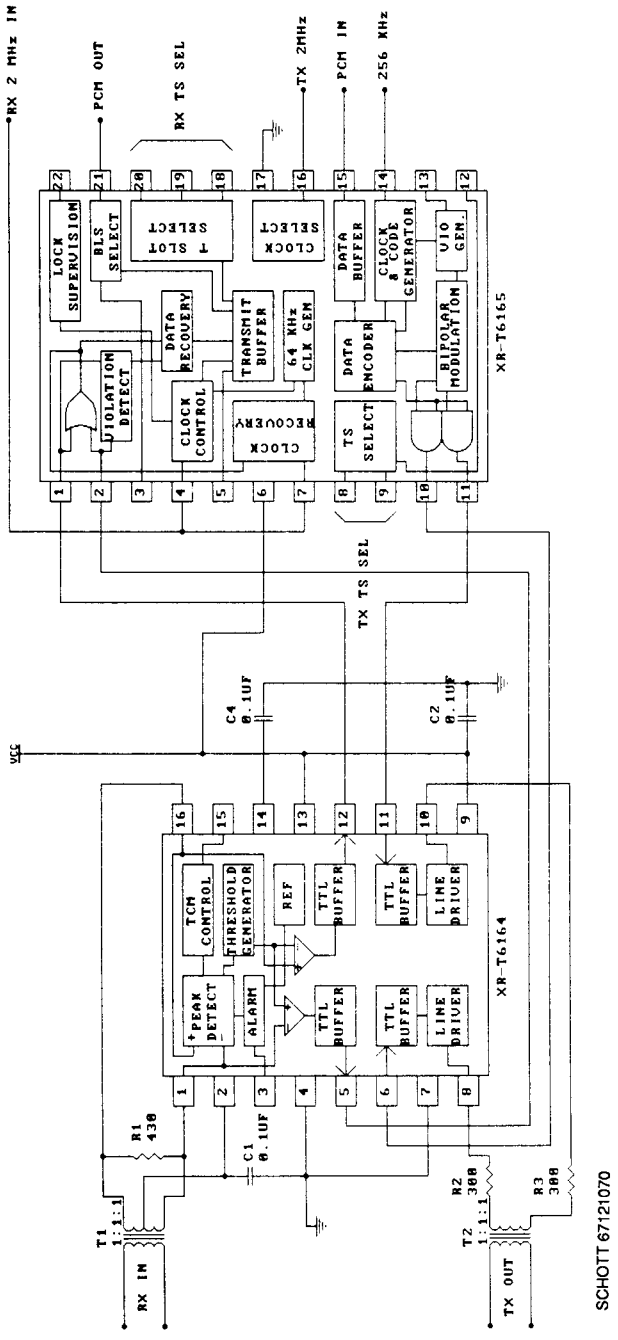

Figure 5. Typical Application Diagram For XR-T6164/65