RFMD
rfmd.com

RF5612

3.0V TO 4.0V, 2.5GHz TO 2.7GHz LINEAR POWER AMPLIFIER

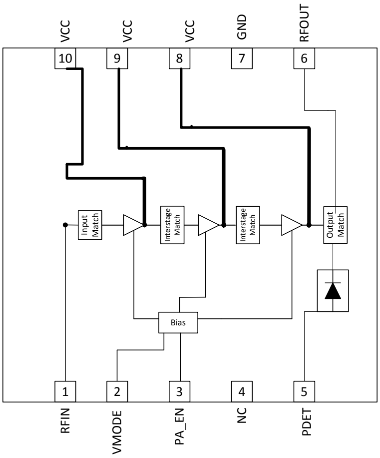
Package: 10-Pin, 4.0mmx4.0mmx0.975mm

Features

- 32dB Typical Gain Across Frequency Band
- LTE UL P_{OUT}=27dBm
- LTE DL P_{OUT}=18dBm
- WiMAX P_{OUT}=25dBm
- 2.5GHz to 2.7GHz Frequency Range
- Integrated Power Detector
- Integrated Input/Output Matched to 50Ω

Applications

- LTE UL for Handset and Data Cards
- Mobile WiMAX Data Cards
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment



Functional Block Diagram

Product Description

The RF5612 is a linear power amplifier IC designed specifically for medium power applications. The device is manufactured on an advanced BiFET Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in LTE Up Link (UL) mobile and Data Cards and 802.11e mobile applications. The device is provided in a 4mmx4mmx0.975mm, 10-Pin, leadless chip carrier with a backside ground. The RF5612 is designed to maintain linearity over a wide range of supply voltages and power outputs.

Ordering Information

RF5612-410	RF5612 Eval Board
RF5612SB	5-Piece bag
RF5612SR	100-Piece reel
RF5612TR7	2500-Piece reel
RF5612SQ	25-Piece bag

Optimum Technology Matching® Applied

☐ GaAs HBT
☐ GaAs MESFET
☑ InGaP HBT
☐ SiGe BiCMOS
☐ Si BiCMOS
☐ SiGe HBT
☐ GaAs pHEMT
☐ Si CMOS
☐ Si BJT
☐ GaN HEMT
☐ BiFET HBT
☐ LDMOS

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF Applied)	-0.5 to +4.5	V
Supply Voltage (No RF Applied)	-0.5 to +6.0	V
DC Supply Current	600	mA
Input RF Power	+10*	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Moisture Sensitivity	TBD	

*Note: Maximum input power with a 50Ω load.

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

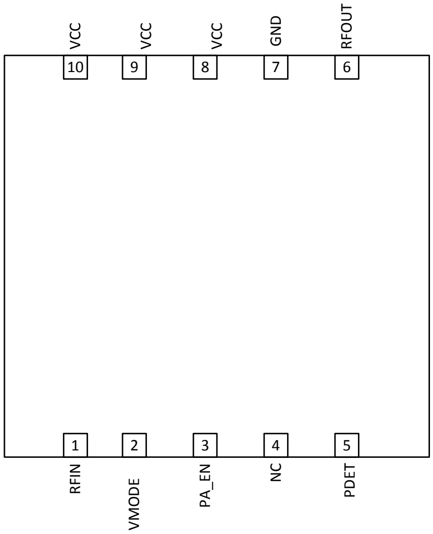
RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Typical Conditions					T=25 °C, V_{CC}=3.3V, , PA_EN=2.85V
Compliance					LTE Uplink; using a 10MHz, LTE UL SC-OFMA waveform, unless other-wise noted.
Frequency	2500		2570	MHz	LTE Band 7
Output Power		27		dBm	
ACP (adjacent Channel)			-33	dBc	At rated P_{OUT}
EVM		2.5	3	%	V_{CC}=3.3V at rated P_{OUT}
Operating Current		425		mA	V_{CC}=3.3V at rated P_{OUT}
Quiescent Current		200		mA	V_{CC}=4.2V, V_{MODE}=0V, RF=OFF
Frequency	2570		2620	MHz	LTE Band 38
Output Power		28		dBm	
ACP (adjacent Channel)			-33	dBc	At rated P_{OUT}
EVM		2.5	3	%	V_{CC}=3.3V at rated P_{OUT}
Operating Current		425		mA	V_{CC}=3.3V at rated P_{OUT}
Quiescent Current		200		mA	
Frequency	2500		2700	MHz	LTE Band 41
Output Power		27		dBm	
ACP (adjacent Channel)			-33	dBc	At rated P_{OUT}
EVM		2.5	3	%	V_{CC}=3.3V at rated P_{OUT}
Gain	30	32		dB	
Gain Variation	-2		2	dB	
Operating Current		425		mA	V_{CC}=3.3V at rated P_{OUT}
Quiescent Current		200		mA	
2nd Harmonic		TBD		dBc	Over all conditions
3rd Harmonic		TBD		dBc	Over all conditions

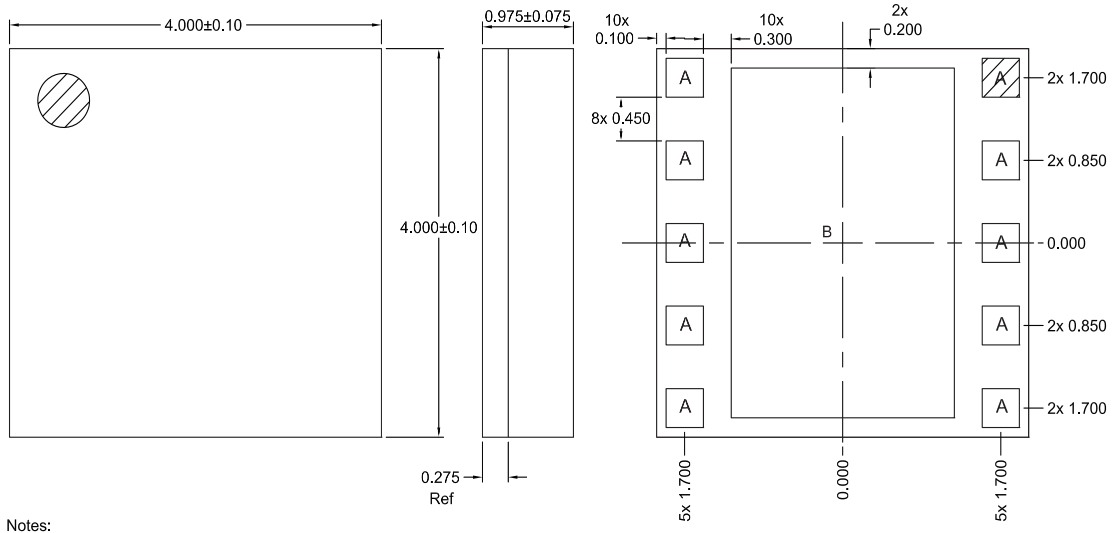
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Compliance					IEEE802.16e, using a 10MHz, IEEE802.16e waveform, unless otherwise noted.
Frequency	2500		2700	MHz	
802.16e Output Power		25		dBm	25 °C 10MHz 802.16e mask
EVM		2.5	3	%	V_{CC}=3.3V at rated P_{OUT}
Gain	30	32		dB	
Gain Variation	-2		2	dB	
Gain in Low Gain/Power Mode	5	7		dB	At V_{MODE}=3.0V
Operating Current		425		mA	V_{CC}=3.3V at rated P_{OUT}
Quiescent Current		200		mA	
2nd Harmonic		-50	-40	dBc	Over all conditions
3rd Harmonic		-50	-40	dBc	Over all conditions
General Spec					
Input Return Loss	10	15		dB	In specified frequency band
Gain in Low Gain/Power Mode	5	7		dB	At V_{MODE}=3.0V
Operating Voltage	3.0	3.3	4.2	V	
V_{MODE}	2.5	3.00	3.3	V	
Operating Current - Low Gain/Power Mode		50		mA	0dBm P_{OUT}, V_{MODE}=3.0V
Power Detect Range	0.2		1	V	
P_{DOWN} Current			5	µA	PA_EN=0V, V_{MODE}=2.85V, V_{CC}=3.3V
Leakage Current		0.5	5	µA	V_{CC}=4.2V, V_{MODE}=2.85V, P_{DOWN}=0V
Turn-on Time			1	µsec	Output stable to within 90% of final gain
Stable into Output VSWR			4:1		No spurs above -47dBm P_{OUT}=0dBm to 29dBm
No Damage into Output VSWR			10:1		50Ω load at rated P_{OUT}
Max Pin (Ruggedness - 50Ω)			10	dBm	No damage
Other					
Thermal Resistance R_{TH_I}		TBD		°C/W	
ESD					
Human Body Model	TBD			V	EIA/JESD22-114A RF Pin to Ground
	TBD			V	EIA/JESD22-114A DC Pin to Ground
Charge Device Model	TBD			V	JESD22-C101C all pins to Ground

Pin	Function	Description
1	**RFIN**	RF input is internally matched to 50Ω and DC blocked.
2	**VMODE**	Bias control pin
3	**PA_EN**	Power down pin. Apply <0.6VDC to power down the three power amplifier stages. Apply 1.75VDC to 5.0VDC to power up.
4	**NC**	No connection
5	**PDET**	Power detector provides an output voltage proportional to RF output power. level May need external decoupling capacitor for module stability. May need external circuitry to bring output voltage to desired level.
6	**RFOUT**	RF Output is internally matched to 50Ω and DC blocked.
7	**GND**	Ground connection
8	**VCC**	This pin is connected internally to the collector of the 3rd stage RF device. To achieve specified performance, the layout of these pins should match the Recommended Land Pattern.
9	**VCC**	This pin is connected internally to the collector of the 2nd stage RF device. To achieve specified performance, the layout of these pins should match the Recommended Land Pattern.
10	**VCC**	This pin is connected internally to the collector of the 1st stage RF device. To achieve specified performance, the layout of these pins should match the Recommended Land Pattern.
Pkg Base	**GND**	Ground connection. The backside of the package should be connected to the ground plane through as short a connection as possible (e.g.: PCB vias under the device are recommended.)

Pin Out

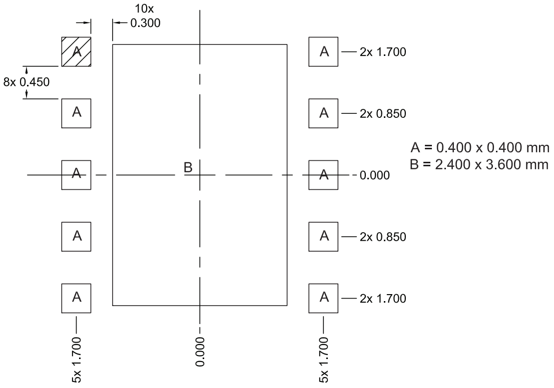


Package Drawing

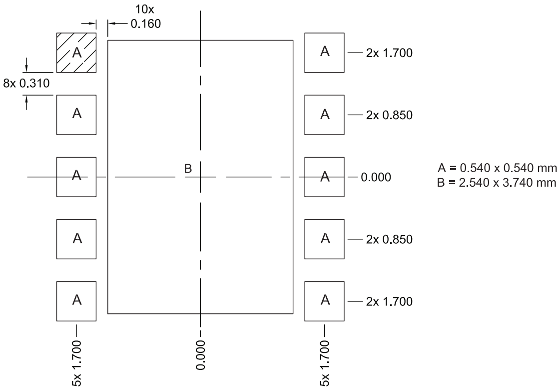


Notes:
1. Shaded area represents Pin 1 location

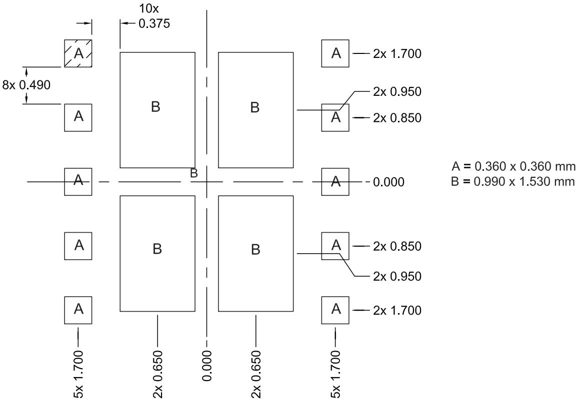
A = 0.400 x 0.400 mm
B = 2.400 x 3.600 mm



PCB METAL LAND PATTERN



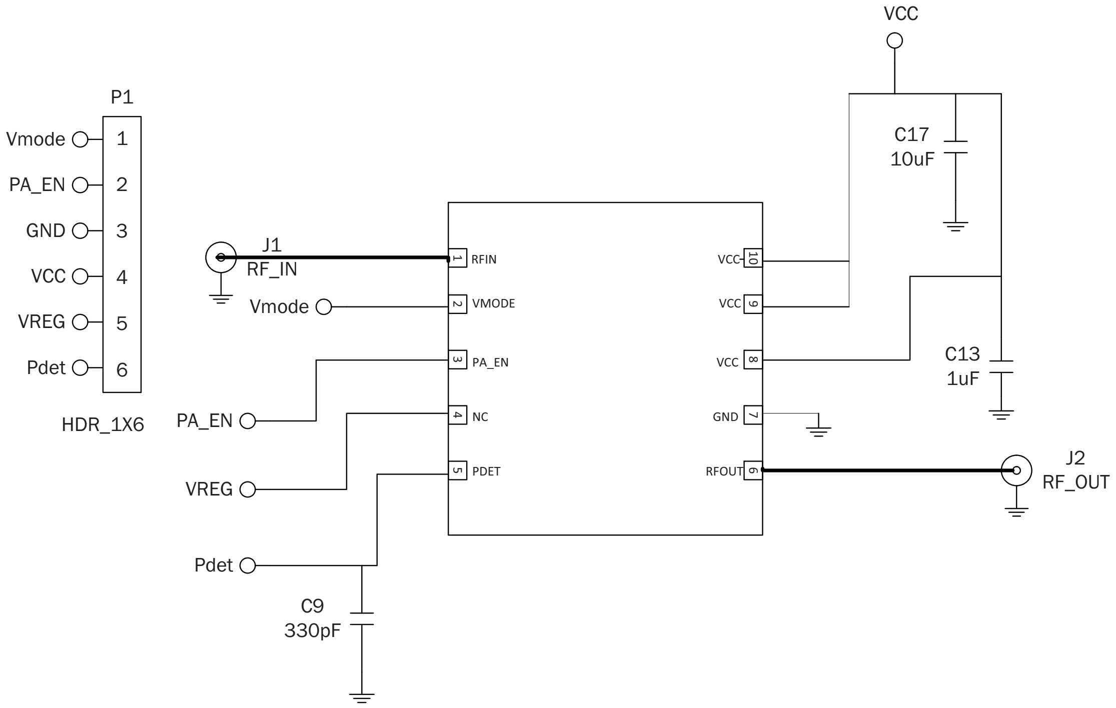
PCB SOLDER MASK PATTERN



PCB STENCIL PATTERN

Note: Thermal vias for center slug “B” should be incorporated into the PCB design. The number and size of thermal vias will depend on the application. Example of the number and size of vias can be found on the RFMD evaluation board layout.

Evaluation Board Schematic



Evaluation Board Layout