MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC1388

WAVEFORM GENERATOR IC FOR MONITOR APPLICATIONS

Advance Information

Geometry Correction Waveform Generator

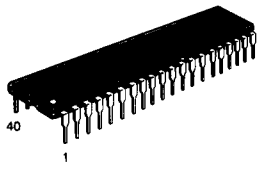
The MC1388 is a bipolar integrated circuit designed to be used with the control circuitry for geometry correction in monitors and HDTV receivers. The function of the integrated circuit is to generate the required voltage waveforms that will be applied to the control circuitry. The control circuitry will apply them in the proper amplitude and combination for use in modulating the horizontal and vertical scan currents.

Features:

- Multistandard Operation Capable (10 kHz ≤ f_H ≤ 63 kHz)(45 ≤ f_V ≤ 120 Hz)
- Constant Amplitude Outputs, Independent of Frequency
- Complementary Output Waveforms (Horizontal Parabola, Horizontal Cubic, Vertical Ramp, Vertical Parabola and Sine Functions)
- Three Input Multiplier
- Minimum of External Components Necessary
- Standard Supplies (±5 Vdc)

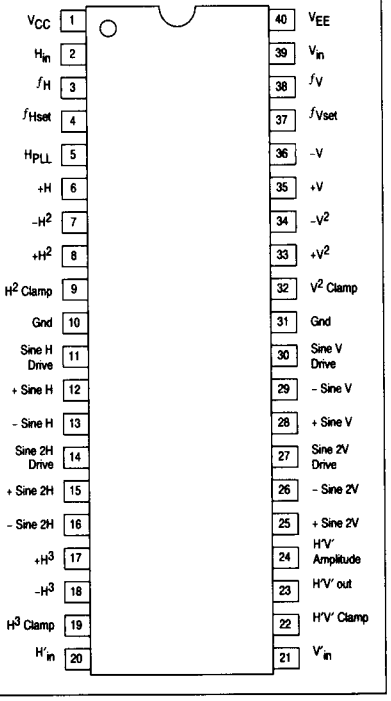
Functions (Ten Waveforms):

- Horizontal Ramp and Vertical Ramp
- Horizontal Parabola and Vertical Parabola
- Horizontal Cube and Cube with Accessible Inputs (H'in, V'in)
- ± Sine H
- ± Sine 2 H
- ± Sine V
- ± Sine 2 V

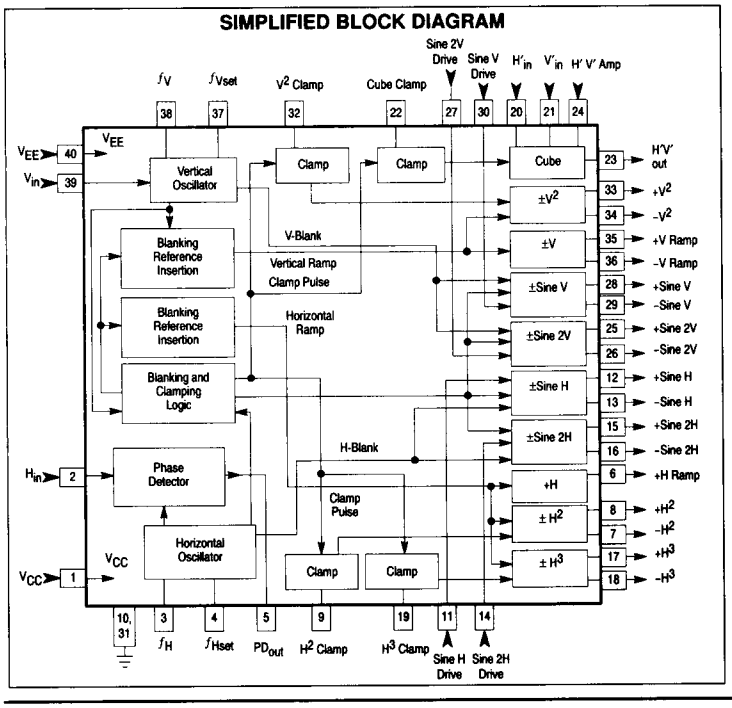


P SUFFIX
PLASTIC PACKAGE
CASE 711

PIN CONNECTIONS
(Top View)



SIMPLIFIED BLOCK DIAGRAM



ORDERING INFORMATION

Device	Temperature Range	Package
MC1388P	0° to +70°C	Plastic DIP

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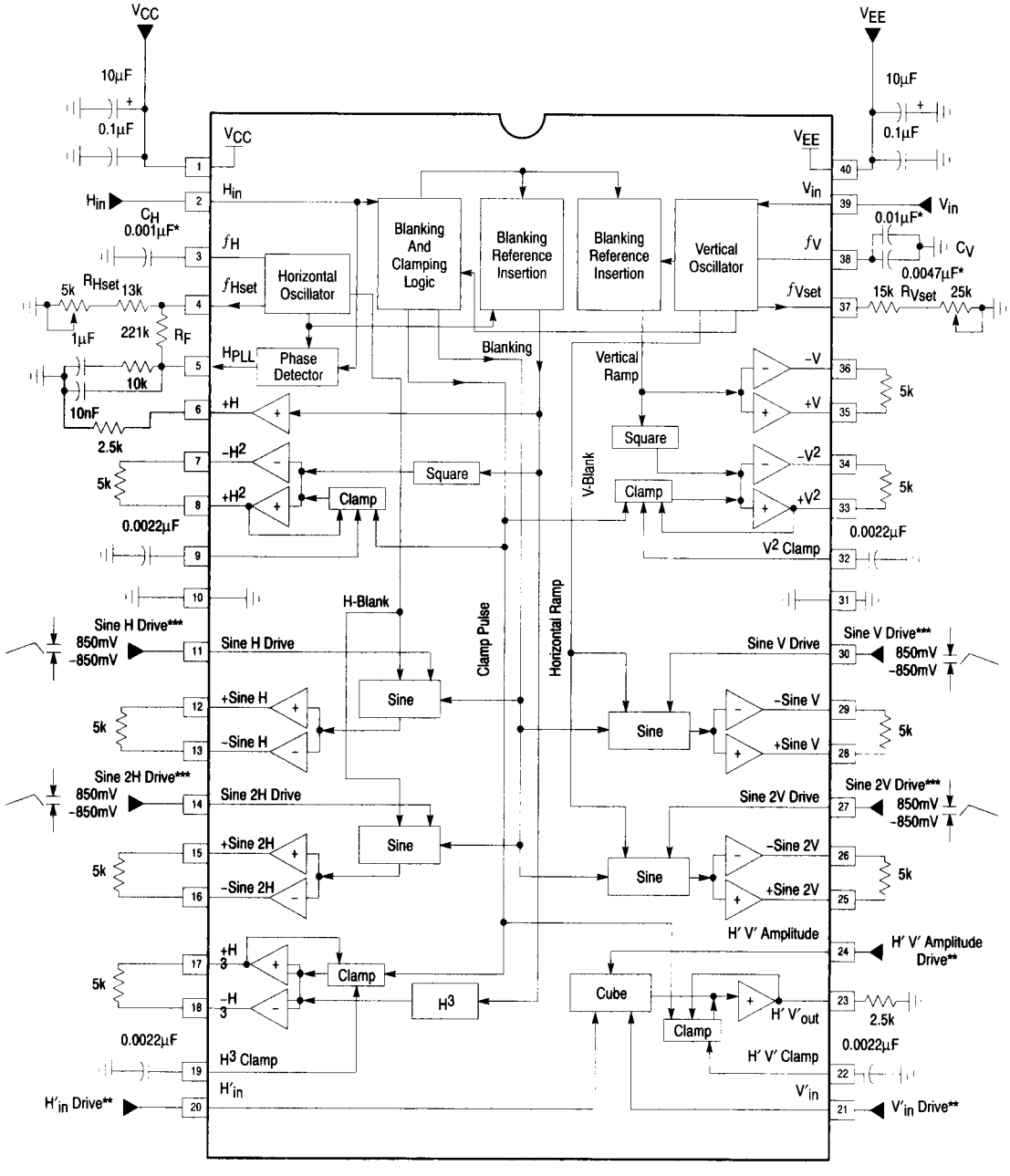
Figure 1. Test Circuit of the MC1388



* Polystyrene
** The three input multiplier was tested by applying a DC voltage to two of the inputs while applying a 1.25 Vp-p ramp input to the third.
*** The inputs applied to the Sine Drive Inputs is a voltage ramped from –850 mV to +850 mV in 10 mV steps.

MAXIMUM OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+6.0 −6.0	Vdc
Input Voltage Maximum Minimum	V_{in}, H_{in}, H'_{in}, V'_{in}, H′ V′ Amplitude	 V_{CC} +0.5 V_{EE} −0.5	Vdc
Storage Temperature	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	+150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Pins(s)	Symbol	Value	Unit
Power Supply Voltage	1 40	V_{CC} V_{EE}	+4.5 to +5.5 −5.5 to −4.5	Vdc
Horizontal Sync Frequency (see Figure 8) Maximum Minimum Pulse Width: Maximum Minimum Pulse Amplitude: Maximum Voltage (Tip) Minimum Voltage (Baseline) Minimum Threshold: Tip Baseline	2	H_{in}	 63 10 <1.0/(2.0f_H) 2.0 V_{CC} V_{EE} +0.5 V_{CC}/2.0 +0.2 V_{CC}/2.0 +0.2	k Hz µs Vdc
Vertical Sync Frequency (see Figure 8) Maximum Minimum Pulse Width: Maximum Minimum Pulse Amplitude: Maximum Voltage (Tip) Minimum Voltage (Baseline) Minimum Threshold: Tip Baseline	39	V_{in}	 120 45 <1.0/(2.0f_V) 2.0 V_{CC} V_{EE} +0.5 V_{CC}/2.0 +0.2 V_{CC}/2.0 +0.2	Hz µs Vdc
Sine H Drive Sine 2H Drive Sine V Drive Sine 2V Drive	11 14 30 27	Sine H Drive Sine 2H Drive Sine V Drive Sine 2V Drive	−0.85 to +0.85	Vdc
H'_{in} V'_{in} H'_{in} V'_{in} Amplitude	20 21 24	H'_{in} V'_{in} H'_{in} V'_{in} Amplitude	−1.25 to +1.25	Vdc
Peak Load Current	6, 7, 8, 12, 13, 15, 16 17, 18, 23, 25, 26, 28 29, 33, 34 35, 36	I_L	5.0	mA
Ambient Temperature		T_A	0 to +70	°C

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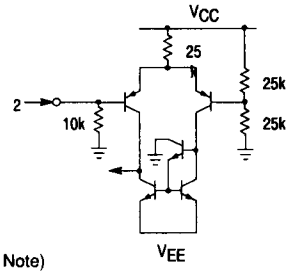
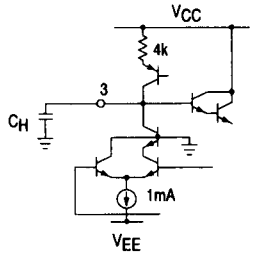
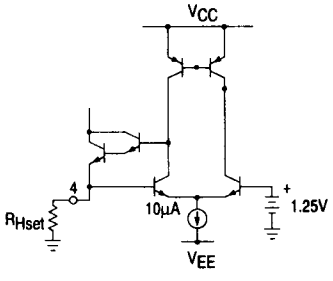
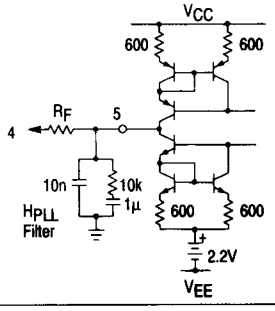
ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = −5.0 V, R_L = 2.5 kΩ, T_A =25°C, f_H = 31,250 Hz, f_V = 1562.5 Hz, see Figure 1, unless otherwise noted.)

Characteristics	Pin(s)	Symbol	Min	Typ	Max	Unit
Supply Current V_{CC} = +5.0 Vdc V_{EE} = −5.0 Vdc	1 40	I_{CC} I_{EE}	29 −50	33 −42	41 −38	mA
Output DC Offset, (All outputs when blanked)	6, 7, 8, 12, 13, 15, 16 17, 18, 23, 25, 26, 28 29, 33, 34 35, 36		−100	±8	100	mV
Pull-In Range Hold In Range (C_H = 1.0 nF, R_F = 221 kΩ, H_{PLL} filter shown)	5	H_{PLL}	±1.5 ±1.5	— ±4.5	— —	kHz
Horizontal Ramp — Amplitude — Non-Symmetry Horizontal Parabola — Amplitude — Non-Symmetry	6 7,8	+H $\pm H^2$	4.4 — 2.2 —	5.0 — 2.6 —	5.3 2.0 3.1 12	Vp-p % Vp–p %
±Sine H — Amplitude (No DC Offset Input) — Zero Crossing Phase Error (Pin 11 Drive as shown in Figure 1)	12, 13	±Sine H	2.8 —	4.0 —	5.6 25	Vp-p Deg
±Sine 2H — Amplitude (No DC Offset Input) — Zero Crossing Phase Error (Pin 14 Drive as shown in Figure 1)	15, 16	±Sine 2H	2.8 —	4.0 —	5.6 25	Vp-p Deg
Horizontal Cubic — Amplitude — Non-Symmetry	17, 18	$\pm H^3$	4.1 —	5.0 —	5.9 12	Vp-p %
±Sine 2V — Amplitude (No DC Offset Input) — Zero Crossing Phase Error (Pin 27 Drive as shown in Figure 1)	25, 26	±Sine 2V	2.8 —	4.0 —	5.6 25	Vp-p Deg
±Sine V — Amplitude (No DC Offset Input) — Zero Crossing Phase Error (Pin 30 Drive as shown in Figure 1)	28, 29	±Sine V	2.8 —	4.0 —	5.6 25	Vp-p Deg
Vertical Parabola — Amplitude — Non-Symmetry	33, 34	$\pm V^2$	2.2 —	2.5 —	3.1 12	Vp-p %
Vertical Ramp — Amplitude — Non-Linearity	35, 36	±V	4.4 —	5.0 —	5.3 2.0	Vp-p %
H′ V′$_{out}$ — Amplitude — Non-Linearity	23	H′ V′$_{out}$	4.2 —	4.8 —	5.4 12	Vp-p %
H′$_{in}$ V′$_{in}$ H′ V′ — Amplitude — Multiplication Factor	20, 21, 24	H′$_{in}$ V′$_{in}$ H′ V′ Amplitude	—	1.0	—	V/V

PIN DESCRIPTIONS

Pin	Symbol	Internal Equivalent Circuit	Description
1	V_{CC}		Positive Rail Voltage. Requires 33 mA at +4.5 < Vdc < +5.5
2	H_{in}	 (* See Note)	Positive Horizontal Flyback input. Input impedance is nominally 10 kΩ. Threshold is at $V_{CC}/2$. See Figure 2.
3	f_H		Horizontal Oscillator Capacitor (C_H). The charge and discharge rate of the capacitor voltage determines the horizontal frequency. Charging current set predominantly by R_{Hset} (Pin 4).
4	f_{Hset}		Horizontal Charge Current Set. An internally regulated 1.25 Vdc, and the external resistance (R_{Hset}) at this pin determines the horizontal free run charging current. Also, the feedback current from the H_{PLL} filter is input at this pin.
5	H_{PLL}		Horizontal Phase Detector output pin. An external filter circuit between this pin and Pin 5 determines the selectivity of the phase detector and provides the feedback path for the horizontal phase locked loop.

* All pins except (V_{CC} and V_{EE}) have ESD diodes between V_{CC} and V_{EE}.

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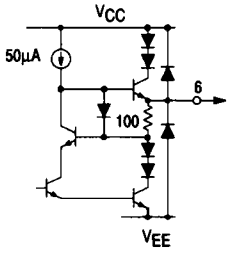
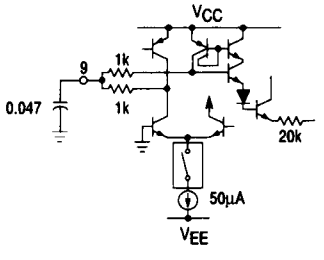
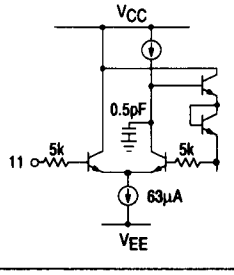
PIN DESCRIPTIONS

Pin	Symbol	Internal Equivalent Circuit	Description
6	+H		Horizontal Ramp output.
7	$-H^2$	(See Pin 6)	Complement Horizontal Parabola output.
8	$+H^2$		Horizontal Parabola output. The squared result of the positive horizontal ramp.
9	H^2clamp		Horizontal Parabola Clamping pin. An external capacitor works to cancel DC offset. Typically coupled to ground with a 0.047 µF capacitor.
10	Gnd		Ground Connection.
11	Sine H Drive		Sine H Drive. A ramp waveform input here will produce a sine wave output (at Pins 12 and 13) with frequency varying with input ramp amplitude, and phase varying with ramp DC offset. Dynamic input impedance is nominally greater than 1.0 MΩ.
12	+Sine H	(See Pin 6)	+Sine H output. The sine wave output developed from the input at Pin 11.
13	–Sine H		–Sine H output. A 180° phase shifted version of +Sine H.
14	Sine 2H Drive	(See Pin 11)	Sine 2H Drive. A ramp waveform input here will produce a sine wave output (at Pins 15 and 16) with frequency varying with input ramp amplitude and phase varying with ramp DC offset. Dynamic input impedance is nominally greater than 1.0 MΩ.
15	+Sine 2H	(See Pin 6)	+Sine 2H output. The sine wave output developed from the input at Pin 14.

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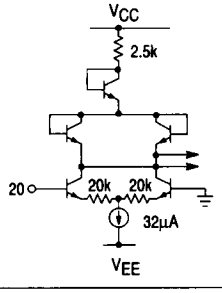
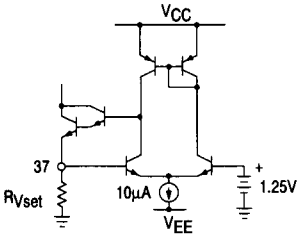
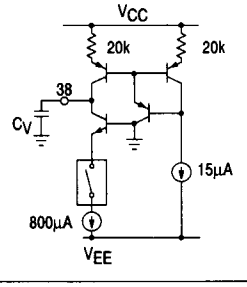
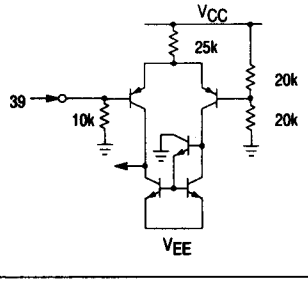
PIN DESCRIPTIONS

Pin	Symbol	Internal Equivalent Circuit	Description
16	–Sine 2H	(See Pin 6)	–Sine 2H output. A 180° phase shifted version of +Sine 2H.
17	$+H^3$		Horizontal Cubic output.
18	$-H^3$		Complement Horizontal Cubic output.
19	H^3_{clamp}	(See Pin 9)	Cubic Clamping pin. An external capacitor works to cancel DC offset. Typically coupled to ground with a 0.047 µF capacitor.
20	H'_{in}		H' Input. Dynamic input impedance in excess of 1.0 MΩ. Valid input voltage range is between V_{EE} and V_{CC}.
21	V'_{in}	(See Pin 20)	V' Input. Dynamic input impedance in excess of 1.0 MΩ. Valid input voltage range is between V_{EE} and V_{CC}.
22	H' V' Clamp	(See Pin 9)	H'_{in}, V'_{in} and H' V' Amplitude Product Clamping pin. An external capacitor works to cancel DC offset. Typically coupled to ground with a 0.047 µF capacitor.
23	H' V' out	(See Pin 6)	H' V' Output Pin. The product of H'_{in}, V'_{in}, H' V' amplitude must be less than 1.9 Vp-p.
24	H' V' Amplitude	(See Pin 20)	H' V' Amplitude. Dynamic input impedance in excess of 1.0 MΩ. Valid input voltage range is between V_{EE} and V_{CC}.
25	+Sine 2V	(See Pin 6)	+Sine 2V output. The sine wave output developed from the input at Pin 27.
26	–Sine 2V		–Sine 2V output. A 180° phase shifted version of +Sine 2V.
27	Sine 2V Drive	(See Pin 11)	Sine 2V Drive. A ramp waveform input here will produce a sine wave output (at Pins 25 and 26) with frequency varying with input ramp amplitude, and phase varying with ramp DC offset. Input impedance is nominally greater than 1.0 MΩ.
28	+Sine V	(See Pin 6)	+Sine V output. The sine wave output developed from the input at Pin 30.
29	–Sine V		–Sine V output. A 180° phase shifted version of +Sine V.
30	Sine V Drive	(See Pin 11)	Sine V Drive. A ramp waveform input here will produce a sine wave output (at Pins 28 and 29) with frequency varying with input ramp amplitude, and phase varying with ramp DC offset. Input impedance is nominally greater than 1.0 MΩ.

PIN DESCRIPTIONS

Pin	Symbol	Internal Equivalent Circuit	Description
31	Gnd		Ground connection.
32	V^2_{clamp}	(See Pin 9)	Vertical Parabola Clamp pin. An external capacitor works to cancel DC offset. Typically coupled to ground with a 0.047 µF capacitor.
33	$+V^2$	(See Pin 6)	Vertical Parabola.
34	$-V^2$		Complement Vertical Parabola.
35	+V		Vertical Ramp.
36	–V		Complement Vertical Ramp.
37	f_{Vset}		Vertical Charge Current Set. An internally regulated 1.25 Vdc, and the external resistance (R_{Vset}) at this pin determines the charging current for the capacitor, C_V, connected to Pin 38.
38	f_V		Vertical Ramp Generator Capacitor (C_V). The charge and discharge rate of the capacitor at this pin determines the vertical ramp rate.
39	V_{in}		Positive Vertical Flyback input pin. Presents 10 kΩ to input waveform. (See Figure 3). Threshold is at $V_{CC}/2$.
40	V_{EE}		Negative Supply pin. Requires 43 mA at –5.5 < Vdc < –4.5.

FUNCTIONAL DESCRIPTION

Introduction

The MC1388 is a multi-frequency capable integrated circuit used for geometry correction in monitors and HDTV receivers. With a few inputs the MC1388 will provide ten functions, eight with complements, as output waveforms. These waveforms can then be used by the control circuitry in any combination to modulate the horizontal and vertical deflection currents for geometry correction.

The MC1388 accomplishes multi-frequency operation by allowing external components to determine the nominal frequency of operation. This is done by choosing resistor-capacitor pairs for the desired horizontal and vertical oscillator frequencies. The horizontal and vertical sync inputs then provide the timing reference to which the output waveforms of the MC1388 adhere.

Horizontal Timing

To ensure proper horizontal timing, the MC1388 uses a phase-locked-loop to provide a reliable time base. The loop is externally accessible at the current controlled oscillator (ICO), Pins 3, 4, and at the output of the phase detector, Pin 5. Figure 2 shows relevant internal circuitry and pin connections. This allows the system designer to tailor the timing and performance of the MC1388.

The ICO is an RC type in which the horizontal frequency is determined by the charge and discharge rate of the capacitor at Pin 3. During charging, the voltage on the capacitor (CH) is increased until it reaches an internally determined trip level. At this trip level the direction of the current at Pin 3 is reversed and the discharge process begins. During discharge, circuitry diverts the current available at Pin 3 internally and the capacitor discharges quickly to the bottom trip level where control circuitry switches the direction of Pin 3 current and the cycle begins again.

The charging current at Pin 3 is determined by the current out of Pin 4, which is mirrored at Pin 3. The current out of Pin 4 is set by a nominal 1.25 V stable reference and the external resistance at this node (R_{Hset}). This also provides a means of modulating the charging current at Pin 3 by injecting the error current from the phase detector (Pin 5).

At Pin 5(H_{PLL}) are the filter components of the horizontal phase-locked-loop.These components were chosen to ensure fast tracking over the possible horizontal operating frequencies and a capture range equal to the lock range over these operating frequencies. (Refer to application notes AN553 and AN535 for information regarding design of the filter). The feedback resistor R_F, and the frequency setting capacitor C_H, are also components of the the horizontal phase-locked-loop. R_F serves two purposes, it provides the feedback path for the error current to Pin 4, and is a factor in the phase detector sensitivity which sets the amount of feedback. C_H influences the characteristics of the loop by being a factor in the oscillator sensitivity.

The error current from the phase detector is determined by the static phase error between the free running frequency and the frequency of the horizontal input at Pin 2, and the value of feedback resistance (R_F) between Pins 4 and 5. The output of the phase detector, Pin 5, will develop a voltage as a result of the phase detector error current acting on the H_{PLL} filter. This voltage difference will appear between Pins 5 and 4 and produce the error current provided to the horizontal oscillator. This error current is:

$$I_{ERROR} = \frac{(V_5 - V_4)}{R_F}$$

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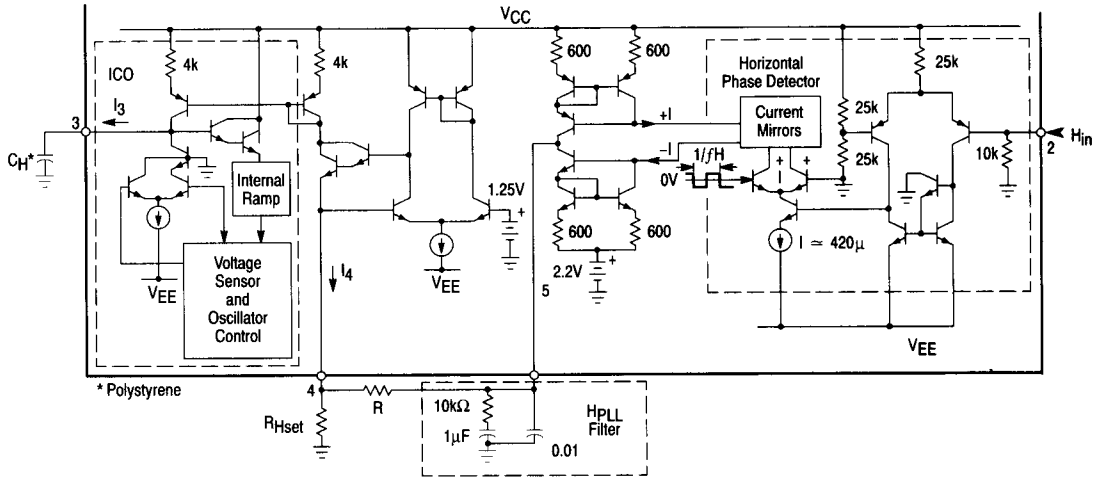
Figure 2. Horizontal Timing



The average voltage difference ($V_5 - V_4$) is capable of approximately ±2.5 V. The changing current is then defined by:

$$I_3 = I_4 = \frac{1.25\ V}{R_{Hset}} - I_{ERROR}$$

Vertical Timing

Vertical timing for the MC1388 is determined by the frequency of the input at Pin 39 and the charging rate of the capacitor at Pin 38. Representative circuitry for relevant pins is shown in Figure 3. The vertical timing is set by an injection oscillator, with the frequency of the generated ramp being determined by the current drawn out of Pin 37.That current is also set with a stable 1.25 Vdc reference and the resistance (R_{Vset}) at this pin. At the beginning of a vertical cycle, the current sourced by Pin 37 is mirrored out of Pin 38 charging the capacitor at Pin 38 with a constant current resulting in a linear ramp. *The charging current of the capacitor (C_V) must be set so the +V output (Pin 35) reaches 2.5 V just before the next vertical sync pulse arrives to trigger the discharge of the capacitor.* The current sourced by Pin 37 is then again provided to the capacitor and the cycle repeats.

WAVEFORMS

Sine Waveforms

The MC1388 has on board circuitry which is capable of producing sine wave like waveforms. Relevant circuitry is shown in Figure 4. A total of four subcircuits are available and each has a 0° and 180° phase shifted output.The sine wave generators require a ramp input which can be provided by the horizontal and vertical ramp outputs of the MC1388.

By modifying the input ramp, the output sine wave can be tailored to meet particular requirements for geometry correction. Figure 5 illustrates an example of geometry errors and the waveforms needed to correct the top to bottom geometry errors. The ramp amplitude affects the number of sine wave cycles and the ramp offset affects the phase. By doubling the peak-to-peak amplitude of an input ramp which created one complete period, a sine wave of two complete periods is produced. By adding DC offset to the input ramp, phase advance or delay is produced. Input ramps to the sine wave generators, which should be DC coupled to provide bias current, are presented to transistor bases with high dynamic impedances in excess of 1.0 MΩ. A means of applying an adjustable ramp is shown in the application section.

Figure 4. Sine Wave Generator

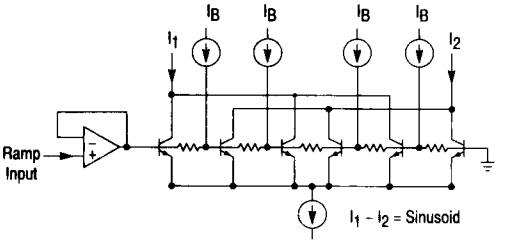


Figure 5. Sine Wave Adjustments

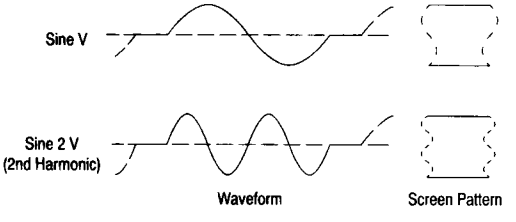
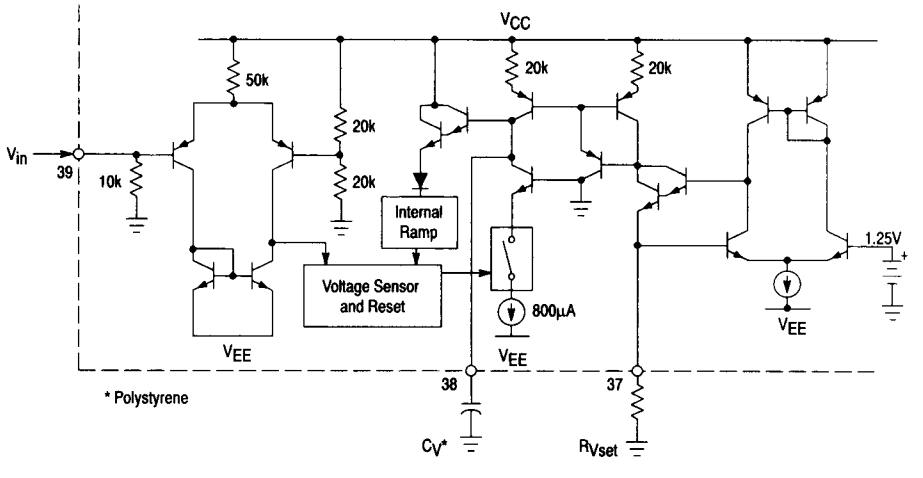


Figure 3. Vertical Timing



Three Input Multiplier (H'_{in}, V'_{in} and H' V' Amplitude)

Pins 20, 21 and 24, are the inputs to a multiplier with the output at Pin 23. All three inputs, although named differently, are the same internally and can be combined in any means to provide the desired output. However, the product of the three inputs is restricted to less than 1.9 Vp-p or the output waveform will experience current limiting. Input bias current must be provide and therefore the input waveforms require DC coupling. The output is clamped and blanked during the appropriate intervals.

Internally Generated Waveforms

Within the MC1388, operations are performed on the horizontal and vertical ramps to produce several waveforms before being provided as outputs through buffers.

Of the internally generated waveforms resulting from operations on the horizontal ramp are a blanked version of the horizontal ramp (+H, Pin 6). A blanked, clamped and squared version of the horizontal ramp ($\pm H^2$, Pins 7 and 8), and a blanked, clamped and cubed version of the horizontal ramp($\pm H^3$, Pins 17 and 18).

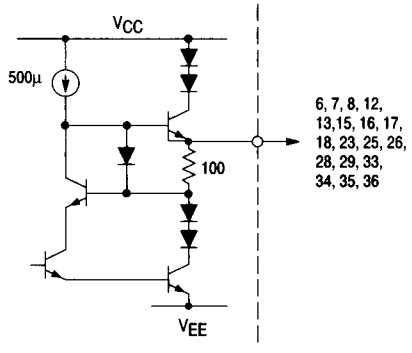
The vertical ramp is blanked and provided at Pins 35 and 36 ($\pm V$). Also, a squared, clamped, and blanked version of the vertical ramp is provided at Pins 33 and 34 ($\pm V^2$).

Blanking of the waveforms occurs once every vertical retrace. Clamping occurs during this blanked interval.

Outputs Buffers and Clamps

The 18 output waveforms are buffered and made available at the output pins. The output buffers are capable of supplying 5.0 mA. A simplified schematic of the output stage is shown in Figure 6.

Figure 6. Output Circuitry



Although all outputs are blanked once each vertical period, not all of them are clamped. Clamping is performed only on the horizontal and vertical parabola outputs ($\pm H^2$, $\pm V^2$), the horizontal cubic outputs ($\pm H^3$), and the three-input multiplier output (H' V'_{out}). Clamping occurs after the leading edge of a vertical sync pulse. Blanking logic zeros the outputs for the time spanned by the first two horizontal pulses during the vertical sync period (see Figure 7B). Clamping circuitry works for the line period between the first two horizontal blanking intervals. Clamping is done by storing a voltage on the clamp capacitor that is proportional to the current required to force the output voltage of the buffer to zero. This provides a sustained current for the next vertical period that is capable of cancelling the DC offset in the waveform. Internal circuitry present at the clamp pins is shown in Figure 7A, and a diagram showing relative timing is shown in Figure 7B.

Figure 7A. Clamp Circuitry for Output Waveforms

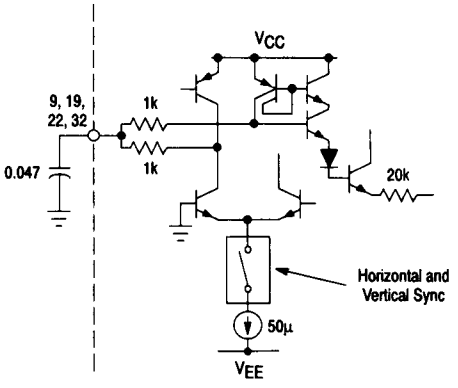
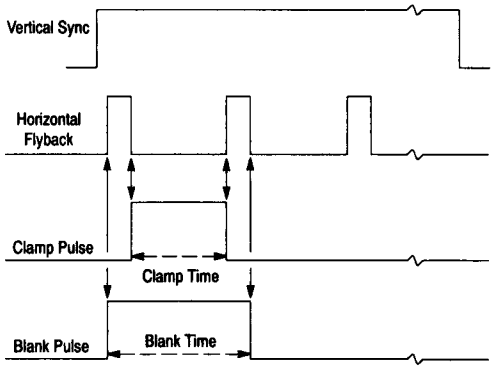


Figure 7B. Blanking and Clamping Diagram



9

APPLICATION INFORMATION

The following information is provided to assist designing in the MC1388.

Horizontal and Vertical Flyback Inputs

Waveforms to the horizontal and vertical flyback inputs (Pins 2 and 39) must meet similar requirements except for the frequencies involved. The requirements can be described as follows:

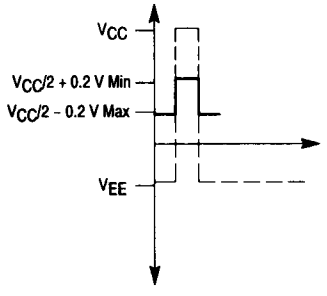
1) $V_{CC}/2.0 + 0.2\ V < V_{in}$ Peak $< V_{CC}$
2) $V_{EE} + 0.5 < V_{in}$ Baseline $\leq V_{CC}/2 - 0.2\ V$
3) 2.0 µs ≤ Pulse Width < $1/(2\ f_H)$ (Horizontal Input)
   2.0 µs ≤ Pulse Width < $1/(2\ f_V)$ (Vertical Input)

and the allowable frequencies of operation are:

A) 10 kHz ≤ f_H ≤ 63 kHz
B) 45 Hz ≤ f_V ≤ 120 Hz

Figure 8 shows the restrictions on the voltage levels for the flyback inputs.

Figure 8. Valid Input Levels for Both the Horizontal (Pin 2) and the Vertical (Pin 39) Inputs.



Since the input pins are equipped with ESD diodes, voltages on these pins should never exceed V_{CC} or V_{EE} by more than 0.5 V.

Horizontal Oscillator and Phase-Locked-Loop

Since the charge and discharge of the capacitor at Pin 3 (C_H) is done with constant currents, the voltage waveform of the capacitor voltage is:

$$\pm\Delta V = \pm \frac{I\,\Delta t}{C}$$

,where Δt is the trace or retrace time.

The horizontal frequency is then the inverse of the sum of the charge time and the discharge time,

$$f_{horizontal} = \frac{1}{(t_{charge} + t_{discharge})}$$

where, t_{charge} = trace time and $t_{discharge}$ = retrace time. This relates the trace and retrace time to element values, internal quantities and a design variable, I_{charge}. So,

$$t_{charge} = \frac{C_H\ \Delta Vp\text{-}p}{I_{charge}} \text{ and } t_{discharge} = \frac{C_H\ \Delta Vp\text{-}p}{I_{discharge}}$$

ΔVp-p and $I_{discharge}$ are fixed ($I_{discharge}$ is typically 1.0 mA and ΔVp-p is ≃ 2.5 ΔVp-p). If C_H is chosen to meet the requirements of retrace time and,

If C_H is chosen to meet the requirements of retrace time and, trace time >> retrace time, then t_{charge} >> $t_{discharge}$.

$$\text{then } f_{horizontal} \simeq \frac{1}{t_{charge}} \text{ or, } f_{horizontal} \simeq \frac{I_{charge}}{C_H\ \Delta V_{p\text{-}p}}$$

By choosing C_H and determining I_{charge} the horizontal frequency can be set, since ΔVp-p is known. Referring to Figure 2, the current out of Pin 4 is the current I_{charge} and is composed of,

$$I_{charge} = \frac{1.25}{R_{Hset}} - I_{ERROR}$$

where I_{ERROR} is the current from the phase detector when the loop is locked and was determined in the FUNCTIONAL DESCRIPTION to be,

$$I_{ERROR} = \frac{(V_5 - V_4)}{R_F}$$

The horizontal frequency is now defined and is,

$$f_{horizontal} = \left\{\frac{1.25}{R_{Hset}} \pm \frac{(V_5 - V_4)}{R_F}\right\}\left(\frac{1}{C_H\ \Delta V_{p\text{-}p}}\right) \text{ or,}$$

$$f_{horizontal} = f_{free\ run} \pm \Delta f,$$

where Δf is the frequency difference between the horizontal free run frequency and the frequency of the input signal, R_{Hset} is the resistance from Pin 4 to ground, R_F is the resistor between Pins 4 and 5, and C_H is the capacitor from Pin 3 to ground. *It is to be emphasized that this equation holds true only when the loop is locked.*

The phase detector sensitivity, K_{PD}, is determined from the slope of the curve which describes the average current output from the phase detector and the phase error related to that current. It is defined by,

$$K_{PD} \simeq \frac{2\ I_{PDmax}}{SW\ 2\pi f_H}\ (A/rad) \text{ or, } \frac{900 \bullet 10^{-6}}{SW\ 2\pi f_H}\ (A/rad).$$

I_{PDmax} is the maximum current that can be sourced or sinked from the phase detector and SW is the width of the horizontal flyback input pulse in seconds. f_H is the frequency of the horizontal flyback input.

The oscillator sensitivity, K_O, defined by $\partial f_H/\partial I$ is,

$$K_O \simeq \frac{1}{2.5\ C_H}\ (Hz/A)$$

Since the maximum average voltage difference between Pins 4 and 5 is capable of about ±2.5 V, the maximum error current transfer from Pin 5 to Pin 4 is,

$$I_{ERRORmax} \leq \frac{\pm\ 2.5\ V}{R_F}.$$

And also redefines the phase detector sensitivity as,

$$K_{PD'} \simeq \frac{2.5\ V}{R_F\ \pi\ SW f_H}$$

The product of the phase detector sensitivity, the oscillator sensitivity and the maximum phase error then defines maximum possible deviation from the free run frequency. The maximum possible phase error is the phase error corresponding to one half the width of the horizontal flyback input pulse or, (SW/2), $2\pi f_H$, so the maximum deviation from the free run frequency is one half the lock range and is,

$$\pm \frac{f_{Flock}}{2} \simeq \frac{1}{C_H R_F}.$$

(The value of f_{Flock} should be kept small enough to prevent loop lock on harmonics. A general rule of thumb is f_{lock} < 10% of the desired horizontal frequency.) Then I_{ERROR} is less than 10% of I_{charge}, and the horizontal frequency is almost entirely determined by,

$$f_{horizontal} \simeq \frac{1.25}{R_{Hset}\, C_H\, \Delta V_{p\text{-}p}}, \quad \Delta V\ p\text{-}p \simeq 2.5,$$

so this becomes, $f_{horizontal} \simeq \frac{1}{2\, R_{Hset}\, C_H}$,

which is also the horizontal free run frequency. The horizontal free run frequency should be set at or very near the desired horizontal frequency since the lock range is centered about this frequency.

Calculating the external components is then based on the following requirements:

1) The value of C_H satisfies the requirements for retrace time, or $C_H \leq 5.6 \bullet 10^{-4}\ t_{discharge}$.
2) The value of the resistance from Pin 5 to ground is given by,

$$R_{Hset} \simeq \frac{1}{2\, f_{horizontal}\, C_H}.$$

(The value of the resistor calculated for R_{Hset} should be considered approximate. The 5.0 kΩ pot shown in the application circuit of Figure 12 is recommended for optimization).

3) The resistor R_F is such that the lock range is a reasonable choice (f_H/10) given by,

$$R_F \simeq \frac{2}{C_H\, (\pm\ f_{lock})}.$$

For 15,625 Hz, recommended values are, C_H = 0.001 µF, R_{Hset} = 30 kΩ + 5.0 kΩ variable, and $R_F \geq$ 620 kΩ. For 31,250 Hz, recommended values are, C_H = 0.001 µF, R_{Hset} = 13 kΩ + 5.0 kΩ variable, and $R_F \geq$ 300 kΩ.

Vertical Timing

To set the vertical timing a capacitor-resistor pair must be chosen (refer to Figure 3). The vertical timing section is similar to the horizontal section in that the frequency is determined by the charge and discharge rate of a capacitor at Pin 38. However, the vertical ramp oscillator is an injection type and the proper peak-to-peak voltage must be set with R_{Vset}.

The basic equation,

$$\pm \Delta V = \pm \frac{I\, \Delta t}{C_V},$$

describes the capacitor voltage for the charge and discharge currents made available at Pin 38. Further, if $t_{retrace} << t_{trace}$ then,

$$f_{vertical} = f_V \simeq \frac{1}{\Delta t_{trace}} = \frac{1}{\Delta t_{charge}}$$

and the vertical frequency is determined by the charging current, ΔV and the capacitor value.

The reference voltage for developing the charging current is present at Pin 37 and is nominally 1.25 V. The charging current is then defined by the resistance at this node,

$$I_{charge} = \frac{1.25}{R_{Vset}}.$$

The resistance required can be determined for a particular frequency and capacitor combination. *The capacitor voltage, ΔV, must be nominally 2.5 Vp-p for the specified full scale vertical outputs.* Using this value, the proper combination R_{Vset} and C_V, can be calculated.

The current available to discharge C_V is approximately 800 µA. So, a practical C_V value is described by, $C_V \leq 3.2 \bullet 10^{-4}\ \Delta t$, where Δt is required retrace time.

This value of C_V is next used to calculate the value R_{Vset} considering the vertical frequency desired,

$$I_{charge} = \frac{1.25}{R_{Vset}} = \frac{C_V\, \Delta V}{\Delta t} = C_V\, \Delta V\, f_V \text{ or,}$$

$$R_{Vset} \simeq \frac{1.25}{C_V\, \Delta V\, f_V} = \frac{1.25}{C_V\, 2.5\, f_V} \simeq \frac{1}{2\, C_V\, f_V}$$

(The equation given for R_{Vset} is approximate and should be used only as a starting point. The 25 kΩ pot in the applications circuit of Figure 12 is used to optimize this value.)

9

Sine Wave Generation

Shown in Figure 9 and 10 are two circuits which can be used to provide drive to the sine generator circuits. These circuits DC couple to the sine drive inputs providing the necessary base drive. The circuit in Figure 9 will provide adequate ramp amplitude for a single cycle of a sine wave at the horizontal or vertical frequency and the circuit in Figure 10 will provide adequate ramp amplitude for two cycles of a sine wave.

Figure 9. Sine H or V Driver

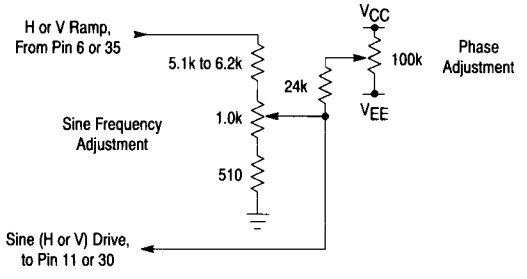
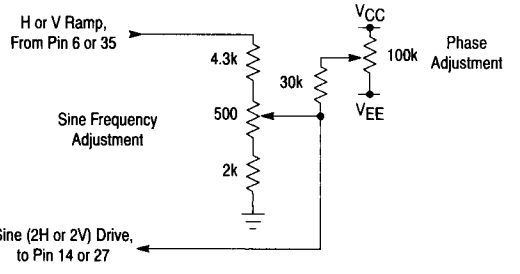


Figure 10. Sine 2H or 2V Driver



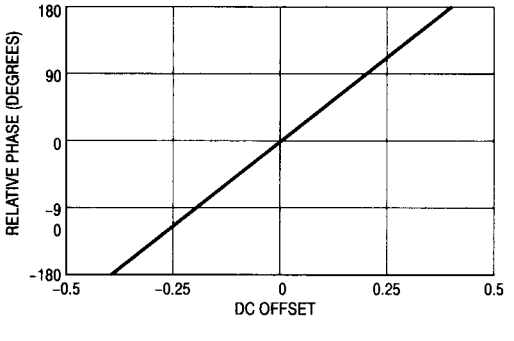
An approximate relation between the number of cycles and peak-to-peak input voltage is,

$$V_{inp\text{-}p} \approx \frac{\text{number of cycles} + 0.2}{1.25}$$

The phase of the output sine wave is a function of the input ramp DC offset. Figure 11 shows the relationship between the phase and the offset.

If a phase change is desired, it should be remembered that the input windows for the sine generators are between –850 mV and +850 mV centered about zero, therefore, a DC offset will reduce the allowable input ramp peak-to-peak amplitude.

Figure 11. Phase versus DC Offset



Multiplier Circuit

The multiplier is made up of three inputs, H′$_{in}$, V′$_{in}$ and H′V′ Amplitude (Pins 20, 21 and 24 respectively), which are internally equivalent. The voltage output on Pin 23 is the product of the voltage on the input pins and is restricted to a maximum output voltage of 1.9 Vp-p, or current limiting will occur. Any combination of the three inputs can be used, provided that the product of all the inputs is less than 5.0 Vp-p.

Application Circuit

Figure 12 shows an application circuit with component values applicable for,

$f_{horizontal}$ = 31.25 kHz $f_{vertical}$ = 60 Hz

$\pm f_{lock} \simeq$ 2.3 kHz $\pm f_{pull\text{-}in} \simeq$ 2.3 kHz

Figure 13 shows the timing of all the vertical waveforms for the application circuit. Figure 14 shows the timing of all the horizontal waveforms for the application circuit.

Figure 12. Application Circuit of the MC1388

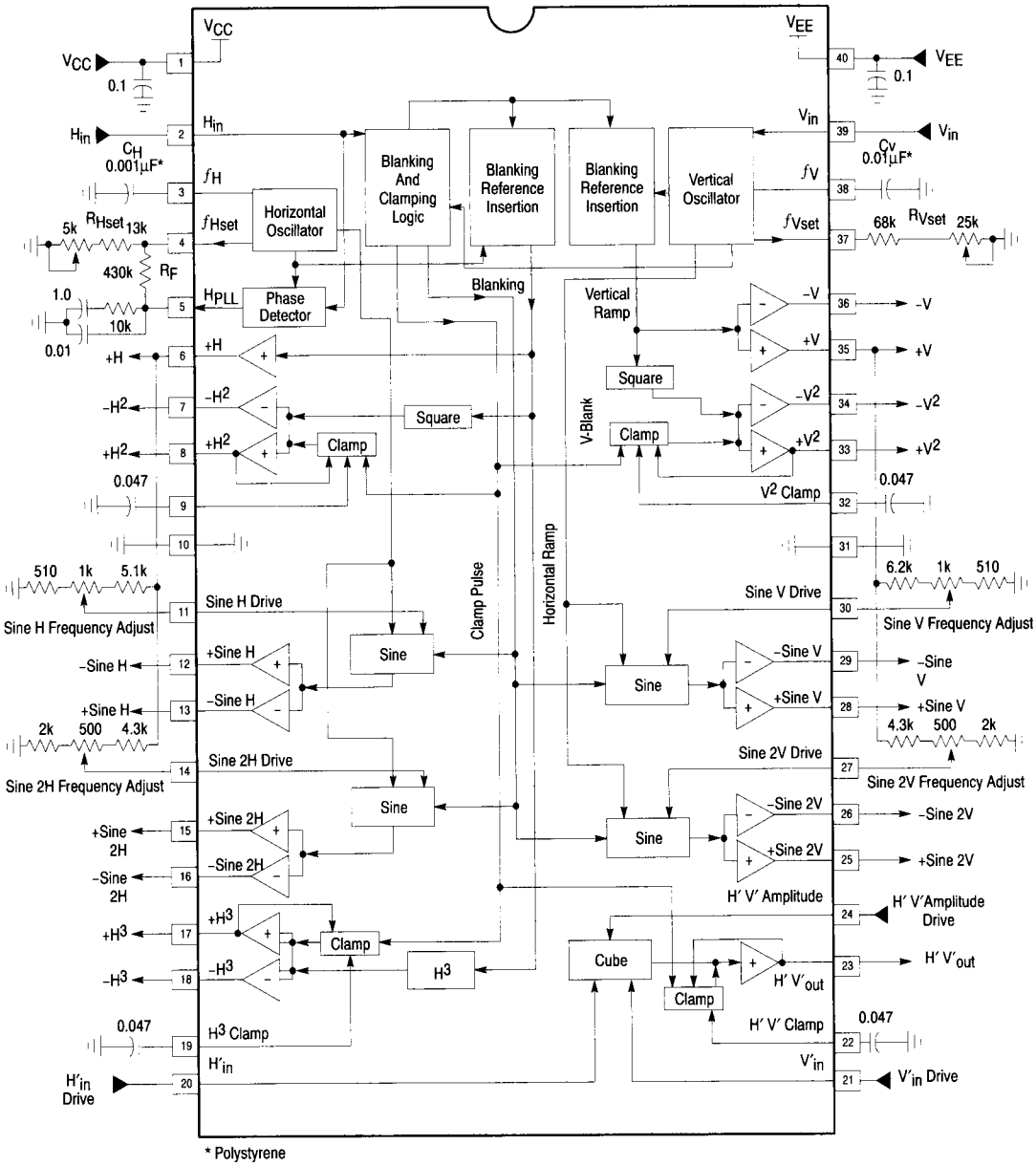


Figure 13. Vertical Timing

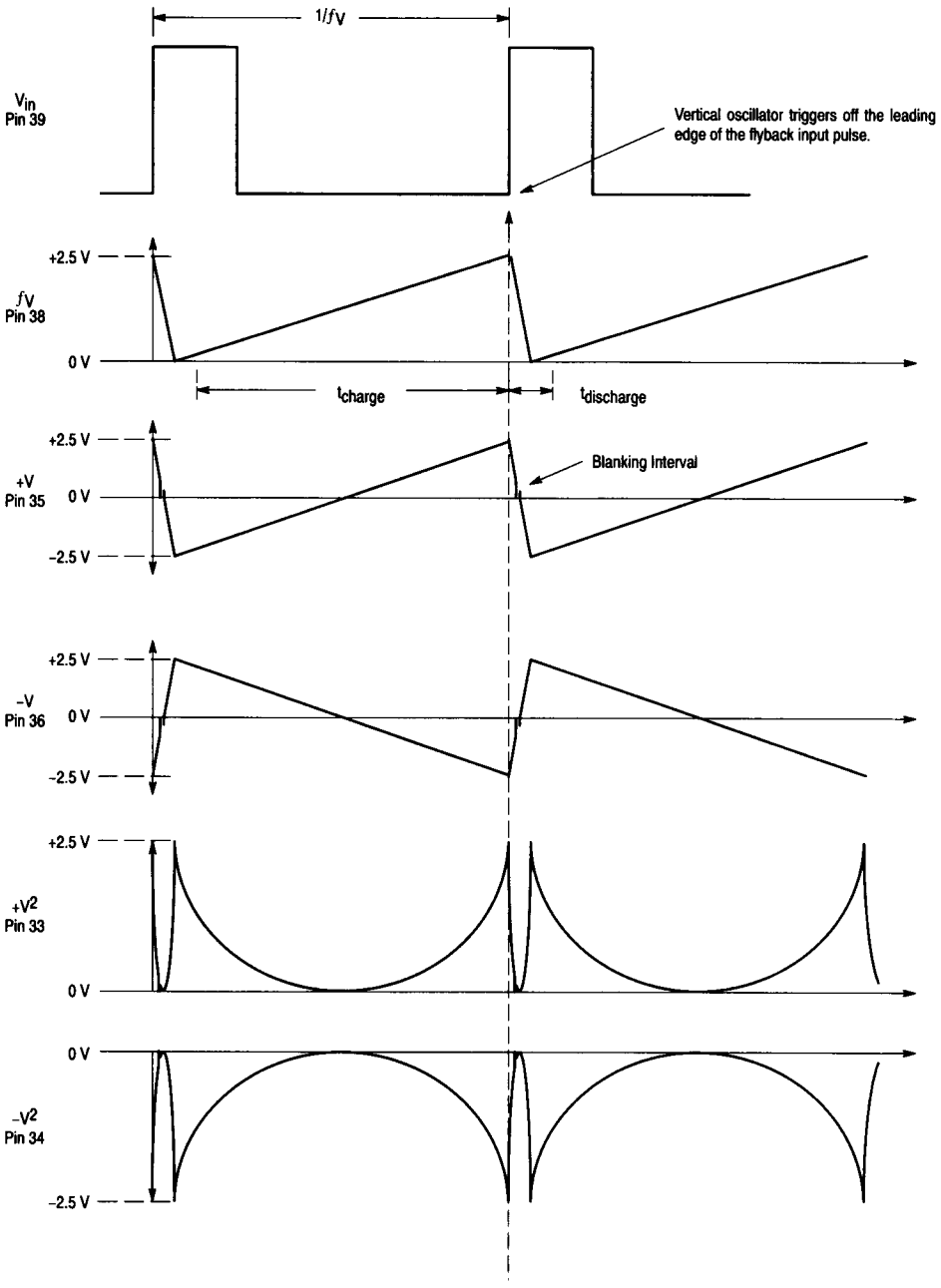


Figure 13. Vertical Timing (continued)

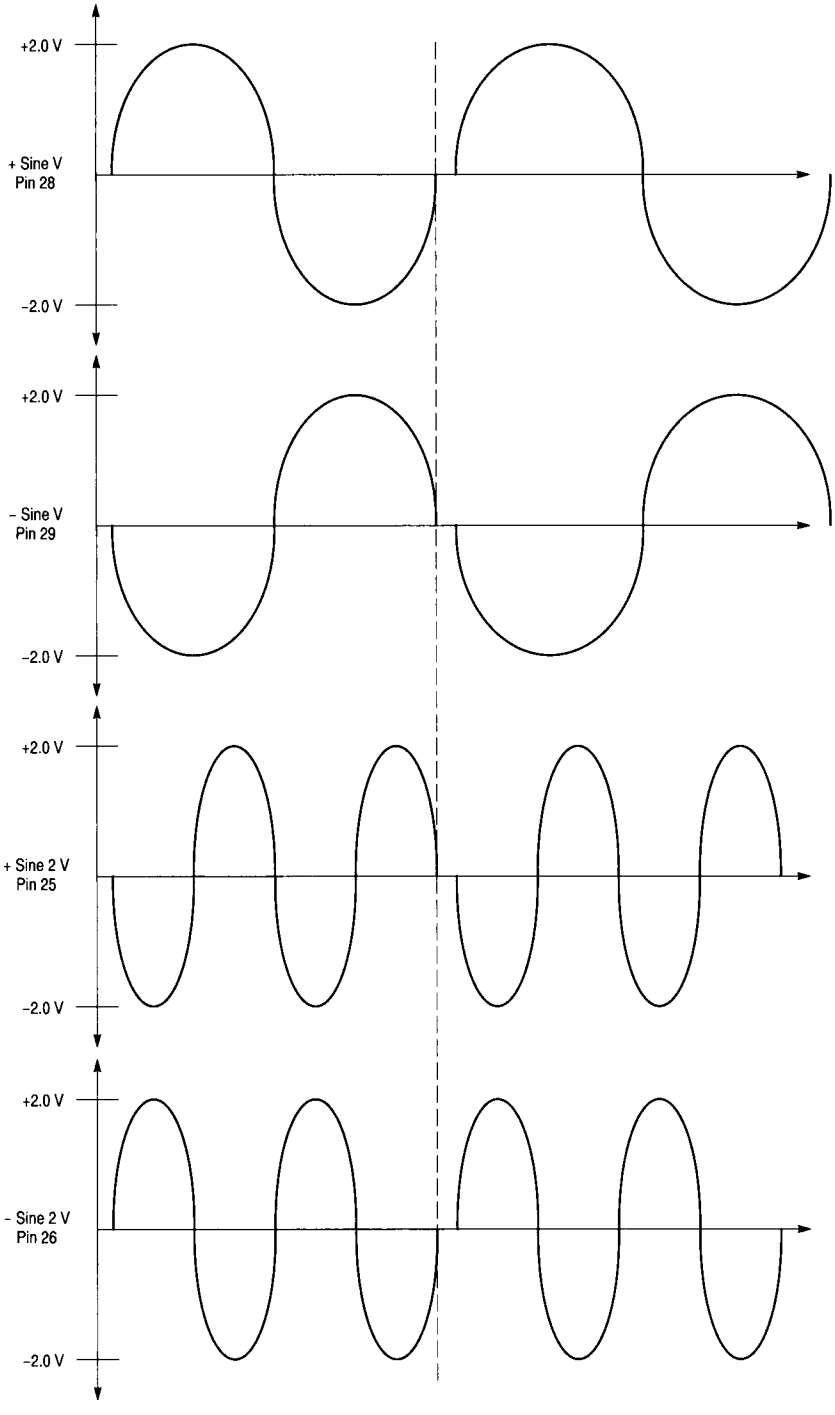


Figure 14. Horizontal Timing

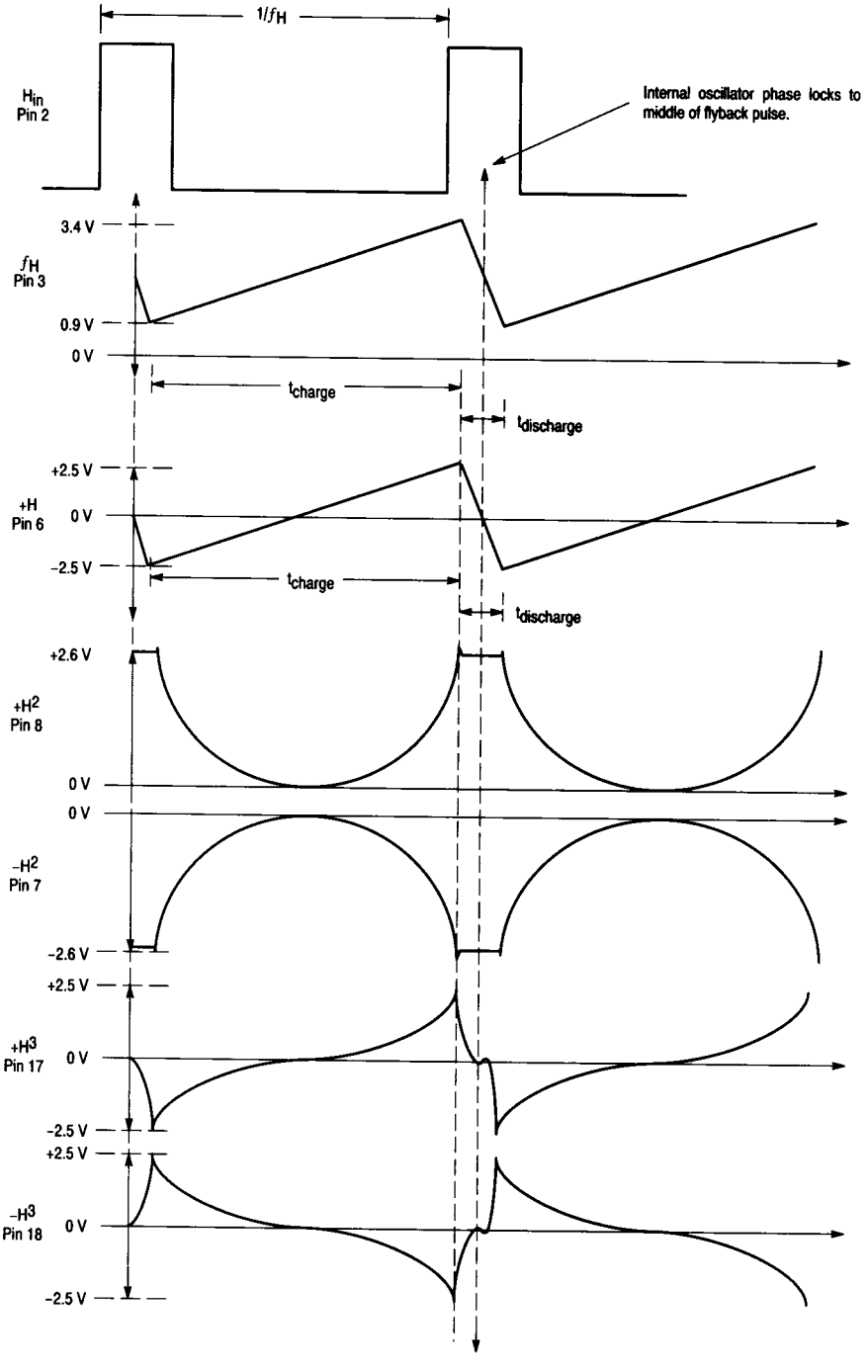


Figure 14. Horizontal Timing (continued)