

FEATURES

- 3.3 and 5V power supply options
- 440ps propagation delay
- Separate and common select
- High bandwidth output transitions
- Internal 75KΩ input pull-down resistors
- ESD protection of 2000V
- Available in 20-pin SOIC package

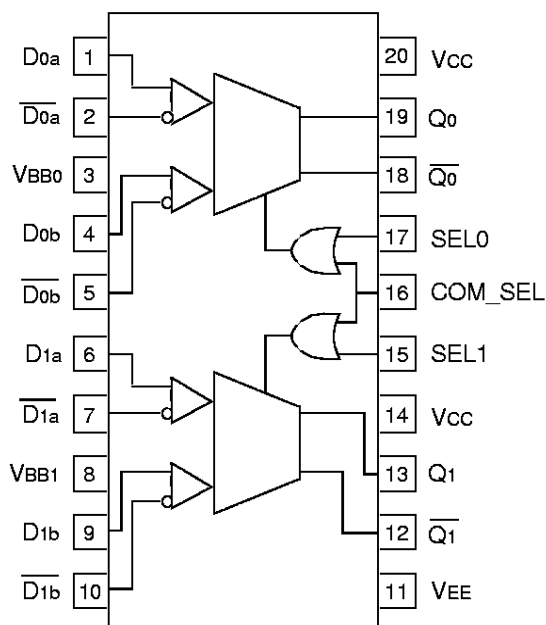
DESCRIPTION

The SY100EL56V is a dual, fully differential 2:1 multiplexer. The differential data path makes the device ideal for multiplexing low skew clock or other skew sensitive signals. Multiple VBB pins are provided to ease AC coupling input signals.

The device features both individual and common select inputs to address both data path and random logic applications.

The differential inputs have special circuitry which ensures device stability under open input conditions. When both differential inputs are left open the D input will pull down to VEE, the \bar{D} input will bias around $V_{CC}/2$ forcing the Q output LOW.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

TRUTH TABLE

SEL	Data
H	a
L	b

PIN NAMES

Pin	Function
D0a–D1a	Input Data a
D0b–D1b	Input Data b
SEL0–SEL1	Individual Select Input
COM_SEL	Common Select Input
Q0–Q1	True Outputs
$\bar{Q}0$ – $\bar{Q}1$	Inverted Outputs

DC ELECTRICAL CHARACTERISTICS⁽¹⁾

$V_{EE} = V_{EE} (\text{Min})$ to $V_{EE} (\text{Max})$; $V_{CC} = \text{GND}$

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
IEE	Power Supply Current	—	20	24	—	20	24	—	20	24	—	20	24	mA
VBB	Output Reference Voltage	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	V
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	μA
I _{INL}	Input LOW Current	$\overline{\text{Dn}}$	0.5	—	—	0.5	—	—	0.5	—	—	0.5	—	μA
		Dn	-600	—	—	-600	—	—	-600	—	—	-600	—	μA
V _{PP} (DC)	Input Sensitivity ⁽²⁾	50	—	—	50	—	—	50	—	—	50	—	—	mV

NOTES:

- Parametric values specified at: 100EL56V Series: (-3.0V to -3.8V) or (-4.2V to -5.5V)
- Differential input voltage required to obtain a full ECL swing on the outputs.

AC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE} (\text{Min})$ to $V_{EE} (\text{Max})$; $V_{CC} = \text{GND}$

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t _{PLH}	Propagation D (Diff)	340	—	540	350	—	550	360	—	560	380	—	580	ps
t _{PHL}	Delay D (SE)	290	—	590	300	—	600	310	—	610	330	—	630	ps
	to Output SEL	430	—	730	440	—	740	440	—	740	450	—	750	
	COM_SEL	430	—	730	440	—	740	440	—	740	450	—	750	
t _{SKEW}	Within Device Skew ⁽¹⁾	—	40	80	—	40	80	—	40	80	—	40	80	ps
	Duty Cycle Skew ⁽²⁾	—	—	100	—	—	100	—	—	100	—	—	100	ps
V _{PP} (AC)	Minimum Input Swing ⁽³⁾	150	—	1000	150	—	1000	150	—	1000	150	—	1000	mV
V _{CMR}	Common Mode Range													V
	$V_{EE} = -3.0\text{V}$ to -3.8V ⁽⁴⁾													
	$V_{PP} < 500\text{mV}$	-2.0	—	-0.4	-2.1	—	-0.4	-2.1	—	-0.4	-2.0	—	-0.4	
	$V_{PP} \geq 500\text{mV}$	-1.8	—	-0.4	-1.9	—	-0.4	-1.9	—	-0.4	-1.9	—	-0.4	
$V_{EE} = -4.2\text{V}$ to -5.5V ⁽⁵⁾	$V_{PP} < 500\text{mV}$	-3.2	—	-0.4	-3.3	—	-0.4	-3.3	—	-0.4	-3.3	—	-0.4	
	$V_{PP} \geq 500\text{mV}$	-3.0	—	-0.4	-3.1	—	-0.4	-3.1	—	-0.4	-3.1	—	-0.4	
t _r t _f	Output Rise/Fall Times Q (20% -80%)	200	—	540	200	—	540	200	—	540	200	—	540	ps

NOTES:

- Within device skew is defined as identical transitions on similar paths through a device.
- Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
- Minimum input swing for which AC parameters are guaranteed.
- The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} (min) and 1V. The lower end of the CMR range varies 1:1 with V_{EE} . The numbers in the spec table assume a nominal $V_{EE} = -3.3\text{V}$. Note for PECL operation, the V_{CMR} (min) will be fixed at $3.3\text{V} - |V_{CMR} (\text{min})|$.
- The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} (min) and 1V. The lower end of the CMR range varies 1:1 with V_{EE} . The numbers in the spec table assume a nominal $V_{EE} = -4.5\text{V}$. Note for PECL operation, the V_{CMR} (min) will be fixed at $5.0\text{V} - |V_{CMR} (\text{min})|$.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100EL56VZC	Z20-1	Commercial
SY100EL56VZCTR	Z20-1	Commercial

20 LEAD PLASTIC SOIC (Z20-1)

FILE/REV #: PD0028A03

PD/0028/ASCORP

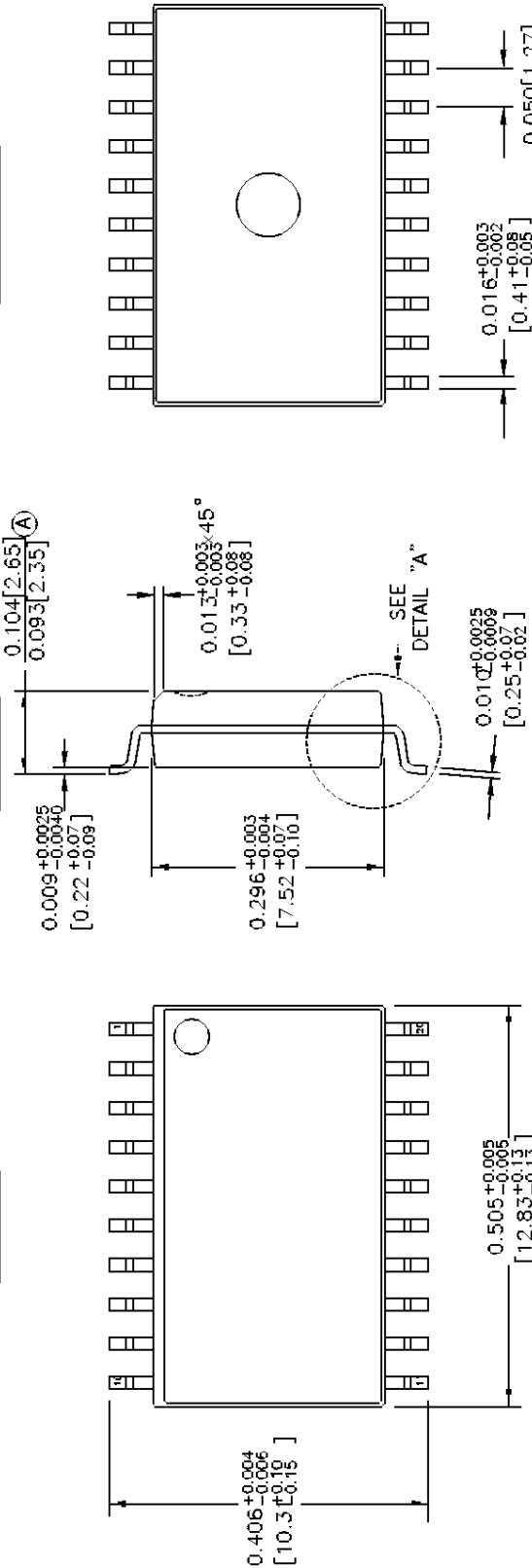
PAGE 1 OF 1

REV	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER VERSION 4.0 FORMAT	12/31/93
02	CONVERT DWG. TO AUTOCAD REL. 12. REFERENCE AM/OP DWG. NO. 00020 REV. 07. MAKE (A) SAME AS JEDEC.	02/28/96
03	CONVERT DWG. TO AUTOCAD REL. 13 AND ONE PAGE DOC. 02/09/98	

TOP VIEW

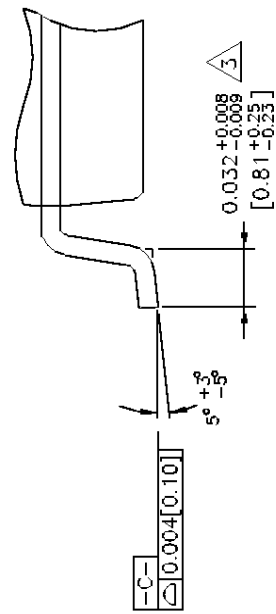
END VIEW

BOTTOM VIEW



NOTES:

1. DIMENSIONS ARE IN INCHES [MM]
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006 [0.15] PER SIDE.
4. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX / MIN



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APPROVALS	DATE	APPROVALS	DATE	SIZE	SCALE
ORIGINATOR: EMIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	N/A
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			REVISION 03
RELEASE DATE:					

20 LEAD PLASTIC SOIC (.300" WIDE)
PACKAGE OUTLINE

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