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IMS2800
High Performance 256K x 1 CMOS Dynamic RAM

inmos®

FEATURES

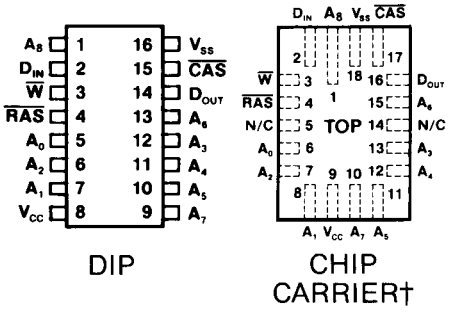
- Ultra High Speed—60, 70, 80, 100, 120 and 150ns $\overline{RAS}$ Access Times Over Full V_{CC} (4.5V to 5.5V) and Temperature (0°C to 70°C) Ranges
- Eliminates Traditional DRAM Multiplexed Address Timing Constraints
- INMOS' Advanced Field Shield Isolated CMOS Process Optimized for Speed
- All Inputs and Outputs are CMOS as Well as TTL Compatible
- Low Power (CMOS Input Levels)
  Standby—10mW
  Active—350mW at 120ns Cycle Times
- JEDEC Standard Pinout
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh as Well as $\overline{RAS}$ Only Refresh
- 4.4ms, 256 Cycle Refresh
- Single 5V ± 10% Supply
- Extended $\overline{RAS}$ Active Time to Facilitate Multiple Accesses Within a Row

DESCRIPTION

The IMS2800 is a 256K x 1 dynamic RAM that has been designed and processed for ultra high performance. The IMS2800 is fabricated with INMOS' advanced CMOS process resulting in low power while providing extremely wide operating margins as well as ultra high speed. The use of a Pseudo P-Well CMOS approach results in considerably lower soft error rates (Better than 64K dynamic RAMs). Furthermore, the use of $V_{CC/2}$ bit line precharging reduces on-chip internal noise, lowers average operating supply current, and reduces transient currents.

Innovative features as well as standard functional options on the IMS2800 provide the system designer with unprecedented DRAM memory design flexibility. With previous generations of DRAM products, the system designer was unable to take full advantage of the device performance of high speed DRAMs because of timing overhead associated with time division multiplexing the

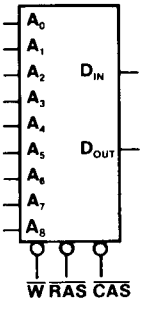
PIN CONFIGURATION



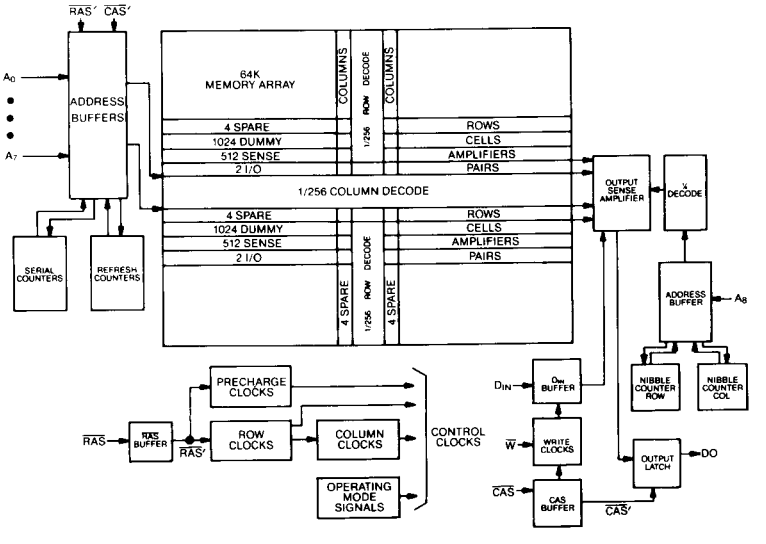
DIP CHIP CARRIER†

†Available in ceramic and plastic.

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_8	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{RAS}$	ROW ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{W}$	WRITE ENABLE
V_{CC}	+5 VOLT SUPPLY INPUT
V_{SS}	GROUND

DESCRIPTION (continued)

addresses. The IMS2800 chip design relieves this constraint by using asynchronous column address decoding in combination with on-chip transparent row address latches which allows a short (4ns; 2ns set-up and 2ns hold) row address capture window. This results in the performance limiting constraints associated with multiplexing the addresses being virtually eliminated. Now, it is possible to achieve system $\overline{RAS}$ access times as fast as 60ns which allows interfacing to the next generation of high speed microprocessors with no wait state penalty. Furthermore, systems that can take advantage of the asynchronous column address accessing (Static Column Decode) via page mode operations can achieve performance levels previously impossible without the use of high speed static RAMs.

The IMS2800 is a cost effective VLSI DRAM for applications that demand high density, reliability, high performance, and extremely wide operating margins. Inmos' improved address multiplexing technique utilizing Static Column Decoding (SCD) provides high density and ultra high performance without paying the power and cost penalties of using static RAM.

GENERAL

All cycles of the IMS2800 are initiated by a high-to-low transition of $\overline{RAS}$. For Read, Write, Read-Modify-Write, or $\overline{RAS}$-Only refresh cycles, the high to low transition of $\overline{RAS}$ causes the state of the 9 external address lines (A0 through A8) to be latched. Eight of the nine address bits are decoded to select one of 256 rows. The ninth row address bit (A8) is saved and becomes part of the ten bit column address which selects one of the 1024 column locations. The IMS2800 uses a transparent latch to capture the row addresses which permits an extremely short capture time for the row addresses with only a 2ns set-up and 2ns hold required. After the short row address capture time has been satisfied, the 9 external address lines can be changed to the column address. Since column address decoding on the IMS2800 is static (asynchronous or ripple-through), no address strobes are required to select 1 bit location out of the 512 column locations within the selected row address field. However, after the high-to-low transition of $\overline{RAS}$, the state of $\overline{CAS}$ and $\overline{W}$ determine whether the cycle is a Read, Write, Read-Modify-Write, or a $\overline{RAS}$-Only refresh cycle.

READ CYCLE

A read cycle is performed on one or more memory locations if $\overline{W}$ is high while both $\overline{RAS}$ and $\overline{CAS}$ are low. With $\overline{RAS}$ and $\overline{CAS}$ low while $\overline{W}$ is high, the output will reflect the contents of the cell addressed by the 9 latched row addresses and the current 9 column addresses provided that all read cycle (or Write-Verify/Write-Read cycle) timing conditions have been satisfied. Asynchronous page operations, where more than one location can be accessed during a single $\overline{RAS}$ active cycle, can be executed by simply changing the column address whenever a new bit within the present page (defined by the 9 latched row addresses) is being accessed. It is not necessary to toggle $\overline{CAS}$ in order to perform page mode read operations, but $\overline{CAS}$ can be toggled, if desired, for the purpose of enabling or disabling the data output buffers.

WRITE CYCLES

The IMS2800 will perform three types of write cycles: Early-Write, Late-Write, and Read-Modify-Write. A write cycle is initiated when $\overline{W}$, $\overline{CAS}$, and $\overline{RAS}$ are low.

If $\overline{W}$ goes low prior to $\overline{CAS}$ going low, an Early-Write cycle is executed. Early-Write cycles are initiated by the falling edge of $\overline{CAS}$ with set-up and hold times for both data-in and column addresses (Column addresses latched during Write cycles to provide additional noise immunity as well as allow pipelined write operations.) being referenced to the falling edge of $\overline{CAS}$. During Early-Write cycles, the data out will remain open (high impedance state) as long as $\overline{W}$ remains low. If $\overline{W}$ goes high following an Early-Write cycle, while $\overline{RAS}$ and $\overline{CAS}$ both remain low, the IMS2800 will execute a Write-Verify or a Write-Read cycle (See timing diagram).

If $\overline{CAS}$ goes low prior to $\overline{W}$ going low, a Late-Write is executed. Late-Write cycles are intiated by the falling edge of $\overline{W}$ with the set-up and hold times for both data-in and column addresses being referenced to the falling edge of $\overline{W}$. Prior to the $\overline{W}$ control input being asserted for a Late-Write cycle, all the input conditions for a read operation are satisfied ($\overline{RAS}$ and $\overline{CAS}$ are both low and $\overline{W}$ is high). If $\overline{W}$ is asserted after a valid read access occurs, the operation is called a Read-Modify-Write cycle. During a Read-Modify-Write cycle, the Data-out will reflect the contents of the addressed cell before it was written until $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$ go high. A Late-Write cycle where $\overline{W}$ is brought low prior to output data accessing will result in an indeterminate data output state, but whatever state was present at the time $\overline{W}$ goes low will be latched until $\overline{RAS}$, $\overline{CAS}$, or $\overline{W}$ go high.

REFRESH CYCLES

Dynamic RAMs retain data by storing charge on a capacitor. Since the charge will leak away over a period of time, it is necessary to access the data in the cell (capacitor) periodically in order to fully restore the stored charge while it is still at a sufficiently high level to be properly detected. For the IMS2800, any $\overline{RAS}$ sequence will fully refresh all storage cells within the single row addressed. To ensure that all cells remain sufficiently refreshed, all 256 rows (all binary combinations of address bits A0 through A7 must be refreshed every 4.4 mS.)

The addressing of the rows for refresh may be sourced either externally or internally. If the refresh row addresses are to be provided from an external source, $\overline{CAS}$ must be high when $\overline{RAS}$ goes low. If $\overline{CAS}$ is high when $\overline{RAS}$ goes low, any type of cycle (Read, Write, Read-Modify-Write, or $\overline{RAS}$-Only) will cause the externally addressed row to be refreshed.

If $\overline{CAS}$ is low when $\overline{RAS}$ falls, the IMS2800 will use an internal 8-bit counter as the source of the row addresses and will ignore the $\overline{W}$ (Write Enable) and the external address inputs. $\overline{CAS}$-Before-$\overline{RAS}$ refresh mode is a refresh-only mode. Also, $\overline{CAS}$-Before-$\overline{RAS}$ refresh does not cause device selection and the state of the data-out will remain unchanged as long as $\overline{CAS}$ remains low.

ABSOLUTE MAXIMUM RATINGS*[a]

Voltage on V_{CC} Relative to V_{SS} . . . . . −1.0V to +7.0V
Storage Temp. (Ceramic Package) −65°C to +150°C
Storage Temp. (Plastic Package) −55°C to +125°C
Power Dissipation. 1W
Short Circuit Output Current. 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS[a, b]

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage		0		V	
V_{IH}	Logic "1" Voltage	2.4		V_{CC} + 1	V	
V_{IL}	Logic "0" Voltage	−1.0V		0.8	V	
T_A	Ambient Operating Temperature	0		70	°C	Still Air

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC_1}	Average V_{CC} Power Supply Current (Operating)		70 60 45	mA mA mA	t_{RL2RL2} = 121ns t_{RL2RL2} = 150ns (c) t_{RL2RL2} = 200ns
I_{CC_2}	V_{CC} Power Supply Current (Active)		15	mA	$RAS \leq V_{IL}$ (max), $CAS \leq V_{IL}$ (max) (d)
I_{CC_3}	Standby Current		2.5 4.5 4.0 5.5	mA mA mA mA	All inputs stable at CMOS levels, $\overline{RAS} \geq (V_{CC} - .4V)$. All inputs stable at TTL levels $\overline{RAS} \geq 2.4V$. All inputs toggling between CMOS levels at 6.25MHZ, $\overline{RAS} \geq (V_{CC} - .4V)$. (e) All inputs (except $\overline{RAS}$) toggling between TTL levels at 6.25MHZ.
I_{IN}	Input Leakage Current (Any Input)	−10	10	µA	$0V \leq V_{IN} \leq 5.5V$, others = 0V
I_{OLK}	Output Leakage Current	−10	10	µA	D_{OUT} = Hi Z, $0V \leq V_{OUT} \leq 5.5V$
V_{OH}	Output High Voltage	2.4		V	$I_O = -5.0mA$
V_{OL}	Output Low Voltage		0.4	V	$I_O = 5.0mA$

Note a: All voltage values in this data sheet are with respect to V_{SS}.
b: After power-up, a pause of 1ms followed by eight initialization memory cycles is required to achieve proper device operation. Any interval greater than 4.4ms with $\overline{RAS}$ inactivity requires eight reinitialization cycles to achieve proper device operation.
c: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with output open.
d: DC current after t_{RLQV} (max), t_{CLQV} (max), and t_{AVQV} delay.
e: CMOS levels are defined as V_{IH} (min) $\geq (V_{CC} - .4V)$ and V_{IL} (max) $\leq 0.4V$. TTL levels are defined as V_{IH} (min) $\geq 2.4V$ and V_{IL} (max) $\leq 0.8V$.

AC TEST CONDITIONS

Input Pulse Levels . . . . . 0 to 3V
Input Rise and Fall Times . . . . 3ns between 0.8 and 2.4V
Input Timing Reference Levels. . . . . 0.8 and 2.4V
Output Timing Reference Levels . . . . . 0.4 and 2.4V
Output Load . . . . . Equivalent to 2 TTL Loads and 50pF

CAPACITANCE

SYMBOL	PARAMETER	MAX	UNITS	COND.
C_{IN}	Input Cap. $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	6	pF	d
C_{IN}	Input Cap. Addresses	5	pF	d
C_{OUT}	Output Cap.	7	pF	d o

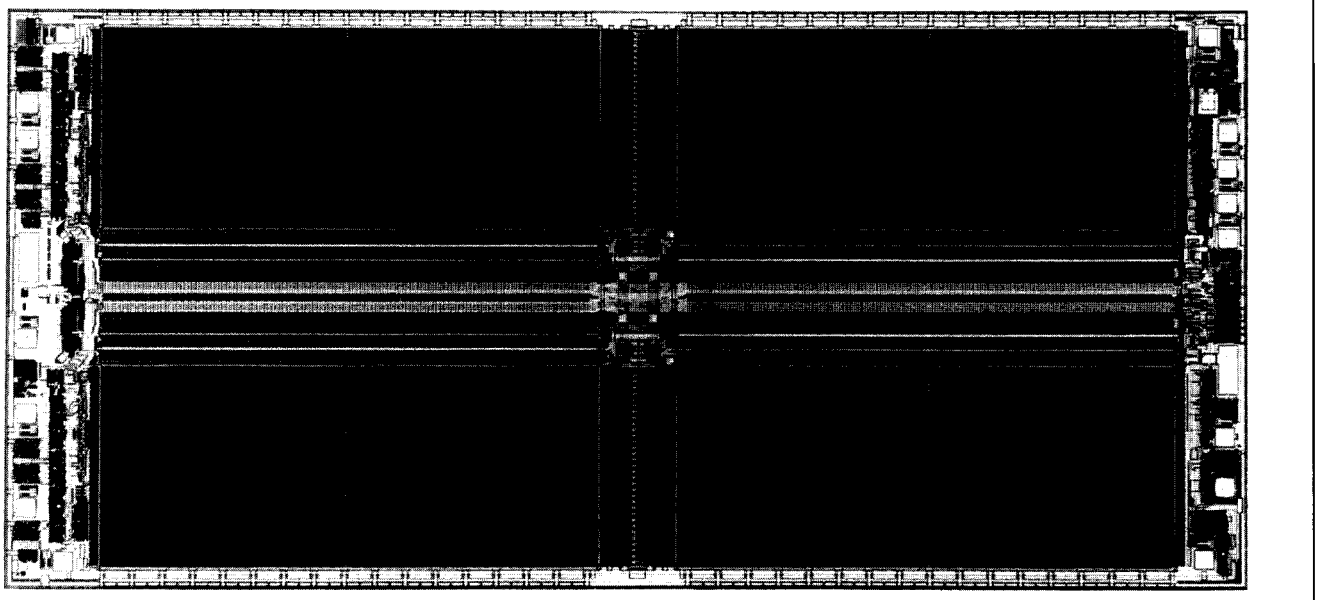
Note d: Capacitance measured with BOONTON METER.
o: $\overline{CAS} = V_{IH}$ to disable D_{OUT}

AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

NO.	SYMBOL	PARAMETER	2800-60		2800-70		2800-80		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{AVAV}	Address Cycle	35		40		46		ns	
2	t_{AVCL2}	Column Address Set-Up (Early Write)	0		0		0		ns	h
3	t_{AVQV}	Column Address Access		32		37		43	ns	
4	t_{AVRL2}	Row Address Set-Up	2		2		2		ns	
5	t_{AVWL2}	Column Address Set-Up (Late Write)	0		0		0		ns	h
6	t_{AXQX}	Output Hold	5		5		5		ns	
7	t_{CH1QZ}	Output Hold	2		2		2		ns	f
8	t_{CH2CL2}	$\overline{CAS}$ Precharge	5		5		5		ns	
9	t_{CH2QZ}	Output Turn-Off Delay		17		18		19	ns	f
10	t_{CH2RL2}	$\overline{CAS}$ To $\overline{RAS}$ Set-Up (Non-$\overline{CAS}$ Before $\overline{RAS}$ Refresh)	3		3		3		ns	
11	t_{CH2WX}	Read Command Hold Time (Reference $\overline{CAS}$)	0		0		0		ns	g
12	t_{CL1AX}	Column Address Hold (Early Write)	6		7		8		ns	h
13	t_{CL1CH1}	$\overline{CAS}$ Pulse Width (Read)	11		12		13		ns	
14	t_{CL1CH1}	$\overline{CAS}$ Pulse Width (Write)	5		5		5		ns	
15	t_{CL1DX}	Data-In Hold (Early Write)	6		7		8		ns	
16	t_{CL1QV}	$\overline{CAS}$ Access		11		12		13	ns	
17	t_{CL1QVN}	$\overline{CAS}$ To Data (Write-Verify/Write-Read)		50		55		60	ns	
18	t_{CL1RH1}	$\overline{CAS}$ To $\overline{RAS}$ Lead	15		18		20		ns	
19	t_{CL1RL2}	$\overline{CAS}$ To $\overline{RAS}$ Set-Up (Refresh)	2		2		2		ns	
20	t_{CL1WH1}	Write Hold (Reference $\overline{CAS}$)	5		5		5		ns	
21	t_{CL1WL2}	$\overline{CAS}$ to $\overline{W}$ Delay (Read/Modify/Write)	11		12		13		ns	i
22	t_{CL2CL2}	Page Read/Write Cycle	35		38		40		ns	
23	t_{CL2QX}	Output Turn-On Delay	0		0		0		ns	
24	t_{DVCL2}	Early Write Data Set-Up (Early Write)	0		0		0		ns	h
25	t_{DVWL2}	Late Write Data Set-Up	0		0		0		ns	
26	t_{RH2AX}	Address Hold Without Data Change	0		0		0		ns	
27	t_{RH2RL2}	$\overline{RAS}$ Precharge	55		60		65		ns	
28	t_{RH2WX}	Read Command Hold Time (Reference $\overline{RAS}$)	0		0		0		ns	g
29	$t_{RL1A(C)X}$	Column Address Hold (Write)	40		43		45		ns	
30	t_{RL1AX}	Row Address Hold	2		2		2		ns	
31	t_{RL1CH1} -	$\overline{CAS}$ Hold ($\overline{CAS}$-Before-$\overline{RAS}$)	2		2		2		ns	
32	t_{RL1CH1}	$\overline{CAS}$ Hold (Early Write)	40		43		45		ns	
33	t_{RL1CL2}	$\overline{CAS}$ Hold (Non Refresh)	2		2		2		ns	
34	t_{RL1DX}	Data Hold (Early Write)	40		43		45		ns	
35	t_{RL1QV}	$\overline{RAS}$ Access		60		70		80	ns	
36	t_{RL1RH1}	$\overline{RAS}$ Pulse Width	60	10^5	70	10K	80	10^5	ns	
37	t_{RL1WH1}	Write Command Hold (Reference $\overline{RAS}$)	40		43		45		ns	
38	t_{RL1WL2}	$\overline{RAS}$ to $\overline{W}$ Delay (Read/Modify/Write)	60		70		80		ns	i
39	t_{RL2RL2}	Random Read/Write Cycle	121		136		151		ns	
40	t_{WH1QX}	Output Hold	0		0		0		ns	
41	t_{WH2CL2}	Read Command Set-Up	0		0		0		ns	
42	t_{WH2QVN}	$\overline{W}$ High to Data (Write-Verify or Write-Read Cycle)		11		12		13	ns	
43	t_{WH2WL2}	Write Precharge	5		5		5		ns	
44	t_{WL1AX}	Column Address Hold (Late Write)	7		7		7		ns	h
45	t_{WL1CH1}	Write To $\overline{CAS}$ Delay	5		5		5		ns	
46	t_{WL1CL2}	Early Write $\overline{W}$ Set-Up	0		0		0		ns	i
47	t_{WL1DX}	Data-In Hold (Late Write)	5		6		7		ns	h
48	t_{WL1QV}	$\overline{W}$ To Data After Late Write		35		38		40	ns	
49	t_{WL1QVN}	Write/Read Cycle Write-Verify/Write Read Access		55		65		74	ns	
50	t_{WL1RH1}	Write To $\overline{RAS}$ Lead	13		15		17		ns	
51	t_{WL1WH1}	Write Pulse	5		5		5		ns	
52	t_{REF}	Refresh Period		4.4		4.4		4.4	ms	
53	t_T	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	j, k

AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

NO.	SYMBOL	PARAMETER	2800-100		2800-120		2800-150		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{AVAV}	Address Cycle	56		63		78		ns	
2	t_{AVCL2}	Column Address Set-Up (Early Write)	0		0		0		ns	h
3	t_{AVQV}	Column Address Access		53		60		75	ns	
4	t_{AVRL2}	Row Address Set-Up	2		2		2		ns	
5	t_{AVWL2}	Column Address Set-Up (Late Write)	0		0		0		ns	h
6	t_{AXQX}	Output Hold	5		5		5		ns	
7	t_{CH1QZ}	Output Hold	2		2		2		ns	f
8	t_{CH2CL2}	$\overline{CAS}$ Precharge	5		5		5		ns	
9	t_{CH2QZ}	Output Turn-Off Delay		21		24		27	ns	f
10	t_{CH2RL2}	$\overline{CAS}$ To $\overline{RAS}$ Set-Up (Non-$\overline{CAS}$ Before $\overline{RAS}$ Refresh)	3		3		2		ns	
11	t_{CH2WX}	Read Command Hold Time (Reference $\overline{CAS}$)	0		0		0		ns	g
12	t_{CL1AX}	Column Address Hold (Early Write)	9		11		15		ns	h
13	t_{CL1CH1}	$\overline{CAS}$ Pulse Width (Read)	16		19		25		ns	
14	t_{CL1CH1}	$\overline{CAS}$ Pulse Width (Write)	5		5		10		ns	
15	t_{CL1DX}	Data-In Hold (Reference $\overline{CAS}$)	9		11		15		ns	
16	t_{CL1QV}	$\overline{CAS}$ Access		16		19		25	ns	
17	t_{CL1QVN}	$\overline{CAS}$ To Data Write-Read		70		80		100	ns	
18	t_{CL1RH1}	$\overline{CAS}$ To $\overline{RAS}$ Lead	25		30		40		ns	
19	t_{CL1RL2}	$\overline{CAS}$ To $\overline{RAS}$ Set-Up (Refresh)	2		2		2		ns	
20	t_{CL1WH1}	Write Hold (Reference $\overline{CAS}$)	5		5		10		ns	
21	t_{CL1WL2}	$\overline{CAS}$ to $\overline{W}$ Delay (Read/Modify/Write)	16		19		25		ns	i
22	t_{CL2CL2}	Page Read/Write Cycle	45		50		65		ns	
23	t_{CL2QX}	Output Turn-On Delay	0		0		0		ns	
24	t_{DVCL2}	Early Write Data Set-Up (Early Write)	0		0		0		ns	h
25	t_{DVWL2}	Late Write Data Set-Up	0		0		0		ns	
26	t_{RH2AX}	Address Hold Without Data Change	0		0		0		ns	
27	t_{RH2RL2}	$\overline{RAS}$ Precharge	70		75		90		ns	
28	t_{RH2WX}	Read Command Hold Time (Reference $\overline{RAS}$)	0		0		0		ns	g
29	$t_{RL1A(C)X}$	Column Address Hold (Write)	50		55		75		ns	
30	t_{RL1AX}	Row Address Hold	2		2		2		ns	
31	t_{RL1CH1}	$\overline{CAS}$ Hold ($\overline{CAS}$-Before-$\overline{RAS}$)	2		2		2		ns	
32	t_{RL1CH1}	$\overline{CAS}$ Hold (Early Write)	50		55		70		ns	
33	t_{RL1CL2}	$\overline{CAS}$ Hold (Non Refresh)	2		2		2		ns	
34	t_{RL1DX}	Data Hold (Early Write)	50		60		70		ns	
35	t_{RL1QV}	$\overline{RAS}$ Access		100		120		150	ns	
36	t_{RL1RH1}	$\overline{RAS}$ Pulse Width	100	10^5	120	10^5	150	10^5	ns	
37	t_{RL1WH1}	Write Command Hold (Reference $\overline{RAS}$)	50		55		70		ns	
38	t_{RL1WL2}	$\overline{RAS}$ to $\overline{W}$ Delay (Read/Modify/Write)	100		120		150		ns	i
39	t_{RL2RL2}	Random Read/Write Cycle	176		201		246		ns	
40	t_{WH1QX}	Output Hold	0		0		0		ns	
41	t_{WH2CL2}	Read Command Set-Up	0		0		0		ns	
42	t_{WH2QVN}	$\overline{WE}$ High To D. (Write-Verify or Write-Read Cycle)		16		19		25	ns	
43	t_{WH2WL2}	Write Precharge	5		5		10		ns	
44	t_{WL1AX}	Column Address Hold (Late Write)	7		7		10		ns	h
45	t_{WL1CH1}	Write To $\overline{CAS}$ Delay	5		5		10		ns	
46	t_{WL1CL2}	Early Write $\overline{WE}$ Set-Up	0		0		0		ns	i
47	t_{WL1DX}	Data-In Hold (Late Write)	8		10		15		ns	h
48	t_{WL1QV}	$\overline{WE}$ To Data After Late Write		45		50		65	ns	
49	t_{WL1QVN}	Write/Read Cycle		92		110		140	ns	
50	t_{WL1RH1}	Write To $\overline{RAS}$ Lead	22		27		32		ns	
51	t_{WL1WH1}	Write Pulse	5		5		10		ns	
52	t_{REF}	Refresh Period		4.4		4.4		4.4	ms	
53	t_T	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	j, k



IMS2800 PHOTOMICROGRAPH

NOTES:

f. Q_Z is defined as the time at which the output achieves the open circuit condition.

g. Either t_{CH2WX} or t_{RH2WX} must be satisfied for a Read cycle.

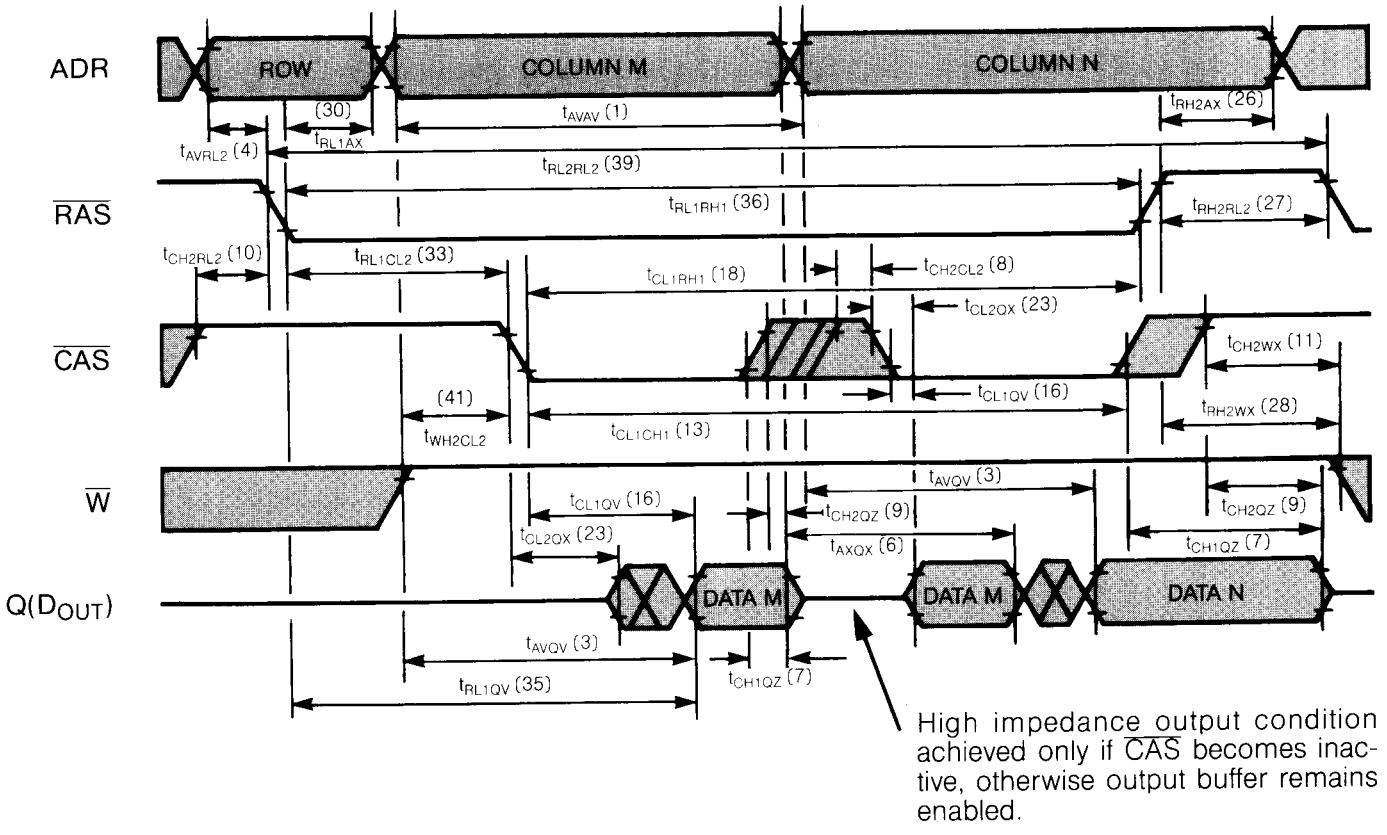
h. Address and data set-up and hold times referenced to $\overline{CAS}$ (t_{AVCL2}, t_{CL1AX}, t_{DVCL2}, and t_{CL1DX}) are restrictive parameters for Early-Write operations only. Address and data set-up times referenced to $\overline{W}$ (t_{AVWL2}, t_{WL1AX}, t_{DVWL2}, and t_{WL1DX}) are restrictive parameters for Late-Write and Read-Modify-Write cycle operations only.

i. t_{WH2CL2}, t_{CL1WL2}, and t_{RL1WL2} are restrictive operating parameters in Read-Write and Read-Modify-Write cycles only. If $t_{WL1CL2} \geq t_{WL1CL2}$ (min) the cycle is an Early-Write cycle and data will remain open circuit unless $\overline{W}$ goes high while $\overline{CAS}$ and $\overline{RAS}$ are both low. If $t_{WH2CL2} \geq t_{WH2CL2}$ (min), $t_{RL1WL2} \geq t_{RL1WL2}$ (min), and $t_{AVQV} \geq t_{AVQV}$ (min) the cycle is a Read-Write and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out is indeterminate at access time and remains so until either $\overline{CAS}$ or $\overline{W}$ returns to V_{IH}.

j. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner. Transition time is measured between V_{IL} (max) and V_{IH} (min).

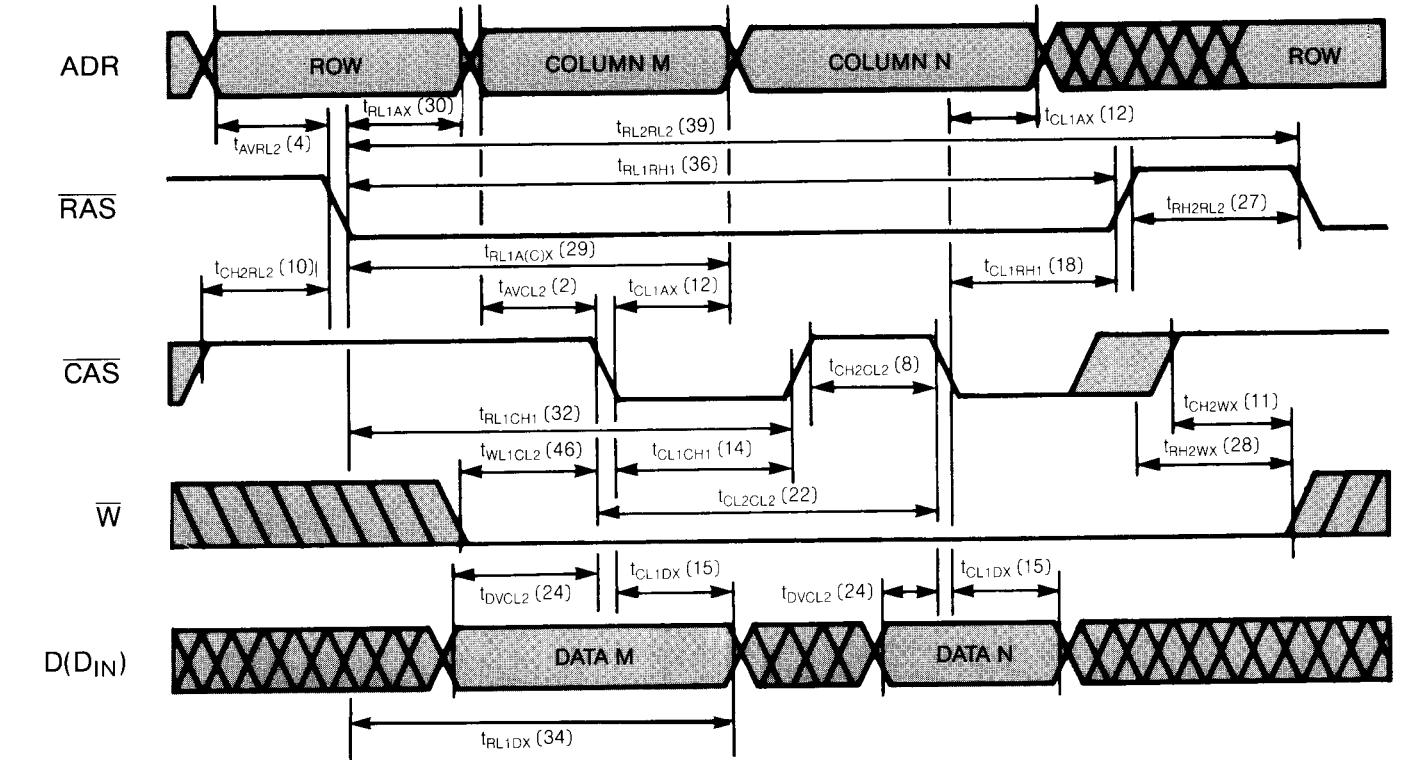
k. 3ns rise and fall times (t_T) are used for cycle time specifications.

READ CYCLE

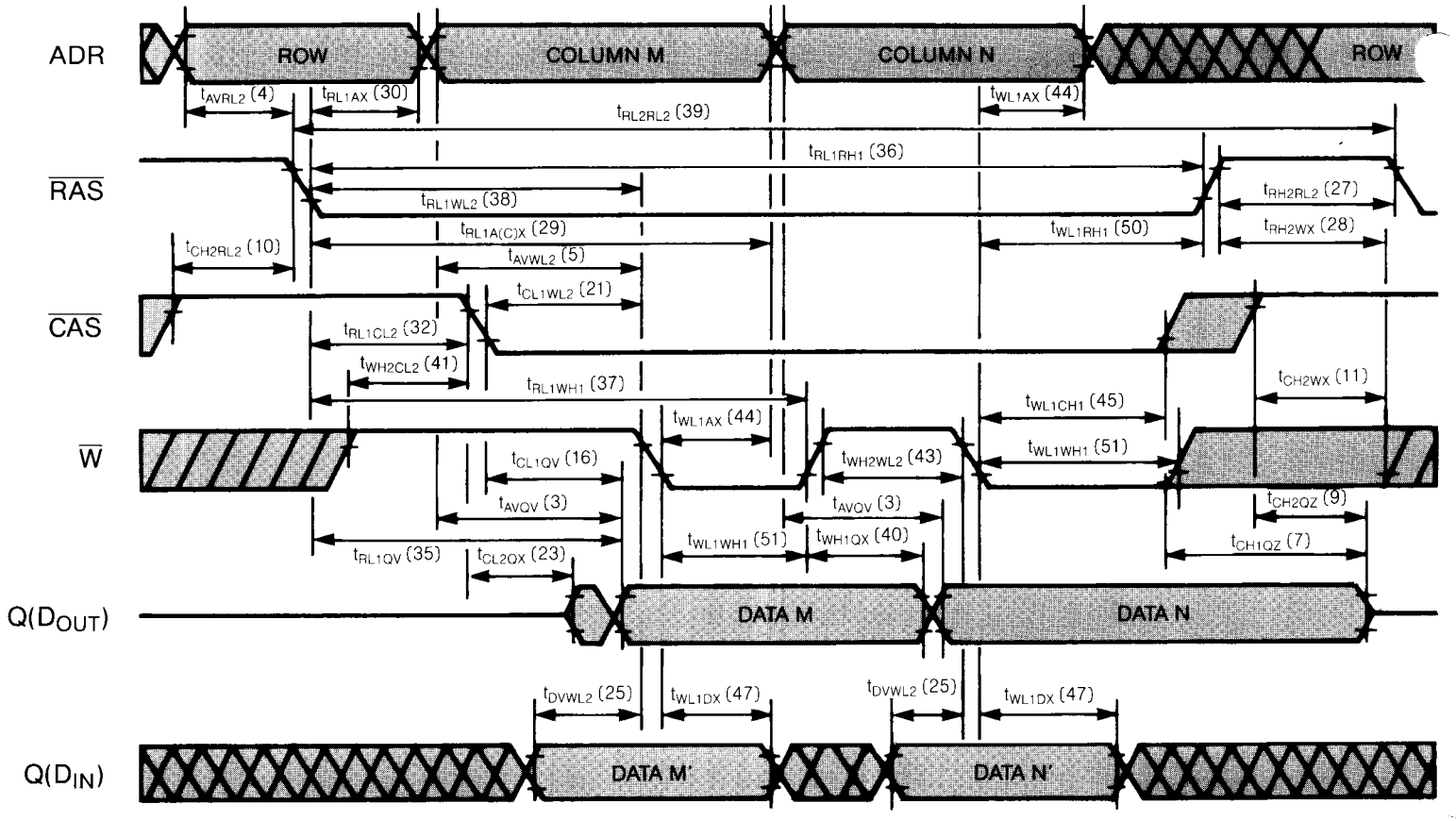


High impedance output condition achieved only if $\overline{CAS}$ becomes inactive, otherwise output buffer remains enabled.

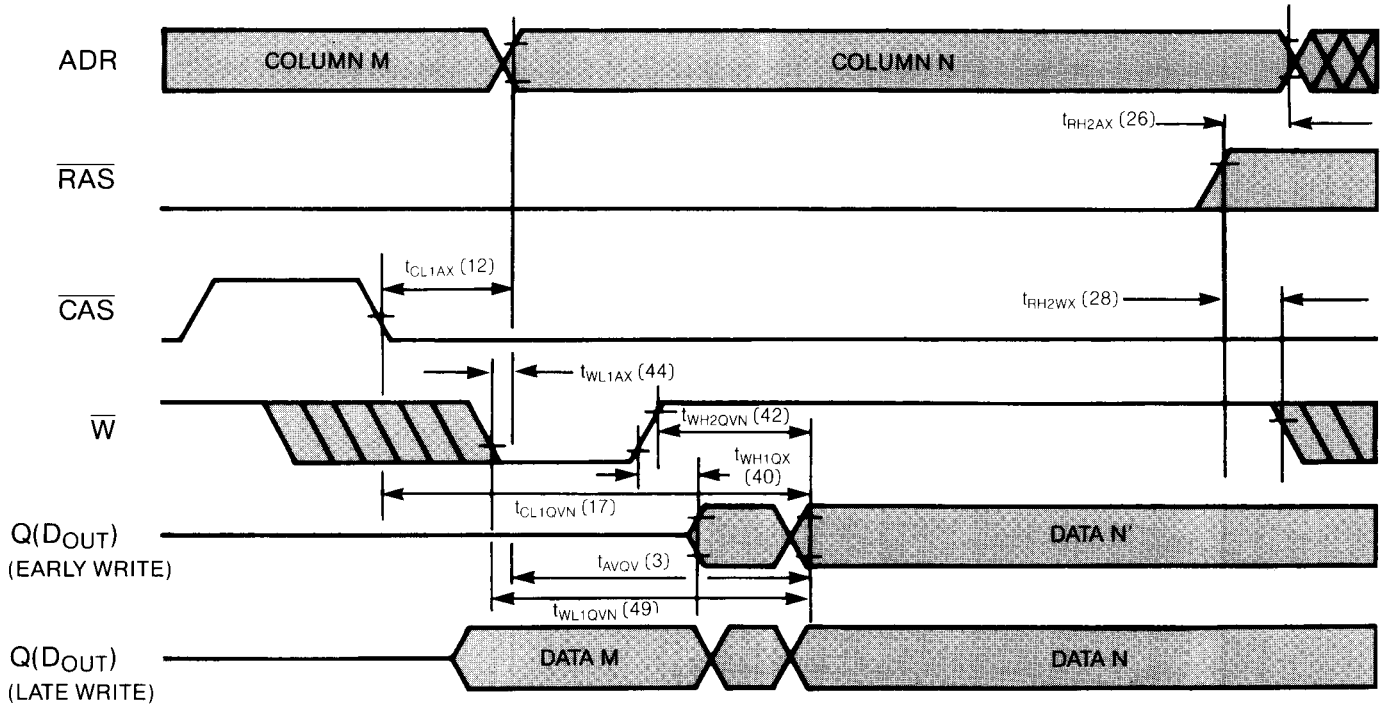
EARLY-WRITE CYCLE



LATE-WRITE/READ-MODIFY-WRITE CYCLE

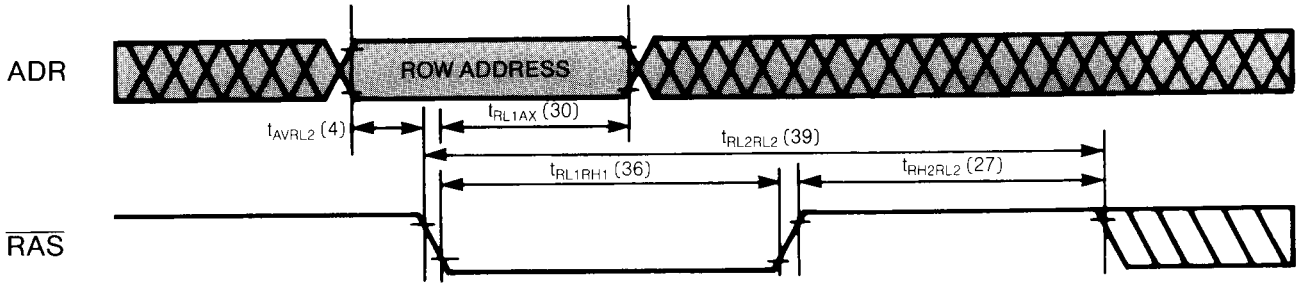


WRITE-VERIFY/WRITE-READ CYCLE

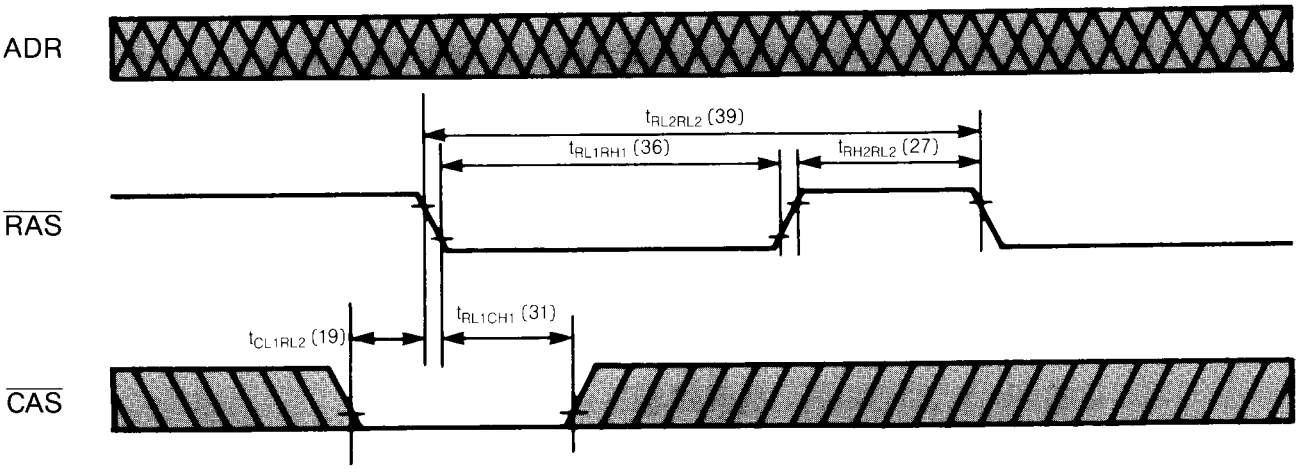


If Column Address N = Column Address M, Cycle is Write-Verify.

$\overline{\text{RAS}}$ ONLY REFRESH [$\overline{\text{CAS}} \geq V_{IH}$ (MIN)]



$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH



APPLICATION

To ensure proper operation of the IMS2800 in a system environment it is recommended that the following guidelines be followed.

POWER DISTRIBUTION

Transient currents are required by dynamics RAMs. These transient current spikes can cause significant power supply and ground noise unless adequate power distribution and decoupling is used. The recommended power distribution scheme combines proper trace layout and placement of decoupling capacitors. The impedance in the decoupling path from the power pin (8) through the decoupling capacitor, to the ground pin (16) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line and the decoupling capacitor.

To reduce the power line impedance, it is recommended that the power trace and ground trace be gridded or provided by separate power planes. To prevent loss of signal margins due to differential ground noise, the ground grid of the memory array should be extended to the TTL drivers in the peripheral circuitry. A high-frequency decoupling capacitor with a value of 0.1μF, should be placed between the rows of memory devices in the array. A larger tantalum capacitor with a value beteween 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These large capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

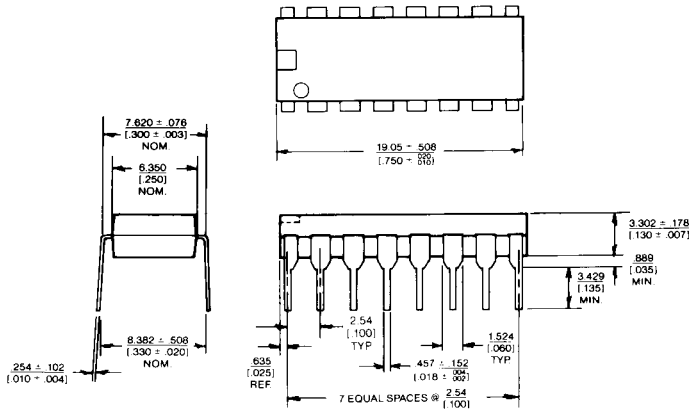
TERMINATION

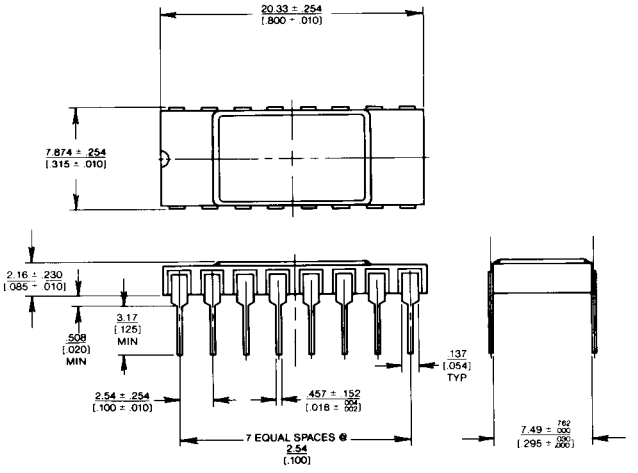
Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propogating down the lines, especially low-going TTL signals, line termination is recommended. The termination may be either parallel or series but the series termination technique has the advantages of drawing no DC current and using a minimum of components. The recommended technique is to use series termination.

A series resistor in the signal line at the output of the TTL driver to match the source impedance of the TTL driver to the signal line will dampen the reflections on the line. The line should be kept short with the driver/termination combination close to the memory array. Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

Proper power distribution techniques, including adequate use of decoupling capacitors, along with proper termination of TTL driver outputs, are among the most important, yet basic guidelines to be followed. These guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment relatively free of noise spikes and signal reflections.

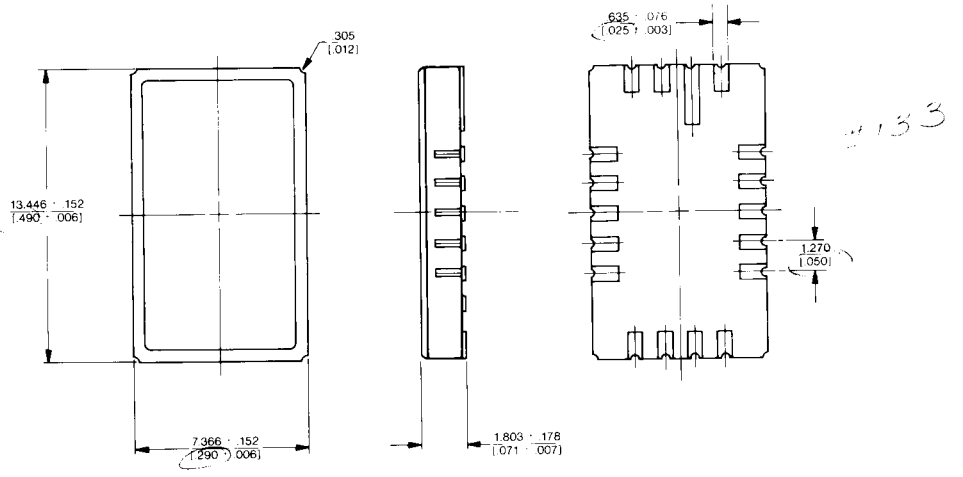
16 PIN PLASTIC DUAL-IN-LINE





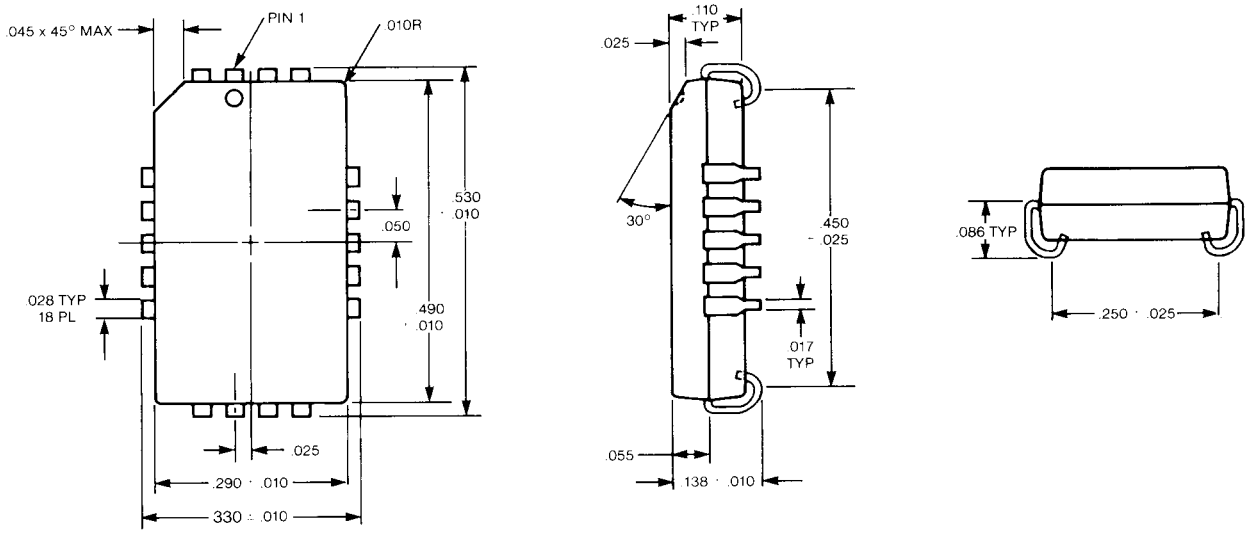
16 PIN CERAMIC DUAL-IN-LINE

18 PIN CERAMIC LEADLESS CHIP CARRIER



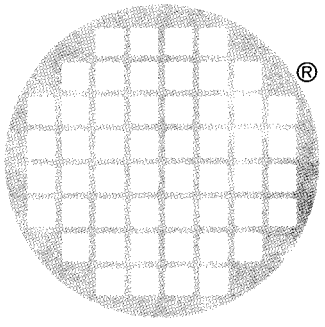
Dimension Note:
Top Number in Millimeters
Bottom Number in Inches

18 PIN PLASTIC CHIP CARRIER



ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS2800	60ns	PLASTIC DIP	IMS2800P-60
	60ns	CERAMIC DIP	IMS2800S-60
	60ns	CERAMIC CHIP CARRIER	IMS2800W-60
	60ns	PLASTIC CHIP CARRIER	IMS2800J-60
	70ns	PLASTIC DIP	IMS2800P-70
	70ns	CERAMIC DIP	IMS2800S-70
	70ns	CERAMIC CHIP CARRIER	IMS2800W-70
	70ns	PLASTIC CHIP CARRIER	IMS2800J-70
	80ns	PLASTIC DIP	IMS2800P-80
	80ns	CERAMIC DIP	IMS2800S-80
	80ns	CERAMIC CHIP CARRIER	IMS2800W-80
	80ns	PLASTIC CHIP CARRIER	IMS2800J-80
	100ns	PLASTIC DIP	IMS2800P-100
	100ns	CERAMIC DIP	IMS2800S-100
	100ns	CERAMIC CHIP CARRIER	IMS2800W-100
	100ns	PLASTIC CHIP CARRIER	IMS2800J-100
	120ns	PLASTIC DIP	IMS2800P-120
	120ns	CERAMIC DIP	IMS2800S-120
	120ns	CERAMIC CHIP CARRIER	IMS2800W-120
	120ns	PLASTIC CHIP CARRIER	IMS2800J-120
	150ns	PLASTIC DIP	IMS2800P-150
	150ns	CERAMIC DIP	IMS2800S-150
	150ns	CERAMIC CHIP CARRIER	IMS2800W-150
	150ns	PLASTIC CHIP CARRIER	IMS2800J-150



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IMS2800 ERRATA SHEET

PARAMETER	-60	-80	-10	-12	
t_{CH2RL2}	3	3	3	3	nsec (min)
t_{WL1RH1}	13	17	22	27	nsec (min)
t_{CH2QZ}	17	19	21	24	nsec (max)
t_{WL1AX}	7	7	7	7	nsec (min)

March 6, 1986