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S-7035C2F

PAGING DECORDER IC(POCSAG)

The S-7035C2F is a signal processor IC that uses the format of "Standard Code and Format International Radio Paging" (POCSAG) of the CCIR suggestion 584.
It processes POCSAG format signals by itself, and transfers data to a CPU.

■ Features

- Two types of user addresses:
  Multi addresses : 4 types of tones
  Urgent address : Single tone
- Battery saving with intermittent operation of RF
- Direct connection to the IDROM
  S-2100R / RF
  S-2980I / IF (with an inverter for $\overline{\text{ROM-RST}}$ terminal)
- BCH decode: Correction of one bit by cyclic code
- Built-in CPU interface

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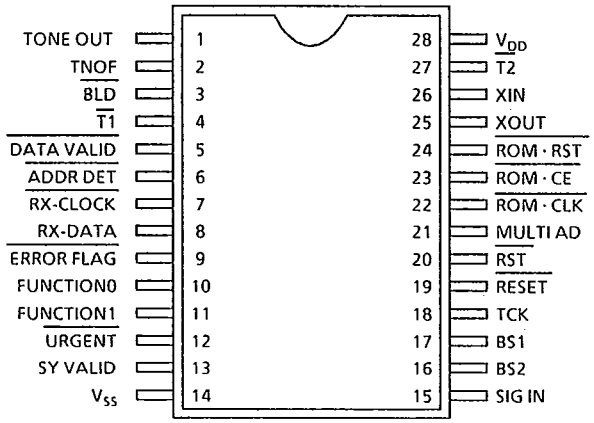
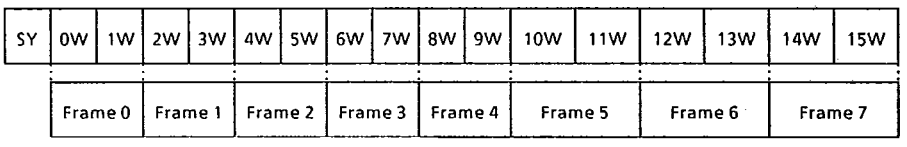
■ Pin Arrangement



Pin names	I/O	Explanations
V_{DD}	I	3.0 V typ.
V_{SS}	I	GND terminal
XIN	I	Connected to 32 kHz quartz oscillator
XOUT	O	
SIG IN	I	Signal input terminal
$\overline{RST}$	I	Hard clear input terminal, active "L"
$\overline{RESET}$	I	Manual reset of tone output, active "L"
$\overline{BLD}$	I	Input terminal of detection signal of lowered current and voltage,active
TONE OUT	O	Tone output terminal
TNOF	I	Tone frequency switching terminal, "L" = 2048 Hz, "H" = 4096 Hz
BS1	O	RF battery control signal, active "H"
BS2	O	
MULTI AD	I	Terminal to input address from ID-ROM
$\overline{ROM - CE}$	O	Output terminal to make CE of ID-ROM active
$\overline{ROM - CLK}$	O	Output terminal of synchronization clock for ID-ROM
$\overline{ROM - RST}$	O	Output terminal of output ID-ROM initial reset signal
SY - VALID	O	Signal to indicate that POCSAG signal can be received
$\overline{ADDR\ DET}$	O	STROBE stands at the "L" level when addresses match
FUNCTION 0	O	Output terminal of message function bit
FUNCTION 1	O	
$\overline{URGENT}$	O	Terminal to indicate that message is urgent. Active "L"
RX - CLOCK	O	Synchronization clock of RX data
RX - DATA	O	Performs BCH decode of input signals, and outputs only messages
$\overline{ERROR\ FLAG}$	O	Becomes "L" level when RX data is error message
$\overline{DATA\ VALID}$	O	Terminal to indicate RX data is valid. Active "L"
$\overline{T1}$	I	Test input terminal
$\overline{T2}$	I	
TCK	I/O	Internal synchronization clock I / O terminal

Every batch comprises a synchronization code word with a fixed 32-bit pattern followed by eight frames.

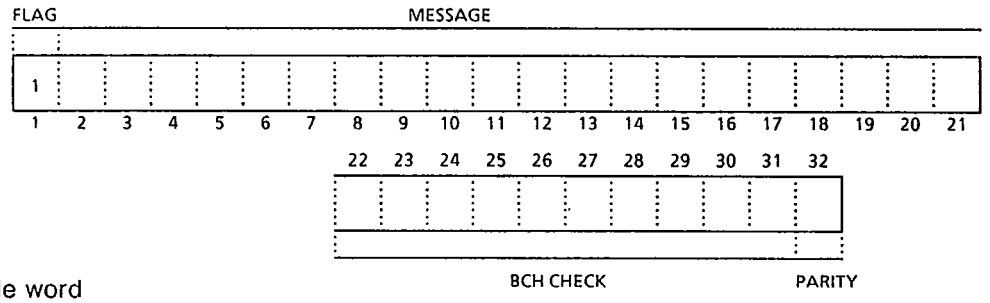
2. Batch



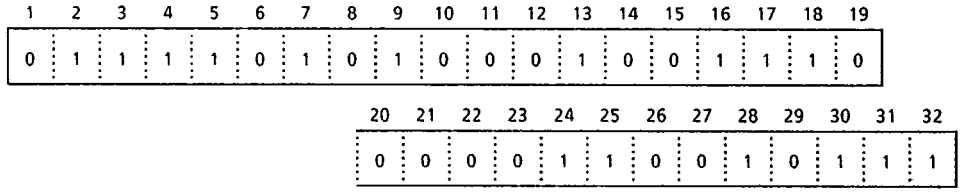
1 word = 32 bits; Sy = Synchronization word

This format has a synchronization word for IC word synchronization and 16 words. A frame consists of two words other than the synchronization word. Batches can be received continuously.

5. Message word



6. Idle word



Address and message words are transferred to a word that does not exist. An idle word is a kind of address word, but cannot be alloted to the terminal itself.

■ Hard Clear

The inside of the IC is entirely initialized by setting the RST terminal to V_{SS}. This is called hard clear. A power-on calling tone is generated immediately after the hard clear is released. Signal input reception is prohibited while the calling tone is being generated. The calling tone stops when the RESET terminal is set to V_{SS} or when eight seconds have passed, then signal inputs can be received. The IC operates as a power-on circuit when a capacitance of about 20 pF is connected between the RST terminal and V_{SS}.

■ Battery Saving

1. Before detecting preambles

   The BS1 terminal is set to "H" level for 62.5 ms every 1062.5 ms.

2. After detecting preambles

   After detecting preambles, the BS1 terminal is kept "H" level until a synchronization code is detected. When a synchronization code is detected, the terminal is set to "L" level. For 32 words after detecting preambles, however, the terminal is set to "L" level when a synchronization code is not detected.

3. After detecting synchronization codes

   The BS1 terminal is set to "H" level at eight bits before a transfer signal comes to the frame which is unique to the terminal, and is kept "H" level until the IC determines that the message is finished. Then the terminal is set to "L" level . Likewise, the BS1 terminal is set to "H" level eight bits before the synchronization code of the transfer signal, and the synchronization code remains "H" level.

4. Retrying when detection of synchronization code fails

   When the synchronization code detection fails N times continuously, the IC enters the mode before detecting preambles. N can be changed by writing data to bits 42, 43, 44 and 45 of the ID-ROM.

ID-ROM ADDRESS	42	43	44	45	
DATA	1	0	0	0	Retry nine times

ID-ROM ADDRESS	42	43	44	45	
DATA	1	1	1	1	Retry 16 times

ID-ROM ADDRESS	42	43	44	45	
DATA	0	0	0	0	Use prohibited

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5. The BS2 terminal is set to "H" level when the BS1 terminal is set to "H" level, and it remains "H" level for eight bits. The timing is shown in figures 1 and 2.

■ Preamble

Reception of continuous eight bits of reverse pattern (1, 0, 1, 0...) is regarded as detection of a preamble. If there is even one bit of error, however, data is searched from the beginning.
Detection of preambles allows synchronization words to be received.

■ Synchronization Code

Synchronization codes are detected after preambles are detected or at the synchronization code word of batches.
Errors up to two bits of synchronization code are allowed; the synchronization code is recognized even with two bits of errors. After detecting preambles, the synchronization code is compared with the newest 32-bit input data whenever one bit of signal input data is input. If they match and the number of errors does not exceed two bits, address data can be received. If they do not match, the next signal input data is received and the same operation is performed.
After once a synchronization word is received, the synchronization code is compared with the 32-bit data that is input at the synchronization code word in the batch. If they match and the number of errors does not exceed two bits, address data can be received.

■ BCH Decode

BCH decode is correction of one bit by cyclic codes.
One bit of error is allowed including BCH errors and parity errors. Errors of two or more bits are determined as errors. One bit of error is corrected and becomes normal data.

BCH error bit	Parity error	Correction	Error flag
0	*	Not done	HIGH
1	Not done	Done	HIGH
1	Done	Done	LOW
2	*	Not done	LOW

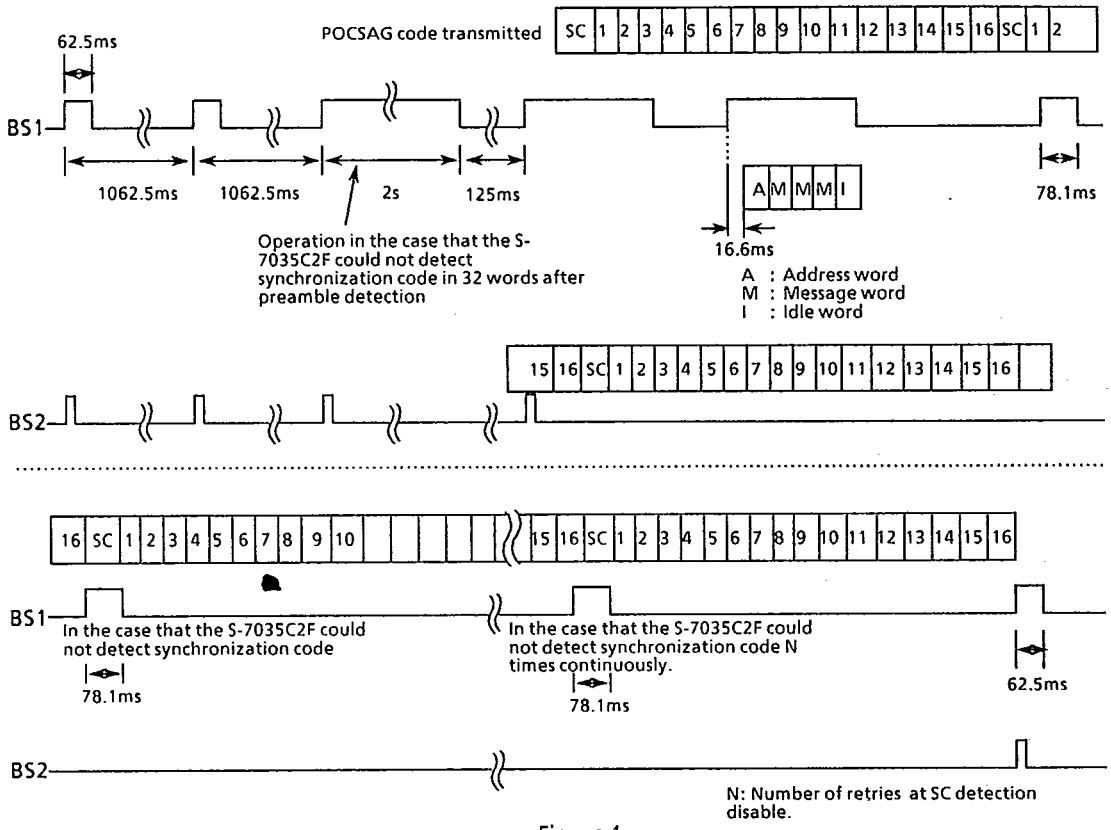
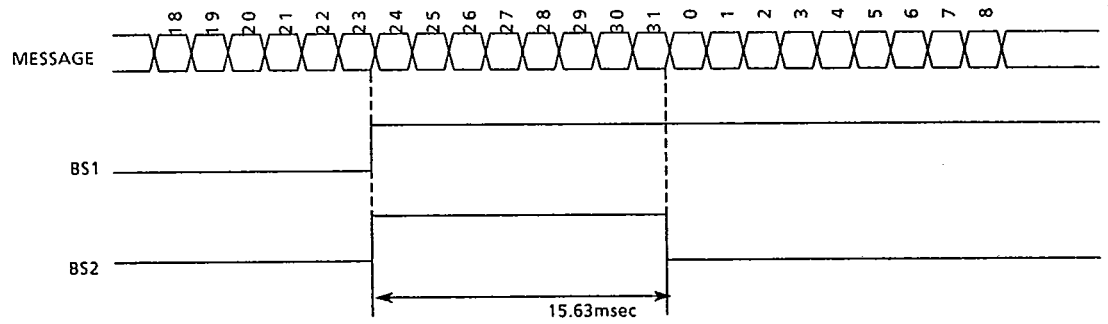


Figure 1



BS2 rises at the same time that the BS 1 rises, and remains "H" level for eight bits.

The relationship between BS1, BS2, and the message after the synchronization code is detected is shown above.

BS1 and BS2 have no relationship with the message when the synchronization code is not detected. They become "H" level every 1062.5 ms.

Figure 2

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Address Comparison

The S-7035C2F can use two types of addresses: multi addresses in normal status and urgent addresses in emergencies.
After the initial period, multi addresses and urgent addresses are loaded from the ID-ROM to the internal register. Frame numbers, addresses, and number of retries when synchronization code detection failed are written in the ID-ROM.

[Note] (The initial period means the eight seconds after the hard clear or the period between the hard clear and manual reset.)

When the address code which has been BCH-decoded in the self-frame is compared with the ID-ROM and matched the multi address or the urgent address, the later messages can be received. When comparing addresses, no single bit must have an error.

Tone Output

The following tones are controlled:

1. Tones in normal hard clear operation
2. Beep by the function bit in multi address call
3. Beep in urgent call
4. Low battery alarm

Tone 2 and 3 start after the message is finished. The tones can be stopped when eight seconds pass or when the $\overline{\text{RESET}}$ terminal is set to Vss.

Tone 4 can be stopped when the battery voltage recovers to normal and the $\overline{\text{RESET}}$ terminal is set to Vss.

Tone frequencies can be switched with the TNOF terminal.
TNOF = L -- 2048 Hz
TNOF = OPEN -- 4096 Hz

BLD

Lowered voltage is detected once while the BS1 terminal is "H" level for searching preambles and detecting synchronization codes. While a tone is output, however, the lowered voltage is not detected. If the lowered battery voltage is detected continuously twice, the low battery alarm will beep.

ID-ROM Write Format

The ID-ROM write format is as follows:

ID-ROM ADDRESS	0	1	2	3	4	5	6	7	8	9
DATA	0	0	U0	U1	U2	U3	U4	U5	U6	U7

ID-ROM ADDRESS	10	11	12	13	14	15	16	17	18	19
DATA	U8	U9	U10	U11	U12	U13	U14	U15	U16	U17

ID-ROM ADDRESS	20	21	22	23	24	25	26	27	28	29
DATA	0	M0	M1	M2	M3	M4	M5	M6	M7	M8

ID-ROM ADDRESS	30	31	32	33	34	35	36	37	38	39
DATA	M9	M10	M11	M12	M13	M14	M15	M16	M17	F3

ID-ROM ADDRESS	40	41	42	43	44	45
DATA	F2	F1	SC3	SC2	SC1	SC0

UN : Urgent address number
MN : Multi address number
FN : Frame number
SCN : Number of retries for redetecting SC when SC detection fails

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Functions

1. CPU interface
   S-7035C2F converts the transmission data, then transmits the data that the CPU needs.

   - Address transfer

     The ADDR DET is set to "L" level when the transfer address is determined to be a self-address. At the trailing edge of the ADDR DET signal, FUNCTION 0, FUNCTION 1 and URGENT are changed to those of transfer address data. When the urgent addresses are compared and matched, the ADDR DET is set to "L" level. (The timing is shown in figure 3.)

   - Message transfer

- Signal to indicate that POCSAG is valid

  The SY-VALID signal is set to "H" level at the detection of the first synchronization signal after no-signal state, and is set to "L" level when the synchronization codes are not detected continuously for the number of times written in the ID-ROM.

2. Test function

- T1, T2

T1	T2	Functions
0	0	Enables the acceleration input of the eight-second timer.
1	0	Sets the output terminal compulsorily to V_{SS}.
0	1	Sets the output terminal compulsorily to V_{DD}.
1	1	Normal

- TCK
  - In the normal state, this is an output terminal of the signal to sample the radio signals input from the SIG IN, or an acceleration input terminal.
  - The eight-second timer can be accelerated by setting T1 = 0 and T2 = 0.

3. Timing extraction

To synchronize the reception data and the system clock in the LSI, this function corrects the generation counter (32-bit counter) of the timing extraction clock (TCK) so that the leading edge of the reception data is at the center of the TCK.

- If the leading edge of the reception data is 0 to 15 of the counter value, the counter value is incremented and the counter becomes a 31-bit counter.
- If the leading edge of the reception data is 16 to 31 of the counter value, the counter value is decremented and the counter becomes a 33-bit counter.
- If the reception data has no leading edge, the counter value is not corrected.

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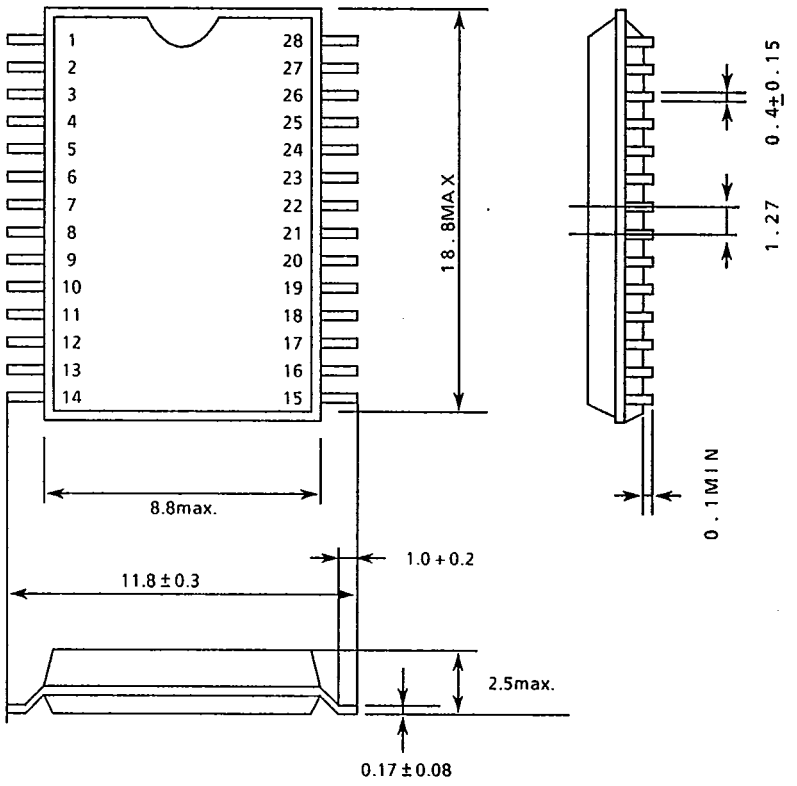
Dimensions (Unit : mm)



Package material : epoxy resin
Chip material : silicon

* This IC is not designed to be radiation-proof.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	-0.3 to + 7	V
Input voltage	V_{IN}	-0.3 toV_{DD} + 0.3	V
Storage temperature	T_{stg}	-55 to + 125	°C
Operating temperature	T_{opr}	-10 to + 70	°C

■ Electrical Characteristics

Unless otherwise specified: V_{DD} = 3.0V, V_{SS} = 0V, Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Measuring circuit	Note
Operating power supply voltage	V_{DD}		2.0	–	3.50	V	I	
Oscillation start voltage	V_{DOB}		2.0	2.0	3.50	V	I	
Average total current consumption	I_N	V_{DD} = 3.0V	–	–	50	µA	I	1
Buzzer driver output current	I_{BOH}	V_{DD} = 2.2V V_{OH} = 1.9V	450	–	–	µA	II	
	I_{BOL}	V_{DD} = 2.2V V_{OL} = 0.3V		–	-450	µA		
Other output currents	V_{OH3}	I_{OH} = -20µA	2.95	–	–	V	III	2
	V_{OL3}	I_{OL} = 20µA	–	–	0.05	V		
Input current	I_{IN}	V_{IN} = V_{DD} or V_{SS}	–	–	±0.1	µA	IV	3
Pull-up resistance	R1	V_{IL} = 0V	150	300	600	kΩ	IV	4
Pull-up resistance	R2	V_{IH} = 2.8V	25	50	100	kΩ	V	5
	R3	V_{IL} = 0V	150	300	600	kΩ	IV	
Pull-up resistance	R4	V_{IH} = 2.8V	25	50	100	kΩ	V	6
	R5	V_{IL} = 0V	0.8	1.5	3.0	MΩ	IV	
Test input pull-up	RT	V_{IL} = 0V	15	30	60	kΩ	V	7
Input voltage $\overline{RST}$	V_{ILR}		–	–	V_{DD}×0.3	V	IV	
Input voltage $\overline{RESET}$	V_{ILRS}		–	–	V_{DD}×0.3	V	IV	
$\overline{RST}$ pulse width	T_{RS}		10	–	–	µs	–	
$\overline{RESET}$ pulse width	T_{RSE}		10	–	–	ms	–	
Unadjustable rate	S_{MAX}	fosc = 32768Hz	580	–	–	BPS	I	
	S_{MIN}		–	–	440			

Note

※1. Signal input wave form is square. It does not include the current flowing through the pull-up resistor.

※2. Applied to the following terminals: BS1, BS2, $\overline{ROM\text{-}CE}$, $\overline{ROM\text{-}RST}$, $\overline{ROM\text{-}CLK}$, SY-VALID, $\overline{ADDR\ DET}$, FUNCTION0, FUNCTION1, $\overline{URGENT}$, $\overline{RX\text{-}CLOCK}$, RX-DATA, and $\overline{DATA\ VALID}$.

※3. Applied to the SIG IN terminal.

※4. Applied to the $\overline{BLD}$ terminal.

※5. Applied to the $\overline{RESET}$ terminal.

※6. Applied to the $\overline{RST}$ terminal.

※7. Applied to the $\overline{T1}$ and $\overline{T2}$ terminals.

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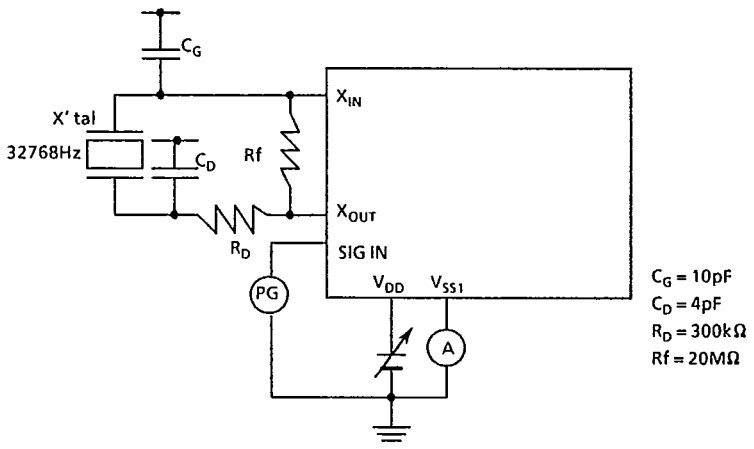
■ Measuring Circuits

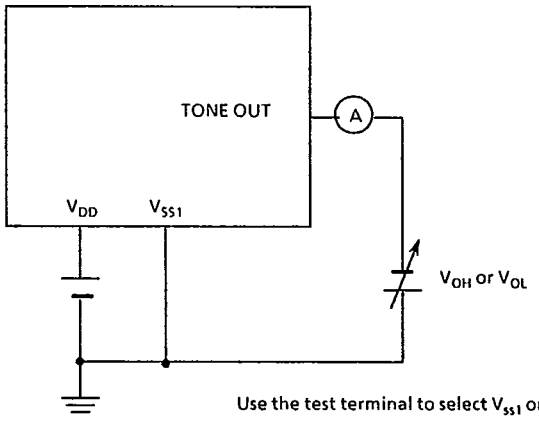
M : Measuring point PG : Pulse generator A : Ammeter

I



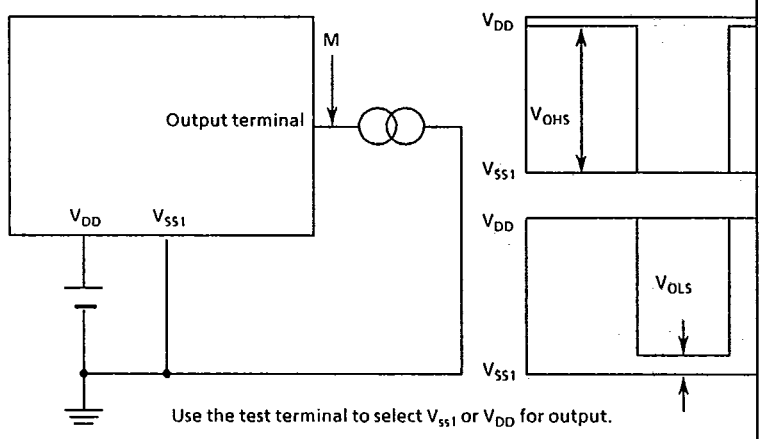
C_G = 10pF
C_D = 4pF
R_D = 300kΩ
Rf = 20MΩ

II



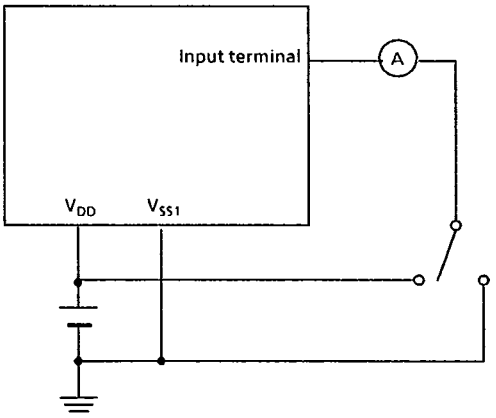
Use the test terminal to select V_{SS1} or V_{DD} for output.

III

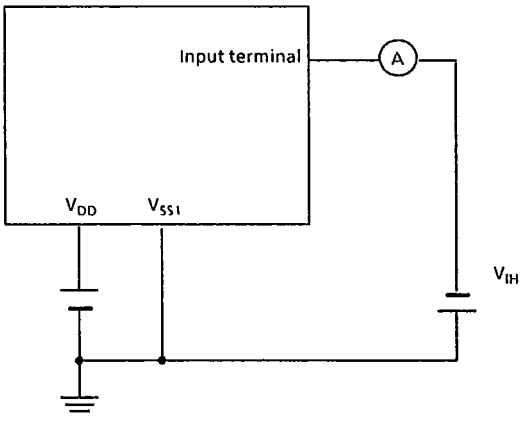


Use the test terminal to select V_{SS1} or V_{DD} for output.

IV



V



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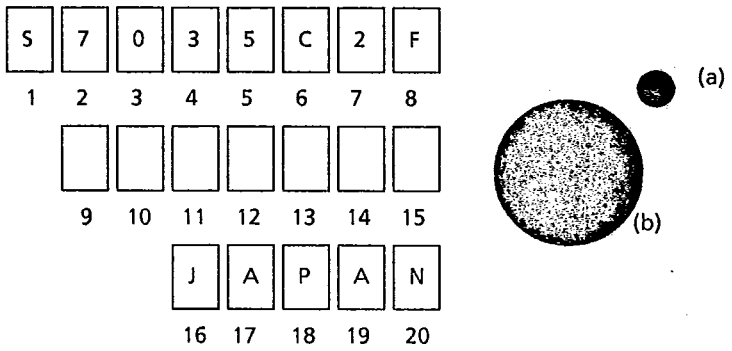
■ Markings



(a) and (b) : Symbols of the company

1 to 8	:	Model name
9	:	Assembly mark
10	:	Year of assembly. Indicated by the last digit of the year.
11	:	Month of assembly. January to September are indicated by 1 to 9, October = X. November = Y, December = Z.
12 to 15	:	Lot No.
16 to 20	:	Fixed as "JAPAN"