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# Dual-Modulus Divider 1:64/65 for 1 GHz with Standby Operation

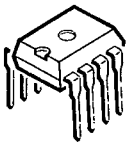
**TBB 212 A**

**Preliminary Data**

**Bipolar IC**

## Features

- High frequency operation: $f_{max}$ = 1100 MHz
- Pulse swallow function: 64/65
- Low power supply current: 8.5 mA typ. $V_S$ = 3 V
- Stable output amplitude: $V_Q$ = 1.0 $V_{pp}$ typ.
- Stable output amplitude is obtained load capacitance of 15 pF.



VPD 05025

P-DIP-8

VPS 05121

P-DSO-8

| Type | Ordering Code | Package |
|---|---|---|
| TBB 212 A | Q67000-H8760 | P-DIP-8 |
| TBB 212 AG | Q67000-H8761 | P-DSO-8 (SMD) |

The TBB 212 is specially intended for applications in radiotelephones. It contains several ECL divider stages, which have a total divider ratio of 1:64/65, depending on the control of the MOD input. It can be employed in standby mode (input STB = low). The IC is particular intended for GSM.

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## Circuit Description

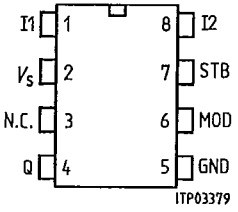
The divider has balanced push-pull inputs. It is driven unbalanced, the unused input has to be blocked by a capacitor (approx. 1.5 nF) with low series inductance. The divider of the component consists of several status-controlled master-slave flipflops, which have a total divider ratio of 1:64/65. The MOD inputs (divider ratio changeover input) and STB (input for standby mode) are controllable with TTL/CMOS levels. The ECL output of the divider is CMOS compatible (**see application circuit**). The typical swing is 1 Vpp.

### Truth Table for Operating Modes

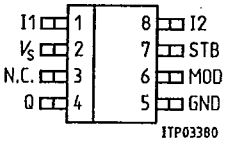
| Input | Level | Function at Q |
|---|---|---|
| MOD | High or unwired *)<br>low | 1:64<br>1:65 |
| STB | High or unwired *)<br>low | Normal<br>Q = high,<br>standby |

### Pin Configurations

(top view)




P-DIP-8

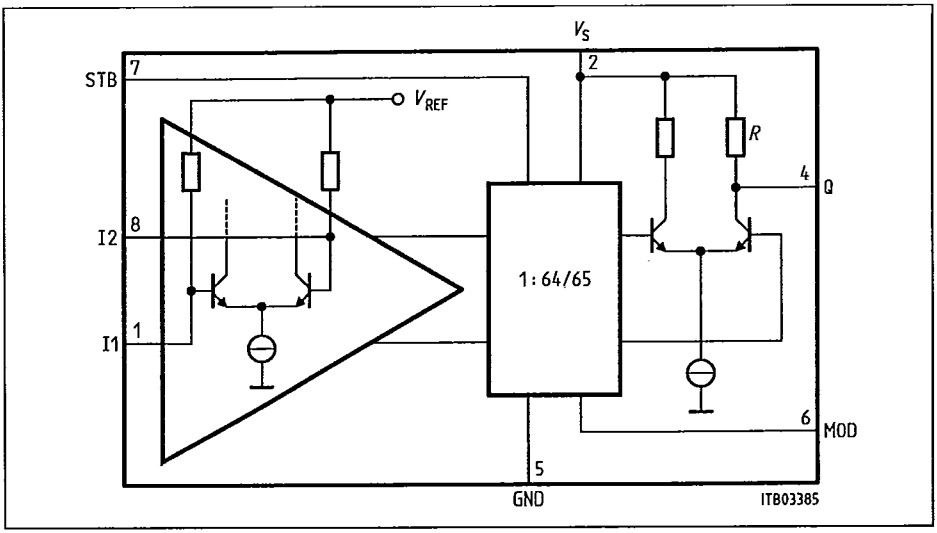



P-DSO-8

### Pin Definitions and Functions

| Pin No. | Symbol | Function |
|---|---|---|
| 1 | I1 | Input |
| 2 | $V_S$ | Supply voltage |
| 3 | N.C. | Not connected |
| 4 | Q | Output |
| 5 | GND | Ground |
| 6 | MOD | Input for control of divider ratio |
| 7 | STB | Input for standby mode |
| 8 | I2 | Input |

*) External circuitry increase noise immunity




**Block Diagram**

**Absolute Maximum Ratings**
$T_A$ = – 40 °C to 85 °C

| Parameter | Symbol | Limit Values | | Unit |
|---|---|---|---|---|
| | | min. | max. | |
| Supply voltage | $V_S$ | – 0.3 | 6 | V |
| Input voltage (pin 1; pin 8)<br>Input voltage (pin 6; pin 7) | $V_I$<br>$V_{MOD}$, $V_{STB}$ | – 0.3<br>– 0.3 | 2.5<br>6 | V<br>V |
| Output voltage (pin 4) | $V_Q$ | | $V_S$ | V |
| Output current (pin 4) | $-I_Q$ | | 10 | mA |
| Junction temperature | $T_j$ | | 125 | °C |
| Storage temperature | $T_{stg}$ | – 65 | 125 | °C |
| Thermal resistance<br>system – air P-DIP-8<br>P-DSO-8 | <br>$R_{th\,SA}$<br>$R_{th\,SA}$ | | <br>105<br>185 | <br>K/W<br>K/W |

**Operating Range**

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_S$ | 3.0 | 5.5 | V |
| Input frequency | $f$ | 140 | 1100 | MHz |
| Ambient temperature | $T_A$ | – 40 | 85 | °C |

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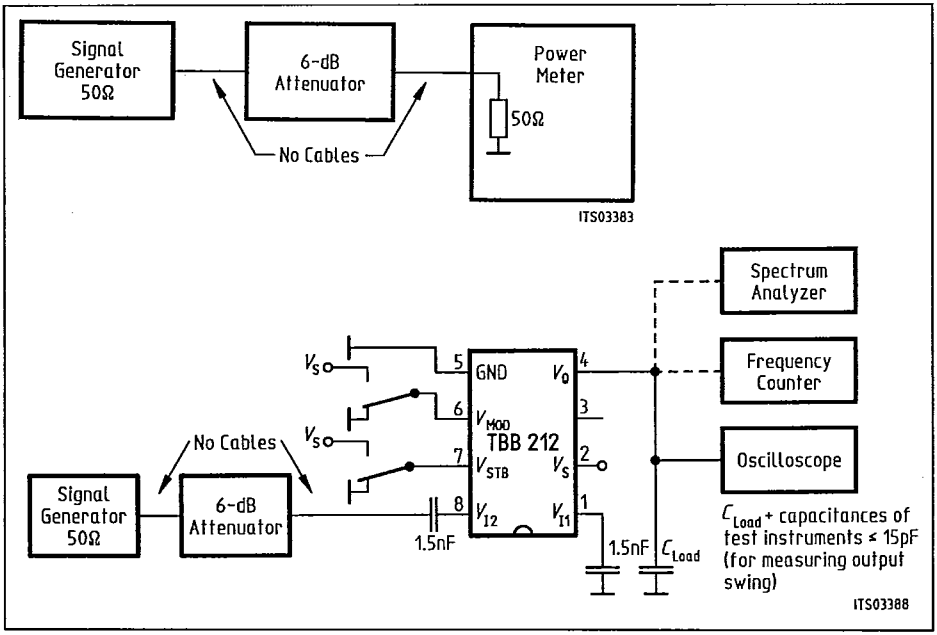
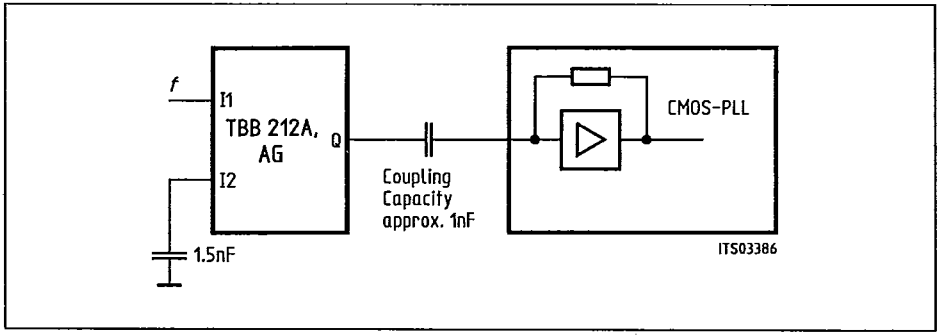
**Characteristics**

$V_S$ = 3.0 V to 5.5 V, $T_A$ = – 40 °C to 85 °C, refer to test circuit

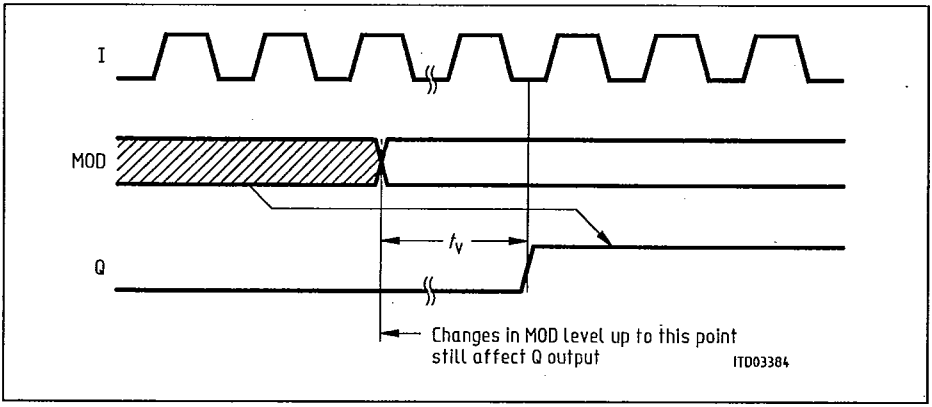
| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Current consumption in operation | | | | | | Inputs blocked<br>STB open, no load<br>$T_A$ = 25 °C |
| | $I_S$ | | 8.5 | | mA | $V_S$ = 3 V |
| | $I_S$ | | 9.5 | 12.8 | mA | $V_S$ = 4 V |
| | $I_S$ | | 10.5 | 13.5 | mA | $V_S$ = 5 V |
| in standby | $I_S$ | | 1.5 | | mA | Output n.c.<br>STB = GND<br>Inputs blocked |
| Input level (input sensitivity) | $V_I$ | | | | | |
| | | 10 | | 100 | mVrms | 140 MHz (sine voltage) |
| | | 5 | | 100 | mVrms | 400 MHz |
| | | 5 | | 100 | mVrms | 600 MHz |
| | | 5 | | 100 | mVrms | 800 MHz |
| | | 7 | | 100 | mVrms | 900 MHz |
| | | 10 | | 100 | mVrms | 1000 MHz |
| **MOD Input** | | | | | | |
| Switching threshold | $V_I$ | | 0.7 | | V | |
| H-input current | $I_{IH}$ | | 0 | 50 | µA | MOD = $V_S$ (1:64) |
| L-input current | $-I_{IL}$ | | 110 | 210 | µA | MOD = ground (1:65) |
| **Standby Input** | | | | | | |
| Switching threshold | $V_{STB}$ | | 0.7 | | V | |
| H-input current | $I_{IH}$ | | | 50 | µA | STB = $V_S$ |
| L-input current | $-I_{IL}$ | | 100 | 200 | µA | STB = ground |
| **Output** | | | | | | |
| Output voltage swing | $V_O$ | | 1 | | Vpp | $C_L \leq$ 15 pF |
| Output resistance | $R$ | | 1 | | kΩ | |
| **Switching Times** | | | | | | |
| Setup time | $t_V$ | | | 24 | ns | |




**Test Circuit**




**Application Circuit**


I
MOD
Q
$t_V$
Changes in MOD level up to this point
still affect Q output
ITD03384

**Diagram**