T-46-13-27

HYBRID

MEMORY PRODUCTS LIMITED

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PUMA 2E1000

PUMA 2E1000-85/10/12

Issue 1.0 : March 1989

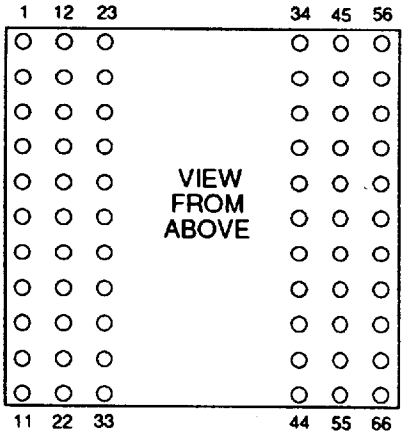
ADVANCE PRODUCT INFORMATION

1,048,576 bit CMOS High Speed E²PROM

Features

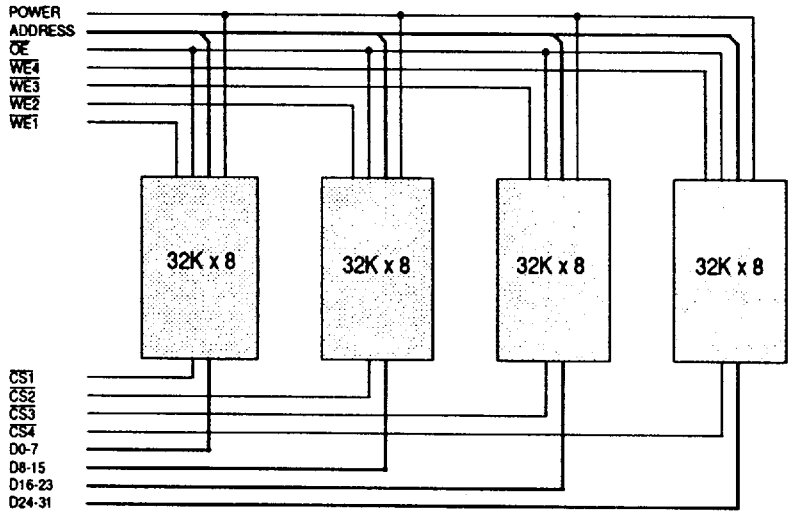
User Configurable as 8,16 or 32 bit wide.
Very fast access times of 85/100/120 nS.
Operating Power 1600mw (max) 32 bit mode
850mw (max) 16 bit mode
475mw (max) 8 bit mode
Low Power Standby 100mw (max) -L version.
Pin grid array gives 2:1 improvement over DIL.
Package Suitable for Thermal Ladder Applications.
Single byte and page write operation
Hardware and Software Data Protection
Endurance : 10^5 Cycles
Data retention : 10 years
May be screened in accordance with BS9400
and MIL-STD-883C (suffix MB)

Pin Definition



For pinout see page 7

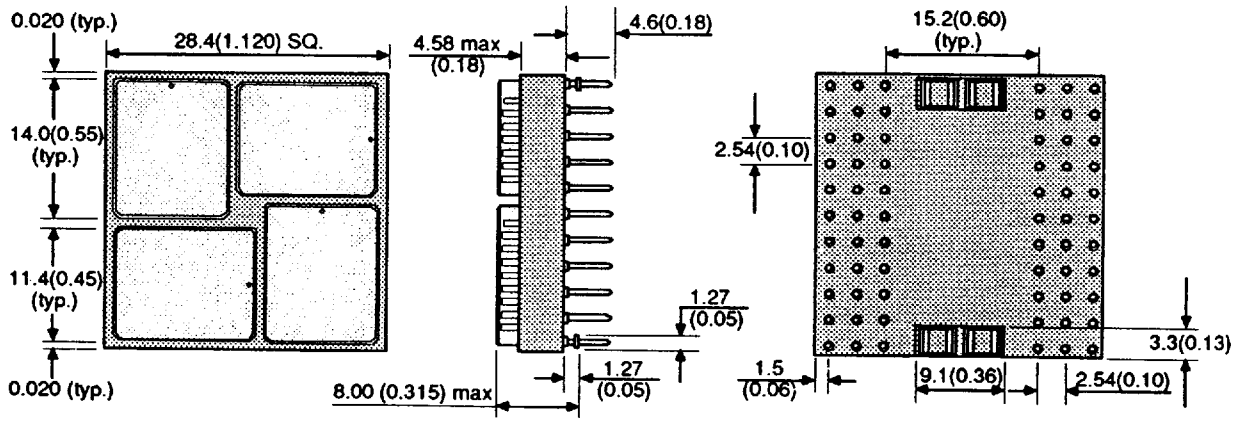
Block Diagram



Pin Functions

A0-14	Address Inputs
D0-31	Data Inputs/Outputs
$\overline{CS1-4}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE1-4}$	Write Enable
NC	No Connect
Vcc	Power (+5V)
GND	Ground

Package Details Dimensions in mm (inches).



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Absolute Maximum Ratings

Operating Temperature	T_{opr}	-55 to +125	°C
Storage Temperature	T_{stg}	-65 to +150	°C
All input voltages (including N.C. pins) with Respect to GND	V_{in1}	-0.6 to +6.26	V
All output voltages with respect to GND	V_{out}	-0.6 to V_{CC} +0.6	V
Voltage on $\overline{OE}$ and A9 with Respect to GND	V_{in2}	-0.6 to +13.5	V

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of The deviceat those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
(2) Pulse Width:-1 v for 50ns.
(3) With Respect to GND.

Recommended Operating Conditions

		min	typ	max	
DC Power Supply Voltage	V_{cc}	4.5	5.0	5.5	V
Input High Voltage	V_{ih}	2.0	-	V_{CC}+1	V
Input Low Voltage	V_{il}	0.3	-	0.8	V
Operating Temp Range	T_a	0	-	70	°C
	T_{al}	-40	-	85	°C (2E1000I)
	T_{am}	-55	-	125	°C (2E1000M, MB)

DC Electrical Characteristics

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{li1}	V_{in}=5.25V,Input $\overline{OE}$	-	-	40	µA
	I_{li2}	All other inputs	-	-	10	µA
Output Leakage Current	I_{out}	V_{out} = 5.25V/0.45V	-	-	40	µA
Operating Power Supply Current	I_{cc}	F=5MHz:I_{out}=0mA	230	260	320	mA
Standby Current	I_{sbl1}	$\overline{CS}$=2.0V to V_{cc}+1	-	-	200	mA
(L-Part)	I_{sbl2}	$\overline{CS}$=2.0V to V_{cc}+1	-	-	20	mA
Input Low Voltage	V_{IL}		-0.1	-	0.8	V
Input High Voltage	V_{IH}		2.0	-	V_{cc}+1	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA	-	-	0.45	V
Output High Voltage	V_{OH}	I_{OH} = -4mA	2.4	-	-	V

Notes : (1) For these currents min, typ & max values represent 8, 16 & 32 bit mode operation respectivly. Each value shown is a maximum.

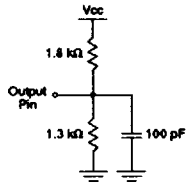
Capacitance (V_{cc}=5V±10%,T_a=25°C)

Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance:	C_{IN}	V_{in} =0V, 8 bit mode	16	24	pF
Output Capacitance:	C_{OUT}	$V_{i/o}$=0V, 8 bit mode	32	48	pF

Note: This parameter is calculated and not measured.

AC Test Conditions

*Input pulse levels: 0.45V to 2.4V
*Input rise and fall times: 5nS
*Input and Output timing reference levels: 1.5V
*Output load: 1 TTL gate + 100pF
*V_{cc}=5V±10%



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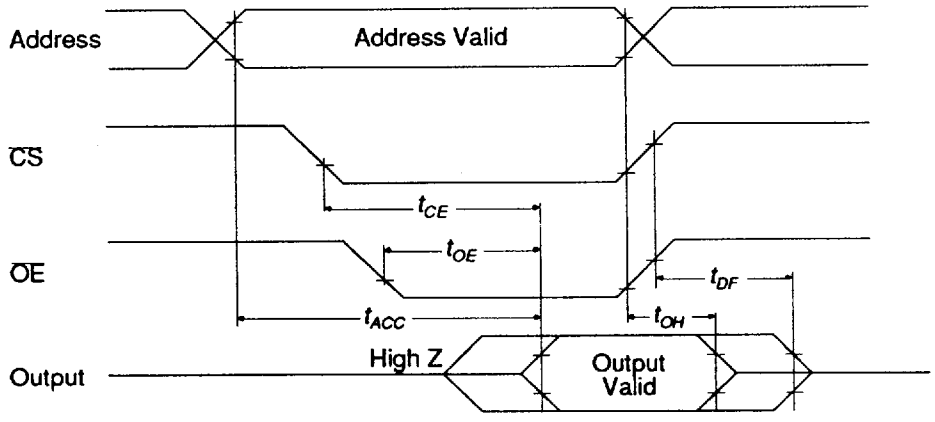
AC READ CHARACTERISTICS

Read Cycle

Parameter	Symbol	-85 min	-85 max	-100 min	-100 max	-120 min	-120 max	Unit
Address to Output Delay	t_{ACC}	-	85	-	100	-	120	ns
$\overline{CS}$ to Output Delay	t_{CS} 1	-	85	-	100	-	120	ns
$\overline{OE}$ to Output Delay	t_{OE} 2	0	35	0	40	0	50	ns
$\overline{CS}$ or $\overline{OE}$ to Output Float	t_{DF} 3,4	0	35	0	40	0	50	ns
Output Hold from $\overline{OE}$, $\overline{CS}$ or Address, (whichever occured first)	t_{OH}	0	-	0	-	0	-	ns

Notes: (1) $\overline{CS}$ may be delayed up to $t_{ACC} - t_{CS}$ after the address transition without impact on t_{ACC}.
(2) $\overline{OE}$ may be delayed up to $t_{CS} - t_{OE}$ after the falling edge of $\overline{CS}$ without impact on t_{CS} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
(3) t_{DF} is specified from $\overline{OE}$ or $\overline{CS}$ whichever occurs first (C_L = 5pF).
(4) This parameter is only sampled and is not 100% tested.

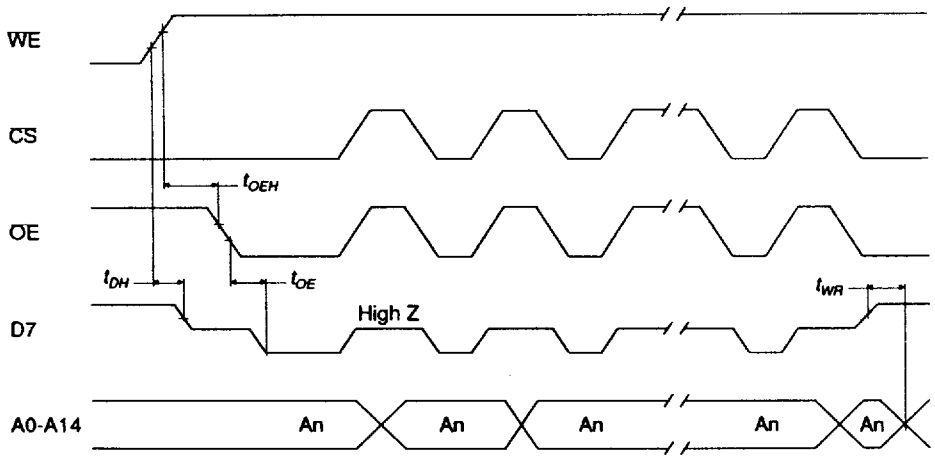
Read Cycle Timing Waveform



DATA Polling Characteristics

Parameter	Symbol	min	typ	max	Unit
Data Hold Time	t_{DH}	0	-	-	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	-	-	ns
$\overline{OE}$ to Output Delay	t_{OE}	-	-	100	ns
Write Recovery Time	t_{DF}	0	0	0	ns

DATA Polling Waveform



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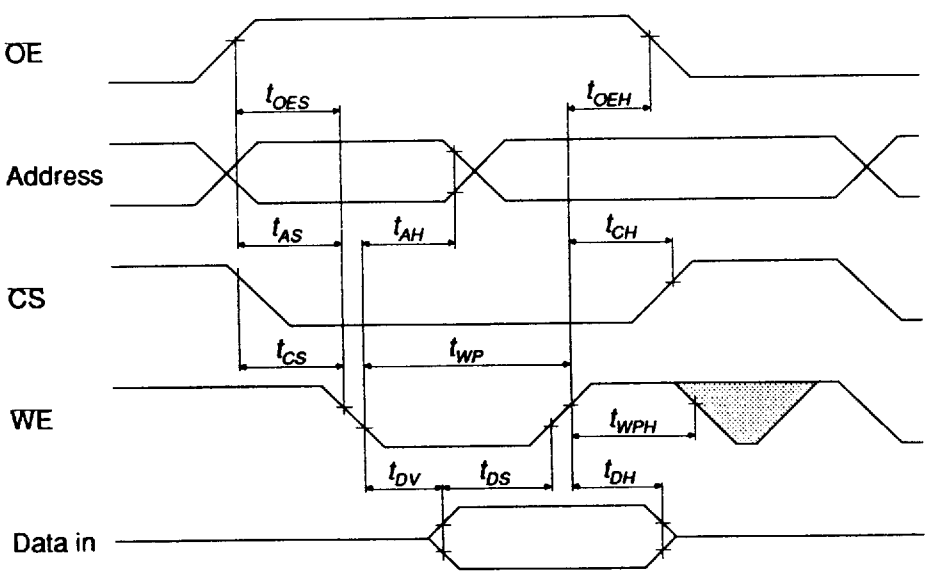
AC WRITE CHARACTERISTICS

Write Cycle

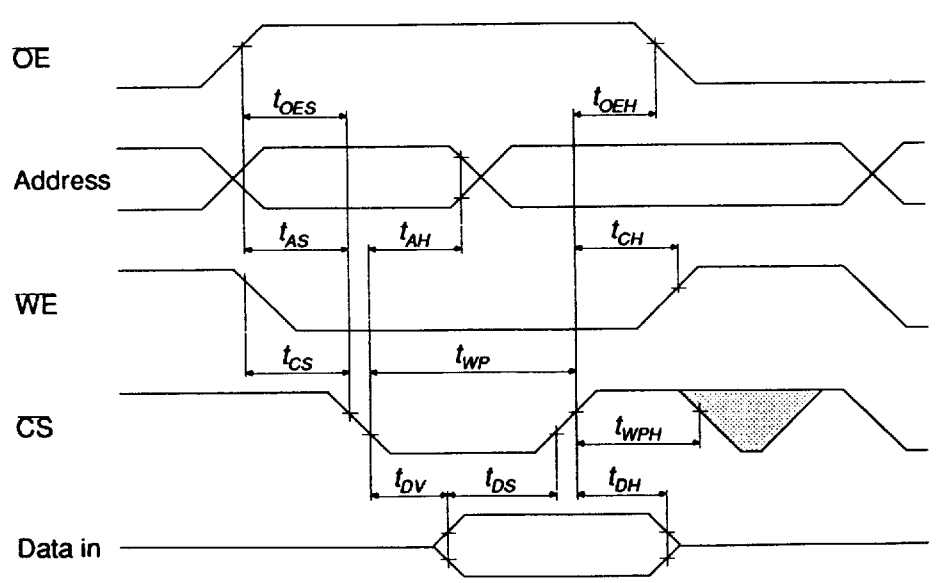
Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Address, OE Set-up Time	t_{AS}, t_{OES}	0	-	-	ns
Address Hold Time	t_{AH}	50	-	-	ns
Chip Select Set-up Time	t_{CS}	0	-	-	ns
Chip Select Hold Time	t_{CH}	0	-	-	ns
Write Pulse Width (WE or CE)	t_{WP}	100	-	-	ns
Data Set-up Time	t_{DS}	50	-	-	ns
Data, OE Hold Time	t_{DH}, t_{OEH}	0	-	-	ns
Time to Data Valid	t_{DV}	NR(1)	-	-	
Write Cycle Time AT28HC256	t_{WC}	0.4	-	10	ms

Note: (1) NR = No Restriction

AC Write Waveform - WE Controlled



AC Write Waveform - CS Controlled



PAGE MODE WRITE CHARACTERISTICS

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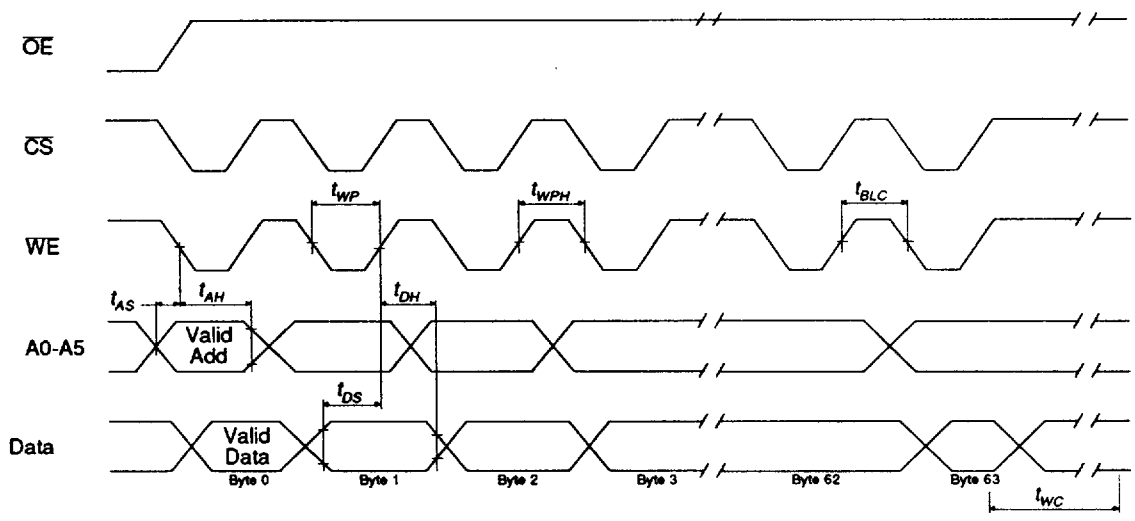
Write Cycle

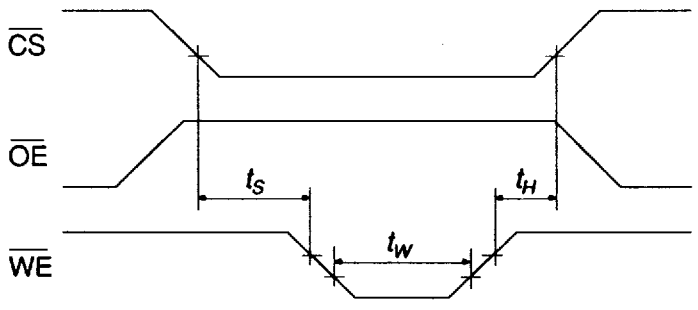
Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Write Cycle Time	t_{WC}	0.4	-	10	mS
Address Set-up Time	t_{AS}	0	-	3.0	mS
Address Hold Time	t_{AH}	50	-	-	nS
Data Set-up Time	t_{DS}	50	-	-	nS
Data Hold Time	t_{DH}	0	-	-	nS
Write Pulse Width	t_{WP}	100	-	-	nS
Byte Load Cycle Time	t_{BLC}	-	-	150	µS
Write Pulse Width High	t_{WPH}	50	-	-	nS

Page Mode Write Waveform



Note: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveform



$t_S = t_H = 5\mu s$

$t_W = 10$ ms

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Device Operation

Read

The PUMA 2E1000 is accessed in the same way as a static RAM, with the data stored at the memory location detemined by the address pins being placed on the output pins when $\overline{CS1\text{-}4}$ and $\overline{OE}$ are low, and $\overline{WE1\text{-}4}$ is high. Whenever $\overline{CS1\text{-}4}$ or $\overline{OE}$ are high, the outputs are in the OFF or high impedance state.

Write

A low pulse on $\overline{WE1\text{-}4}$ with $\overline{CS1\text{-}4}$ low or a low pulse on CS1-4 with WE1-4 low indicates a write cycle. The address is latched on the falling edge of $\overline{CS1\text{-}4}$ or $\overline{WE1\text{-}4}$, and the data is latched on the first rising edge of CS1-4 or $\overline{WE1\text{-}4}$. Once a byte write has begun it will automatically time itself to completion.

Page Mode Write

This operation mode allows 2 to 64 bytes of data to be loaded into a device, which are then simultaneously written. Once the first byte has been written, each subsequent byte must have the high to low transition of $\overline{WE1\text{-}4}$ (or $\overline{CS1\text{-}4}$) within 100µs of the same transition of the previous byte. If this 100µs time is exceeded, the load period ends and internal programming starts. A6 to A14 specify the page address (which must be valid during the above transitions) and A0 to A5 specify witch bytes within the page are to be written. Note that the bytes may be loaded in any order and may be changed within the same load period.

$\overline{DATA}$ Polling

In order to detect the end of a write cycle, two methodes are provided. During a write opeation (byte or page) an attempt to read the device will result in the complementof the last byte written appearing on the outputs. Once the write cycle is complete true data appears on the outputs and the next write cycle may begin.

Alternatively, during a write operation succesive attempts to read data will result in D6 (or D14, D22, D30 depending on the device selected) toggling between 1 and 0. Once a write is complete, this toggling will stop and valid data will be read.

Data Protection

Both hardware and software protection is provided as described below.

Four types of harware protection give high security against accidental writes:

(a) If VCC < 3.8V write is inhibited
(b) At power on, the device times out 5ms before allowing a write.
(c) $\overline{OE}$ low, $\overline{CS1\text{-}4}$ or $\overline{WE1\text{-}4}$ high inhabits writes.
(d) Pulses of less than 15ns on $\overline{WE1\text{-}4}$ or $\overline{CS1\text{-}4}$ do not indicatae a write cycle.

Software controlled data protection, once enabled by the user, means that a software algorithm must be used before any write can be performed. To enable this feature the algorithm opposite is followed, and must be reused for each subsequent write operation. Once set the data protection remains operational until it is disabled by the using the second algorithm opposite; power transitions will not reset this feature.

Device Indentification

An extra 64bytes of EEPROM memory are avaliable to the user, accesed by placing 12V±0.5V on A9. Address $7FC0_H$ to $7FFF_H$ then selects these bytes, which can be accessed in the same way as the normal memory array.

Operating Modes

The table below shows the logic inputs required to control the operating modes of each EEPROM on the PUMA 2E1000.

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	*Outputs*
Read	0	0	1	Data Out
Write (1)	0	1	0	Data In
Standby	1	X	X	Floating
Write Inhibit	X	X	X	
	X	0	X	
Output Disable	X	1	X	Floating
Chip Erase	0	V_H	0	Floating

1 = V_{IH} 0 = V_{IL} X = Don't care V_H = 12.0V±0.5V

Note: (1) Refer to AC Programming Waveforms

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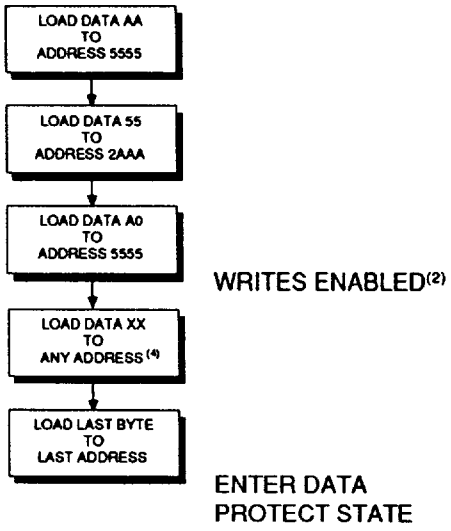
Connection Table

PGA Pin No.	Signal Name	PGA Pin No.	Signal Name	PGA Pin No.	Signal Name	PGA Pin No.	Signal Name	PGA Pin No.	Signal Name
1	D8	2	D9	3	D10	4	A13	5	A14
6	NC	7	NC	8	NC	9	D0	10	D1
11	D2	12	$\overline{WE2}$	13	$\overline{CS2}$	14	GND	15	D11
16	A10	17	A11	18	A12	19	Vcc	20	$\overline{CS1}$
21	NC	22	D3	23	D15	24	D14	25	D13
26	D12	27	$\overline{OE}$	28	NC	29	$\overline{WE1}$	30	D7
31	D6	32	D5	33	D4	34	D24	35	D25
36	D26	37	A6	38	A7	39	NC	40	A8
41	A9	42	D16	43	D17	44	D18	45	Vcc
46	$\overline{CS4}$	47	$\overline{WE4}$	48	D27	49	A3	50	A4
51	A5	52	$\overline{WE3}$	53	CS3	54	GND	55	D19
56	D31	57	D30	58	D29	59	D28	60	A0
61	A1	62	A2	63	D23	64	D22	65	D21
66	D20								

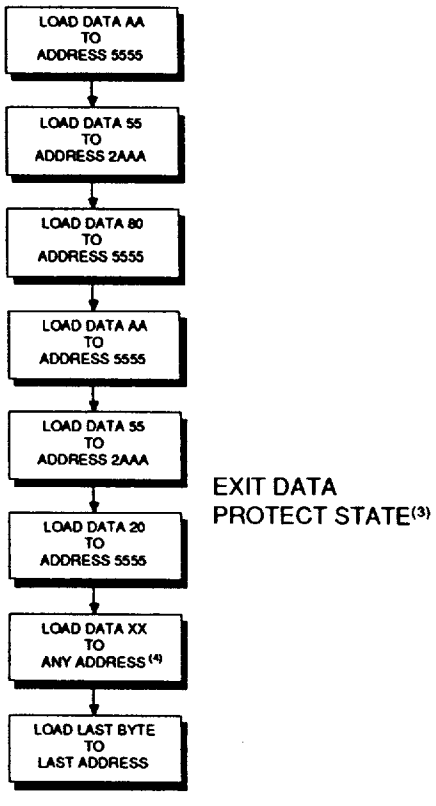
Software Data Protection

The algorithms below describe the process by which an industrial 32K x 8 device on the PUMA may be software write protected and unprotected. Thus, these algorithms apply to the PUMA operate in 8 bit mode; if 16 or 32 bit modes are being used, then the relevantdata would be placed on the 16 or 32 bit buses as two and four 8 bit bytes respectively. In the case of 16 bit mode, this process would be repeated twice with the appropiate devices selected.

Enable Algorithm(1)



Disable Algorithm(1)



Notes: (1) Data Format I/O7-I/O0 (Hex); Address Format: A14-A0 (Hex).

(2) Write Protect state will be activated at end of write even if no other data is loaded.

(3) Write Protect state will be deactivated at end of write period even if no other data is loaded.

(4) 1 to 64 bytes of data may be loaded.

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Military Screening Procedure

Module Screening Flow for high reliability product is in accordance with MIL-STD-883C method 5004 Level B and is detailed below:

MB MODULE SCREENING FLOW

SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
External visual	2017 Condition B (or manufacturers equivalent)	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to +150°C)	100%
Burn-In		
Pre Burn-in Electrical	Per Applicable device Specifications at Ta = +25°C (optional)	100%
Burn-In	Method 1015, Codition D, Ta = +125°C	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective Allowable (PDA)	Calculated at Post Burn-in at Ta=+25°C	10%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per HMP or customer specification	

Ordering Information

PUMA 2E1000LMB-10

Speed	85	= 85 ns
	10	= 100 ns
	12	= 120 ns
Temp. range/screening	Blank	= Commercial Temp.
	I	= Industrial Temp.
	M	= Military Temp.
	MB	= High Reliability MIL STD 883C Screening
Power Consumption	Blank	= Standard Part
	L	= Low Power Part
Memory Type	E	= EEPROM

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