

TOSHIBA

**Quad Physical
Layer Controller**

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T C 3 5 8 2 3 F

P R E L I M I N A R Y

R E V I S I O N 0 . 4

D A T A B O O K

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Description

Toshiba's TC35823F single-chip Quad Physical Layer Controller (QPLC) is ideal for use in multi-port asynchronous transfer mode (ATM) switch applications. Its integrated clock functions eliminate the need for external clock data recovery and help reduce costs and space requirements in ATM applications including switches, hubs, routers, bridges, enterprise and access multiplexers, video servers, file servers and FTTC/FTTH.

The four channels of 155.52Mbps SONET/SDH framing functions are integrated with four transmit and receive ports. Each receive port has a clock recovery Phase Locked Loop with a current-regulated, constant amplitude voltage controlled oscillator to achieve low jitter.

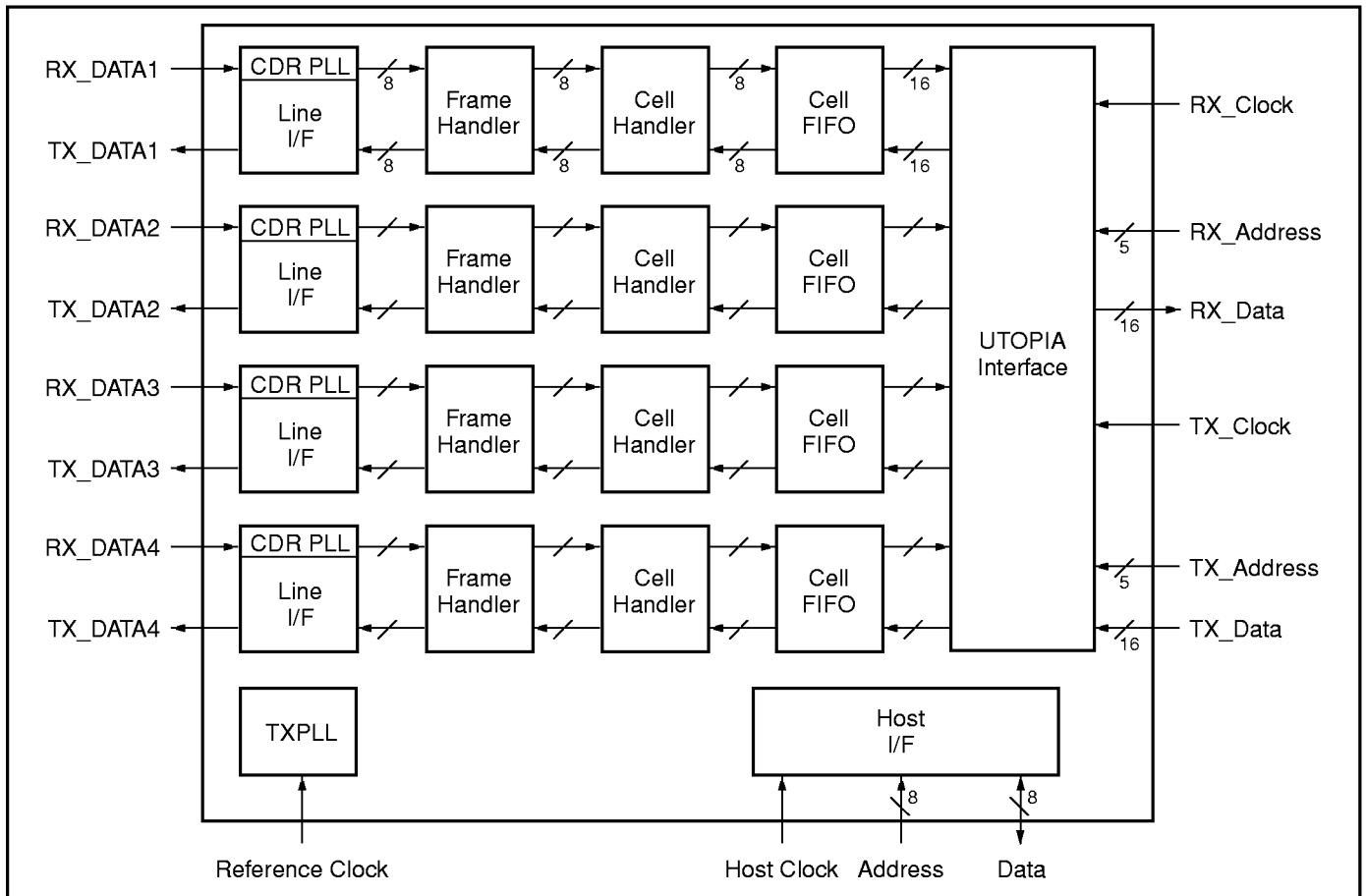
The QPLC supports the industry standard Universal Test and Operations Physical Layer Interface for ATM (UTOPIA), Level 2. It is also fully compatible with the Synchronous Optical Network (SONET) and the Synchronous Digital Hierarchy (SDH) standards for high speed digital transmission. The TC35823F

supports SONET standards STS-3C (155.52Mbps), STS-1 (51.84Mbps) and STS-1/2 (25.92Mbps) and SDH at STM-1 (155.52Mbps). The bit rate at each port can be set separately to each of the three supported data transfer rates.

The QPLC offers programmable section overhead (SOH)/path overhead (POH) handling. Its 0.6 micron triple well, double-layer metal CMOS structure prevents noise in the digital port from flowing into the analog portion of the chip and provides isolation between the ports. The TC35823F operates internally at 19.44MHz with a maximum 50MHz UTOPIA-interface operation, and requires a single +5V power supply.

The analog portion consists of four clock/data recovery blocks (Line I/Fs) and a transmit PLL (TXPLL). The line I/F converts a serial bit stream to a byte stream using a bit clock recovered from receive data by a receive PLL (RXPLL), and also converts a byte stream to a transmit bit stream. The TXPLL generates a transmit clock from a 19.44MHz external clock. A Pseudo-ECL (PECL) interface is used for the line interface.

The digital frame handling portions of the chip include a frame handler, cell handler and cell FIFO for each channel. The frame handler provides frame synchronization and descrambling for receive, and frame pattern insertion for transmit. The cell handler performs ATM cell delineation, header error correction (HEC), and ATM cell payload descrambling for receive, and HEC generation and ATM cell payload scrambling for transmit. The cell FIFO provides the asynchronous interface between the cell handler and the cell interface. The receive/transmit FIFO can accommodate four cells each per port. The cell interface arbitrates ATM cell streams from the cell FIFO to the ATM layer device based on UTOPIA Level 2. The host interface provides access to registers (one of which selects SONET/SDH) and memory in the QPLC.



Preface Figure 1 QPLC Block Diagram

Primary Features of QPLC

1. 4 ports of SONET: STS-3c, STS-1, STS-1/2, SDH:STM-1.
2. 156MHz PECL serial line interface with on-chip clock recovery and on-chip clock synthesis.
3. Cell interface based on UTOPIA Level-2, Multi-Phy, 16 bit mode (Current version of QPLC does not support UTOPIA Level-2, Multi-Phy, 8-bit mode. Next version will support this.).
4. Firmware programmable SOH/POH handling.
5. 19.44MHz/6.48MHz/3.24MHz internal operation.
6. Maximum 50MHz cell interface operation.
7. 0.6 μ m CMOS technology.

8. Operation on +5.0V single power supply
9. 240-pin thin plastic QFP with heat spreader.

Benefits

- Reduces cost and board space
- Integrated clock functions eliminates need for external clock data recovery
- Maintains data transfer rate with low jitter

Applications

- ATM switches and hubs
- Routers and bridges
- Enterprise and access multiplexers
- Video and file servers
- FTTC/FTTH

Functional Summary of QPLC

Receive Functions

1. Clock recovery from 156/52/26Mbps NRZ signal.
2. Byte alignment and frame synchronization.
3. Frame descrambling.
4. Frame overhead analysis.
5. ATM cell synchronization.
6. ATM cell header error correction.
7. ATM cell payload descramble.

Transmit Functions

1. ATM cell payload scramble.
2. ATM HEC generation.
3. Frame overhead generation.
4. Frame assembly.
5. Frame scrambling.

The QPLC supports SONET STS-3c, STS-1 and STS-1/2. The following sections in this chapter review the frame format, frame overhead, error status, alarm signaling and performance monitoring of STS-3c(STM-1), STS-1 and STS-1/2.

Frame Format

STS-3c(STM-1)

The STS-3c has a frame of 270 columns (in bytes) and 9 rows, with 9 columns of overhead and 261 columns of payload as shown in Figure 1-1. The virtual container VC4 is mapped into the payload area of STS-3c. VC4 has a column of overhead called POH (Path Overhead) and 260 columns of payload. The ATM cells are mapped into the payload area of VC4.

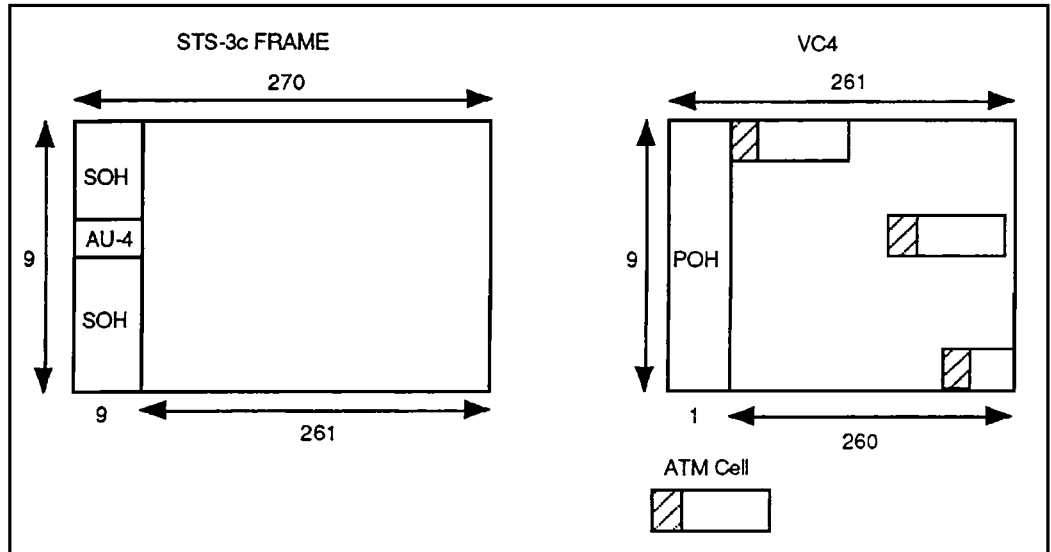


Figure 1-1 STS-3c Frame Format

STS-1, STS-1/2

The STS-1 has a frame of 90 columns (in bytes) and 9 rows, with 3 columns of overhead called SOH and 87 columns of payload as shown in Figure 1-2. The STS-1 SPE (=Synchronous Payload Envelope), which is mapped into the payload area, has a column of overhead called POH (=Path Overhead) and 87 columns of payload. The ATM cells are mapped into the payload area of STS-1 SPE except for the 30th and 59th columns which are designated stuff columns. STS-1/2 has the same frame format with STS-1.

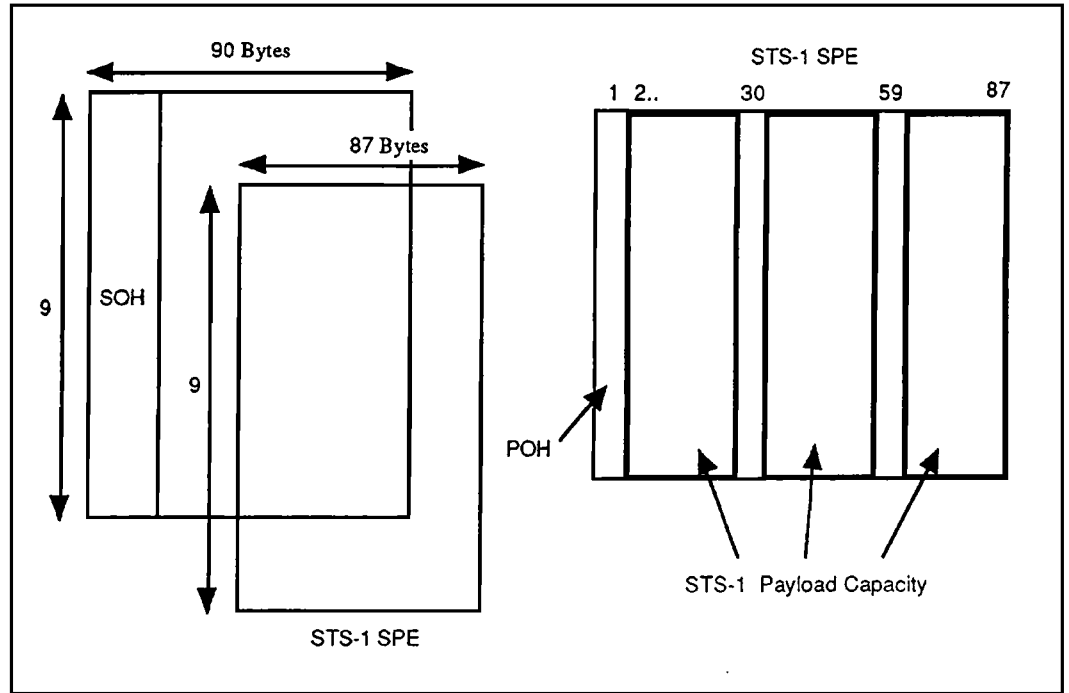


Figure 1-2 STS-1 (STS-1/2) Frame Format

Frame Overhead

The overhead bytes are assigned into SOH and POH as shown in Table 1-1 for STS-3c(STM-1) and Table 1-2 for STS-1 and STS-1/2.

Table 1-1 STS-3c(STM-1) Overhead Byte Assignment

SOH									POH
A1	A1	A1	A2	A2	A2	C1	C1	C1	J1
B1	-	-	E1	-	-	F1	-	-	B3
D1	-	-	D2	-	-	D3	-	-	C2
H1	H1	H1	H2	H2	H2	H3	H3	H3	G1
B2	B2	B2	K1	-	-	K2	-	-	F2
D4	-	-	D5	-	-	D6	-	-	H4
D7	-	-	D8	-	-	D9	-	-	Z3
D10	-	-	D11	-	-	D12	-	-	Z4
Z1	Z1	Z1	Z2	Z2	Z2	E2	-	-	Z5

Table 1-2 STS-1 (STS-1/2) Overhead Byte Assignment

SOH			POH
A1	A2	C1	J1
B1	E1	F1	B3
D1	D2	D3	C2
H1	H1	H1	G1
B2	K1	K2	F2
D4	D5	D6	H4
D7	D8	D9	Z3
D10	D11	D12	Z4
Z1	Z2	E2	Z5

The usage of these bytes are almost common for STS-3c(STM-1), STS-1 and STS1/2. Table 1-3 and Table 1-4 summarize the usage of the overhead bytes in SOH and POH, respectively.

Table 1-3 Overhead Byte Functions in SOH

Name	Function
A1, A2	Frame synchronization.
C1	Identify STS1's in STS-N frame (SONET)/dentify STM-1's in STM-N frame (SDH).
B1	Section BIP-8 error.
E1	Not used in UNI.
F1	Not used in UNI.
D1-D3	Not used in UNI.
H1, H2	AU pointer and Path-AIS.
H3	Stuff operation.
B2	Line BIP-24 for STS-3c and Line BIP-8 in STS-1.
K1	Not used in UNI.
K2	Line AIS and Line RDI.
D4-D12	Not used in UNI.
Z1	Not used in UNI.
Z2	Line FEBE.

Table 1-4 Overhead Byte Functions in POH

Name	Function
J1	Check the path connection.
B3	Monitor Path BIP-8 error.
C2	Indicate the payload type. For ATM cell, the value should be 13H.
G1	Path RDI and Path FEBE.
F2	Not used in UNI.
H4	Indicate the location of the first ATM cell following H4.
Z3	Not used in UNI.
Z4	Not used in UNI.
Z5	Not used in UNI.

Error Status

QPLC detects the following five error status.

Table 1-5 LOS: Loss of Signal

	Condition/Action
Detection	No signal condition continues for $T1\mu\text{sec}$ ($2.3 \leq T1 \leq 100$).
Release	Two consecutive valid frame alignment patterns (A1s and A2s) have been detected without LOS between the two valid frame alignment patterns.
Action	Once LOS is detected, the equipment will send Line AIS, Line RDI, Path AIS or Path RDI.

Table 1-6 OOF: Out of Frame

	Condition/Action
Detection	Four consecutive invalid framing patterns have been received.
Release	Two consecutive valid frame alignment patterns have been detected.
Action	The equipment should monitor the duration of OOF.

Table 1-7 LOF: Loss of Frame

	Condition/Action
Detection	OOF has continued for 3msec.
Release	In frame condition has continued for 3msec.
Action	Once LOF is detected, the equipment shall send Line AIS, Line RDI, Path AIS or Path RDI.

Table 1-8 LOP: Loss of Pointer

	Condition/Action
Detection	A valid pointer is not found in N consecutive frames or N consecutive NDF's are detected, where $8 \leq N \leq 10$.
Release	A valid pointer with normal NDF, or a concatenation indicator, is detected in three consecutive frames. When an all 1s pointer (AIS) is detected in three consecutive frames, the equipment should exit from the LOP state and enter the Path AIS state.
Action	Once LOP is detected, the equipment shall send Path AIS or Path RDI.

Table 1-9 LOC: Loss of Cell Delineation

	Condition/Action
Detection	Seven consecutive HEC errors have been detected.
Release	Seven consecutive normal HECs have been detected.
Action	When LOC is detected, the equipment shall send Path AIS or Path RDI.

Alarm Signaling

QPLC supports the following five alarm signals.

Table 1-10 Line AIS (MS-AIS)

	Definition
Condition of Generation	State of LOS or LOF.
Generation	$K2(b6-8) = 111$ and all-ones in the payload of STS-3c/STS-1 frame.
Condition of Removal	Exit from LOS and LOF.
Removal	$K2(b6-8) \neq 111$.
Detection of Generation	$K2(b6-8) = 111$ in five consecutive frames (SONET)/in at least three consecutive frames (SDH).
Detection of Removal	$K2(b6-8) \neq 111$ in five consecutive frames (SONET)/in at least three consecutive frames (SDH).

Table 1-11 Line RDI (MS-RDI)

	Definition
Condition of Generation	Detection of LOS, LOF or Line AIS.
Generation	$K2(b6-8) = 110$.
Condition of Removal	Exit from LOS, LOF and Line AIS.
Removal	$K2(b6-8) \neq 110$.
Detection of Generation	$K2(b6-8) = 110$ in five consecutive frames (SONET)/in at least three consecutive frames (SDH).
Detection of Removal	$K2(b6-8) \neq 110$ in five consecutive frames (SONET)/in at least three consecutive frames (SDH).

Table 1-12 Path AIS

	Definition
Condition of Generation	Detection of LOS, LOF, LOP, LOC or Line AIS.
Generation	All-ones in the H1/H2/H3 bytes and the entire payload.
Condition of Removal	Exit from LOS, LOF, LOP, LOC and Line AIS.
Removal	A correct STS pointer with NDF set to '1001' followed by normal pointer operations and normal data in the payload.
Detection of Generation	All-ones in the H1/H2 bytes for three consecutive frames (for SONET and SDH as well).
Detection of Removal	A valid STS Pointer with NDF set to '1001', or a valid STS Pointer with normal NDF in three consecutive frames (for SONET and SDH as well).

Table 1-13 Path RDI (P-FERF)

	Definition
Condition of Generation	Detection of LOS, LOF, LOP, LOC, Line AIS or Path AIS.
Generation	G1(b5) = 1.
Condition of Removal	Exit from LOS, LOF, LOP, LOC, Line AIS and Path AIS.
Removal	G1(b5) = 0.
Detection of Generation	G1(b5) = 1 in five consecutive frames (SONET)/in at least three consecutive frames (SDH).
Detection of Removal	G1(b5) = 0 in five consecutive frames (SONET)/in at least three consecutive frames (SDH).

Table 1-14 Path YEL

	Definition
Condition of Generation	Detection of LOS, LOF, LOP, LOC, Line AIS or Path AIS for T sec where $2 \leq T \leq 10$.
Generation	G1(b5) = 1.
Condition of Removal	Exit from LOS, LOF, LOP, LOC, Line AIS and Path AIS for T sec where $2 \leq T \leq 10$.
Removal	G1(b5) = 0.
Detection of Generation	G1(b5) = 1 in five consecutive frames.
Detection of Removal	G1(b5) = 0 in five consecutive frames.

Performance Monitoring

QPLC supports the following two performance monitors.

Line FEBE

Line BIP-24 is calculated over the entire area of each frame after descrambling except for the first to third rows of SOH based on 24 bits interleaved parity calculation using even parity. The calculated BIP-24 code is compared with the triple B2 bytes of the following frame. Differences indicates the line level bit errors. The bit errors are counted and inserted to the third Z2 byte of transmit SOH as shown in Figure 1-3.

Z2	Z2	Z2
00H	00H	0 L-FEBE[6:0]

Figure 1-3 L-FEBE Insertion to Z2 Byte

Path FEBE

Path BIP-8 is calculated over the entire area of each VC4 (or SPE for STS-1) after descrambling based on 8 bits interleaved parity calculation using even parity. The calculated BIP-8 code is compared with the B3 byte of the following frame. Differences indicates the section level bit errors. The bit errors are counted and inserted to the higher 4 bits of G1 byte of transmit SOH as shown in Figure 1-4.

G1	
P-FEBE[3:0]	0000

Figure 1-4 P-FEBE Insertion to G1 Byte

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Block Diagram

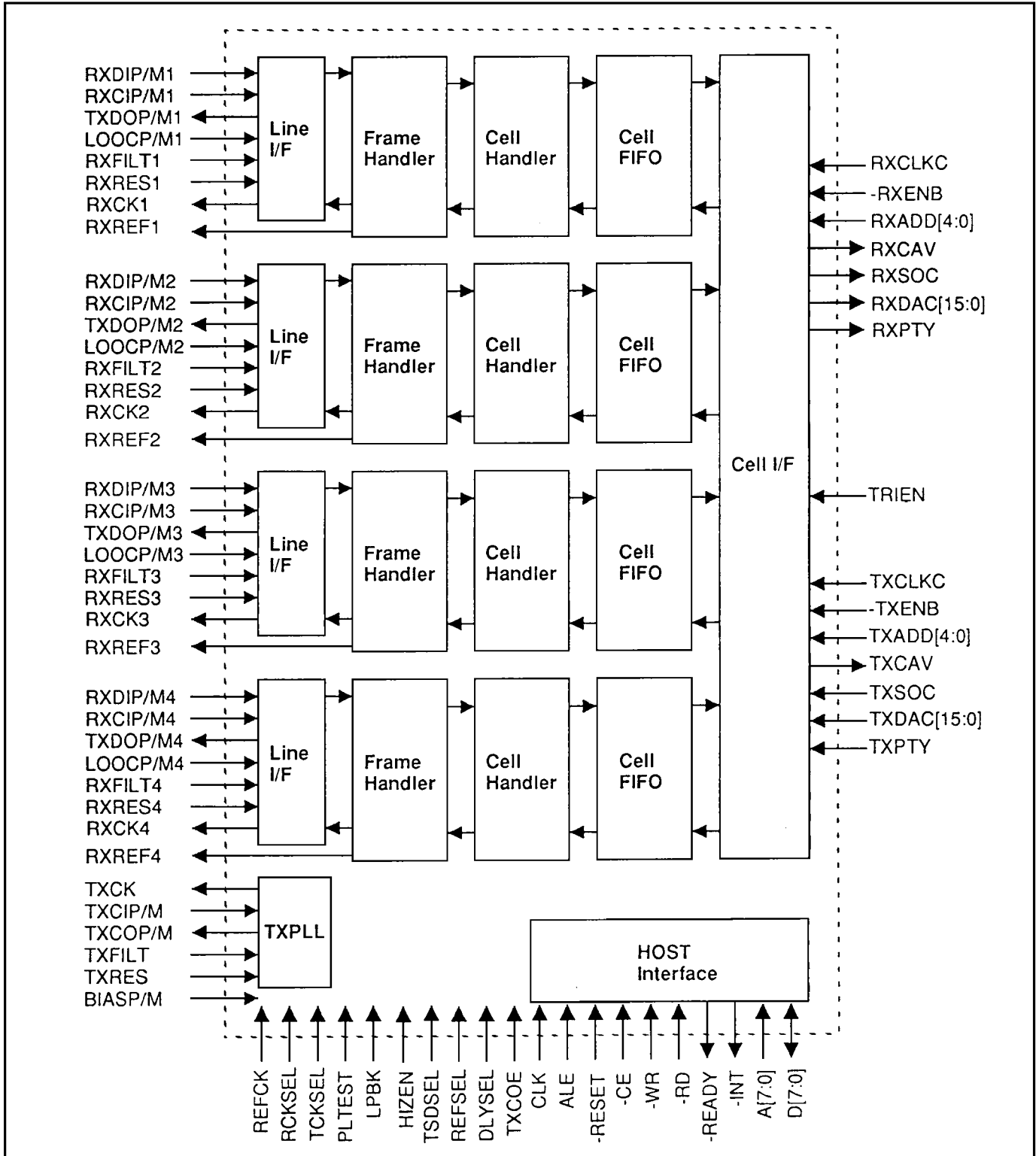


Figure 2-1 QPLC Block Diagram

Pin Diagram

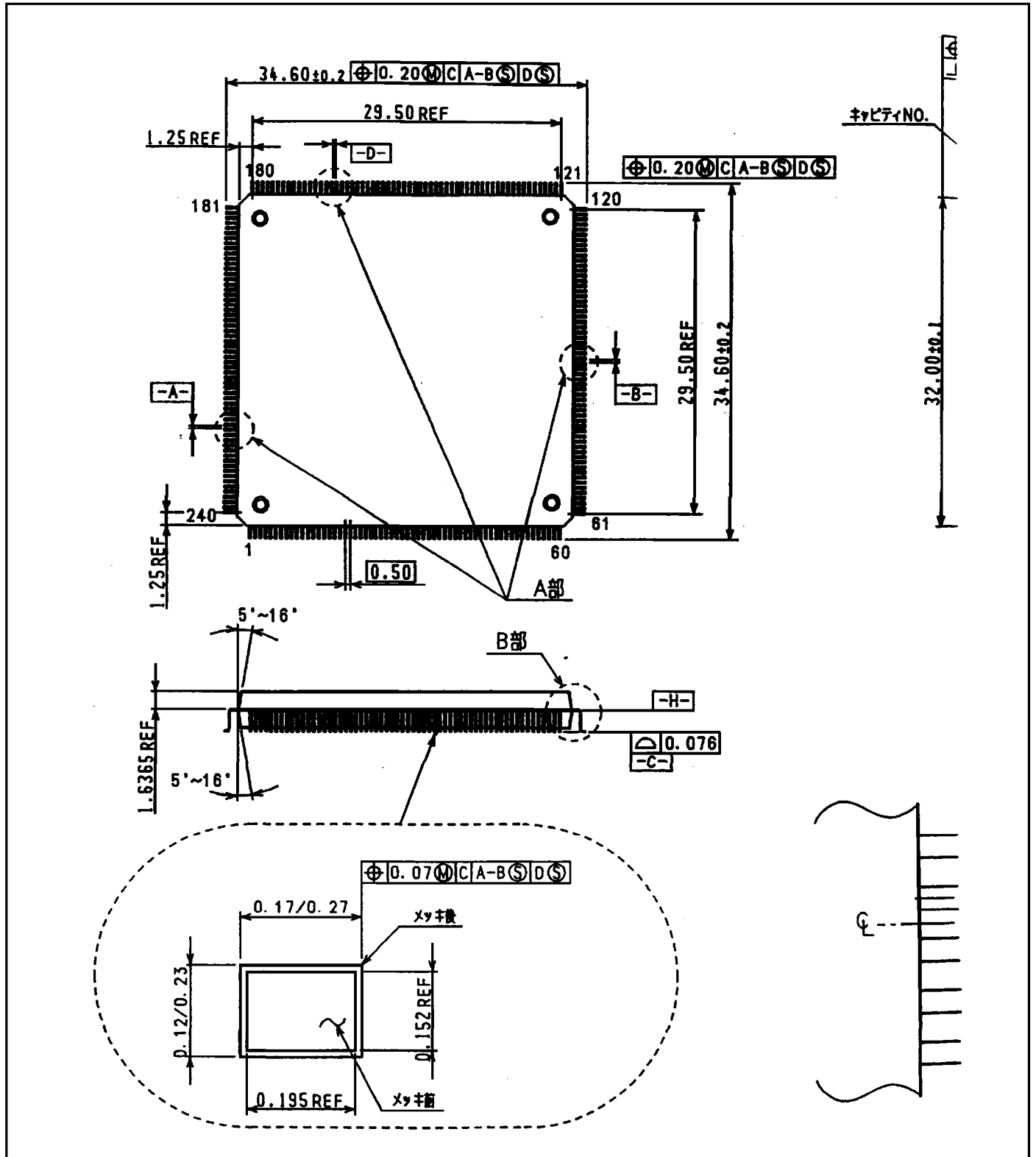


Figure 2-1 HQFP240-P-3232-0.50A

Pin Description

Table 2-1 Line I/F (49 Pin)

Pin Name	Pin No.	I/O	Type	Description
RXDIP1 RXDIM1	186 187	I	P-ECL	Port 1 receives differential data input. Both pins should be terminated to 3.0V voltage source via 50ohm.
RXDIP2 RXDIP2 RXDIM2	199 200	I	P-ECL	Port 2 receives differential data input. Both pins should be terminated to 3.0V voltage source via 50ohm.
RXDIP3 RXDIP3 RXDIM3	224 225	I	P-ECL	Port 3 receives differential data input. Both pins should be terminated to 3.0V voltage source via 50ohm.
RXDIP4 RXDIP4 RXDIM4	238 239	I	P-ECL	Port 4 receives differential data input. Both pins should be terminated to 3.0V voltage source via 50ohm.
RXCIP1 RXCIM1	189 190	I	P-ECL	Port 1 receives differential clock input for diagnostic text only. This input is active when RCKSEL is tied low.
RXCIP2 RXCIM2	202 203	I	P-ECL	Port 2 receives differential data input. Termination should be provided externally. This input is active when RCKSEL is tied low.
RXCIP3 RXCIM3	227 228	I	P-ECL	Port 3 receives differential data input. Termination should be provided externally. This input is active when RCKSEL is tied low.
RXCIP4 RXCIM4	2 3	I	P-ECL	Port 4 receives differential data input. Termination should be provided externally. This input is active when RCKSEL is tied low.
LOOCP1 LOOCM1	192 193	I	P-ECL	Port 1 loss of optical carrier detection signal from O/E module. Termination should be provided externally. When LOOCP1 is high and LOOCM1 is low, QPLC assumes that the optical power to port 1 is below threshold.
LOOCP2 LOOCM1	205 206	I	P-ECL	Port 2 loss of optical carrier detection signal from O/E module. Termination should be provided externally. When LOOCP2 is high and LOOCM2 is low, QPLC assumes that the optical power to port 2 is below threshold.
LOOCP3 LOOCM3	230 231	I	P-ECL	Port 3 loss of optical carrier detection signal from O/E module. Termination should be provided externally. When LOOCP3 is high and LOOCM3 is low, QPLC assumes that the optical power to port 3 is below threshold.
LOOCP4 LOOCM4	5 6	I	P-ECL	Port 4 loss of optical carrier detection signal from O/E module. Termination should be provided externally. When LOOCP4 is high and LOOCM4 is low, QPLC assumes that the optical power to port 4 is below threshold.
TXDOP1 TXDOM1	182 183	O	P-ECL	Port 1 transmit differential data output.
TXDOP2 TXDOM2	196 197	O	P-ECL	Port 2 transmit differential data output.

Table 2-1 Line I/F (49 Pin) (continued)

Pin Name	Pin No.	I/O	Type	Description
TXDOP3 TXDOM3	220 221	O	P-ECL	Port 3 transmit differential data output.
TXDOP4 TXDOM4	234 235	O	P-ECL	Port 4 transmit differential data output.
TXCIP TXCIM	212 213	I	P-ECL	Transmit differential clock input. When TCKSEL input is tied low, TXDOP/M1, TXDOP/M2, TXDOP/M3 and TXDOP/M4 are updated on clock derived from this clock. 155.52MHz clock should be input.
TXCOP TXCOM	216 217	O	P-ECL	Differential clock monitor output. When TCKSEL is tied high, TXPLL output is observed. When TCKSEL is tied low, TXCIP/M is observed. This output is disabled when TXCOE is tied high.
BIASP BIASM	208 209	I	P-ECL	These input generate P-ECL output voltage level. To be terminated with 3.0V voltage source via 50ohm resistors respectively.
RXFILT1	161	AO	Analog	To be connected with external LPF for receiving PLL of Port 1.
RXFILT2	165	AO	Analog	To be connected with external LPF for receiving PLL of Port 2.
RXFILT3	169	AO	Analog	To be connected with external LPF for receiving PLL of Port 3.
RXFILT4	173	AO	Analog	To be connected with external LPF for receiving PLL of Port 4.
RXRES1	162	AO	Analog	To be connected with resistor for reference current of Port 1.
RXRES2	166	AO	Analog	To be connected with resistor for reference current of Port 2.
RXRES3	170	AO	Analog	To be connected with resistor for reference current of Port 3.
RXRES4	174	AO	Analog	To be connected with resistor for reference current of Port 4.
TXFILT	177	AO	Analog	To be connected with external LPF for transmit PLL.
TXRES	178	AO	Analog	To be connected with resistor for reference current in transmit.
REFCK	143	I	CMOS	Reference clock of 19.44MHz should be used.

Table 2-2 Mode Select (8 Pin)

Pin Name	Pin No.	I/O	Type	Description
TXCOE	154	I	CMOS	Low active output enable for TXCOP/M.
RCKSEL	157	I	CMOS	Receive Clock Select. When tied high, the internal clock recovery PLL is activated and RXCIP/MRXC input buffer is put in stand-by mode. When tied low, the internal clock recovery is put in stand-by mode and RXCIP/M is used to sample RXDIP/M1-4.
TCKSEL	158	I	CMOS	Transmit Clock Select. When tied high, TXPLL is used to serialize transmit data. When tied low, TXCIP/M is used to serialize transmit data. In loop-timing mode, the receive clock is used as transmit clock too and TCKSEL has no effect.
LPBK	148	I	CMOS	When tied low, normal operation is selected. When tied high, the receive input data is directly loop-backed to transmit output and transmit data generated in QPLC is loop-backed to receive input.

Table 2-2 Mode Select (8 Pin) (continued)

Pin Name	Pin No.	I/O	Type	Description
REFSEL	149	I	CMOS	When tied high, RXPLL generates x8 clock from REFCK. When tied low, RXPLL recovers clock from receive data basically.
TSDSEL	152	I	CMOS	Transmit Data Select. When tied low, normal transmit data is output from TXDOP/M1-4. When tied high, RXPLL output of each port or RXCIP/M is output from TXDOP/M1-4 depending on RCKSEL.
BCKM	153	I	CMOS	BCKM controls byte clock outputs RXCK1-4. When tied high, RXCK2-4 are disabled and byte clock from one of 4 ports is output from RXCK1 pin. When tied low, RXCK1-4 pins output byte clocks of corresponding port.
DLYSEL	146	I	CMOS	When tied low, RXDIP/M1-4 is sampled at rising edge of RXCIP/M1-4. When tied high, RXDIP/M1-4 is sampled at falling edge of RXCIP/M1-4. In both cases, RCKSEL should be tied low for RXDIP/M1-4 to be sampled by RXCIP/M1-4.
HIZEN	147	I	CMOS	This input selects following mode: 1: All the output pins including bi-directional pins are set to HI-Z state. 0: Normal Operation.

Table 2-3 UTOPIA Level-2 I/F (53 Pin)

Pin Name	Pin No.	I/O	Type	Description
TXDAC[15:0]	62 - 65, 68 - 71, 73 - 76, 79 - 82	I	TTL	The transmit cell data bus.
TXSOC	85	I	TTL	The transmit start of cell indication is asserted when TXDAC contains the first byte of cell data.
-TXENB	57	I	TTL	The active low cell transfer enable signal is activated when TXDAC contains valid cell data.
TXCAV	59	TO	TTL	The transmit cell available is asserted high on pooling when QPLC2 can receive a complete cell data from ATM layer.
TXCLKC	56	I	TTL	The operation clock for the transmit cell interface.
TXPTY	84	I	TTL	The parity bit for TXDAC. Both odd parity and even parity are selectable.
TXADD[4:0]	86, 88, 89, 92, 93	I	TTL	TX Phy port address.
RXDAC[15:0]	15, 17, 18, 21, 22, 24, 25, 28, 29, 32, 33, 35, 36, 39, 40, 42	TO	TTL	The receive cell data bus.
RXSOC	44	TO	TTL	The receive start of cell indication is asserted high when RXDAC contains the first byte of cell data.

Table 2-3 UTOPIA Level-2 I/F (53 Pin) (continued)

Pin Name	Pin No.	I/O	Type	Description
-RXENB	11	I	TTL	The active low receive cell transfer enable signal is asserted low when ATM layer device will sample cell data in the next cycle.
RXCAV	14	TO	TTL	The receive cell available is asserted high when QPLC is ready to transfer a complete cell data to ATM layer.
RXCLKC	9	I	TTL	The operation clock for the receive cell interface.
RXPTY	43	TO	TTL	The parity bit for RXDAC. Both odd parity and even parity are selectable.
RXADD[4:0]	49 - 47 52, 51	I	TTL	RX Phy port address.
TRIEN	53	I	CMOS	Tristate Enable. When this input is tied high, TXCAV, RXDAC[15:0], RXSOC, RXCAV and RXPTY operate as tri-state output. When tied low, these signal pins are always in drive mode.

Table 2-4 CPU I/F (24 Pin)

Pin Name	Pin No.	I/O	Type	Description
A[7:0]	110 - 113, 116 - 119	I	TTL	Address Bus.
D[7:0]	99 - 102, 105 - 108	Bidirect	TTL	Data Bus.
ALE	122	I	TTL	Address Latch Enable.
-CE	123	I	TTL	Active Low Chip Select.
-RD	124	I	TTL	Active Low Read Command.
-WR	125	I	TTL	Active Low Write Command.
-READY	127	O	TTL	Active Low Ready Signal.
-RESET	97	I	TTL	Active Low Hardware Reset.
-INT	128	O	TTL	Active Low Interrupt Signal.
CLK	95	I	TTL	CPU I/F Clock. Should be connected with the same clock source as REFCK.

Table 2-5 Monitor Output (9 Pin)

Pin Name	Pin No.	I/O	Type	Description
RXCK1	136	O	CMOS	When BCKM is tied low, byte clock of port 1 is output. When BCKM is tied high, one of the byte clocks of port 1-4 is output. In the latter case, just one byte clock should be enabled by setting RXCKE bit register TMODE (address: 0DH/4DH/8DH/CDH).
RXCK2	137	O	CMOS	When BCKM is tied low, byte clock of port 2 is output. When BCKM is tied high, RXCK2 pin is disabled.
RXCK3	138	O	CMOS	When BCKM is tied low, byte clock of port 3 is output. When BCKM is tied high, RXCK3 pin is disabled.

Table 2-5 Monitor Output (9 Pin) (continued)

Pin Name	Pin No.	I/O	Type	Description
RXCK4	139	O	CMOS	When BCKM is tied low, byte clock of port 4 is output. When BCKM is tied high, RXCK4 pin is disabled.
TXCK	140	O	CMOS	Transmit byte clock (19.44MHz) is output. When TCKSEL is tied high, transmit byte clock is derived from TX PLL output. When TXCSEL is tied low, transmit byte clock is derived from TXCIP/M.
RXREF1	131	O	TTL	8KHz/4KHz frame clock of port 1. It's set for one byte clock cycle at 2430 clock interval (STS-3/STM-1) or 810 clock interval (STS-1, STS-1/2).
RXREF2	132	O	TTL	8KHz/4KHz frame clock of port 2. It's set for one byte clock cycle at 2430 clock interval (STS-3/STM-1) or 810 clock interval (STS-1, STS-1/2).
RXREF3	133	O	TTL	8KHz/4KHz frame clock of port 3. It's set for one byte clock cycle at 2430 clock interval (STS-3/STM-1) or 810 clock interval (STS-1, STS-1/2).
RXREF4	134	O	TTL	8KHz/4KHz frame clock of port 4. It's set for one byte clock cycle at 2430 clock interval (STS-3/STM-1) or 810 clock interval (STS-1, STS-1/2).

Table 2-6 VDD/GND (72 Pin)

Pin Name	Pin No.	I/O	Type	Description
DVDD	13, 20, 27, 30, 38, 46, 54, 60, 67, 78, 87, 90, 94, 98, 104, 114, 120, 126, 130, 142, 150, 155	-	-	For internal logic and CMOS input and output.
DVDD	4, 8, 184, 188, 194, 198, 210, 214, 219, 223, 229, 233, 237, 240	-	-	For PECL input and output.

Table 2-6 VDD/GND (72 Pin) (continued)

Pin Name	Pin No.	I/O	Type	Description
DVSS	10, 12, 16, 19, 23, 26, 31, 34, 37, 41, 45, 50, 55, 58, 61, 66, 72, 77, 83, 91, 96, 103, 109, 115, 121, 129, 135, 141, 144, 151, 156	–	–	For internal logic and CMOS input and output.
DVSS	181, 185, 191, 195, 201, 204, 207, 204, 207, 211, 215, 218, 222, 226, 232, 236	–	–	For PECL input and output.
AVDDR	160, 164, 168, 172	–	–	The power pin for RXPLL's.
AVSSR	163, 167, 171, 175	–	–	The ground pin for RXPLL's.
AVDDT	176	–	–	The power pin for TXPLL's.
AVSST	179	–	–	The ground pin for TXPLL's.
TVSS	159, 180	–	–	Guard Pwell bias. These input should be tied to quiet ground.

QPLC Pin Layout

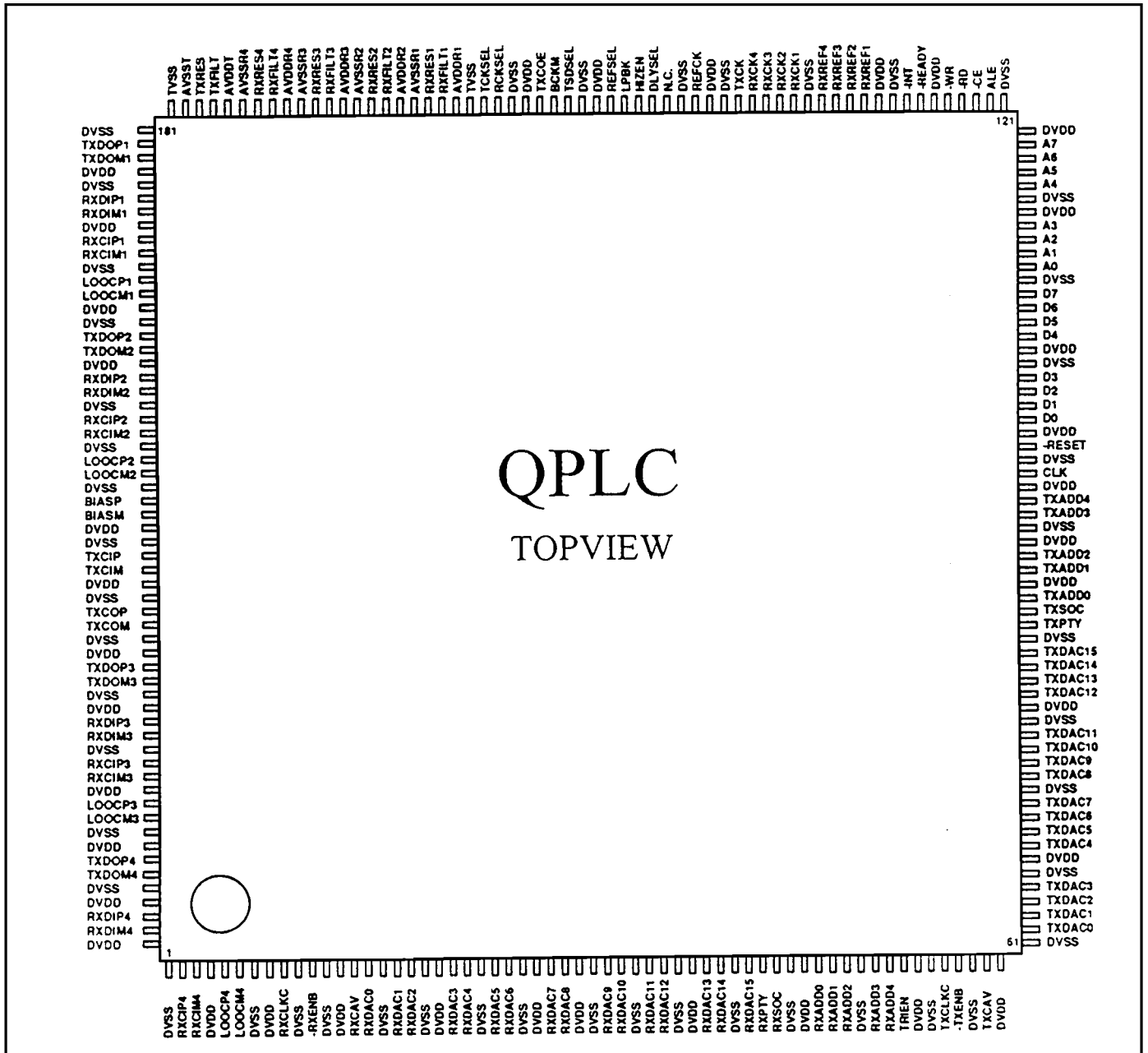


Figure 2-2 QPLC Pin Assignment

Pin Assignments

Table 2-7 QPLC Pin Assignments

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	DVSS	44	RXSOC	87	DVDD
2	RXCIP4	45	DVSS	88	TX9DD1
3	RXCIM4	46	DVDD	89	TX9DD2
4	DVDD	47	RXADD0	90	DVDD
5	LOOCP4	48	RXADD1	91	DVSS
6	LOOCM4	49	RX9DD2	92	TX9DD3
7	DVSS	50	DVSS	93	TXADD4
8	DVDD	51	RXADD3	94	DVDD
9	RXCLKC	52	RXADD4	95	CLK
10	DVSS	53	TRIEN	96	DVSS
11	-RXENB	54	DVDD	97	-RESET
12	DVSS	55	DVSS	98	DVDD
13	DVDD	56	TXCLKC	99	D0
14	RXCAV	57	-TXENB	100	D1
15	RXDACO	58	DVSS	101	D2
16	DVSS	59	TXCAV	102	D3
17	RXDAC1	60	DVDD	103	DVSS
18	RXDAC2	61	DVSS	104	DVDD
19	DVSS	62	TXDAC0	105	D4
20	DVDD	63	TXDAC1	106	D5
21	RXDAC3	64	TXDAC2	107	D6
22	RXDAC4	65	TXDAC3	108	D7
23	DVSS	66	DVSS	109	DVSS
24	RXDAC5	67	DVDD	110	A0
25	RXDAC6	68	TXDAC4	111	A1
26	DVSS	69	TXDAC5	112	A2
27	DVDD	70	TXDAC6	113	A3
28	RXDAC7	71	TXDAC7	114	DVDD
29	RXDAC8	72	DVSS	115	DVSS
30	DVDD	73	TXDAC8	116	A4
31	DVSS	74	TXDAC9	117	A5
32	RXDAC9	75	TXDAC10	118	A6
33	RXDAC10	76	TXDAC11	119	A7
34	DVSS	77	DVSS	120	DVDD
35	RXDAC11	78	DVDD	121	DVSS
36	RXDAC12	79	TXDAC12	122	ALE
37	DVSS	80	TXDAC13	123	-CE
38	DVDD	81	TXDAC14	124	-RD
39	RXDAC13	82	TXDAC15	125	-WR
40	RXDAC14	83	DVSS	126	DVDD
41	DVSS	84	TXPTY	127	-READY
42	RXDAC15	85	TXSOC	128	-INT
43	RXPTY	86	TXADD0	129	DVSS

Table 2-8 QPLC Pin Assignments (continued)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
130	DVDD	167	AVSSR2	204	DVSS
131	RXREF1	168	AVDDR3	205	LOOCP2
132	RXREF2	169	RXFILT3	206	LOOCM2
133	RXREF3	170	RXRES3	207	DVSS
134	RXREF4	171	AVSSR3	208	BIASP
135	DVSS	172	AVDDR4	209	BIASM
136	RXCK1	173	RXFILT4	210	DVDD
137	RXCK2	174	RXRES4	211	DVSS
138	RXCK3	175	AVSSR4	212	TXCIPI
139	RXCK4	176	AVDDT	213	TXCIM
140	TXCK	177	TXFILT	214	DVDD
141	DVSS	178	TXRES	215	DVSS
142	DVDD	179	AVSST	216	TXCOP
143	REFCK	180	TVSS	217	TXCOM
144	DVSS	181	DVSS	218	DVSS
145	N.C.	182	TXDOP1	219	DVDD
146	DLYSEL	183	TXDOM1	220	TXDOP3
147	HIZEN	184	DVDD	221	TXDOM3
148	LPBK	185	DVSS	222	DVSS
149	REFSEL	186	RXDIP1	223	DVDD
150	DVDD	187	RXDIM1	224	RXDIP3
151	DVSS	188	DVDD	225	RXDIM3
152	TSDSEL	189	RXCIP1	226	DVSS
153	BCKM	190	RXCIM1	227	RXCIP3
154	TXCOE	191	DVSS	228	RXCIM3
155	DVDD	192	LOOCP1	229	DVDD
156	DVSS	193	LOOCM1	230	LOOCP3
157	RCKSEL	194	DVDD	231	LOOCM3
158	TCKSEL	195	DVSS	232	DVSS
159	TVSS	196	TXDOP2	233	DVDD
160	AVDDR1	197	TXDOM2	234	TXDOP4
161	RXFILT1	198	DVDD	235	TXDOM4
162	RXRES1	199	RXDIP2	236	DVSS
163	AVSSR1	200	RXDIM2	237	DVDD
164	AVDDR2	201	DVSS	238	RXDIP4
165	RXFILT2	202	RXCIP2	239	RXDIM4
166	RXRES2	203	RXCIM2	240	DVDD

VDD	13, 20, 27, 30, 38, 46, 54, 60, 67, 78, 87, 90, 94, 98, 104, 114, 120, 126, 130, 142, 150, 155	(22 pin for Digital)			
VDD	4, 8, 184, 188, 194, 198, 204, 210, 214, 219, 223, 229, 233, 237, 240	(14 pin for PECL)			
VSS	10, 12, 16, 19, 23, 26, 31, 34, 37, 41, 45, 50, 55, 58, 61, 66, 72, 77, 83, 91, 96, 103, 109, 115, 121, 129, 135, 141, 144, 151, 156	(31 pin for Digital)			
VSS	1, 7, 181, 185, 191, 195, 201, 204, 207, 211, 215, 218, 222, 226, 232, 236	(16 pin for PECL)			
AVDDR	160, 164, 168, 172	AVDDT	176	TVSS	159, 180
AVSSR	163, 167, 171, 175	AVSST	179	Total 95 pin for VDD GND	

Line Interface

Receive Line Interface

RXCIP/M1-4

The bit serial receive clock input, RXCIP/M1-4 is used when the on-chip clock recovery is disabled. The frequency should be 155.52MHz for STS-3, 51.84MHz for STS-1 and 25.92MHz for STS-1/2. When the on-chip clock recovery is enabled, RXCIP/M1-4 is not used. This selection is done with RCKSEL.

RXDIP/M1-4

The receive differential serial data input is sampled on the rising edge of RXCIP/M when the bit serial receive clock input, RXCIP/M1-4 is used. Optionally, RXCIP/M1-4 can be sampled on the falling edge of RXXCIP/M1-4.

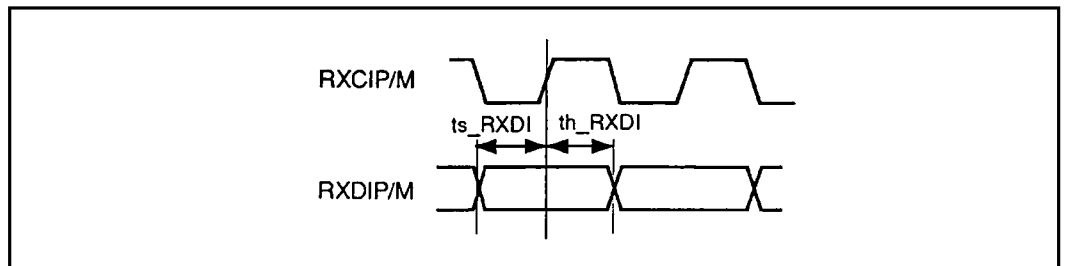


Figure 2-3 Receive Interface Timing

Transmit Line Interface

TXCIP/M

The differential transmit clock input is used when the on-chip transmit clock synthesis is disabled. The frequency should be 155.52MHz for STS-3, 51.84MHz for STS-1 and 25.92MHz for STS-1/2. When the on-chip transmit clock synthesis is enabled or looptiming mode is selected, TXCIP/M is not used.

TXDOP/M1-4

The transmit differential serial data output is updated on the falling edge of TXCIP/M.

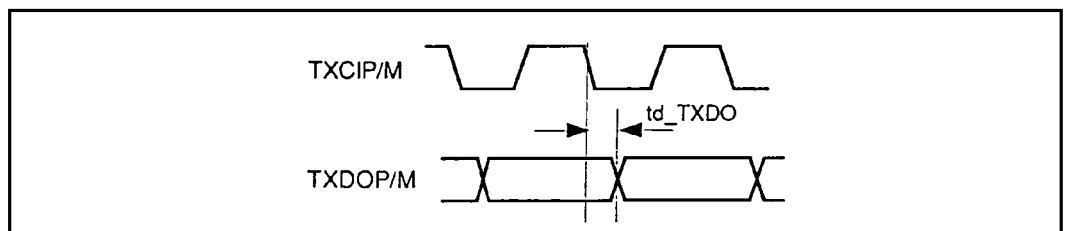


Figure 2-4 Transmit Interface Timing

Cell Interface

The QPLC supports UTOPIA-Level2 Multi-PHY, 16-bit mode only. 8-bit operation is not supported in current version of QPLC.

Transmit Cell Interface

The transmit cell interface operates basically in cell mode instead of byte mode, that is, the QPLC asserts TXCAV when one of four ports is polled and it can receive a complete cell into the transmit cell FIFO. But the ATM layer can halt ongoing cell transmission anytime by deasserting -TXENB.

TXCLKC

Transmit cell interface clock provided by the ATM layer.

TXCAV

Active high, cell available signal asserted by the QPLC to indicate it can receive a complete cell. When one of four port in QPLC is polled, QPLC drives TXCAV high or low in the following cycle, depending on the condition of the transmit cell FIFO of the port. When the FIFO can receive a cell, TXCAV is driven high, otherwise TXCAV is driven low. TXCAV is always driven by QPLC when TRIEN is tied low.

-TXENB

-TXENB indicates that TXDAC[15:0] contains valid data when asserted low. It is also used to select a port to send cell data. For port selection, -TXENB is kept high and at the same time, TXADD[4:0] indicates which port should be selected. In the following cycle, -TXENB is asserted and TXDAC[15:0] outputs valid cell data.

TXSOC

Active high, start of cell indication asserted by the ATM layer.

TXADD[4:0]

Polling address driven by the ATM layer.

TXDAC[15:0]

Transmit cell data bus driven by the ATM layer.

TXPTY

The parity bit for TXDAC[15:0]. Both odd parity and even parity are selectable. When a parity error is detected in a cell received by the QPLC, it is reported to the host CPU and the cell is not discarded.

Figure 2-5 shows polling at transmit interface. The polling takes two steps. For instance, at clock edge #2, ATM layer indicates that port “N” is to be polled. Then at clock edge #3, ATM layer does not change the level of -TXENB and QPLC drives or not drive TXCAV depending on the condition in QPLC. The QPLC drives TXCAV high if port “N” exists in QPLC and the port is ready to receive a cell from the ATM layer. It drives TXCAV low if port “N” exists in QPLC and the port is not ready to receive a cell from the ATM layer. It does not drive TXCAV at clock edge #3 if port address “N” does not match any one of port address in QPLC. The port address is stored in the CIADR register of each port. the ATM layer should not change the level of -TXENB from high to low during polling phase because such a move is considered by QPLC as “selection” and QPLC starts to receive cell. Care should be taken that when ATM layer transmits cell to port N, it should not poll the port N. Such polling behavior is not assumed.

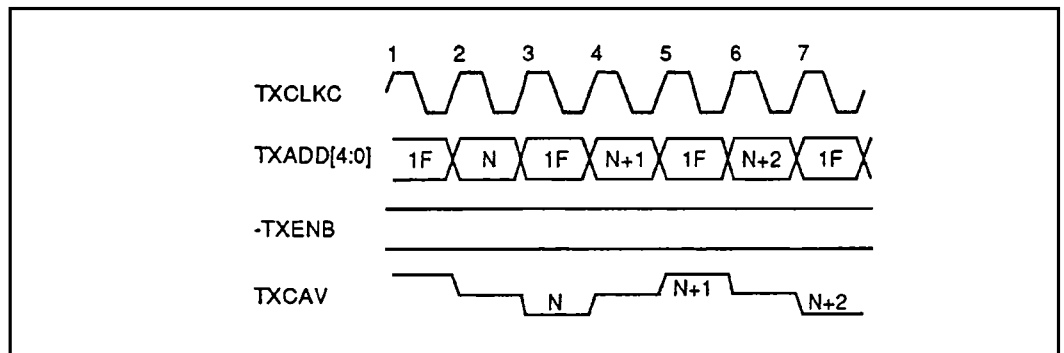


Figure 2-5 Polling at Transmit Interface

Figure 2-6 shows selection at transmit interface. At clock edge #4 the ATM layer indicates the port address to be selected on TXADD[4:0] and at clock edge #5 asserts -TXENB to indicate that selection is being done. At clock edge #5, the ATM layer starts cell transmission. This figure shows a case of the minimum interval between adjacent cell transmission.

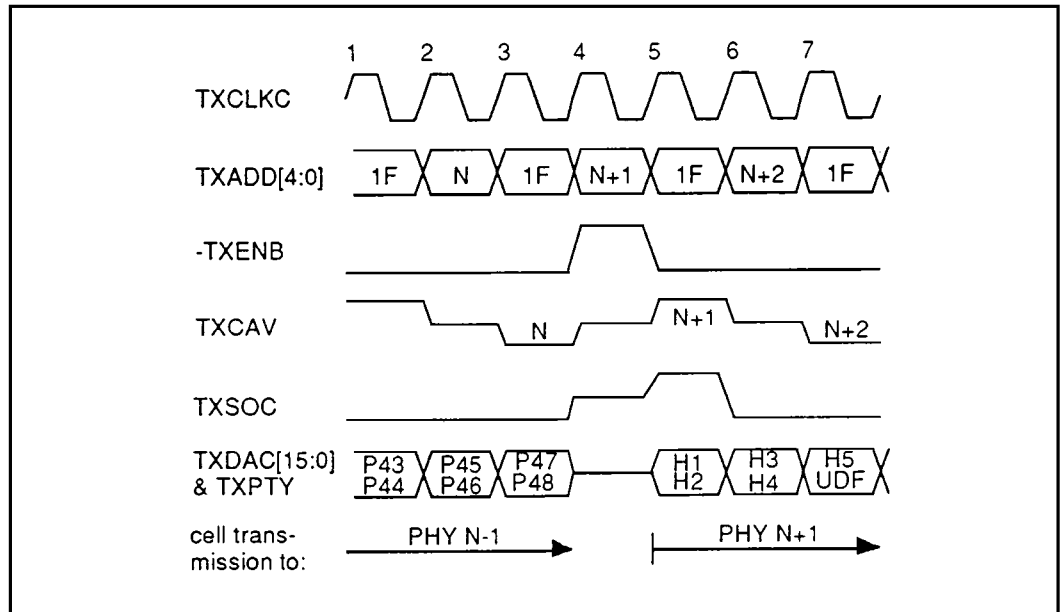


Figure 2-6 Selection at Transmit Interface

Figure 2-7 shows a case where polling is done before restart of cell transmission. During polling, the ATM layer leaves TXSOC, TXPTY and TXADD[15:0] in Hi-Z state.

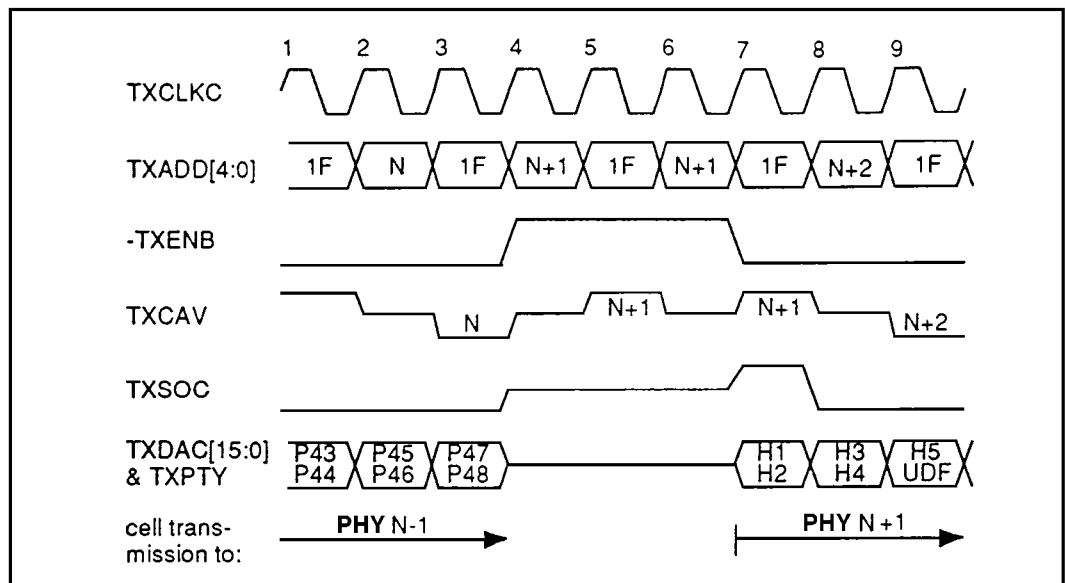


Figure 2-7 End and Restart of Cell Transmission at Transmit Interface

Figure 2-8 shows a case where cell transmission is paused halfway. To restart the cell transmission the ATM layer selects port M explicitly at clock edge #7.

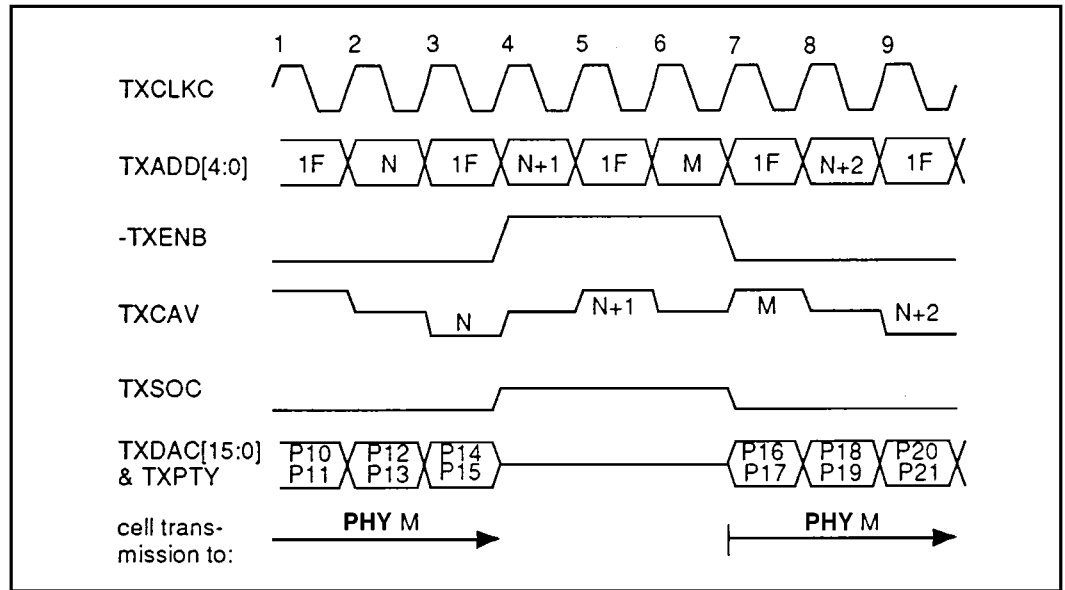


Figure 2-8 Cell Transmission to Phy Paused for Three Cycles

Receive Cell Interface

The receive cell interface operates basically in cell mode instead of byte mode, that is, the QPLC starts cell transmission when it has a complete cell in the receive cell FIFO. But the ATM layer can halt the cell transmission by deasserting -RXENB.

RXCLKC

Receive cell interface operation clock.

RXCAV

Active high, cell available signal asserted by the QPLC to indicate it can transmission a complete cell. When one of four ports in QPLC is polled, QPLC drives RXCAV high or low in the following cycle, depending on the condition of the receive cell FIFO of the port. When the FIFO contains a complete cell to transmission, RXCAV is driven high, otherwise RXCAV is driven low. RXCAV is always driven by QPLC when TRIEN is tied low.

-RXENB

-RXENB indicates that RXDAC[15:0] should contain valid data in the following cycle when asserted low. It is also used to select a port to transmission cell data. For port selection, -RXENB is deasserted and at the same time, RXADD[4:0] indicates which port is selected. In the following cycle, -RXENB is asserted and RXDAC[15:0] is sampled from the following cycle.

RXSOC

Active high, start of cell signal asserted by the QPLC when the first byte of the cell appears on RXDAC[15:0].

RXADD[4:0]

Polling address driven by the ATM layer.

RXDAC[15:0]

Receive cell data bus is driven by the PLC. RXDAC[15:0] is tri-state type. When TRIEN is set low, RXDAC is always driven by the QPLC. When TRIEN is set high, RXDAC[15:0] is driven by the QPLC only in cycles following those with -RXENB asserted.

RXPTY

The parity bit for RXDAC[15:0]. Both odd parity and even parity are selectable. When TRIEN is set low, RXPTY is always driven by the QPLC. When TRIEN is set high, RXPTY is driven by the QPLC only in cycles following those with -RXENB asserted.

Figure 2-9 shows polling at receive interface. The polling takes two steps. For instance, at clock edge #2, ATM layer indicates that port “N” is to be polled. Then at clock edge #3, ATM layer does not change the level of -RXENB and QPLC drives or does not drive RXCAV depending on the condition in QPLC. The QPLC drives RXCAV high if port “N” exists in QPLC and the port is ready to transmit a cell to the ATM layer. It drives RXCAV low if port “N” exists in QPLC and the port is not ready to transmit a cell to the ATM layer. It does not drive RXCAV at clock edge #3 if port address “N” does not match any one of port address in QPLC. The port address is stored in CIADR register of each port. The ATM layer should not change the level of -RXENB from high to low during polling phase because such a move is considered by QPLC as “selection” and QPLC starts to transmit cell. Care should be taken when the ATM layer receives a cell from port N, it should not poll the port N. Such polling behavior is not assumed.

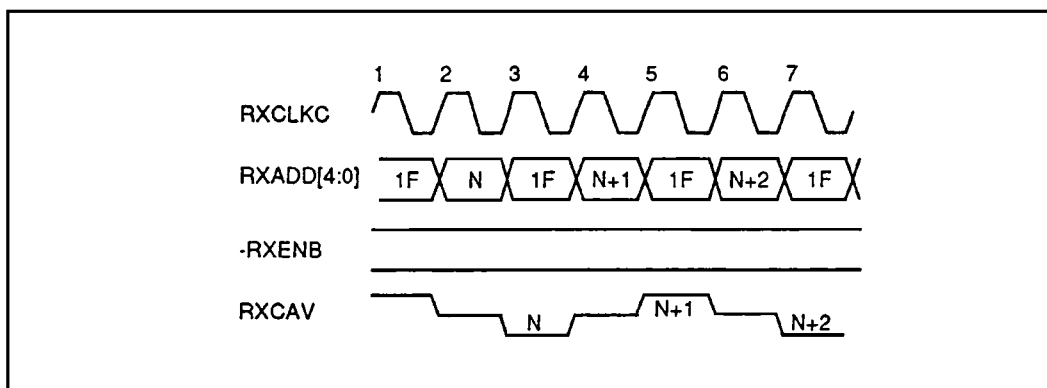


Figure 2-9 Polling at Receive Interface

Figure 2-10 shows selection at receive interface. At clock edge #3 the ATM layer indicates the port address to be selected on TXADD[4:0] and at clock edge #4 asserts -RXENB to indicate that selection is being done. At clock edge #5, QPLC starts cell transmission to the ATM layer. This figure shows a case of the minimum interval between adjacent cell transmission of different port.

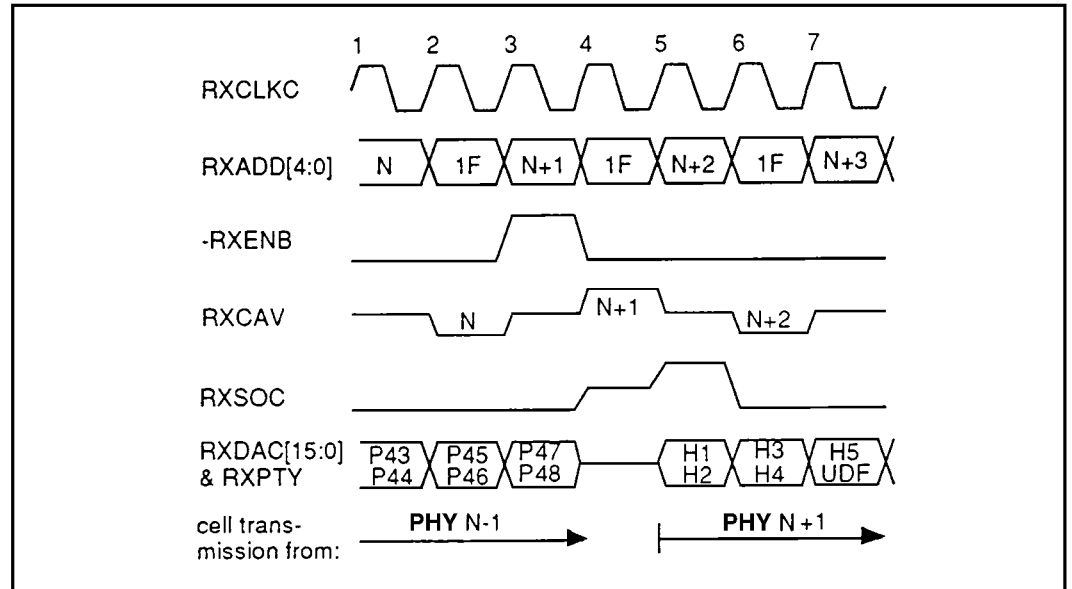


Figure 2-10 Selection at Receive Interface

Figure 2-11 shows a case where polling is done before restart of cell transmission. At clock edge #4, the ATM layer finds no port other than port N-1 is ready to transmit a cell to the ATM layer and let -RXENB asserted to see if port N-1 is ready to transmit a cell. At clock edge #5, the ATM layer finds that port N-1 has no more cell because QPLC leaves RXSOC low. Then the ATM layer deasserts -RXENB to indicate that cell transmission is over. During the cycle of clock edge #5, QPLC continues driving RXSOC, RXPTY and RXDAC[15:0] because -RXENB was asserted during the cycle of clock edge #4. Polling continues during such transaction. At clock edge #8, the ATM layer find that port N+2 is ready to transmit a cell. Then port N+2 is selected at clock edge #9. Port N+2 starts cell transmission at clock edge #10.

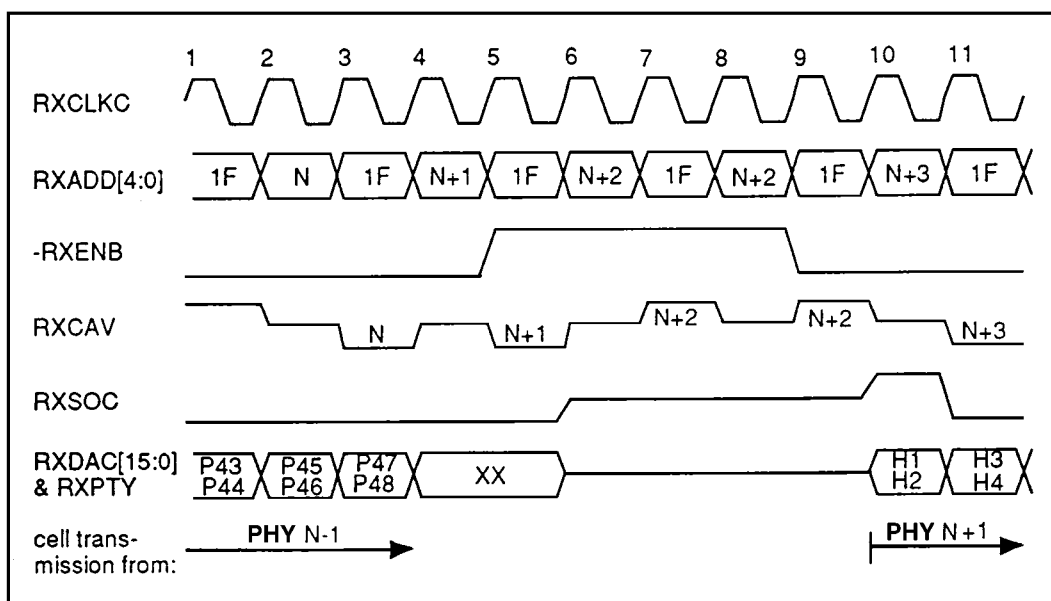


Figure 2-11 End and Restart of Cell Transmission at Receive Interface

Figure 2-12 shows a case of back to back cell transmission. At clock edge #5, the ATM layer leaves -RXENB asserted because no other port than PHY N is ready to transmit a cell. At clock edge #6, port N finds that it is invited to transmit one more cell and the port happens to have a cell to transmit, then it starts to transmit a cell.

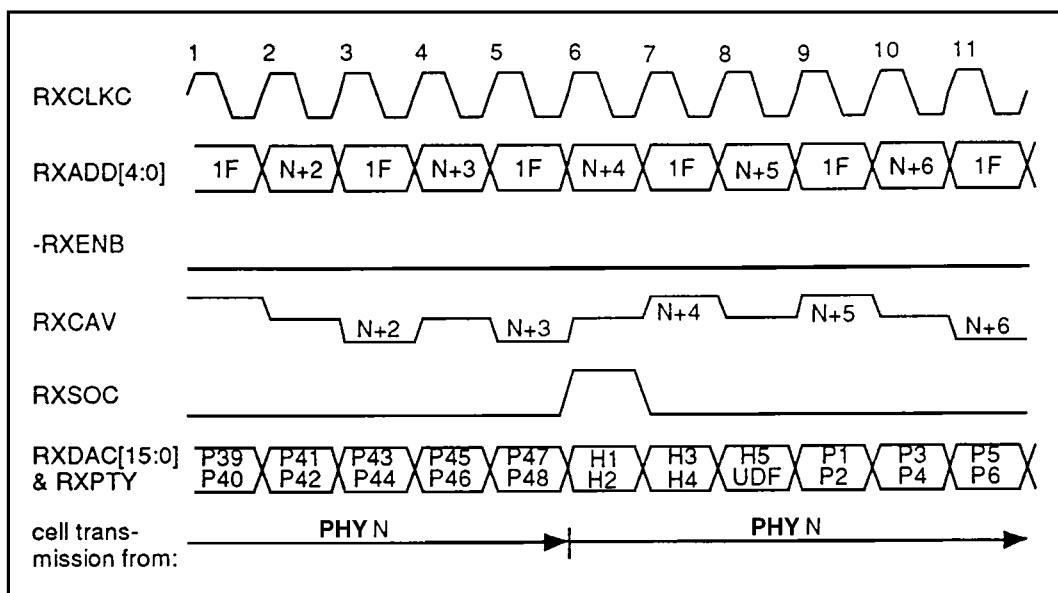


Figure 2-12 Two Subsequent Cells from Same Phy

Figure 2-13 shows the ATM layer stops cell transmission halfway by deasserting -RXENB for three cycles. The ATM layer should select the port (in this case port "M") again before restarting cell transmission. The ATM layer can continue polling when it suspends cell transmission.

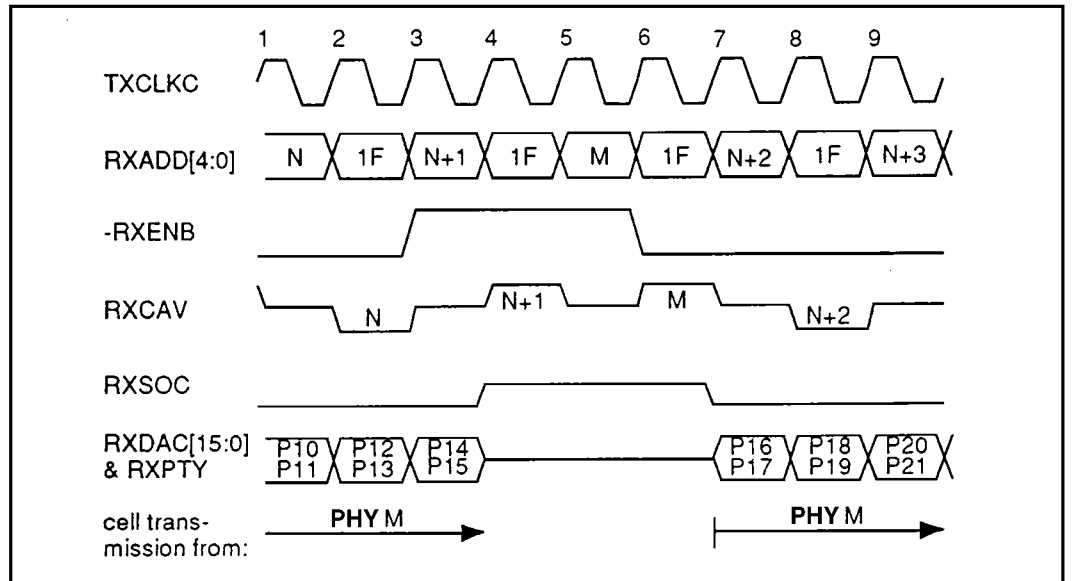


Figure 2-13 Cell Transmission from Phy Paused for Three Cycles

CPU Interface

The host CPU can read/write registers and memories in QPLC by the procedures described below. The registers can be accessed directly while the internal memories should be accessed via MEMAL/H and MEMD registers.

Read Access

The CPU puts the read address on address bus A[7:0] and asserts ALE. The valid address on A[7:0] must have setup time (ts_A) and hold time (th_A) to the falling edge of ALE. The data bus D[7:0] is driven by QPLC when $(-CE + -RD)$ is low. The data access time from $(-CE + -RD)$ is defined as td_RD . $-READY$ goes high when $-CE$ is asserted and goes low when the valid data appears on D[7:0].

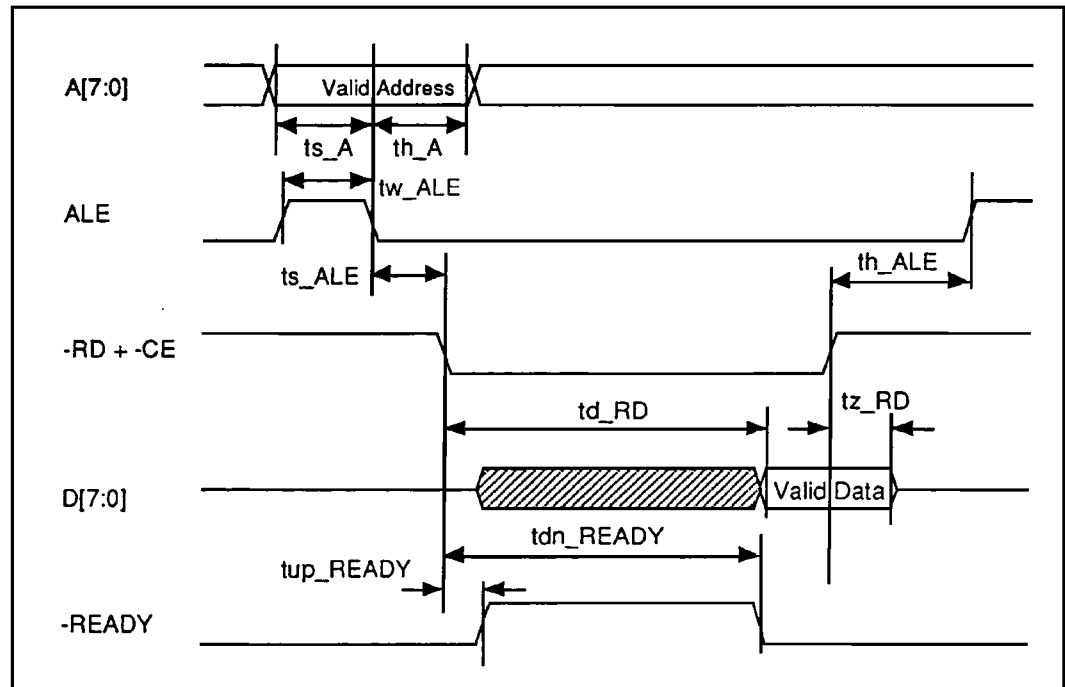


Figure 2-14 Host CPU Read Access Timing

Write Access

The CPU puts the write address on the address bus A[7:0] and asserts ALE. The address on A[7:0] must have setup time (t_{s_A}) and hold time (t_{h_A}) to the falling edge of ALE. The valid write data must have setup time t_{s_WD} to the falling edge of $(-CE + -WR)$ and hold time t_{h_WD} from the rising edge of $(-CE + -WR)$. $-READY$ goes high when $-CS$ is asserted. When the write access is finished in the PLC, $-READY$ goes low. The pulse width of $(-CE + -WR)$ must have minimum pulse width t_{w_CEWR} to ensure successful write access.

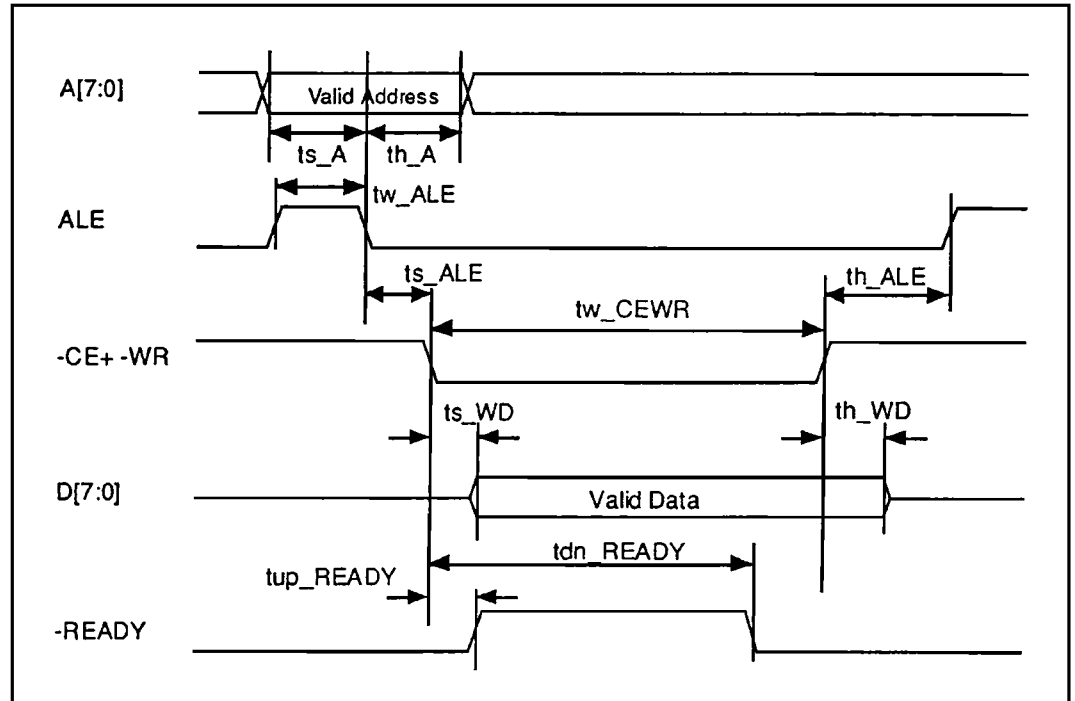


Figure 2-15 Host CPU Write Access Timing

Register Map

The following registers can be accessed from the host CPU.

Table 3-1 Common Configuration Registers

Address	Name	Type	Function
00H	CONT	R/W	Common Control Register
01H	FRMS	R/W	Frame Management Register
02H	CMS1	R/W	Cell Management Register 1
03H	CMS2	R/W	Cell Management Register 2
04H	J1POSH	R/W	Position of J1 Byte in TX Frame (Horizontal)
05H	J1POSV	R/W	Position of J1 Byte in TX Frame (Vertical)
06H	TSMOD	R/W	Test Mode Register

Table 3-2 Common Interrupt Register

Address	Name	Type	Function
07H	INTREG	R	Indicates the interrupting port

Table 3-3 Port 1 Configuration Registers

Address	Name	Type	Function
08H	PCONT	R/W	Reset/Stop of Port 1
09H	TC	R/W	TC Frame Selection
0AH	LOOP	R/W	Loop Control
0BH	TXALM1	R/W	Alarm Signal Control 1
0CH	TXALM2	R/W	Alarm Signal Control 2
0DH	TMODE	R/W	Test Mode Register 1
0EH	TSGEN	R/W	Test Mode Register 2
0FH	GFC	R/W	GFC Control

Table 3-4 Port 2 Configuration Registers

Address	Name	Type	Function
48H	PCONT	R/W	Reset/Stop of Port 2
49H	TC	R/W	TC Frame Selection
4AH	LOOP	R/W	Loop Control
4BH	TXALM1	R/W	Alarm Signal Control 1
4CH	TXALM2	R/W	Alarm Signal Control 2
4DH	TMODE	R/W	Test Mode Register 1
4EH	TSGEN	R/W	Test Mode Register 2
4FH	GFC	R/W	GFC Control

Table 3-5 Port 3 Configuration Registers

Address	Name	Type	Function
88H	PCONT	R/W	Reset/Stop of Port 3
89H	TC	R/W	TC Frame Selection
8AH	LOOP	R/W	Loop Control
8BH	TXALM1	R/W	Alarm Signal Control 1
8CH	TXALM2	R/W	Alarm Signal Control 2
8DH	TMODE	R/W	Test Mode Register 1
8EH	TSGEN	R/W	Test Mode Register 2
8FH	GFC	R/W	GFC Control

Table 3-6 Port 4 Configuration Registers

Address	Name	Type	Function
C8H	PCONT	R/W	Reset/Stop of Port 4
C9H	TC	R/W	TC Frame Selection
CAH	LOOP	R/W	Loop Control
CBH	TXALM1	R/W	Alarm Signal Control 1
CCH	TXALM2	R/W	Alarm Signal Control 2
CDH	TMODE	R/W	Test Mode Register 1
CEH	TSGEN	R/W	Test Mode Register 2
CFH	GFC	R/W	GFC Control

Table 3-7 Port 1 Status Registers

Address	Name	Type	Function
10H	INTSEL1	R/W	Interrupt Control Register 1
11H	INTSEL2	R/W	Interrupt Control Register 2
12H	–	–	rsvd
15H	INTIND1	R	Interrupt Status Register 1
16H	INTIND2	R	Interrupt Status Register 2
17H	–	–	rsvd
1AH	STATUS1	R	Status Register 1
1BH	STATUS2	R	Status Register 2
1CH	–	–	rsvd
1EH	RGFC	R	Receive GFC Status
1FH	CIADR	R/W	Port Address

Table 3-8 Port 1 Error Counters

Address	Name	Type	Function
20H	B1ERRL	R	B1-SBIP8 Error Counter [7:0]
21H	B1ERRH	R	B1-SBIP8 Error Counter [15:8]
22H	B2ERRL	R	B2-LBIP24 Error Counter [7:0]
23H	B2ERRM	R	B2-LBIP24 Error Counter [15:8]
24H	B2ERRH	R	B2-LBIP24 Error Counter [19:16]
25H	B3ERRL	R	B3-PBIP8 Error Counter [7:0]
26H	B3ERRH	R	B3-PBIP8 Error Counter [15:8]
27H	LFEBEL	R	R-LFEBE Counter [7:0]
28H	LFEBEM	R	R-LFEBE Counter [15:8]
29H	LFEBEH	R	R-LFEBE Counter [19:16]
2AH	PFEBEL	R	R-PFEBE Counter [7:0]
2BH	PFEBEH	R	R-PFEBE Counter [15:8]
2CH	FCUPD	R/W	Error Counter Update Flag

Table 3-9 Port 1 Cell Counters

Address	Name	Type	Function
30H	COHER	R	Corrected Cell Header Error Counter
31H	UCHER	R	Uncollected Cell Header Error Counter
32H	RXCCL	R	Receive Valid Cell Counter [7:0]
33H	RXCCM	R	Receive Valid Cell Counter [15:8]
34H	RXCCH	R	Receive Valid Cell Counter [19:16]
35H	TXCCL	R	Transmit Valid Cell Counter [7:0]
36H	TXCCM	R	Transmit Valid Cell Counter [15:8]
37H	TXCCH	R	Transmit Valid Cell Counter [19:16]
38H	CCUPD	R/W	Cell Counter Update Flag

Table 3-10 Port 1 Memory Access Registers

Address	Name	Type	Function
3DH	MEMAL	R/W	Address Register [7:0]
3EH	MEMAH	R/W	Address Register [12:8], Write Enable
3FH	MEMD	R/W	Data Register

Table 3-11 Port 2 Status Registers

Address	Name	Type	Function
50H	INTSEL1	R/W	Interrupt Control Register 1
51H	INTSEL2	R/W	Interrupt Control Register 2
52H	–	–	rsvd
55H	INTIND1	R	Interrupt Status Register 1
56H	INTIND2	R	Interrupt Status Register 2
57H	–	–	rsvd
5AH	STATUS1	R	Status Register 1
5BH	STATUS2	R	Status Register 2
5CH	–	–	rsvd
5EH	RGFC	R	Receive GFC Status
5FH	CIADR	R/W	Port Address

Table 3-12 Port 2 Error Counters

Address	Name	Type	Function
60H	B1ERRL	R	B1-SBIP8 Error Counter [7:0]
61H	B1ERRH	R	B1-SBIP8 Error Counter [15:8]
62H	B2ERRL	R	B2-LBIP24 Error Counter [7:0]
63H	B2ERRM	R	B2-LBIP24 Error Counter [15:8]
64H	B2ERRH	R	B2-LBIP24 Error Counter [19:16]
65H	B3ERRL	R	B3-PBIP8 Error Counter [7:0]
66H	B3ERRH	R	B3-PBIP8 Error Counter [15:8]
67H	LFEBEL	R	R-LFEBE Counter [7:0]
68H	LFEBEM	R	R-LFEBE Counter [15:8]
69H	LFEBEH	R	R-LFEBE Counter [19:16]
6AH	PFEBEL	R	R-PFEBE Counter [7:0]
6BH	PFEBEH	R	R-PFEBE Counter [15:8]
6CH	FCUPD	R/W	Error Counter Update Flag

Table 3-13 Port 2 Cell Counters

Address	Name	Type	Function
70H	COHER	R	Corrected Cell Header Error Counter
71H	UCHER	R	Uncollected Cell Header Error Counter
72H	RXCCL	R	Receive Valid Cell Counter [7:0]
73H	RXCCM	R	Receive Valid Cell Counter [15:8]
74H	RXCCH	R	Receive Valid Cell Counter [19:16]
75H	TXCCL	R	Transmit Valid Cell Counter [7:0]
76H	TXCCM	R	Transmit Valid Cell Counter [15:8]
77H	TXCCH	R	Transmit Valid Cell Counter [19:16]
78H	CCUPD	R/W	Cell Counter Update Flag

Table 3-14 Port 2 Memory Access Registers

Address	Name	Type	Function
7DH	MEMAL	R/W	Address Register [7:0]
7EH	MEMAH	R/W	Address Register [12:8], Write Enable
7FH	MEMD	R/W	Data Register

Table 3-15 Port 3 Status Registers

Address	Name	Type	Function
90H	INTSEL1	R/W	Interrupt Control Register 1
91H	INTSEL2	R/W	Interrupt Control Register 2
92H	–	–	rsvd
95H	INTIND1	R	Interrupt Status Register 1
96H	INTIND2	R	Interrupt Status Register 2
97H	–	–	rsvd
9AH	STATUS1	R	Status Register 1
9BH	STATUS2	R	Status Register 2
9CH	–	–	rsvd
9EH	RGFC	R	Receive GFC Status
9FH	CIADR	R/W	Port Address

Table 3-16 Port 3 Error Counters

Address	Name	Type	Function
A0H	B1ERRL	R	B1-SBIP8 Error Counter [7:0]
A1H	B1ERRH	R	B1-SBIP8 Error Counter [15:8]
A2H	B2ERRL	R	B2-LBIP24 Error Counter [7:0]
A3H	B2ERRM	R	B2-LBIP24 Error Counter [15:8]
A4H	B2ERRH	R	B2-LBIP24 Error Counter [19:16]
A5H	B3ERRL	R	B3-PBIP8 Error Counter [7:0]
A6H	B3ERRH	R	B3-PBIP8 Error Counter [15:8]
A7H	LFEBEL	R	R-LFEBE Counter [7:0]
A8H	LFEBEM	R	R-LFEBE Counter [15:8]
A9H	LFEBEH	R	R-LFEBE Counter [19:16]
AAH	PFEBEL	R	R-PFEBE Counter [7:0]
ABH	PFEBEH	R	R-PFEBE Counter [15:8]
ACH	FCUPD	R/W	Error Counter Update Flag

Table 3-17 Port 3 Cell Counters

Address	Name	Type	Function
B0H	COHER	R	Corrected Cell Header Error Counter
B1H	UCHER	R	Uncollected Cell Header Error Counter
B2H	RXCCL	R	Receive Valid Cell Counter [7:0]
B3H	RXCCM	R	Receive Valid Cell Counter [15:8]
B4H	RXCCH	R	Receive Valid Cell Counter [19:16]
B5H	TXCCL	R	Transmit Valid Cell Counter [7:0]
B6H	TXCCM	R	Transmit Valid Cell Counter [15:8]
B7H	TXCCH	R	Transmit Valid Cell Counter [19:16]
B8H	CCUPD	R/W	Cell Counter Update Flag

Table 3-18 Port 3 Memory Access Registers

Address	Name	Type	Function
BDH	MEMAL	R/W	Address Register [7:0]
BEH	MEMAH	R/W	Address Register [12:8], Write Enable
BFH	MEMD	R/W	Data Register

Table 3-19 Port 4 Status Registers

Address	Name	Type	Function
D0H	INTSEL1	R/W	Interrupt Control Register 1
D1H	INTSEL2	R/W	Interrupt Control Register 2
D2H	–	–	rsvd
D5H	INTIND1	R	Interrupt Status Register 1
D6H	INTIND2	R	Interrupt Status Register 2
D7H	–	–	rsvd
DAH	STATUS1	R	Status Register 1
DBH	STATUS2	R	Status Register 2
DCH	–	–	rsvd
DEH	RGFC	–	Receive GFC Status
DFH	CIADR	–	Port Address

Table 3-20 Port 4 Error Counters

Address	Name	Type	Function
E0H	B1ERRL	R	B1-SBIP8 Error Counter [7:0]
E1H	B1ERRH	R	B1-SBIP8 Error Counter [15:8]
E2H	B2ERRL	R	B2-LBIP24 Error Counter [7:0]
E3H	B2ERRM	R	B2-LBIP24 Error Counter [15:8]
E4H	B2ERRH	R	B2-LBIP24 Error Counter [19:16]
E5H	B3ERRL	R	B3-PBIP8 Error Counter [7:0]
E6H	B3ERRH	R	B3-PBIP8 Error Counter [15:8]
E7H	LFEBEL	R	R-LFEBE Counter [7:0]
E8H	LFEBEM	R	R-LFEBE Counter [15:8]
E9H	LFEBEH	R	R-LFEBE Counter [19:16]
EAH	PFEBEL	R	R-PFEBE Counter [7:0]
EBH	PFEBEH	R	R-PFEBE Counter [15:8]
ECH	FCUPD	R/W	Error Counter Update Flag

Table 3-21 Port 4 Cell Counters

Address	Name	Type	Function
F0H	COHER	R	Corrected Cell Header Error Counter
F1H	UCHER	R	Uncollected Cell Header Error Counter
F2H	RXCCL	R	Receive Valid Cell Counter [7:0]
F3H	RXCCM	R	Receive Valid Cell Counter [15:8]
F4H	RXCCH	R	Receive Valid Cell Counter [19:16]
F5H	TXCCL	R	Transmit Valid Cell Counter [7:0]
F6H	TXCCM	R	Transmit Valid Cell Counter [15:8]
F7H	TXCCH	R	Transmit Valid Cell Counter [19:16]
F8H	CCUPD	R/W	Cell Counter Update Flag

Table 3-22 Port 4 Memory Access Registers

Address	Name	Type	Function
FDH	MEMAL	R/W	Address Register [7:0]
FEH	MEMAH	R/W	Address Register [12:8], Write Enable
FFH	MEMD	R/W	Data Register

Hereafter, each register is described in detail. A register field table shows:

Bit Number
Field Name
Default Value on Reset

Address: 00H
 Name: CONT
 Type: R/W
 Function: Common Control Register

7	6	5	4	3	2	1	0
MONSEL	HSTOP	TXCKE	AUTOCS	RCT	DWLD	STBY	HRESET
0	0	0	0	0	0	0	0

HRESET

Reset to common configuration registers and common interrupt register. While in reset state, access to internal registers except for CONT register is prohibited.

- 0: Normal operation.
- 1: Following registers are loaded with default values; CONT, FRMS, CMS1, CMS2, J1POSH, J1POSV, INTREG.

STBY

PECL buffer control.

- 0: Normal operation.
- 1: All PECL input and output buffers including BIASP/M are forced into stand-by mode.

DWLD

DWLD is used for production test only.

- 0: Normal operation.
- 1: Download mode operation.

RCT

RCT is used for production test only.

- 0: Cell delineation is enabled after frame synchronization is established.
- 1: Cell delineation is enabled regardless of frame synchronization.

AUTOCS

Receive PLL control.

- 0: Receive PLL recovers clock from receive data or generates x8 clock from REFCK depending on the state of REFSEL.
- 1: Receive PLL usually recovers clock from receive data. When LOOC input is tied high or no signal transition is detected for 80-bit period or recovered clock deviates more than 224 ppm from reference clock, the receive PLL automatically switches reference source from receive data to reference clock, as far as REFSEL is tied low.

TXCKE

TXCKE controls transmit byte clock output TXCK.

- 0: TXCK pin is fixed to zero.
- 1: TXCK pin outputs transmit byte clock.

HSTOP

HSTOP is used for production test only.

- 0: Out of lock detector for transmit PLL is enabled.
- 1: Out of lock detector for transmit PLL is stopped.

MOSEL

MOSEL is used for production test only.

0: RXREF1-4 signal is output at RXREF1-4 pin, respectively.

1: REFSYN1-4 signal is output at RXREF1-4 pin, respectively.

rsvd

These fields are reserved for future use. For normal operation these fields should be set to zero.

Address: 01H
 Name: FRMS
 Type: R/W
 Function: Frame Management

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	rsvd	NODSBF	NOSCBF	NOSTF	rsvd
-	-	-	-	0	0	0	-

NOSTF

The NOSTF bit selects stuff byte mode in STS-1 operation.

0: Columns 30 and 59 are treated as fixed bytes in STS-1 and STS-1/2 operation.

1: Columns 30 and 59 are treated as data bytes in STS-1 and STS-1/2 operation.

NOSCBF

The NOSCBF bit controls the scramble of transmit frame.

0: Enable the scramble of transmit frame.

1: Disable the scramble of transmit frame.

NODSBF

The NODSBF bit controls the descramble of receive frame.

0: Enable the descramble.

1: Disable the descramble.

rsvd

These fields are reserved for future use. For normal operation these fields should be set to zero.

Address: 02H
 Name: CMS1
 Type: R/W
 Function: Cell Management Register 1

7	6	5	4	3	2	1	0
rsvd	TXF2	TXF1	UDF	PARITY	rsvd	rsvd	rsvd
–	0	0	0	0	–	–	–

PARITY

The PARITY bit selects parity mode.

- 0: Odd Parity.
- 1: Even Parity.

UDF

The UDF bit controls HEC insertion in 16-bit cell format.

- 0: UDF1 for HEC.
- 1: UDF2 for HEC.

TXF2/TXF1

The TXF2/TXF1 bits control the transmit FIFO depth.

TXF2	TXF1	FIFO Depth
0	0	4 cell deep
0	1	1 cell deep
1	0	2 cell deep
1	1	3 cell deep

Address: 03H
 Name: CMS2
 Type: R/W
 Function: Cell Management Register 2

7	6	5	4	3	2	1	0
rsvd	NOTC	NOSCBC	NOHEC	NORC	NODSBC	PASS	DROP
0	0	0	0	0	0	0	0

DROP

The DROP bit controls the cell delineation.

0: Normal cell delineation as specified in ITU-T I.432.

1: All received cells with header error are discarded.

PASS

The PASS bit controls the cell delineation.

0: Normal cell delineation as specified in ITU-T I.432.

1: All cells are passed, regardless of header error, toward the ATM layer. The cell delineation state transition is treated as specified in ITU-T I.432.

NODSBC

The NODSBC bit controls descramble of received cell.

0: Enable the payload descramble of received cell.

1: Disable the payload descramble of received cell.

NORC

The NORC bit controls HEC calculation option of received cell.

0: The coset polynomial, $X^6+X^4+X^2+1$, is added (modulo2) in HEC calculation of received cell.

1: No polynomial is added.

NOHEC

The NOHEC bit controls HEC calculation of transmit cell.

0: Enable calculation and insertion of HEC of transmit cell.

1: Disable calculation and insertion of HEC of transmit cell. The HEC field of transmit cell is as received from ATM layer.

NOSCBC

The NOSCBC bit controls payload scramble of transmit cell.

0: Enable the payload scramble of transmit cell.

1: Disable the payload scramble of transmit cell.

NOTC

The NOTC bit controls HEC calculation option of transmit cell.

0: The coset polynomial, $X^6+X^4+X^2+1$ (55H), is added (modulo2) in HEC calculation of transmit cell.

1: No polynomial is added

Address: 04H
 Name: J1POSH
 Type: R/W
 Function: Set the horizontal position of J1 byte in transmit frame

7	6	5	4	3	2	1	0
rsvd	J1H[6:0]						
-	0	0	0	0	0	1	1

Address: 05H
 Name: J1POSV
 Type: R/W
 Function: Set the vertical position of J1 byte of transmit frame

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	rsvd	J1V[3:0]			
-	-	-	-	0	0	1	1

J1POSH and J1POSV registers are intended for production test. In normal operation, these registers should have default value.

J1H[6:0]

When initializing QPLC, set the horizontal position of J1 byte of transmit frame. In STS-3 mode, the base position is left side of frame and count up is every 3 bytes toward right side. The default value, 3 is set on reset.

J1V[3:0]

When initializing QPLC, set the vertical position of J1 byte of transmit frame. In STS-3 mode, the base position is first line of frame and count up is every 1 byte. The default value, 3 is set on reset.

Note: The value of J1POSH and J1POSV must be consistent with the value of H1/H2 byte in transmit overhead memory.

EXAMPLE:

POINTER	J1V	J1H
0	3	3
522	0	3
782	2	89

Address: 06H
 Name: TSMOD
 Type: R
 Function: Indicates the interrupting port

7	6	5	4	3	2	1	0
OOLTST	TSTCK	TXCM	RFHLT	PORT4	LOOCE	CIE	TXCOE
0	0	-	-	0	0	0	0

TXCOE

The TXCOE bit controls the mode of TXCOP/M output.

0: TXCOP/M output is set in drive mode.

1: TXCOP/M output is set in Hi-Z mode.

CIE

The CIE bit controls the mode of RXCIP/M and TXCIP/M input buffer.

0: RXCIP/M and TXCIP/M input buffer is set in operation mode.

1: RXCIP/M and TXCIP/M input buffer is set in stand by mode.

LOOCE

The LOOCE bit controls the mode of input buffers of LOOCP/M1, LOOCP/M2, LOOCP/M3 and LOOCP/M4.

0: LOOCP/M1, LOOCP/M2, LOOCP/M3 and LOOCP/M4 input buffer is set in operation mode.

1: LOOCP/M1, LOOCP/M2, LOOCP/M3 and LOOCP/M4 input buffer is set in stand by mode.

EXTLOS

The EXTLOS bit defines whether LOOC input is included as LOS condition.

0: LOOC has no effect on LOS.

1: When LOOCP/Mn (n=1~4) input is tied low, LOS status bit is set high immediately.

RFHLT

The RFHLT bit is for diagnostics only.

TXCM

The TXCM bit is for diagnostics only.

TSTCK

The TSTCK bit controls the clock of digital part of QPLC. This bit is for diagnostics only.

0: When LPBK input is tied high, REFCK is fed to the digital part of QPLC directly in STS3 mode, divided by 3 in STS1 mode or divided by 6 in STS1/2 mode.

1: REFCK is always fed to the digital part of QPLC directly regardless of TC frame.

OOLTST

The OOLTST bit controls the operation of OOL detector in QPLC. This bit is for diagnostics only.

0: When RCKSEL is tied low, OOL detector is set in stand by mode.

1: Regardless of RCKSEL is tied low, OOL detector is set in operation mode..

TSTCK

These fields are reserved for future use. For normal operation these fields should be set to zero.

Address: 07H
 Name: INTREG
 Type: R
 Function: Indicates the interrupting port

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	rsvd	PORT4	PORT3	PORT2	PORT1
–	–	–	–	0	0	0	0

This register is used to find which port is responsible for the interrupt.

PORT1

Indicates whether Port 1 has active interrupt status or not.

0: Port 1 has no active interrupt status.

1: Port 1 has active interrupt status.

PORT2

Indicates whether Port 2 has active interrupt status or not.

0: Port 2 has no active interrupt status.

1: Port 2 has active interrupt status.

PORT3

Indicates whether Port 3 has active interrupt status or not.

0: Port 3 has no active interrupt status.

1: Port 3 has active interrupt status.

PORT4

Indicates whether Port 4 has active interrupt status or not.

0: Port 4 has no active interrupt status.

1: Port 4 has active interrupt status.

Address: 08H/48H/88H/C8H
 Name: PCONT
 Type: R/W
 Function: Reset/Stop of PLC

7	6	5	4	3	2	1	0
TOMINI	LOOCDE	PLLINI	OOLDE	TXFRES	RXFRES	STOP	RESET
1	0	0	0	0	0	1	1

RESET

Software reset bit. When this bit is set to one, all the registers and counters in each port are initialized. A hardware reset clears the RESET bit. The RESET bit should be set for at least 20 cycles of the slowest clock provided to QPLC. While in reset state, access to internal registers except for this PCONT register is prohibited.

- 0: QPLC is not held in reset.
- 1: QPLC is held in reset.

STOP

Software stop bit. When this bit is set to one, each port of QPLC stops operation, but does not change the state in QPLC. The host CPU can set value to registers and counters for diagnostic or initializing purposes. The default value of the STOP bit on a hardware reset is 1.

- 0: QPLC is not held in stop mode.
- 1: QPLC is held in stop mode.

RXFRES

The RXFRES bit controls the state of the receive FIFOs. Setting this bit does not corrupt ongoing receive cell transfer. That is, after the last byte of cell has been transferred, the receive FIFOs stop operation. The RXFRES bit should be asserted to at least 10.8 s.

- 0: The receive FIFOs operates normally.
- 1: All cells in the receive FIFOs are discarded. The receive FIFOs stop operation.

TXFRES

The TXFRES bit controls the state of the transmit FIFOs. Setting this bit affects ongoing transmit cell transfer. That is, after the last byte of the cell has been transferred, the cell is discarded. The TXFRES bit should be asserted to at least 10.8 s.

- 0: The transmit FIFOs operate normally.
- 1: All cells in the transmit FIFOs are discarded. The transmit FIFOs stop operation.

OOLDE

The OOLDE bit controls the OOL detector.

- 0: The OOL detector output is ignored.
- 1: When the OOL detector output is set high, meaning the recovered clock is out of 244ppm range from REFCK, the clock recovery PLL is set into reference clock mode.

PLLINI

The PLLINI bit controls the mode of the clock recovery PLL.

- 0: No effect on the clock recovery PLL.
- 1: The clock recovery PLL is set into reference clock mode.

LOOCDE

The LOOCDE bit controls internal loss of optical carrier detector which examines receive signal data to determine if it is active or not. When receive data has 80-bit consecutive 1 or 0, the detector produce signal.

- 0: Internal loss of optical carrier detector is disabled.
- 1: Internal loss of optical carrier detector is enabled.

TOMINI

The TOMINI bit controls the transmit processor operation on transmit overhead memory. When some SOH/POH bytes like K1 should be written by external processor, TOMINI bit should be set to one.

- 0: Zero insertion to unused bytes of SOH/POH is enabled. Externally written data to these bytes are overwritten with zero within 125 sec.
- 1: Zero insertion to unused bytes of SOH/POH is enabled. Externally written data to these bytes are left.

Notice: The definition of "unused bytes of SOH/POH"

QPLC inserts other non-zero values to A1, A2, C1, B1, H1, H2, H3, B2, K2, Z2(the third one), B3, C2, G1 and H4 bytes. Other bytes are "unused bytes of SOH/POH".

Address: 09H/49H/89H/C9H
 Name: TC
 Type: R/W
 Function: TC Frame Selection

7	6	5	4	3	2	1	0
SDH	rsvd	rsvd	rsvd	rsvd	rsvd	TC1	TC0
0	-	-	-	-	-	0	0

TC1, TC0

The TC1 and TC0 define the transmission frame.

TC1	TC0	Frame
0	Don't care	STS-3/STM-1
1	0	STS-1
1	1	STS-1/2

SDH

The SDH bit controls QPLC operation in terms of the difference between SONET and SDH.

- 0: QPLC operates in SONET mode.
- 1: QPLC operates in SDH mode.

The difference of operation by QPLC between SONET/SDH is summarized below.

	SONET mode	SDH mode
C1 bytes in transmit frame	01H/02H/03H	01H/AAH/AAH
SS bits of H1 byte in transmit frame	'00'	'10'
L-RDI detection	5 consecutive frames	3 consecutive frames
L-AIS detection	5 consecutive frames	3 consecutive frames
P-RDI detection	5 consecutive frames	3 consecutive frames

Address: 0AH/4AH/8AH/CAH
 Name: LOOP
 Type: R/W
 Function: Loop Mode Select

7	6	5	4	3	2	1	0
LOOP2EN	rsvd	rsvd	LOOPL	LOOPPT	LOOPU	LOOP2	LOOP1
0	-	-	0	0	0	0	0

LOOP1

The LOOP1-bit controls diagnostic loop back mode in LSI side. When this bit is set to one, TXDOP/M is connected to RXDIP/M internally so that the transmit serial data is just returned as the receive serial data.

- 0: Normal operation.
- 1: Enable diagnostic loopback.

LOOP2

The LOOP2-bit controls line loop back mode. When this bit is set to one, RXDIP/M is connected with TXDOP/M internally and the received data is just returned as the transmit data.

- 0: Normal operation.
- 1: Enable line loop back mode.

LOOPU

The LOOPU bit controls UTOPIA loop back mode.

- 0: Normal operation.
- 1: Transmit parallel data output is looped back to receive parallel input.

LOOPPT

When the LOOPPT bit is set to one, the transmit clock of QPLC is synchronized with a clock extracted from received data. (Loop Timing Mode)

- 0: Disable Loop Timing Mode. The transmit clock is synchronized with the reference clock, REFCK.
- 1: Enable Loop Timing Mode.

LOOPL

The LOOPL bit controls (shallow) line loop back mode.

- 0: Normal operation.
- 1: Receive serial input RXDIP/M is looped back to TXDOP/M directly.

LOOP2EN

The LOOP2EN bit controls whether LOOP2 bit of LOOP register is writable from the receive processor in QPLC. This bit is for diagnostics only.

- 0: LOOP2-bit of LOOP register is not writable from the receive processor in QPLC.
- 1: LOOP2-bit of LOOP register is writable from the receive processor in QPLC.

Address: 0BH/4BH/8BH/CBH
 Name: TXALM1
 Type: R/W
 Function: Alarm Signal Control 1

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	PYEL	PAIS	PRDI	LAIS	LRDI
-	-	-	0	1	0	1	0

QPLC can send the following alarm status automatically by setting this field.

LRDI

The LRDI bit controls automatic transmission of Line RDI.

- 0: Disable automatic transmission.
- 1: Enable automatic transmission, when QPLC detects LOS, LOF or LAIS.

LAIS

The LAIS bit controls automatic transmission of Line AIS.

- 0: Disable automatic transmission.
- 1: Enable automatic transmission, when QPLC detects LOS or LOF.

PRDI

The PRDI bit controls automatic transmission of Path RDI. This bit should not be set high when the PYEL bit is set high since alarm signals PRDI and PYEL use the same field of G1 byte.

- 0: Disable automatic transmission.
- 1: Enable automatic transmission, when QPLC detects LOS, LOF, LOP, LOC, LAIS or PAIS.

PAIS

The PAIS bit controls automatic transmission of Path AIS.

- 0: Disable automatic transmission.
- 1: Enable automatic transmission, when QPLC detects LOS, LOF, LOP, LOC or LAIS.

PYEL

The PYEL bit controls automatic transmission of Path YEL. This bit should not be set high when PRDI bit is set high since alarm signals PRDI and PYEL use the same field of G1 byte.

- 0: Disable automatic transmission.
- 1: Enable automatic transmission, when QPLC detects LOS, LOF, LOP, LOC, LAIS or PAIS continues for 5 seconds.

Note: When automatic alarm transmission is used by setting this register, the corresponding bit of TXALM2 register must be set to zero.

Address: 0CH/4CH/8CH/CCH
 Name: TXALM2
 Type: R/W
 Function: Alarm Signal Control 2

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	PYEL	PAIS	PRDI	LAIS	LRDI
–	–	–	0	0	0	0	0

QPLC can be forced to send the following alarm signals by using this field. While each bit is set to one, QPLC continues to send a corresponding alarm signal.

LRDI

The LRDI bit controls forced transmission of Line RDI.

- 0: Stop sending L-RDI.
- 1: Start sending L-RDI.

LAIS

The LAIS bit controls forced transmission of Line AIS.

- 0: Stop sending L-AIS.
- 1: Start sending L-AIS.

PRDI

The PRDI bit controls forced transmission of Path RDI.

- 0: Stop sending P-RDI.
- 1: Start sending P-RDI.

PAIS

The PAIS bit controls forced transmission of Path AIS.

- 0: Stop sending P-AIS.
- 1: Start sending P-AIS.

PYEL

The PYEL bit controls forced transmission of Path YEL.

- 0: Stop sending P-YEL.
- 1: Start sending P-YEL.

Note: When the forced alarm transmission is used by setting this register, corresponding bit of TXALM1 register must be set to zero.

Address: 0DH/4DH/8DH/CDH
 Name: TMODE
 Type: R/W
 Function: Test Mode Register 1

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	RXCKE	RXPLE	NOTP	NORP	REG
-	-	-	0	1	0	0	0

This register is used for diagnostic or LSI internal testing purposes. Usually this register should be set to zero.

REG

Register operation mode.

- 0: Write to read only register is not allowed.
- 1: Write to read only registers is allowed.

NORP

Receive processor operation mode.

- 0: Normal operation.
- 1: Stop receive processor.

NOTP

Transmit processor operation mode.

- 0: Normal operation.
- 1: Stop transmit processor.

RXPLE

The RXPLE bit controls receive PLL.

- 0: Receive PLL is disabled.
- 1: Receive PLL is enabled.

RXCKE

The RXCKE bit controls RXn pin (n=1~4). When BCKM pin is tied to high,

- 0: RXCKn (n=1~4) is fixed to zero.
- 1: RXCKn (n=1~4) outputs receive byte clock of port n (n=1~4).

When BCKM pin is tied to low, one of receive byte clocks is output from RXCLK1. This is summarized below.

Pin Name	BCKM=0	BCKM=1
RXCK1	Receive byte clock of port 1 is output when RXCKE bit of TMODE(0DH) is set to high. Fixed to zero when RXCKE bit of TMODE(0DH) is set to low.	One of receive byte clocks is output. Port 1 receive byte clock is output when RXCKE bit of TMODE(0DH) is set to high. Port 2 receive byte clock is output when RXCKE bit of TMODE(4DH) is set to high. Port 3 receive byte clock is output when RXCKE bit of TMODE(8DH) is set to high. Port 4 receive byte clock is output when RXCKE bit of TMODE(CDH) is set to high.

Pin Name	BCKM=0	BCKM=1
RXCK2	Receive byte clock of port 2 is output when RXCKE bit to TMODE(4DH) is set to high. Fixed to zero when RXCKE bit of TMODE(4DH) is set to low.	Forced into Hi-Z state regardless of TMODE(4DH).
RXCK3	Receive byte clock of port 3 is output when RXCKE bit to TMODE(8DH) is set to high. Fixed to zero when RXCKE bit of TMODE(8DH) is set to low.	Forced into Hi-Z state regardless of TMODE(8DH).
RXCK4	Receive byte clock of port 4 is output when RXCKE bit to TMODE(CDH) is set to high. Fixed to zero when RXCKE bit of TMODE(CDH) is set to low.	Forced into Hi-Z state regardless of TMODE(CDH).

Notice: When BCKE is tied to high, no more than one RXCKE bit should be set to high.

Address: 0EH/4EH/8EH/CEH
 Name: TSGEN
 Type: R/W
 Function: Test Mode Register 2

7	6	5	4	3	2	1	0
rsvd	rsvd	HECI	LOCI	BIPI	LOPI	OOFI	LOSI
–	–	0	0	0	0	0	0

This register is used for diagnostic or LSI internal testing purposes. Usually this register should be set to zero.

LOSI

Transmit frame option 1.

- 0: Normal operation.
- 1: Transmit all 00H data.

OOFI

Transmit frame option 2.

- 0: Normal operation.
- 1: A1/A2 bytes of the transmit frame are set to 00H .

LOPI

Transmit frame option 3.

- 0: Normal operation.
- 1: H1/H2 pointer of the transmit data is set to invalid value.

BIPI

Transmit frame option 4.

- 0: Normal operation.
- 1: B1/B2/B3 bytes of the transmit frame are bit-reversed.

LOCI

Transmit frame option 5.

- 0: Normal operation.
- 1: HEC byte of the transmit cells are bit-reversed.

HECI

Transmit frame option 6.

- 0: Normal operation.
- 1: The LSB of HEC byte of the transmit cells are bit-reversed.

Address: 0FH/4FH/8FH/CFH
 Name: GFC
 Type: R/W
 Function: GFC Control

7	6	5	4	3	2	1	0
TGFC[3:0]				OPT	UAC	GFCHLT	TGFCEN
0	0	0	0	0	0	0	0

TGFCEN

The TGFCEN controls whether to insert TGFC[3:0] to GFC field of every assigned cell to transmit.

- 0: GFC field of assigned cell to transmit is not changed.
- 1: TGFC[3:0] is inserted to the GFC field of every assigned cell to transmit.

GFCHLT

The GFCHLT bit controls the GFC function. When the GFC field of received cell indicates HALT ("1xxx"), QPLC can withhold the transmission of valid cells. When valid cells are withheld, IDLE cells are transmitted instead.

- 0: Disable GFC function.
- 1: Enable GFC function.

UAC

The UAC bit controls idle/unassigned cell insertion.

- 0: When there is no cell in transmit FIFOs, idle cells are inserted into the transmit frame.
- 1: When there is no cell in transmit FIFOs, unassigned cells with a GFC field set to 0001 are inserted into the transmit frame.

OPT

The OPT bit controls the GFC field of unassigned cells generated in QPLC.

- 0: Pattern 0001 is inserted to the GFC field of unassigned cells generated in QPLC.
- 1: TGFC[3:0] is inserted to the GFC field of unassigned cells generated in QPLC.

TGFC[3:0]

When TGFCEN is set, TGFC[3:0] is inserted to the GFC field of every assigned cell to transmit.

Address: 10H/50H/90H/D0H
 Name: INTSEL1
 Type: R/W
 Function: Interrupt Control Register of STATUS1

7	6	5	4	3	2	1	0
LOOC	TXOOL	RXOOL	LOC	LOP	LOF	OOF	LOS
0	0	0	0	0	0	0	0

Each bit of the INTSEL1 register controls interrupt generation of a corresponding bit of STATUS1 register.

LOS

The LOS bit controls LOS interrupt.

- 0: Disable an interrupt generation.
- 1: Enable an interrupt generation, when Loss of Signal status change is detected.

OOF

The OOF bit controls OOF interrupt.

- 0: Disable an interrupt generation.
- 1: Enable an interrupt generation, when an Out of Frame status change is detected.

LOF

The LOF bit controls LOF interrupt.

- 0: Disable an interrupt generation.
- 1: Enable an interrupt generation, when a Loss of Frame status change is detected.

LOP

The LOP bit controls LOP interrupt.

- 0: Disable an interrupt generation.
- 1: Enable an interrupt generation, when a Loss of Pointer status change is detected.

LOC

The LOC bit controls LOC interrupt.

- 0: Disable an interrupt generation.
- 1: Enable an interrupt generation, when a Loss of Cell delineation status change is detected.

RXOOL

- 0: Disable an interrupt generation.
- 1: Enable an interrupt generation, when the receive PLL gets out of lock.

TXOOL

- 0: Disable an interrupt generation.
- 1: Enable an interrupt generation, when the transmit PLL gets out of lock.

LOOC

- 0: Disable an interrupt generation.
- 1: Enable an interrupt generation, when the LOOCP/M input is tied high.

rsvd

These fields are reserved for future use. For normal operation these fields should be set to zero.

Address: 11H/51H/91H/D1H
 Name: INTSEL2
 Type: R/W
 Function: Interrupt Control Register 2

7	6	5	4	3	2	1	0
GFC	PTY	RFOV	PYEL	PAIS	PRDI	LAIS	LRDI
0	0	0	0	0	0	0	0

Each bit of the INTSEL2 register controls interrupt generation of a corresponding bit of STATUS2 register.

LRDI

The LRDI bit controls LRDI interrupt.

- 0: Disable an interrupt generation.
- 1: Enable an interrupt generation, when the Line-RDI status changes.

LAIS

The LAIS bit controls LAIS interrupt.

- 0: Disable an interrupt generation.
- 1: Enable an interrupt generation, when the Line-AIS status changes.

PRDI

The PRDI bit controls PRDI interrupt.

- 0: Disable an interrupt generation.
- 1: Enable an interrupt generation, when the Path-RDI status changes.

PAIS

The PAIS bit controls Path AIS interrupt.

- 0: Disable an interrupt generation.
- 1: Enable an interrupt generation, when the Path-AIS status changes.

PYEL

The PYEL bit controls Path YEL interrupt.

- 0: Disable an interrupt generation.
- 1: Enable an interrupt generation, when the Path-YEL status changes.

RFOV

- 0: Disable an interrupt generation.
- 1: Enable an interrupt generation, when a receive FIFO overflow is detected.

PTY

- 0: Disable an interrupt generation.
- 1: Enable an interrupt generation, when a parity error is detected.

GFC

- 0: Disable an interrupt generation.
- 1: Enable an interrupt generation, when QPLC detects a command in GFC field of received cell.

Address: 15H/55H/95H/D5H
 Name: INTIND1
 Type: R
 Function: Interrupt Status Register 1

7	6	5	4	3	2	1	0
LOOC	TXOOL	RXOOL	LOC	LOP	LOF	OOF	LOS
0	0	0	0	0	0	0	0

The INTIND1 register indicates interrupt status, when QPLC generates an interrupt. Each bit of this register is one, when the corresponding status of the STATUS1 register has any transition to 1. The host CPU can find an interrupt cause by reading this register, when interrupt has occurred. Each bit is cleared when 0 is written by the host CPU.

LOS

- 0: Indicates no transition in LOS status.
- 1: Indicates transition in LOS status.

OOF

- 0: Indicates no transition in OOF status.
- 1: Indicates transition in OOF status.

LOF

- 0: Indicates no transition in LOF status.
- 1: Indicates transition in LOF status.

LOP

- 0: Indicates no transition in LOP status.
- 1: Indicates transition in LOP status.

LOC

- 0: Indicates no transition in LOC status.
- 1: Indicates transition in LOC status.

RXOOL

- 0: Indicates no transition in RXOOL status.
- 1: Indicates transition in RXOOL status.

TXOOL

- 0: Indicates no transition in TXOOL status.
- 1: Indicates transition in TXOOL status.

LOOC

- 0: Indicates no transition in LOOC status.
- 1: Indicates transition in LOOC status.

rsvd

These fields are reserved for future use. For normal operation these fields should be set to zero.

Address: 16H/56H/96H/D6H
 Name: INTIND2
 Type: R
 Function: Interrupt Status Register 2

7	6	5	4	3	2	1	0
GFC	PTY	RFOV	PYEL	PAIS	PRDI	LAIS	LRDI
0	0	0	0	0	0	0	0

The INTIND2 register indicates interrupt status, when QPLC generates an interrupt. Each bit of this register is one, when the corresponding status of the STATUS2 register has any transition or transition to 1. The host CPU can find an interrupt cause by reading this register, when interrupt has occurred. Each bit is cleared when 0 is written by the host CPU.

LRDI

- 0: Indicates no transition in LRDI status.
- 1: Indicates transition in LRDI status.

LAIS

- 0: Indicates no transition in LAIS status.
- 1: Indicates transition in LAIS status.

PRDI

- 0: Indicates no transition in PRDI status.
- 1: Indicates transition in PRDI status.

PAIS

- 0: Indicates no transition in PAIS status.
- 1: Indicates transition in PAIS status.

PYEL

- 0: Indicates no transition in PYEL status.
- 1: Indicates transition in PYEL status.

RFOV

- 0: Indicates no transition to 1 in RFOV status.
- 1: Indicates transition to 1 in RFOV status.

PTY

- 0: Indicates no transition to 1 in PTY status.
- 1: Indicates transition to 1 in PTY status.

GFC

- 0: Indicates no transition to 1 in GFC status.
- 1: Indicates transition to 1 in GFC status.

Address: 1AH/5AH/9AH/DAH
 Name: STATUS1
 Type: R
 Function: Receive Status Register

7	6	5	4	3	2	1	0
LOOC	TXOOL	RXOOL	LOC	LOP	LOF	OOF	LOS
0	0	0	0	0	0	0	0

LOS

This bit indicates status of Loss of Signal. When LOS is detected, QPLC sets this field to one. When LOS condition disappears, this bit is cleared.

OOF

This bit indicates status of Out of Frame. When OOF is detected, QPLC sets this bit to one. When OOF condition disappears, this bit is cleared.

LOF

This bit indicates status of Loss of Frame. When LOF is detected, QPLC sets this bit to one. When LOF condition disappears, this bit is cleared.

LOP

This bit indicates status of Loss of Pointer. When LOP is detected, QPLC sets this bit to one. When LOP condition disappears, this bit is cleared.

LOC

This bit indicates status of Loss of Cell delineation. When LOC is detected, QPLC sets this bit to one. When LOC condition disappears, this bit is cleared.

RXOOL

When the receive PLL is out of lock, this bit is set to one. When the receive PLL is in lock, this bit is set to zero.

TXOOL

When the transmit PLL is out of lock, this bit is set to one. When the transmit PLL is in lock, this bit is set to zero.

LOOC

When the LOOC input is tied high, this bit is set to one. When the LOOC input is tied low, this bit is set to zero.

rsvd

These fields are reserved for future use. For normal operation these fields should be set to zero.

Note: This register indicates the current status. It is not cleared when accessed by the host CPU.

Address: 1BH/5BH/9BH/DBH
 Name: STATUS2
 Type: R
 Function: Alarm Status Register

7	6	5	4	3	2	1	0
GFC	PTY	RFOV	PYEL	PAIS	PRDI	LAIS	LRDI
0	0	0	0	0	0	0	0

LRDI

This bit indicates L-RDI state of receiving frame. When L-RDI is judged to be set, QPLC sets this bit to one. When L-RDI is judged to be reset, this bit is cleared.

LAIS

This bit indicates L-AIS state of receiving frame. When L-AIS is judged to be set, QPLC sets this bit to one. When L-AIS is judged to be reset, this bit is cleared.

PRDI

This bit indicates P-RDI state of receiving frame. When P-RDI is judged to be set, QPLC sets this bit to one. When P-RDI is judged to be reset, this bit is cleared.

PAIS

This bit indicates P-AIS state of receiving frame. When P-AIS is judged to be set, QPLC sets this bit to one. When P-AIS is judged to be reset, this bit is cleared.

PYEL

This bit indicates P-YEL state of receiving frame. When P-YEL is judged to be set, QPLC sets this bit to one. When P-YEL is judged to be reset, this bit is cleared.

RFOV

When the receive FIFO overflow is detected, QPLC sets this bit to one. When the receive FIFO overflow is cleared, QPLC sets this bit to zero.

PTY

When QPLC detects parity error in received cell at transmit side cell interface, this bit is set to one. When QPLC detects normal parity, this bit is cleared.

GFC

When QPLC detects GFC commands (1xxx, x1xxx or xx1x) in the GFC field of received cell, QPLC sets this bit to one. When QPLC detects "000x" in the GFC field of received cell, QPLC sets this bit to zero.

Note: This register indicates current status. It is not cleared when accessed by the host CPU.

Address: 1EH/5EH/9EH/DEH
 Name: RGFC
 Type: R
 Function: Receive GFC Status

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	rsvd	RGFC[3:0]			
–	–	–	–	0	0	0	0

RGFC[3:0]

RGFC[3:0] indicates the GFC field of received cell. It is updated when the GFC field of the current cell is different from the preceding one.

Address: 1FH/5FH/9FH/DFH
 Name: CIADR
 Type: R/W
 Function: Port Address

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	ADDR[4:0]				
–	–	–	0	0	0	0	0

ADDR[4:0]

The port address for each port should be set. The address of respective ports should be different from each other for proper QPLC operation.

Address: 20H/60H/A0H/E0H
 Name: B1ERRL
 Type: R
 Function: B1-SBIP8 Error Counter [7:0]

7	6	5	4	3	2	1	0
B1ERR[7:0]							
0	0	0	0	0	0	0	0

Address: 21H/61H/A1H/E1H
 Name: B1ERRH
 Type: R
 Function: B1-SBIP8 Error Counter [15:8]

7	6	5	4	3	2	1	0
B1ERR[15:8]							
0	0	0	0	0	0	0	0

This register indicates B1-SBIP8 error count. When B1 bit of the FCUPD register is set to one, this counter is updated within 150 s. The value of this counter is kept until the next update is requested by setting B1 bit to one.

Address: 22H/62H/A2H/E2H
 Name: B2ERRL
 Type: R
 Function: B2-LBIP24 Error Counter [7:0]

7	6	5	4	3	2	1	0
B2ERR[7:0]							
0	0	0	0	0	0	0	0

Address: 23H/63H/A3H/E3H
 Name: B2ERRM
 Type: R
 Function: B2-LBIP24 Error Counter [15:8]

7	6	5	4	3	2	1	0
B2ERR[15:8]							
0	0	0	0	0	0	0	0

Address: 24H/64H/A4H/E4H
 Name: B2ERRH
 Type: R
 Function: B2-LBIP24 Error Counter [19:16]

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	rsvd	B2ERR[19:16]			
-	-	-	-	0	0	0	0

This register indicates B2-LBIP24 error count. When B2 bit of the FCUPD register is set to one, this counter is updated within 150 s. The value of this counter is kept until the next update is requested by setting B2 bit to one.

Address: 25H/65H/A5H/E5H
 Name: B3ERRL
 Type: R
 Function: B3-PBIP8 Error Counter [7:0]

7	6	5	4	3	2	1	0
B3ERR[7:0]							
0	0	0	0	0	0	0	0

Address: 26H/66H/A6H/E6H
 Name: B3ERRH
 Type: R
 Function: B3-PBIP8 Error Counter [15:8]

7	6	5	4	3	2	1	0
B3ERR[15:8]							
0	0	0	0	0	0	0	0

This register indicates B3-PBIP8 error count. When B3 bit of the FCUPD register is set to one, this counter is updated within 150 s. The value of this counter is kept until the next update is requested by setting B3 bit to one.

Address: 27H/67H/A7H/E7H
 Name: LFEBEL
 Type: R
 Function: Receive LFEBE Counter [7:0]

7	6	5	4	3	2	1	0
LFEBE[7:0]							
0	0	0	0	0	0	0	0

Address: 28H/68H/A8H/E8H
 Name: LFEBEM
 Type: R
 Function: Receive LFEBE Counter [15:8]

7	6	5	4	3	2	1	0
LFEBE[15:8]							
0	0	0	0	0	0	0	0

Address: 29H/69H/A9H/9H
 Name: LFEBEH
 Type: R
 Function: Receive LFEBE Counter [19:16]

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	rsvd	LFEBE[19:16]			
-	-	-	-	0	0	0	0

This register indicates received L-FEBE count. When LFEBE bit of the FCUPD register is set to one, this counter is updated within 150 s. The value of this counter is kept until the next update is requested by setting LFEBE bit to one.

Address: 2AH/6AH/AAH/EAH
 Name: PFEBEL
 Type: R
 Function: Receive PFEBE Counter [7:0]

7	6	5	4	3	2	1	0
PFEBE[7:0]							
0	0	0	0	0	0	0	0

Address: 2BH/6BH/ABH/EBH
 Name: PFEBEH
 Type: R
 Function: Receive PFEBE Counter [15:8]

7	6	5	4	3	2	1	0
PFEBE[15:8]							
0	0	0	0	0	0	0	0

This register indicates received P-FEBE count. When PFEBE bit of the FCUPD register is set to one, this counter is updated within 150 s. The value of this counter is kept until the next update is requested by setting B2 bit to one.

Address: 2CH/6CH/ACH/ECH
 Name: FCUPD
 Type: R/W
 Function: Error Counter Update Flag

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	PFEBE	LFEBE	B3	B2	B1
–	–	–	0	0	0	0	0

B1

When this bit is set to one, the B1-SBIP8 error counter is updated and this bit is cleared automatically.

- 0: No update request.
- 1: Update request to B1-SBIP8 error counter.

B2

When this bit is set to one, the B2-LBIP24 error counter is updated and this bit is cleared automatically.

- 0: No update request.
- 1: Update request to B1-LBIP24 error counter.

B3

When this bit is set to one, the B3-PBIP8 error counter is updated and this bit is cleared automatically.

- 0: No update request.
- 1: Update request to B3-PBIP8 error counter.

LFEBE

When this bit is set to one, the receive LFEBE counter is updated and this bit is cleared automatically.

- 0: No update request.
- 1: Update request to receive LFEBE counter.

PFEBE

When this bit is set to one, the receive PFEBE counter is updated and this bit is cleared automatically.

- 0: No update request.
- 1: Update request to receive PFEBE counter.

Address: 30H/70H/B0H/F0H
 Name: COHER
 Type: R
 Function: Corrected Cell Header Error Counter

7	6	5	4	3	2	1	0
COHER[7:0]							
0	0	0	0	0	0	0	0

This register indicates a corrected header error count. After being read, this register is cleared automatically. When no header error correction mode is selected, this counter has no meaning.

Address: 31H/71H/B1H/F1H
 Name: UCHER
 Type: R
 Function: Uncorrected cell Cell Header Error Counter

7	6	5	4	3	2	1	0
UCHER[7:0]							
0	0	0	0	0	0	0	0

This register indicates an uncorrected header error count. After being read, this counter is cleared automatically.

Address: 32H/72H/B2H/F2H
 Name: RXCCL
 Type: R
 Function: Receive Valid Cell Counter [7:0]

7	6	5	4	3	2	1	0
RXCC[7:0]							
0	0	0	0	0	0	0	0

Address: 33H/73H/B3H/F3H
 Name: RXCCM
 Type: R
 Function: Receive Valid Cell Counter [15:8]

7	6	5	4	3	2	1	0
RXCC[15:8]							
0	0	0	0	0	0	0	0

Address: 34H/74H/B4H/F4H
 Name: RXCCH
 Type: R
 Function: Receive Valid Cell Counter [19:16]

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	rsvd	RXCC[19:16]			
–	–	–	–	0	0	0	0

This register indicates received valid cell count. When RXCC bit of the CCUPD register is set to one, this counter is updated within 1 s. The value of this counter is kept until the next update is requested by setting RXCC bit to one.

Address: 35H/75H/B5H/F5H
 Name: TXCCL
 Type: R
 Function: Transmit Valid Cell Counter [7:0]

7	6	5	4	3	2	1	0
TXCC[7:0]							
0	0	0	0	0	0	0	0

Address: 36H/76H/B6H/F6H
 Name: TXCCM
 Type: R
 Function: Transmit Valid Cell Counter [15:8]

7	6	5	4	3	2	1	0
TXCC[15:8]							
0	0	0	0	0	0	0	0

Address: 37H/77H/B7H/F7H
 Name: TXCCH
 Type: R
 Function: Transmit Valid Cell Counter [19:16]

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	rsvd	TXCC[19:16]			
–	–	–	–	0	0	0	0

This register indicates transmit valid cell count. When TXCC bit of the CCUPD register is set to one, this counter is updated within 1 s. The value of this register is kept until the next update is requested by setting TXCC bit to one.

Address: 38H/78H/B8H/F8H
 Name: CCUPD
 Type: R/W
 Function: Cell Counter Update Flag

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	rsvd	rsvd	rsvd	TXCC	RXCC
-	-	-	-	-	-	0	0

RXCC

When this bit is set to one, the RXCC counter is updated within 1 s and this bit is cleared automatically.

- 0: No update request.
- 1: Update request for RXCC counter.

TXCC

When this bit is set to one, the TXCC counter is updated within 1 s and this bit is cleared automatically.

- 0: No update request.
- 1: Update request for TXCC counter.

Address: 3DH/7DH/BDH/FDH
 Name: MEMAL
 Type: R/W
 Function: Memory Address Register [7:0]

7	6	5	4	3	2	1	0
MEMAL[7:0]							
0	0	0	0	0	0	0	0

Address: 3EH/7EH/BEH/FEH
 Name: MEMAH
 Type: R/W
 Function: Memory Address Register [3:0]

7	6	5	4	3	2	1	0
MEMWR	rsvd	rsvd	MEMAH[4:0]				
0	-	-	0	0	0	0	0

Address: 3FH/7FH/BFH/FFH
 Name: MEMD
 Type: R/W
 Function: Data Control Register

7	6	5	4	3	2	1	0
MEMD[7:0]							
0	0	0	0	0	0	0	0

These registers are used to access the QPLC internal memory. For access, follow the steps below.

Read Operation

- (1) Set address to MEMAH register.
- (2) Set address to MEMAL register.
- (3) Wait for TBD nsec.
- (4) Read MEMD register.

Write Operation

- (1) Set address to MEMAH register with MEMWR set high.
- (2) Set address to MEMAL.
- (3) Write the value to MEMD register.

Address mapping is as follows:

0x0000-0x07ff	RX firmware
0x0800-0x0bff	TX firmware
0x0c00-0x0cff	RX overhead memory
0x0d00-0x0dff	TX overhead memory
0x0e00-0x0eff	RX cell FIFO
0x0f00-0x0fff	TX cell FIFO
0x1000-0x10ff	RX internal registers
0x1100-0x11ff	TX internal registers

Field assignment in RX/TX overhead memory is shown below. The address is increased from the upper left corner to righthand and then downward. For instance, the address of G1 byte in RX overhead memory is 0x0c39.

The SOH/POH bytes are extracted from received data and stored in RX overhead memory every frame. The other area in RX overhead memory is used as working storage by the internal processor.

In TX overhead memory, A1, A2, C1, C2, B1, B3, H1, H3, G1, B2, K2, H4 and (third) Z2 bytes are automatically updated by the internal processor. Other SOH/POH are filled with zero when TOMINI bit of PCONT register is set high or left untouched otherwise.

A1	A1	A1	A2	A2	A2	C1	C1	C1	J1										
B1	-	-	E1	-	-	F1	-	-	B3										
D1	-	-	D2	-	-	D3	-	-	C2										
H1	H1	H1	H2	H2	H2	H3	H3	H3	G1										
B2	B2	B2	K1	-	-	K2	-	-	F2										
D4	-	-	D5	-	-	D6	-	-	H4										
D7	-	-	D8	-	-	D9	-	-	Z3										
D10	-	-	D11	-	-	D12	-	-	Z4										
Z1	Z1	Z1	Z2	Z2	Z2	E2	-	-	Z5										

Figure 3-1 Field Assignment of RX/TX Overhead Memory

Receive Clock

External Clock Mode

When the RCKSEL pin is tied low, the externally provided clock, RXCIP/M1-4, is used for each part of QPLC and the clock recovery PLLs are deactivated. Usually RXDIP/M1-4 is sampled at the rising edge of RXCIP/M1-4. Optionally, RXDIP/M1-4 can be sampled at the falling edge of RXCIP/M1-4 by trying the DLYSEL pin to high.

On-Chip Clock Recovery Mode

When the RCKSEL pin is tied high, the receive side of QPLC operates on an internally recovered clock. The recovered clock is divided by 8 and compared with the reference clock REFCK. When the recovered clock frequency is out of the ± 244 ppm range of REFCK, the clock recovery PLL is judged to be out of lock and RXOOL bit of STATUS1 register is set. The clock recovery PLL automatically switches to REFCK for reference source to keep oscillation in the vicinity of 155.52MHz (for STS-3) or 51.84MHz (for STS-1) when the recovered clock is out of the ± 244 ppm range of REFCK or an 80-bit period of no transition in receive data is detected or LOOC input is tied high and the AUTOCSE bit in the CONT register is set high. During the period when the clock recovery PLL locks to REFCK, the data transition detector keeps sampling the receive data. When the data transition detector detects at least one data transition in an 80-bit period and LOOC input is tied low and the clock recovery PLL generates clock at frequency in the ± 244 ppm range of REFCK, the clock recovery PLL switches back to receive data for reference. The case stated above is typical. There are many options available.

1. 80-bit transition detector can be masked by setting zero to LOOCDE bit of PCONT register (address:08H/48H/88H/C8H).
2. External LOOCP/M input can be masked by setting one to LOOCE bit of TSMOD register (address:06H).
3. Automatic switching between clock recovery mode in which RX PLL locks to receive data and reference mode in which RX PLL locks to REFCK can be cancelled by setting zero to AUTOCSE bit of CONT register (address:00H).
4. 244 ppm detector can be masked by setting zero to OOLDE bit of PCONT register (address:08H/48H/88H/C8H).

5. When AUTOCSE bit is zero, RX PLL operation mode can be controlled by external pin REFSEL and PLLINI bit of PCONT register. The operation is as follows:

REFSEL=1 or PLLINI=1:RXPLL locks to REFCK.
Otherwise: RX PLL locks to receive data.

6. Even when AUTOCSE is set to one, RX PLL can be forced into reference mode by making REFSEL=1 or PLLINI=1.

Frame Synchronization

STS-3c(STM-1)

HUNT

The framing pattern of three consecutive A1s followed by three consecutive A2s are searched. When the framing pattern is found, framing operation enters a PRESYNC mode.

PRESYNC

When one more expected framing pattern is within the 2430 byte interval, the framing operation enters the SYNC mode.

SYNC

The framing pattern is checked every frame. If invalid framing patterns are found in four consecutive frames, OOF is set in the STATUS1 register and the framing operation enters the HUNT mode.

STS-1, STS-1/2

HUNT

The framing pattern of one A1 followed by one A2 is searched. When the framing pattern is found, framing operation enters PRESYNC mode.

PRESYNC

When one more framing pattern is found within the 810 byte interval, the framing operation enters the SYNC mode.

SYNC

The framing pattern is checked every frame. If invalid framing patterns are found in four consecutive frames, OOF is set in the STATUS1 register and the framing operation enters the HUNT mode.

Frame Descrambling

The received frame data is descrambled by a quasi-random pattern generated by the polynomial $1+x^6+x^7$. The first line of SOH (i.e., A1, A2, C1 bytes) is excluded from the descramble operation. The descramble operation starts from the byte following the last C1 byte with the initial data for the generating polynomial '1111111'. The descramble operation can optionally be disabled by setting 1 to NODSBF bit in the FRMSEL register.

BIP/FEBE Count

Section BIP-8

Section BIP-8 is calculated over the entire area of each received frame before descrambling based on the 8 bits interleaved parity calculation using even parity. The calculated BIP-8 code is compared with the B1 byte of the following frame bit by bit. The differences indicate the section level bit errors. The bit errors are counted and accumulated in an internal counter frame by frame. This counter value can be accessed via B1ERRL/H register. The host CPU is required to read them every one second for performance monitoring. Before reading them, the host CPU should set 1 to B1 bit in FCUPD register. In about 125 μ s, B1ERRL/H are updated and the B1 bit in the FCUPD register is automatically cleared. Section BIP-8 counter stops counting when 4 MSB bits become '1111'.

Line BIP-24

Line BIP-24 is calculated over the entire area of each frame after descrambling except for the first to third rows of SOH based on the 24 bits interleaved parity calculation using even parity. The calculated BIP-24 code is compared with the three B2 bytes of the following frame bit by bit. The differences indicate the line level bit errors. The bit errors are counted and the count is inserted to the Z2 byte of the transmit SOH as Line FEBE, as well as accumulated in an internal counter frame by frame. This counter value can be accessed via B2ERRL/M/H register. The host CPU is required to read them every one second for performance monitoring. Before reading them, the host CPU should set 1 to B2 bit in FCUPD

register. In about 125 μ s, B2ERRL/M/H are updated and the B2 bit in the FCUPD register is automatically cleared. Line BIP-24 counter stops counting when 4 MSB bits become '1111'.

Path BIP-8

Path PIB-8 is calculated over the entire area of each VC4 (or SPE for STS-1) after descrambling based on the 8 bits interleaved parity calculation using even parity. The calculated BIP-8 code is compared with the B3 byte of the following frame bit by bit. The differences indicate the path level bit errors. The bit errors are counted and inserted to the G1 byte of the transmit POH as Path FEBE, as well as accumulated in a internal counter frame by frame. This counter value can be accessed via B3ERRL/H register. The host CPU is required to read them every one second for performance monitoring. Before reading them, the host CPU should set 1 to B3 bit in the FCUPD register. In about 125 μ s, B3ERRL/H are updated and the B3 bit in the FCUPD register is automatically cleared. Path BIP-8 counter stops counting when 4 MSB bits become '1111'.

Line FEBE

Line FEBE value of every received frame is accumulated in Line FEBE counter. This counter value can be accessed via LFEBEL/M/H registers. The host CPU is required to read them every one second for performance monitoring. Before reading them, the host CPU should set 1 to LFEBE bit in the FCUPD register. In about 125 μ s, LFEBEL/M/H are updated and the FEBE bit in the FCUPD register is automatically cleared. Line FEBE counter stops counting when 4 MSB bits become '1111'.

Path FEBE

The path FEBE value of every received frame is accumulated in the Path FEBE counter. This counter value can be accessed via PFEBEL/H registers. The host CPU is required to read them every one second for performance monitoring. Before reading them, the host CPU should set 1 to PFEBE bit in the FCUPD register. In about 125 μ s, PFEBEL/H are updated and the FEBE bit in the FCUPD register is automatically cleared. Path FEBE counter stops counting when 4 MSB bits become '1111'.

Pointer Operation

The first H1 and the first H2 in SOH are used to locate the J1 byte of VC4 (or SPE for STS-1). The second and third H1 bytes have a fixed value of 93H. The second and third H2 bytes have a fixed value of FFH. The second and third H1/H2 bytes are not used for pointer operation. Figure 4-1 shows the field assignment of the first H1/H2 bytes.

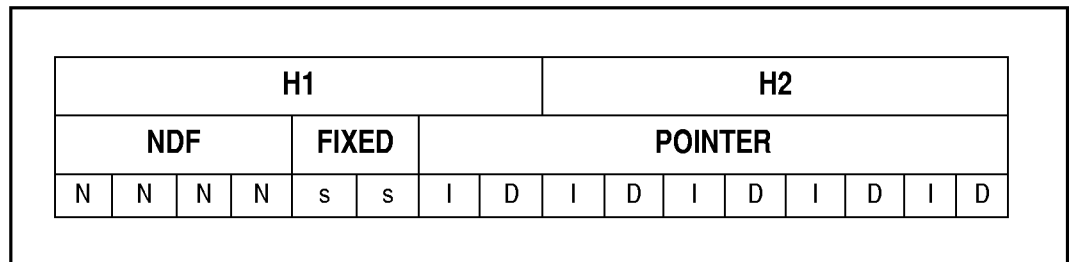


Figure 4-1 Field Assignment of H1/H2 Bytes

NDF has two values; NNNN=0110 and indicates no change in the pointer value while NNNN=1001 and indicates change in the pointer value.

The FIXED field is usually ignored. The normal value is depends on whether the receive data is SONET type or SDH type. When the receive data is SONET type, ss=00. When the receive data is SDH type, ss=10. When H1 and H2 bytes should carry PAIS, ss=11.

POINTER usually locates the J1 byte. The pointer value is a binary number with a range from 0 to 782, which indicates the offset between the third H3 and the J1 byte of VC4. SOH bytes are not counted in the offset. For example, a pointer value of 0 indicates the J1 byte immediately follows the third H3 byte, whereas an offset of 522 indicates that the J1 byte immediately follows the third C1 byte. The POINTER field is also used to indicate stuff operation. If the POINTER value of the current frame equals the POINTER value of the previous frame with 3 or more 1 bits inverted, it is the positive stuff indication. If the POINTER value of the current frame equals the POINTER value of the previous frame with 3 or more D bits inverted, it is the negative stuff indication.

There are six cases for the pointer operation.

New Data Flag Active

Normally NDF has a value of 0110. If NDF=1001 or 0001 or 1101 or 1011 or 1000, the New Data Flag indication is considered active. The coincident POINTER value replaces the previous pointer value as long as the POINTER value is normal, that is in the range from 0 to 782. The updated pointer value takes effect from the first J1 byte following H1, H2. When the New Data Flag is considered active, the positive stuff indication and the negative stuff indication are ignored.

Positive Stuff Operation

When the following conditions are met, the positive stuff operation is executed.

1. Three or more I bits are inverted.
2. Two or less D bits, if at all, are inverted.
3. New Data Flag indication is not active.
4. The pointer is not updated in preceding three frames.

In positive stuff operation, three bytes (one byte is STS-1) following the third H3 byte is ignored as payload only in the current frame. The pointer value is incremented by one.

Negative Stuff Operation

When the following conditions are met, the negative stuff operation is executed.

1. Three or more D bits are inverted.
2. Two or less I bits, if at all, are inverted.
3. New Data Flag indication is not active.
4. The pointer is not updated in preceding three frames.

In a negative stuff operation, three H3 bytes (one H3 byte for STS-1) are included as part of VC4 (or SPE in STS-1) only in the current frame. The pointer value is reduced by one.

Three Consecutive, Consistent New Value

When consistent, a normal (in the range of 0 to 782) new pointer value is received for three consecutive frames, the pointer value replaces the previous value.

Detection of Path AIS

If an "1" pattern is detected in H1 and H2 for three consecutive frames, the PAIS bit is set in STATUS1 register. The PAIS bit is reset when valid pointers are detected for three consecutive frames.

LOP Detection

The LOP bit in the STATUS1 register is set when a valid pointer is not found for 8 consecutive frames or when 8 consecutive fields with the value of 1001 are detected. The LOP bit is reset when a valid pointer with normal field is detected for three consecutive frames or an "1" pattern is detected in H1 and H2 for three consecutive frames.

Detection of Irregular State

LOS: Loss of Signal

The receive data is sampled by the REFCK clock and compared with the data sampled one cycle before. The LOS is declared and the LOS bit in STATUS1 register is set when no data transition is observed for 20 μ sec. LOS is defined in TA-NWT-000253 as no signal condition lasting more than T_{μ sec where T is more than 2.3 and less than 100.

OOF: Out of Frame

The framing operation is set by the OOF bit in the STATUS1 register when four consecutive invalid frame alignment patterns (A1, A2) have been received and will reset the OOF bit when two consecutive valid frame alignment patterns have been detected.

LOF: Loss of Frame

The receive processor checks the OOF status every frame. When the OOF is set for 24 consecutive frames (i.e., for 3msec), the LOF bit in the STATUS1 register is set. If the OOF is found reset for 24 consecutive frames, the LOF bit is cleared.

LOP: Loss of Pointer

The LOP bit in the STATUS1 register is set when a valid pointer is not found for 8 consecutive frames or when 8 consecutive fields with the value of 1001 are detected. The LOP bit is reset when a valid pointer with normal field is detected for three consecutive frames or an "1" pattern (that is PAIS) is detected in H1 and H2 for three consecutive frames.

LOC: Loss of Cell Delineation

The LOC bit in the STATUS1 register is set when the cell delineation is in the HUNT STATE. The LOC bit is reset when the cell delineation enters the SYNC STATE. For the cell delineation, refer to the Cell Processing section.

Detection of Alarm Signals

The receive processor checks the K2 and G1 bytes to detect Line AIS, Line RDI, Path RDI along with H1/H2 bytes to detect Path AIS. When one of these alarms are detected, a corresponding bit in STATUS2 register is set. The alarm detection criteria is different for SONET and SDH. For SDH mode operation, SDH bit of TC register (address:09H/49H/89H/C9H) should be set to one.

1. LAIS: Line Alarm Indication Signal

When a 111 binary pattern is detected in bits 6, 7, 8 of the K2 byte for five consecutive frames (SONET mode) or three consecutive frames (SDH mode), LAIS is declared and the LAIS bit of STATUS2 register is set high. LAIS is removed when any pattern other than 111 is detected in bits 6, 7, 8 of K2 bytes for five consecutive frames (SONET mode) or three consecutive frames (SDH mode).

2. LRDI: Line Remote Defect Indication

When a 110 binary pattern is detected in bits 6, 7, 8 of the K2 byte for five consecutive frames (SONET mode) or three consecutive frames (SDH mode), LRDI is declared and the LRDI bit of STATUS2 register is set high. LRDI is removed when any pattern other than 110 is detected in bits 6, 7, 8 of K2 bytes for five consecutive frames (SONET mode) or three consecutive frames (SDH mode).

3. PAIS: Path Alarm Indication Signal

When an 1 binary pattern is detected in the H1/H2 bytes for three consecutive frames, PAIS is declared and the PAIS bit of STATUS2 register is set high. PAIS is removed when a valid pointer with the NDF is set to '1001' is detected or when the same valid pointer with normal NDF is detected in three consecutive frames .

4. PRDI: Path Remote Defect Indication

When bit 5 of the G1 byte is detected to be one for five consecutive frames (SONET mode) or three consecutive frames (SDH mode), PRDI is declared and the PRDI bit of STATUS2 register is set high. PRDI is removed when bit 5 of the G1 byte is detected to be zero for five consecutive frames (SONET mode) or three consecutive frames (SDH mode).

5. **PYEL: Path Yellow**

When bit 5 of the G1 byte is detected to be 1 for ten consecutive frames, PYEL is declared and PYEL bit of STATUS2 register is set high. PYEL is removed when bit 5 of the G1 bytes is detected to be 0 for ten consecutive frames.

Cell Processing

The payload is extracted from the STS-3c(STM-1)/STS-1 frame in a framing operation and provided to the cell delineation operation.

1. **Cell Delineation**

HUNT

The cell delineation operation searches the cell header with correct HEC. When a correct HEC is found, the cell delineation operation enters the PRESYNC state.

PRESYNC

With 53 byte intervals, the cell header is checked for HEC. If correct HECs are found for 6 cells, the cell delineation enters the SYNC state. If an incorrect HEC is found before that, the cell delineation operation returns to the HUNT state.

SYNC

The HEC pattern is checked cell by cell. If 7 consecutive incorrect HECs are found, the cell delineation returns to the HUNT state. The SYNC state has two modes; CORRECTION mode and DETECTION mode. The cell delineation enters the CORRECTION mode from the PRESYNC state. When a one bit HEC error is found in the CORRECTION mode, it is corrected and the cell delineation enters the DETECTION mode. If multiple bit HEC errors are found in the CORRECTION mode, the cell is dropped and the operation enters the DETECTION mode. When a correct HEC is found in the DETECTION mode, the operation returns to the CORRECTION mode.

2. **Cell Payload Descramble**

The 48 byte cell payload is descrambled by the sequence generated by the polynomial ' $x^{43}+1$.' The descramble operation can optionally be disabled by setting 1 to NODSBC in the CMS2 register.

3. **FIFO Control**

Receive cell data is stored in the 4 cell deep receive FIFO. The receive FIFO is controlled on a cell basis. When the FIFO is full of cells and

there are more cells to be stored, these additional cells are discarded and RFOV bit in STATUS2 register is set high. The receive FIFO can be reset independently by setting the RXFRES bit of the PCONT register. In reset state, the receive FIFO discards cells stored in it and ignores writes. The RXFRES bit should be set for at least 10.8 μ s.

4. **Receive Cell Interface**

The receive cell interface operates according to UTOPIA level-2, MPhy, 16-bit mode defined in the ATM Forum. An 8-bit mode operation is not supported. The maximum operation frequency is 50MHz. For parity bit, odd parity and even parity are selectable. Parity selection is done by setting the PARITY bit of the CMS1 register. HEC can be inserted in UDF1 or UDF2. This selection is done by setting the UDF bit of the CMA1 register. Details of the receive cell interface operation is described in the Cell Interface section.

5. **Performance Monitoring**

The number of cells which have been passed with an HEC error corrected are counted in 8-bit COHER while the number of cells which have been dropped due to an HEC error are counted in an 8-bit UNHER counter (address:31H/71H/B1H/F1H). COHER counter and UNHER counter stop counting when the count value become FFH. The number of normal or corrected cells which have been sent to receive cell FIFO are counted in a 20-bit internal counter. The count value can be read via the RXCCL/M/H register. The RXCCL/M/H are updated by setting 1 to RXCC bit in the CCUPD register. The receive cell counter stops counting when 4 MSB bits become '1111'.

6. **Optional Mode**

When the DROP bit in the CMS2 register is set high, every cell with at least one HEC error is dropped in the SYNC mode. No HEC correction is made.

When the PASS bit in the CMS2 register is set high, every cell is passed to the receive cell FIFO regardless of the HEC error in the SYNC mode.

In these optional modes, cell delineation state transition is made using the normal mode.

7. **GFC Handling**

The GFC field is checked in every cell. When QPLC finds any command (1xxx, x1xx or xx1x) in GFC field of a received cell, it sets the GFC bit of the STATUS2 register. When the command is HALT(1xxx) and the GFCHLT bit is set in GFC register, transmission of cells is stopped. The GFC field of a received cell is stored in the RGFC register.

Transmit Clock Generation

1. **Loop Timing Mode**

QPLC transmit side operates in the loop timing mode when the LOOPT bit of LOOP register is set high. In the loop timing mode, the transmit clock is the same as the receive side clock. Even when the clock recovery PLL fails to lock with the receive data, the transmit clock frequency is guaranteed because the clock recovery PLL switches the reference source to an externally provided REFCK.

2. **Internal Clock Generation Mode**

QPLC generates transmit serial clock (155.52MHz/51.84MHz) from the REFCK when the LOOPT bit of the LOOP register is set low and the TCKSEL pin is tied high.

3. **External Clock Mode**

The QPLC transmit part operates on an externally provided serial clock, TXCIP/M, when the LOOPT bit of the LOOP register is set low and the TCKSEL pin is tied low.

Frame Scrambling

The transmit data is scrambled by a quasi-random pattern generated by the polynomial $1+x^6+x^7$. The first line of SOH (A1, A2, C1) is excluded from the scramble operation. The scramble operation starts from the byte data following C1 with initial data for the polynomial being '1111111.' This scramble operation can optionally be disabled by setting 1 to NODSBF in the FRMSEL register.

BIP Calculation

1. **Section BIP-8**

The section BIP-8 is calculated over the entire area of each frame after scramble is based on the 8 bits interleaved parity calculation using even parity. The calculated BIP-8 code is inserted into the B1 byte in the following frame before scrambling.

2. **Line BIP-24**

Line BIP-24 is calculated over the entire area of each frame the before scrambling, except for the first to third rows of SOH based on 24 bits interleaved parity calculation using even parity. The calculated BIP-24 code is inserted into the B2 bytes in the following frame before scrambling.

3. **Path BIP-8**

The path BIP-8 is calculated over the entire area of each VC4 (or SPE for STS-1) before scrambling based on the 8 bits interleaved parity calculation using even parity. The calculated BIP-8 code is inserted into the B3 byte in the following frame before scrambling.

SOH Bytes Insertion

1. **A1, A2**

The A1 value should be F6H, A2 is set at 28H. These values are automatically inserted to transmit SOH in QPLC.

2. **C1**

The value should be 01H/02H/03H for SONET and 01H/AAH/AAH for SDH. These values are automatically inserted to transmit SOH in QPLC.

3. **B1**

The section BIP-8 is calculated and inserted to the B1 byte in the transmit SOH.

4. **H1, H2**

The H1 and H2 bytes are automatically set to the value shown in Figure 5-1 by the internal processor. The value is 0. The value of SS is 00 for SONET and 10 for SDH. For SDH mode operation, the SDH bit of TC register (address:09H/49H/89H/C9H) should be set to 1. For diagnostic purposes, H1 and H2 bytes in the transmit frame can be written from outside. In this case, the internal transmit processor should be stopped by setting 1 in the NOTP bit of the TMODE register. The pointer value in H1 and H2 bytes must be consistent with the value set to the J1POS register. Table 5-1 shows some examples.

Table 5-1 Correspondence Between POINTER and J1V/J1H

POINTER	J1V	J1H
0	3	3
86	3	89
521	8	89
522	0	3
782	2	89

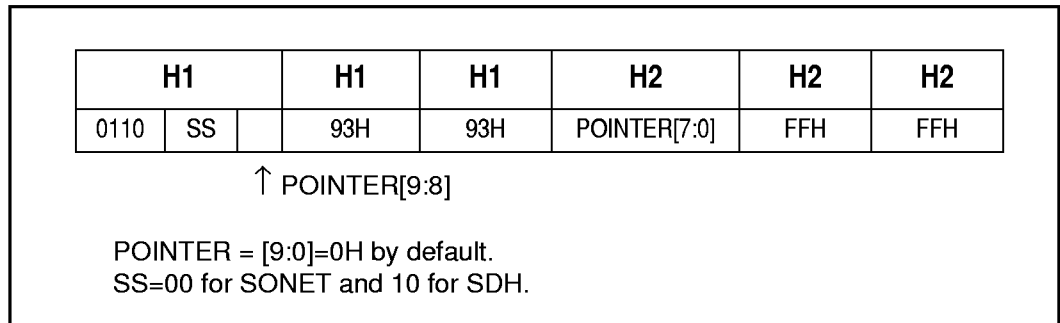


Figure 5-1 Value for Three H1s and Three H2s in Transmit SOH

5. **H3**

The H3 bytes are set automatically in the transmit SOH. The value is usually 00H, when QPLC generates PAIS, FFH.

6. **B2**

Line BIP-24 is calculated automatically and inserted into the B2 bytes of the transmit frame.

7. **K2**

Line AIS and line RDI are set into the K2 byte automatically in QPLC according to the condition tabulated in the Alarm Signaling section.

8. **Z2**

Line FEBE is calculated automatically and inserted to the Z2 byte.

9. **Others**

The other SOH bytes are automatically filled with zero by setting one to TOMINI bit of PCONT register (address:08H/48H/88H/C8H). When arbitrary data should be written to these bytes, TOMINI bit should be set to zero.

POH Bytes Insertion

1. **B3**
Path BIP-8 is calculated automatically and inserted into the B3 byte.
2. **C2**
The value should be 13H because payload type is always ATM for QPLC. This value is automatically inserted to transmit POH in QPLC.
3. **G1**
Path RDI is inserted automatically to the G1 byte according to the condition tabulated in the Alarm Signaling section. Additionally, Path FEBE is calculated and inserted to the G1 byte.
4. **H4**
The cell offset is counted automatically and set into the H4 byte.
5. **Others**
The other POH bytes are automatically filled with zero by setting one to TOMINI bit of PCONT register (address:08H/48H/88H/C8H). When arbitrary data should be written to these bytes, TOMINI bit should be set to zero.

Alarm Signal Insertion

1. **LAIS: Line Alarm Indication Signal**
When LOS or LOF is detected in the receive side, Line AIS is automatically inserted by transmitting the code 111 in bit 6, 7, 8 of the K2 byte of transmitting frame, if the LAIS bit is set in TXALM1 register. LAIS is inserted without condition when the LAIS bit is set high in the TXALM2 register.
2. **LRDI: Line Remote Defect Indication**
When LOS or LOF is detected or LAIS is declared in the receive side, Line RDI is automatically inserted by transmitting the code 110 in bit 6, 7, 8 of the K2 byte of transmitting frame, if the LRDI bit is set in TXALM1 register. LRDI is inserted without condition when the LRDI bit is set high in the TXALM2 register.

3. **PAIS: Path Alarm Indication Signal**

When LOS, LOF, LOP, LOC is detected or LAIS is declared in the receive side, Path AIS is automatically inserted by setting all "1" in H1/H2/H3 bytes and the entire payload field if the PAIS bit is set in the TXALM1 register. PAIS is also inserted without condition when the PAIS bit is set high in the TXALM2 register.

4. **PRDI: Path Remote Defect Indication**

When LOS, LOF, LOP, LOC is detected or LAIS or PAIS is declared in the receive side, Path RDI is automatically inserted by setting 1 in bit 5 of the G1 byte of the transmitting frame, if the PRDI bit is set in the TXALM1 register. PRDI is inserted without condition when the PRDI bit is set high in the TXALM2 register.

5. **PYEL: Path Yellow**

When LOS, LOF, LOP, LOC is detected or LAIS or PAIS is declared in the receive side for 5 seconds, Path YEL is automatically inserted by setting 1 in bit 5 of the G1 byte of the transmitting frame, if the PYEL bit is set in the the TXALM1 register. PYEL is inserted without condition when the PYEL bit is set high in the TXALM2 register.

Transmit Cell Processing

1. **Transmit Cell Interface**

The transmit cell interface operates according to UTOPIA level-2, MPHY, 16-bit mode defined in the ATM Forum. The maximum operation frequency is 50MHz. For parity bit, odd parity and even parity can be selected. HEC can be inserted in UDF1 or UDF2. The parity selection and HEC selection are set in the CMS1 register. Details of the transmit cell interface operation are described in the Cell Interface section.

2. **FIFO Control**

Transmit cell data received from the ATM layer is stored in the transmit FIFO. The transmit FIFO is controlled in the cell level. The FIFO is programmable to be 1, 2, 3 or 4 cell deep. When the FIFO is full of cell data, QPLC rejects receiving more cells from the ATM layer by deasserting TXCAV when it is polled. The transmit FIFO can be reset independently by setting the TXFRES bit of the PCONT register. In reset state, the transmit FIFO discards stored cells and ignores writes. The TXFRES bit should be set for at least 10.8µsec.

3. Cell Header Calculation

A CRC-8 calculation is performed over the first four header bytes. A parallel implementation of the polynomial, x^8+x^2+x+1 is used. The coset polynomial, $x^6+x^4+x^2+1$ is added by module 2 to the residue. The result is inserted to the fifth byte of the ATM cell. The coset polynomial addition can optionally be disabled by setting 1 to NOTC in the CMS2 register. The cell header calculation can optionally be disabled by setting 1 to the NOHEC bit in the CMS2 register. In this case, the 5th byte of the cell data goes through unchanged.

4. Cell Payload Scrambling

The 48 bytes of cell payload is scrambled with the sequence generated by the polynomial ' $x^{43}+1$.' The scramble operation can optionally be disabled by setting high to NOSCBC in the CMS2 register.

5. Performance Monitoring

The number of assigned or unassigned cells which have been read from the transmit cell FIFO and inserted in the transmit frames are counted in an internal 20-bit counter. The count value can be read via the TXCCL/M/H register. The TXCCL/M/H is updated by setting 1 to the TXCC bit in the CCUPD register. The transmit cell counter stops counting when 4 MSB bits become '1111'.

6. GFC Handling

Transmission of cells is stopped when GFCHLT bit is set in GFC register and the HALT bits are set in the GFC field of received cells. When the TGFCEN bit is set in the GFC register, TGFC[3:0] in the GFC register is inserted in the GFC field of assigned/unassigned cells transmitted from the ATM layer. Additionally, when the OPT bit in the GFC register is set high, TGFC[3:0] in the GFC register is also inserted in unassigned cells generated in QPLC.

7. Idle/Unassigned Cell Insertion

When there is no cell in the transmit FIFO, QPLC inserts an idle/unassigned cell into the transmit frame dependent on register control. If the UAC bit is set high in the GFC register, QPLC inserts unassigned cells with the GFC field set to '0001' or TGFC[3:0] depending on OPT bit in the GFC register. If the UAC bit is set low, QPLC inserts idle cells.

Startup Procedure

For startup, follow the procedures below.

1. **Hardware Reset**

The -RESET pin should be tied low for 10 cycles of CLK to reset the configuration registers. These configuration registers have default values after reset.

2. **Software Reset**

Set RESET bits of the PCONT registers to high for at least 10 cycles of REFCK to reset internal registers and then clear these RESET bits.

3. **Operation Mode Set**

Set configuration registers according to the usage. If default values are sufficient, skip this step.

4. **Overhead Memory Initialization**

Initialize the SOH/POH portion of the transmit overhead memory.

5. **Clear Stop**

Clear the stop bit of the PCONT register of each port to start normal operation.

Setting the STOP bit high during normal operation is not recommended because it results in a loss of frames and cells.

Loop Back

The Loop back mode is controlled by the LOOP register, the LPBK pin and the TSDSEL pin.

1. **Setting Line Loop Back**

Setting one to LOOPL bit of LOOP register or tying TSDSEL pin to high forces QPLC into serial loop back mode. In this mode, receive serial data RXDIP/Mi (i=1~4) is directly output from transmit serial port TXDOP/Mi (i=1~4).

2. Parallel Line Loop Back

Setting one to LOOP2 bit of LOOP register or tying LPBK pin to high forces QPLC into parallel loop back mode. In this mode, receive serial data RXDIP/Mi (i=1~4) is serial/parallel converted in receive section and then parallel/serial converted in transmit section and output from transmit port TXDOP/Mi (i=1~4).

3. Serial UTOPIA Loop Back

Setting one to LOOP1 bit of LOOP register forces QPLC into serial UTOPIA loop back mode. In this mode, transmit serial data is looped back to receive serial input internally.

4. Parallel UTOPIA Loop Back

Setting one to LOOPU bit of LOOP register forces QPLC into parallel UTOPIA loop back mode. In this mode, transmit parallel data is looped back to receive part and at the same time parallel/serial converted and output from TXDOP/Mi (i=1~4). Tying LPBK pin to high has similar effect. Transmit parallel data is looped back to receive part. The difference is in TXDOP/Mi (i=1~4). When LPBK is tied high, RXDIP/Mi (i=1~4) appears at TXDOP/Mi (i=1~4).

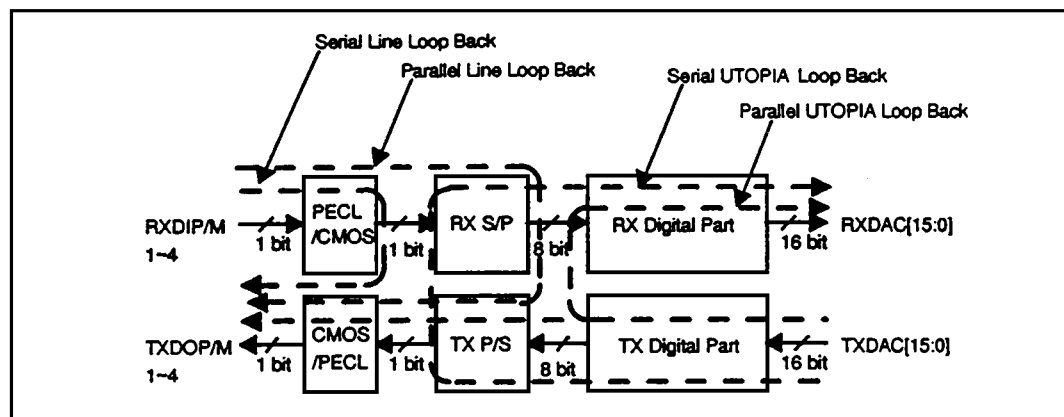


Figure 6-1 Parallel UTOPIA Loop Back

Diagnostic Test

The receive state detection capability can be tested in the loop back mode using the TSGEN register. LOS, OOF, LOP, BIP error, LOC detection test can be made by setting the corresponding bit in the TSGEN register.

Line Interface

RX Line Interface

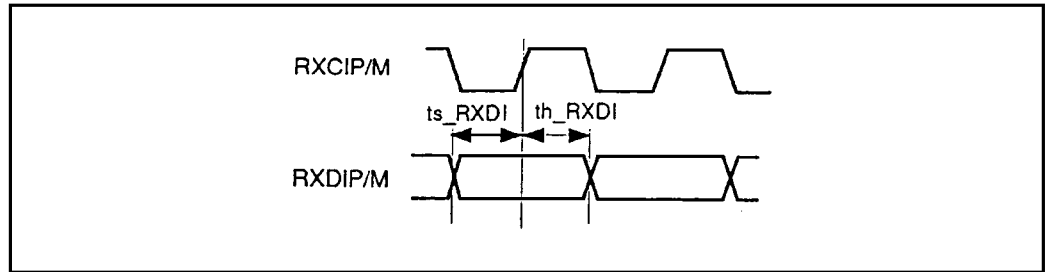


Figure 7-1 RX Line Interface Timing

Table 7-1 RX Line Interface

Symbol	Description	Min	Max	Units
-	RXCIP/M Duty Cycle	45	55	ns
-	RXCIP/M Frequency Tolerance	-20	+20	ppm
ts_RXDI	RXDIP/M Setup Time to RXCIP/M High	2	-	ns
th_RXDI	RXDIP/M Hold Time to RXCIP/M High	2	-	ns

TX Line Interface

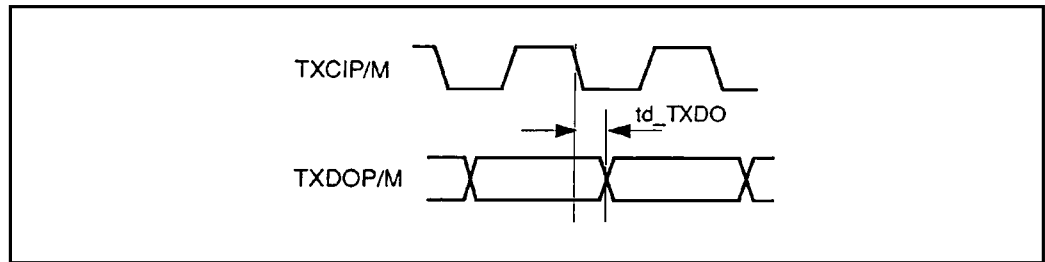


Figure 7-2 TX Line Interface Timing

Table 7-2 TX Line Interface

Symbol	Description	Min	Max	Units
-	TXCIP/M Duty Cycle	45	55	ns
-	TXCIP/M Frequency Tolerance	-20	+20	ppm
ts_TXDO	TXDOP/M Delay from TXCIP/M Low	-2	2	ns

Cell Interface

TX Cell Interface

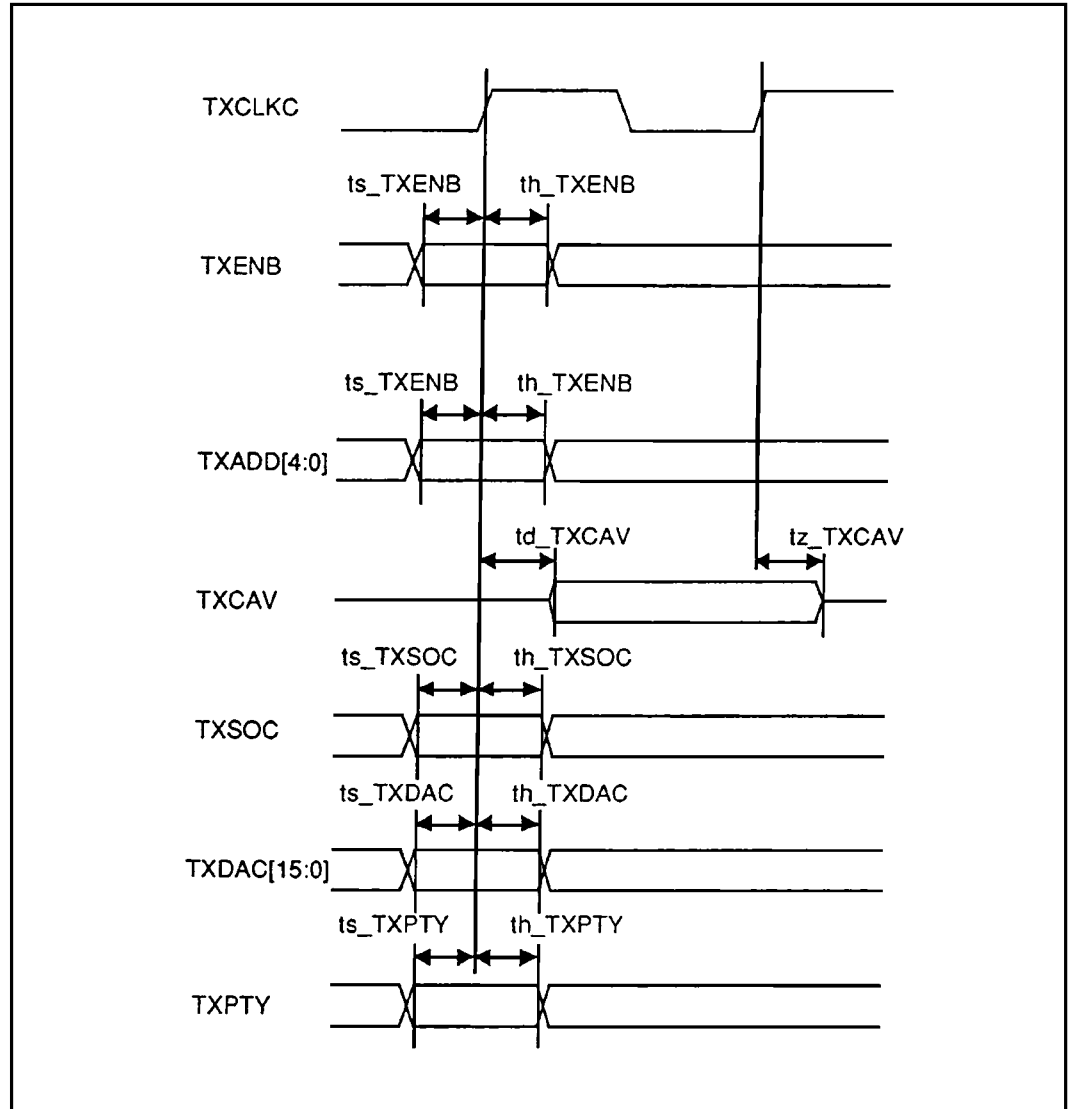


Figure 7-3 TX Cell Interface Timing

Table 7-3 TX Cell Interface

Symbol	Description	Min	Max	Units
–	TXCLKC Frequency	–	50	MHz
–	TXCLKC Duty Cycle	40	60	%
ts_TXENB	TXENB Setup Time to TXCLKC High	4	–	ns
th_TXENB	TXENB Hold Time to TXCLKC High	1	–	ns
ts_TXADD	TXADD[4:0] Setup Time to TXCLKC High	4	–	ns
th_TXADD	TXADD[4:0] Hold Time to TXCLKC High	1	–	ns
td_TXCAV	TXCAV Delay from TXCLKC High	1	16	ns
tz_TXCAV	TXCAV Hi-Z from TXCLKC High	1	16	ns
ts_TXSOC	TXSOC Setup Time to TXCLKC High	4	–	ns
th_TXSOC	TXSOC Hold Time to TXCLKC High	1	–	ns
ts_TXDAC	TXDAC Setup Time to TXCLKC High	4	–	ns
th_TXDAC	TXDAC Hold Time to TXCLKC High	1	–	ns
ts_TXPTY	TXPTY Setup Time to TXCLKC High	4	–	ns
th_TXPTY	TXPTY Hold Time to TXCLKC High	1	–	ns

RX Cell Interface

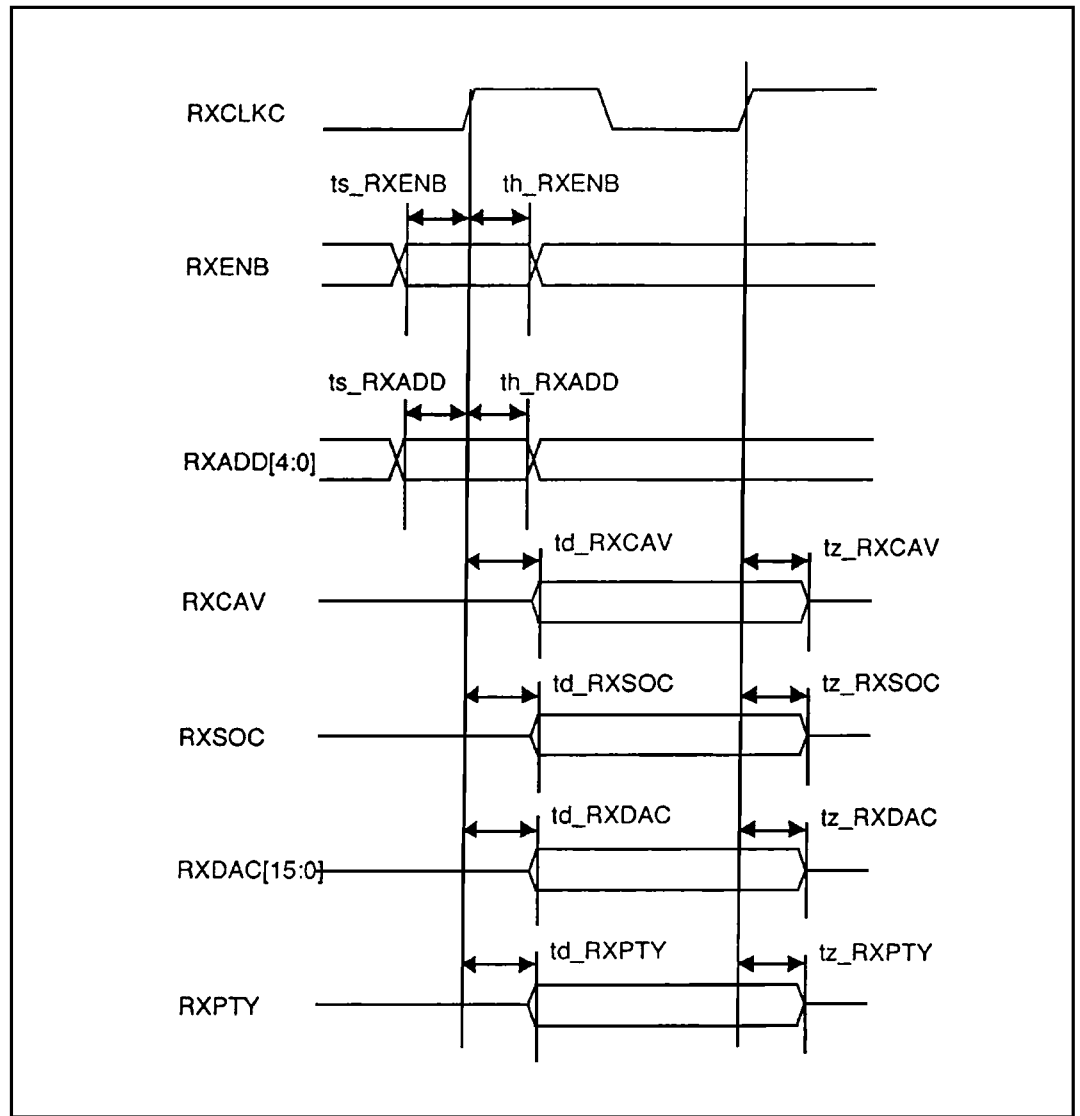


Figure 7-4 RX Cell Interface Timing

Table 7-4 RX Cell Interface

Symbol	Description	Min	Max	Units
–	RXCLKC Frequency	–	50	MHz
–	RXCLKC Duty Cycle	40	60	%
ts_RXENB	RXENB Setup Time to RXCLKC High	4	–	ns
th_RXENB	RXENB Hold Time to RXCLKC High	1	–	ns
ts_RXADD	RXADD[4:0] Setup Time to RXCLKC High	4	–	ns
th_RXADD	RXADD[4:0] Hold Time to RXCLKC High	1	–	ns
td_RXCAV	RXCAV Delay from RXCLKC High	1	16	ns
tz_RXCAV	RXCAV Hi-Z from RXCLKC High	1	16	ns
td_RXSOC	RXSOC Delay from RXCLKC High	1	16	ns
tz_RXSOC	RXSOC Hi-Z from RXCLKC High	1	16	ns
td_RXDAC	RXDAC [15:0] Delay from RXCLKC High	1	16	ns
tz_RXDAC	RXDAC [15:0] Delay from RXCLKC High	1	16	ns
td_RXPTY	RXPTY Delay from RXCLKC High	1	16	ns
tz_RXPTY	RXPTY Delay from RXCLKC High	1	16	ns

CPU Interface

CPU Interface Read Time

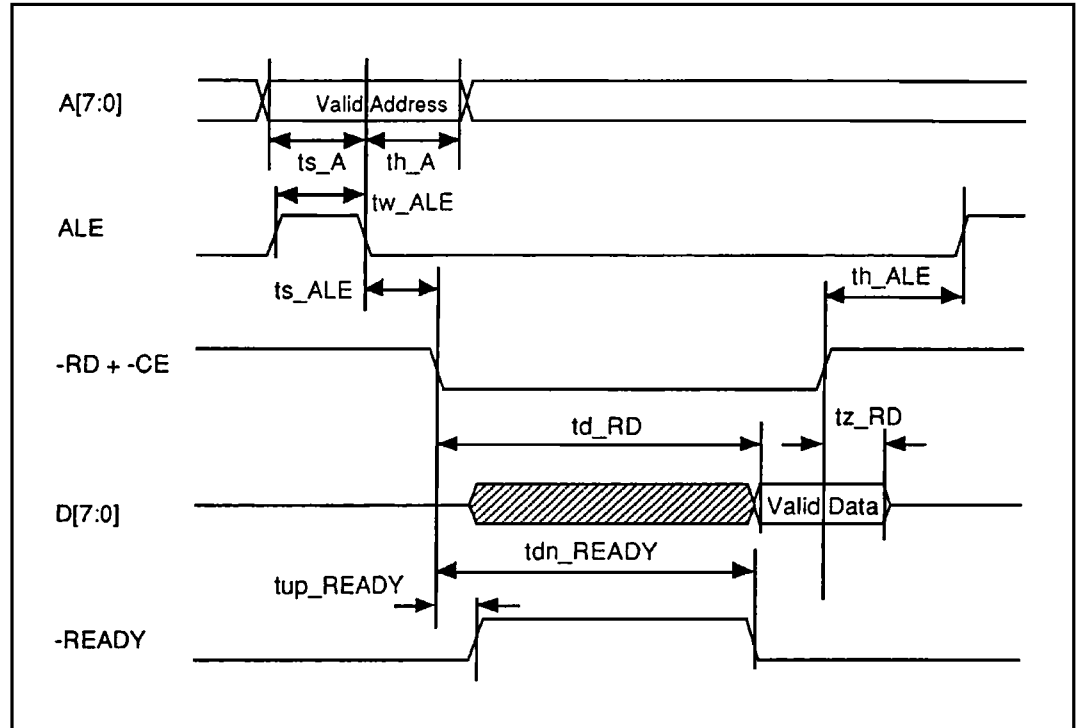


Figure 7-5 CPU Interface Read Timing

Read access starts when (-RD + -CE) goes down and ends when (-RD + -CE) goes up.

Table 7-5 CPU Interface Read Timing

Symbol	Description	Min	Max	Units
ts_A	Valid Address Setup Time to ALE	25	–	ns
th_A	Valid Address Hold Time to ALE	5	–	ns
tw_ALE	ALE High Pulse Width	20	–	ns
ts_ALE	ALE Low Setup Time to Read Start	0	–	ns
th_ALE	ALE Low Hold Time to Read End	(1)	–	ns
td_RD	Valid Data Delay from Read Start	–	(2)	ns
tz_RD	Data Output Hi-Z from Read End	1	20	ns
tup_READY	READY High Delay from CE	1	20	ns
tdn_READY	READY Low Delay from Read Start	–	(3)	ns

$$(1) th_ALE(min) = (1/Fmin) * 2 [ns]$$

$$(2) td_RD (max) = (1/Fmin) * 3 + 50 [ns]$$

$$(3) tdn_READY (min) = (1/Fmin) * 3 + 50 [ns]$$

where Fmin is lower frequency of Byte clock and CLK. Byte clock is 19.44MHz for STS-3(STM-1), 6.38MHz for STS-1 and 3.24MHz for STS-1/2. CLK 19.44MHz. When access is toward RX/TX overhead memory, it takes up to 100 Byte clock cycles before -READY goes down.

CPU Interface Write Timing

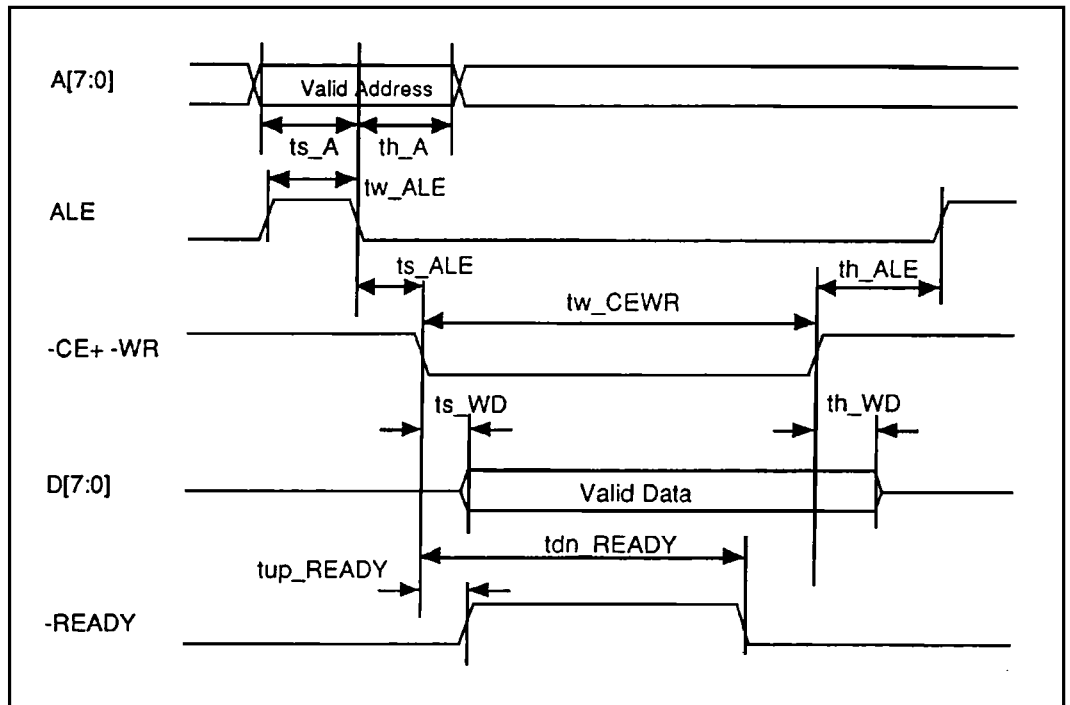


Figure 7-6 CPU Interface Write Timing

Write access starts when (-WR + -CE) goes down and ends when (-WR + -CE) goes up.

Table 7-6 CPU Interface Write Timing

Symbol	Description	Min	Max	Units
ts_A	Valid Address Setup Time to ALE	25	–	ns
th_A	Valid Address Hold Time to ALE	5	–	ns
tw_ALE	ALE High Pulse Width	20	–	ns
ts_ALE	ALE Low Setup Time to Write Start	0	–	ns
th_ALE	ALE Low Hold Time to Write End	(1)	–	ns
tw_CEWR	Write pulse width	(2)	–	ns
ts_WD	Write Data Setup Time to Write Start	0	–	ns
th_WD	Write Data Hold Time to Write End	0	–	ns
tup_READY	READY High Delay from CE	2	20	ns
tdn_READY	READY Low Delay from Write Start	–	(3)	ns

(1) $th_ALE(\min) = (1/F_{\min}) * 2$ [ns]

(2) $tw_CEWR(\min) = (1/F_{\min}) * 4$ [ns]

(3) $tdn_READY(\min) = (1/F_{\min}) * 3 + 50$ [ns]

where F_{\min} is lower frequency of Byte clock and CLK. Byte clock is 19.44MHz for STS-3(STM-1), 6.38MHz for STS-1 and 3.24MHz for STS-1/2. CLK 19.44MHz. When access is toward RX/TX overhead memory, it takes up to 100 Byte clock cycles before -READY goes down.

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Table 8-1 TTL Level Input and Output

Symbol	Parameters	Min	Max	Units	Conditions
VOLt	TTL Output Low Voltage	–	0.4	Volts	–
VOHt	TTL Output High Voltage	2.4	–	Volts	–
VILt	TTL Input Low Voltage	–	0.8	Volts	–
VIHt	TTL Input High Voltage	2.0	–	Volts	–
IILt	TTL Input Low Current	–	–	μA	–
IIHt	TTL Input High Current	–	–	μA	–

Table 8-2 CMOS Level Input and Output

Symbol	Parameters	Min	Max	Units	Conditions
VOLc	CMOS Output Low Voltage	–	0.8	Volts	–
VOHc	CMOS Output High Voltage	4.2	–	Volts	–
VILc	CMOS Input Low Voltage	–	2.0	Volts	–
VIHc	CMOS Input High Voltage	3.0	–	Volts	–
IILc	CMOS Input Low Current	–	–	μA	–
IIHc	CMOS Input High Current	–	–	μA	–

Table 8-3 PECL Input and Output

Symbol	Parameters	Min	Max	Units	Conditions
VOLp	PECL Output Low Voltage	VDD -1.9	VDD -1.5	Volts	Terminated to 3.0V via 50Ω resistor.
VOHp	PECL Output High Voltage	VDD -1.15	VDD -0.75	Volts	Terminated to 3.0V via 50Ω resistor.
VILp	PECL Input Low Voltage	–	VDD -1.5	Volts	–
VIHp	PECL Input High Voltage	VDD -1.15	–	Volts	–
IILp	PECL Input Low Current	–	–	μA	–
IIHp	PECL Input High Current	–	–	μA	–

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Table 9-1 Absolute Maximum Ratings

Parameter	Ratings
Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	TBD
Supply Voltage	TBD
Voltage on Any Pin	TBD
Static Discharge Voltage	TBD
Latch-Up Current	TBD
DC Input Current	TBD
Lead Temperature	TBD
Absolute Maximum Junction Temperature	TBD
Power Dissipation	TBD

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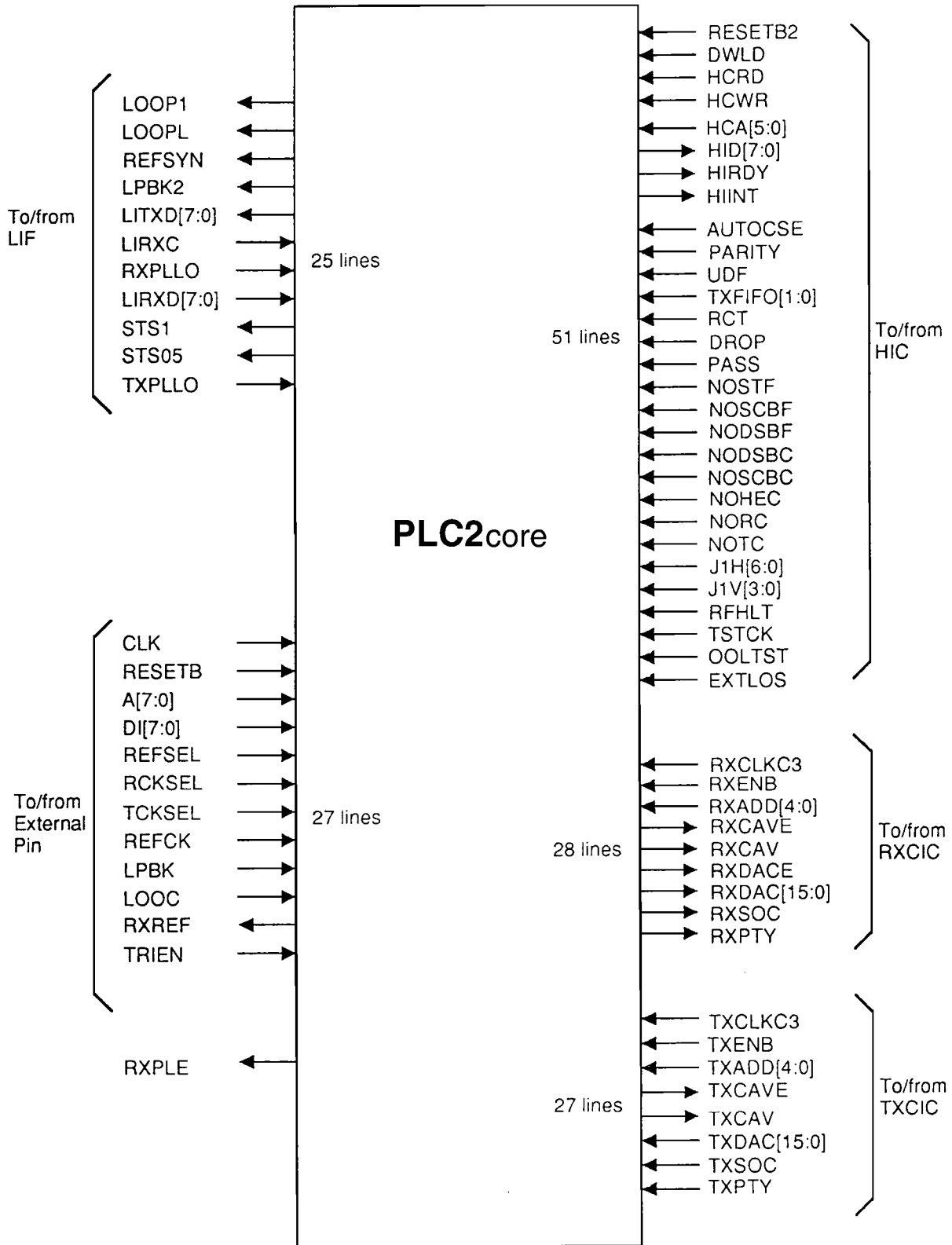


Figure A-1 PLC2 Core Connection

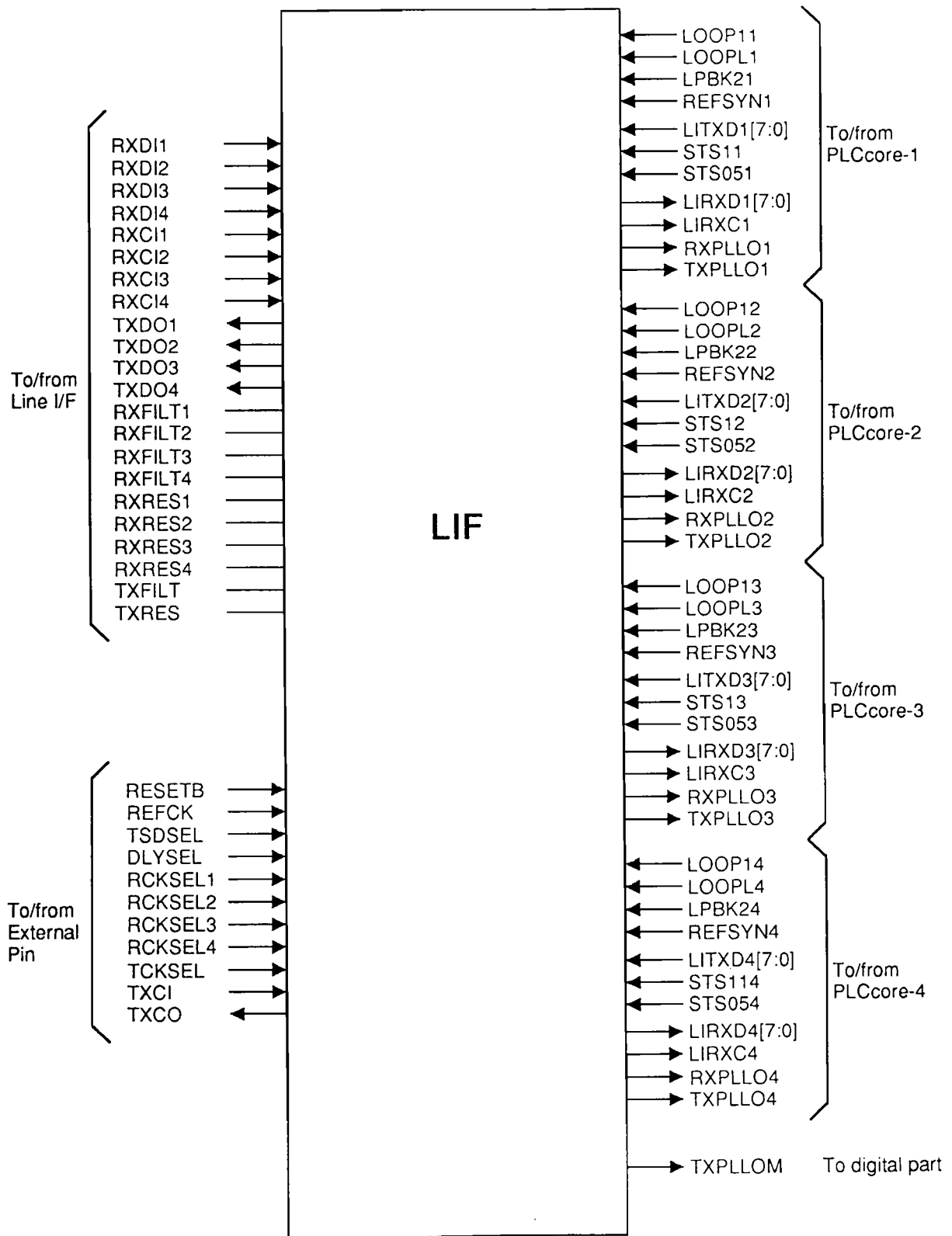


Figure A-2 LIF Connection

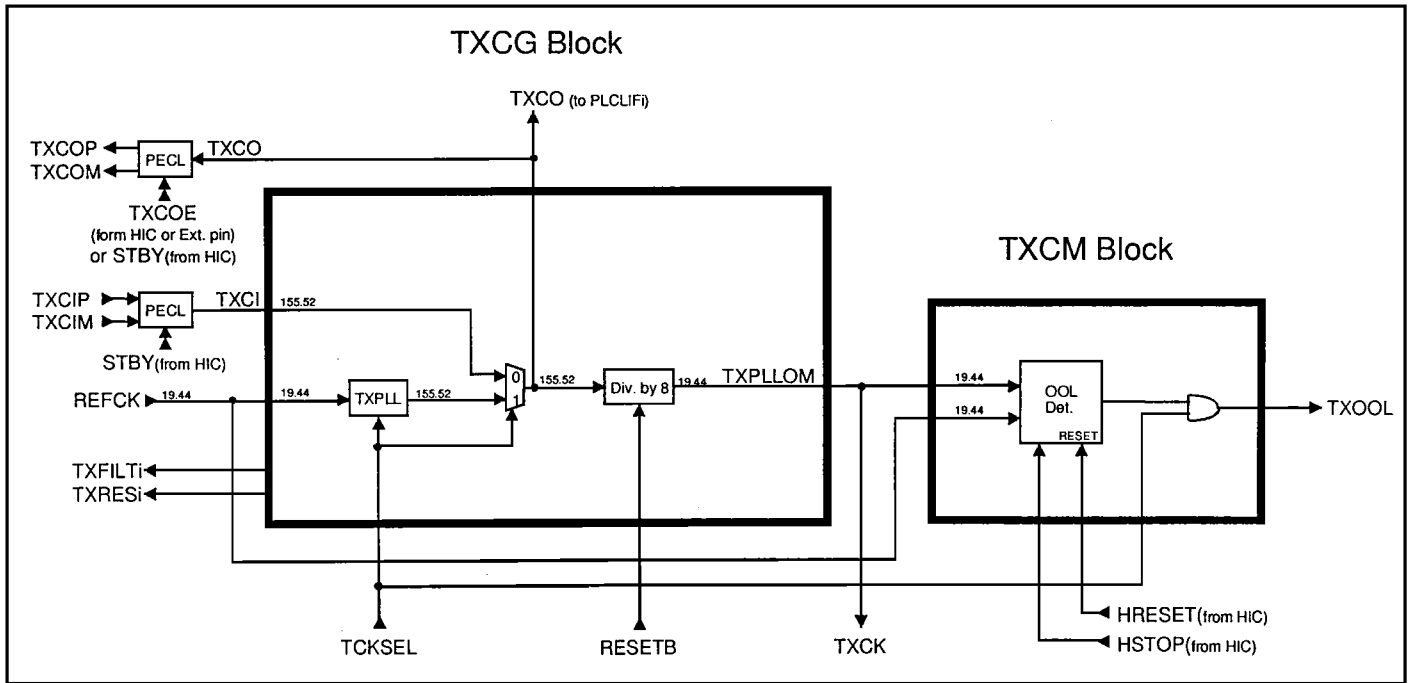


Figure A-4 TXCG Block

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