MOTOROLA

Quad Driver

Military 10E512

Product Preview

ELECTRICALLY TESTED PER:
10E512

The 10E512 is a quad driver with two pairs of OR/NOR outputs form each gate, and a common, buffered enable input. Using the data inputs the device can serve as an ECL memory address fan-out driver. Using just the enable input, the device serves as a clock driver, although the 10E511 is designed specifically for this purpose, and offers lower skew than the E512.

- 600 ps Max. Propagation Delay
- Common Enable Input
- 75 kΩ Input Pulldown Resistors

PIN NAME

Pin	Function
D_0 - D_3	Data Inputs
$\overline{EN}$	Enable Inputs
Q_{na} - Qnb	True Outputs
$\overline{Q_{na}}$ - $\overline{Qnb}$	Inverting Outputs

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: X

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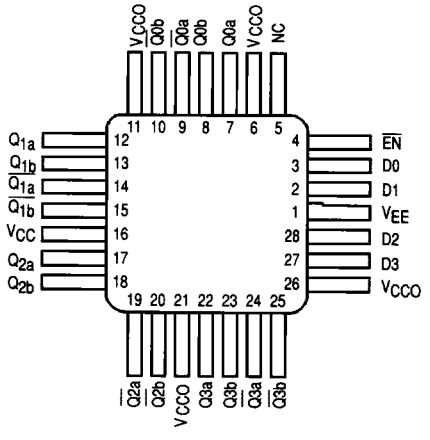
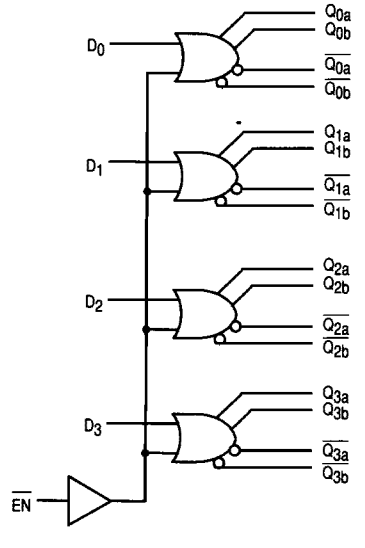


LOGIC DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

10E Series DC CHARACTERISTICS: V_{EE} = -5.2 V ± 5%; V_{CC} = V_{CCO} = GND[1]

Symbol	Parameter	Limits						Units
		+ 25° C		+ 125° C		– 55° C		
		Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	-980	-810	TBA		TBA		mV
V_{OL}	Output LOW Voltage	-1950	-1630	TBA		TBA		mV
V_{IH}	Input HIGH Voltage	-1130	-810	TBA		TBA		mV
V_{IL}	Input LOW Voltage	-1950	-1480	TBA		TBA		mV
I_{IL}	Input LOW Current	0.5		TBA		TBA		µA

1. 10E series circuits are designed to meet the dc specifications shown in the table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 volts, except bus outputs where specified, are terminated into 25Ω.

DC CHARACTERISTICS: V_{EE} = V_{EE}(min) to V_{EE}(max), V_{CC} = V_{CCO} = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current								
	D		200		200		200	µA	
	$\overline{EN}$		150		150		150	µA	
I_{EE}	Power Supply Current		56		56		56	mA	

AC CHARACTERISTICS: V_{EE} = V_{EE}(min) to V_{EE}(max), V_{CC} = V_{CCO} = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output								
	D	200	600	200	600	200	600	ps	
	$\overline{EN}$	275	675	275	675	275	675	ps	
t_{Skew}	Within-device Skew								
	Dn to Qn, $\overline{Qn}$	80		80		80		ps	(Note 1)
	Dna to Qnb	40		40		40		ps	(Note 2)
t_r t_f	Rise/Fall Times 20 - 80%	275	700	275	700	275	700	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Skew defined between common OR or common NOR outputs of a single gate.

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