AWC6313R

HELP3™ Dual-band 3.4 V Japan Cellular & IMT CDMA Linear Power Amplifier Module

PRELIMINARY DATA SHEET - Rev 1.1

FEATURES

- InGaP HBT Technology
- High Efficiency:
  38 % @ maximum P_{OUT}
  21 % @ +15 dBm P_{OUT}
- Low Quiescent Current: 8 mA
- Internal Voltage Regulation
- Common V_{MODE} Control Line
- Simplified V_{CC} Bus PCB routing
- Reduced External Component Count
- Low Profile Surface Mount Package: 1 mm
- CDMA 1x RTT, 1x EV-DO Compliant
- RoHS Compliant Package, 250 °C MSL-3

APPLICATIONS

- CDMA/EVDO Dual-band Japan Cellular/IMT Wireless Handsets and Data Devices

PRODUCT DESCRIPTION

The AWC6313 addresses the demand for increased integration in dual-band handsets for KDDI's Japan CDMA network. The small footprint 3 mm x 5 mm x 1 mm surface mount RoHS compliant package contains independent RF PA paths to ensure optimal performance in both frequency bands, while achieving a 25% PCB space savings compared with solutions requiring two single-band PAs. The package pinout was chosen to enable handset manufacturers to easily route V_{CC} to both power amplifiers and simplify control with a common V_{MODE} pin. The device is manufactured on an advanced InGaP HBT MMIC technology offering state-of-the-art reliability, temperature stability, and ruggedness. The AWC6313R incorporates ANADIGICS' HELP3™ technology to provide low power consumption without the need for an external voltage regulator. Two operating modes provide optimum efficiency at high and medium/low power output levels, thereby dramatically increasing handset talk-time and standby-time. Its built-in voltage regulator eliminates the need for external voltage regulation and load switches. The 3 mm x 5 mm x 1 mm surface mount package incorporates matching networks optimized for output power, efficiency and linearity in a 50 Ω system.

M28 Package
14 Pin 3 mm x 5 mm x 1 mm
Surface Mount Module

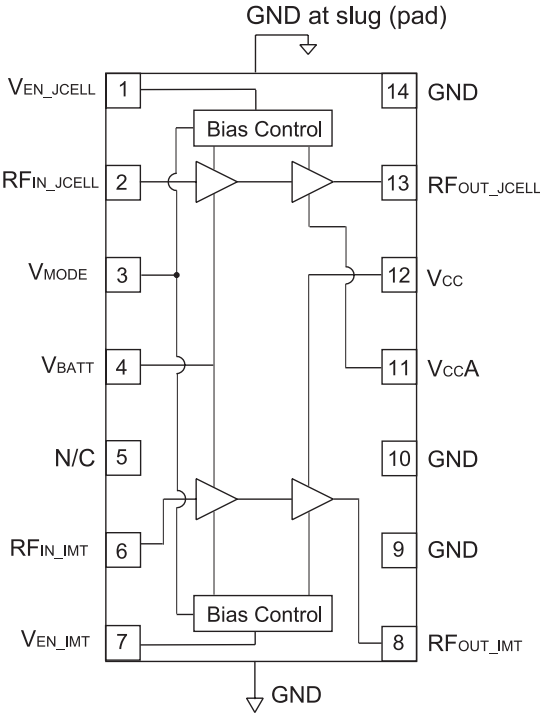


Figure 1: Block Diagram

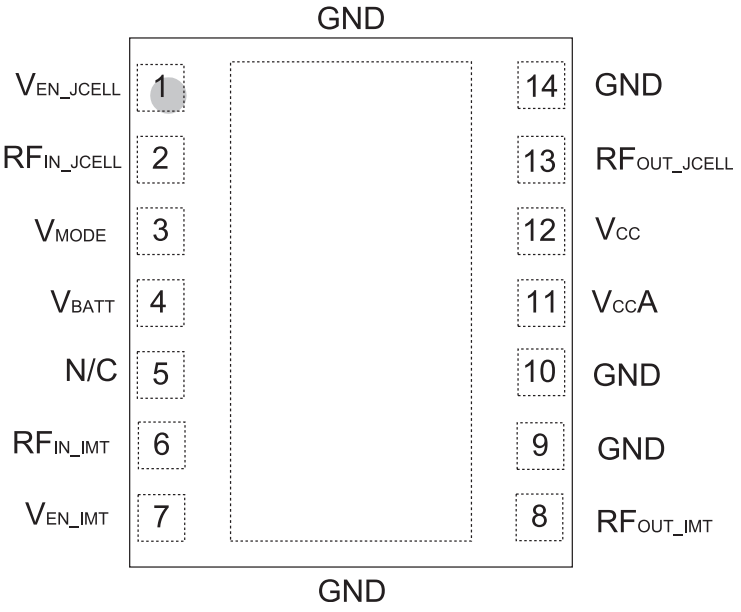


Figure 2: Pinout

Table 1: Pin Description

PIN	NAME	DESCRIPTION
1	V_{EN_JCELL}	Enable Voltage for JCell Band
2	RF_{IN_JCELL}	RF Input for JCell Band
3	V_{MODE}	Mode Control Voltage
4	V_{BATT}	Battery Voltage
5	N/C	No Connection
6	RF_{IN_IMT}	RF Input for IMT Band
7	V_{EN_IMT}	Enable Voltage for IMT Band
8	RF_{OUT_IMT}	RF Output for IMT Band
9	GND	Ground
10	GND	Ground
11	$V_{CC}A$	Battery Voltage A
12	V_{CC}	Supply Voltage
13	RF_{OUT_JCELL}	RF Output for JCell Band
14	GND	Ground

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Supply Voltage (V_{BATT}, V_{CC}, $V_{CC}A$)	0	+5	V
Mode Control Voltage (V_{MODE1})	0	+3.5	V
Enable Voltage (V_{EN_CELL}, V_{EN_PCS})	0	+3.5	V
RF Input Power (P_{IN})	-	+10	dBm
Storage Temperature (T_{STG})	-40	+150	°C

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (f)	898 1920	-	925 1940	MHz	Japan Cellular IMT
Supply Voltage (V_{CC} and V_{BATT})	+3.2	+3.4	+4.2	V	
Enable Voltage (V_{EN})	+2.2 0	+2.4 -	+3.1 +0.5	V	PA "on" PA "shut down"
Mode Control Voltage (V_{MODE})	+2.2 0	+2.4 -	+3.1 +0.5	V	Low Bias Mode High Bias Mode
Japan Cellular RF Output Power (P_{OUT}) IS-95 CDMA 2000	 +27.5 (1) +27.0 (1)	 +28.0 +27.5	 - -	dBm	
PCS RF Output Power (P_{OUT}) IS-95 CDMA 2000	 +27.5 (1) +27.0 (1)	 +28.0 +27.5	 - -	dBm	
Case Temperature (T_C)	-30	-	+85	°C	

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Notes:
(1) For operation at V_{CC} = +3.2 V, P_{OUT} is derated by 0.5 dB.

Table 4: Electrical Specifications - Japan Cellular Band
(T_C = +25 °C, V_{BATT} = V_{CC} = +3.4 V, V_{ENABLE} = +2.4 V, 50 Ω system)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS	
					P_{OUT}	V_{MODE}
Gain	25.5 13	28 15	30.5 18	dB	+28 dBm +15 dBm	0 V 2.4 V
Adjacent Channel Power at ± 885 kHz offset (1) Primary Channel BW = 1.23 MHz Adjacent Channel BW = 20 kHz	 - -	 -50 -51	 -47 -47	dBc	P_{OUT} = +28 dBm, V_{MODE} = 0 V $P_{OUT} \leq$ +15 dBm, V_{MODE} = +2.4 V	
Adjacent Channel Power at ± 1.98 MHz offset (1) Primary Channel BW = 1.23 MHz Adjacent Channel BW = 30 kHz	 - -	 -63 -59	 -57 -56	dBc	P_{OUT} =+28 dBm, V_{MODE}=0 V $P_{OUT} \leq$+15 dBm, V_{MODE}=+2.4 V	
Power-Added Efficiency (1)	35 18	38 21	- -	%	+28 dBm +15 dBm	0 V 2.4 V
Quiescent Current (Icq)	-	8	13	mA	V_{MODE} = +2.4 V	
Mode Control Current	-	0.35	0.8	mA	through V_{MODE} pin, V_{MODE} = +2.4 V	
Enable Current	-	0.5	0.8	mA	through V_{ENABLE} pin	
BATT Current	-	3.0	5	mA	through V_{BATT} pin, V_{MODE} = +2.4 V	
Leakage Current	-	<1	5	µA	V_{BATT} = +4.2 V, V_{CC} = +4.2 V, V_{ENABLE} = 0 V, V_{MODE} = 0 V	
Noise in Receive Band (2)	- -	-134 -140	- -	dBm/Hz	P_{OUT} = +28 dBm, V_{MODE} = 0 V, V P_{OUT} = +15 dBm, V_{MODE} = +2.4 V	
Harmonics 2fo 3fo, 4fo	 - -	 -41 -45	 -30 -35	dBc	$P_{OUT} \leq$ +28 dBm	
Input Impedance	-	-	2:1	VSWR		
Spurious Output Level (all spurious outputs)	-	-	-70	dBc	See Note 3	
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating range	

Notes:
(1) ACLR and Efficiency measured at 911.5 MHz.
(2) 843 MHz to 870 MHz.
(3) POUT < +28 dBm, In-band load VSWR < 5:1, Out-of-band load VSWR < 10:1. Applies over all operating conditions.

Table 5: Electrical Specifications - IMT Band
(T_C = +25 °C, V_{BATT} = V_{CC} = +3.4 V, V_{ENABLE} = +2.4 V, 50 Ω system)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS	
					P_{OUT}	V_{MODE}
Gain	25 12	27.5 14.0	29.5 17	dB	+28 dBm +15 dBm	0 V 2.4 V
Adjacent Channel Power at ±1.25 MHz offset Primary Channel BW - 1.23 MHz Adjacent Channel BW = 30 kHz	 - -	 -50 -57	 -47 -47	dBc	P_{OUT} =+28.0 dBm, V_{MODE} = 0 V P_{OUT} ≤ +15 dBm, V_{MODE} = +2.4 V	
Adjacent Channel Power at +1.98 MHz Primary Channel BW=1.23 MHz Adjacent Channel BW=30 kHz	 - -	 -57 -64	 -53 -57	dBc	P_{OUT} =+28.0 dBm, V_{MODE} = 0 V P_{OUT} ≤ 15 dBm, V_{MODE} = +2.4 V	
Adjacent Channel Power at ±2.25 MHz offset Primary Channel BW = 1.23 MHz Adjacent Channel BW = 30 kHz	 - -	 -61 -64	 -57 -57	dBc	P_{OUT}=+28.0 dBm, V_{MODE} = 0 V P_{OUT}≤ +15 dBm, V_{MODE} =+2.4 V	
Power-Added Efficiency (1)	35 17	38 20	- -	%	P_{OUT}=+28 dBm,V_{MODE} = 0 V P_{OUT} =+15 dBm, V_{MODE} =+2.4 V	
Quiescent Current (Icq) Low Bias Mode	-	8	13	mA	V_{MODE} = +2.4 V	
Mode Control Current	-	0.35	0.8	mA	through V_{MODE} pins, V_{MODE} = +2.4 V	
Enable Current	-	0.35	0.8	mA	through V_{ENABLE} pin	
BATT Current	-	3	5	mA	through V_{BATT} pin, V_{MODE} = 2.4 V	
Leakage Current	-	<1	5	µA	V_{BATT} = +4.2 V, V_{CC} = +4.2 V, V_{ENABLE} = 0 V, V_{MODE} = 0 V	
Noise in Receive Band (2)	- -	-137 140	- -	dBm/Hz	P_{OUT} = +28 dBm, V_{MODE} = 0 V P_{OUT} = +15 dBm, V_{MODE} = 2.4 V	
Harmonics 2fo 3fo, 4fo	 - -	 -38 -42	 -30 -35	dBc		
Input Impedance	-	-	2:1	VSWR		
Spurious Output Level (all spurious outputs)	-	-	-70	dBc	See Note 3	
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating range	

Notes:
(1) ACLR and Efficiency measured at 1930 MHz.
(2) 2110 MHz to 2130 MHz.
(3) P_{OUT} < +28 dBm, In-Band VSWR < 5:1, Out-Of-Band VSWR < 10:1. Applies to all operating conditions.

APPLICATION INFORMATION

To ensure proper performance, refer to all related Application Notes on the ANADIGICS web site: http://www.anadigics.com

Shutdown Mode

The power amplifier may be placed in a shutdown mode by applying logic low levels (see Operating Ranges table) to the V_{ENABLE} and V_{MODE} voltages.

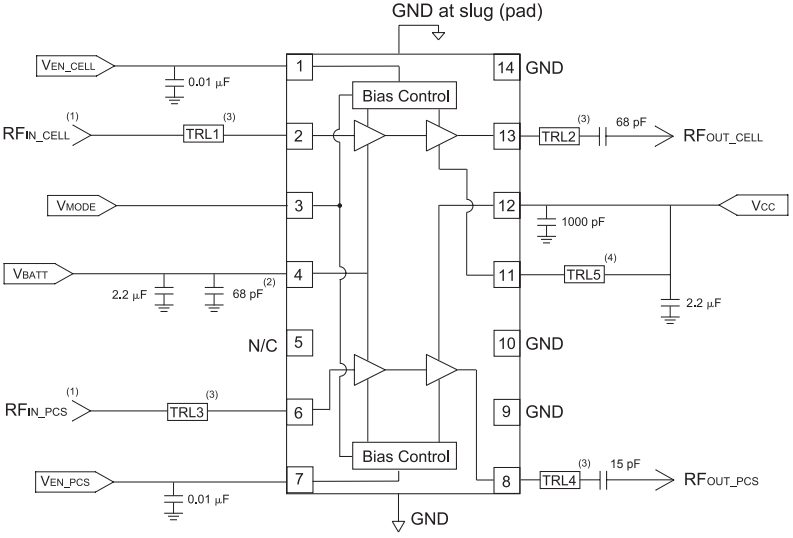
Bias Modes

The power amplifier may be placed in either a Low Bias mode or a High Bias mode by applying the appropriate logic level (see Operating Ranges table) to V_{MODE}. The Bias Control table lists the recommended modes of operation for various applications. V_{MODE2} is not necessary for this PA.

Two operating modes are available to optimize current consumption. High Bias/High Power operating mode is for P_{OUT} levels > 16 dBm. At around 15 dBm output power, the PA should be "Mode Switched" to Medium/Low power mode for lowest quiescent current consumption.

Table 6: Bias Control

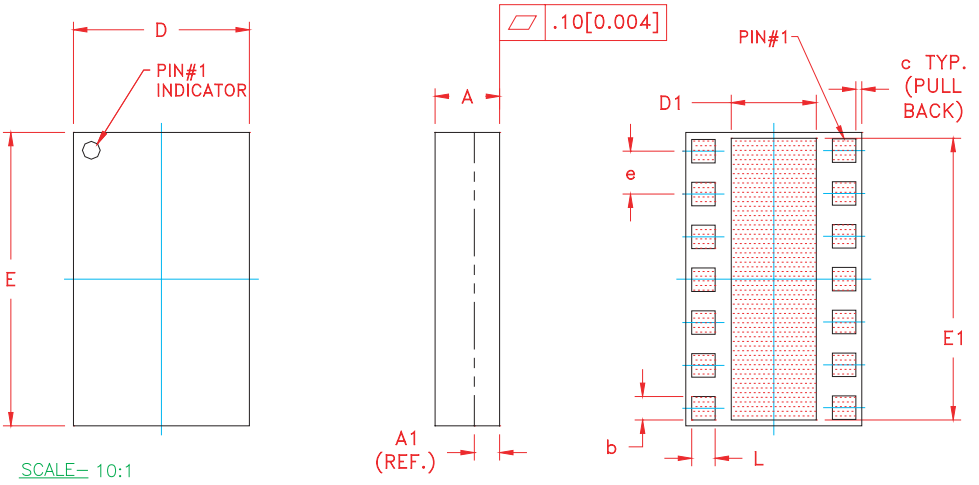
APPLICATION	P_{OUT} LEVELS	BIAS MODE	V_{ENABLE}	V_{MODE}	V_{CC}	V_{BATT}
CDMA - high power	> +15 dBm	High	+2.4 V	0 V	3.2 - 4.2 V	≥ 3.2 V
CDMA - low power	≤ +15 dBm	Low	+2.4 V	+2.4 V	3.2 - 4.2 V	≥ 3.2 V
Optional lower V_{CC} in low power mode	≤ +6 dBm	Low	+2.4 V	+2.4 V	1.5 V	≥ 3.2 V
Shutdown	-	Shutdown	0 V	0 V	3.2 - 4.2 V	≥ 3.2 V



Note:
(1) Add blocking cap if DC voltage is present on input pin.
(2) 68 pF cap should be placed as close as possible to Pin 4.
(3) TRL should be short and of 50 Ω characteristic impedance.
(4) TRL 5 should be as long as possible (minimum of 0.1 λ at 800 MHz) and capable of handling 750 mA current. Optional 4.7 nH Inductor may be substituted.

Figure 3: Application Circuit

PACKAGE OUTLINE



SYMBOL	MILLIMETERS			INCHES			NOTE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.90	1.00	1.10	0.035	0.039	0.043	–
A1	0.35 (REF.)			0.014 (REF.)			–
b	0.37	–	0.57	0.015	–	0.022	3
c	–	0.10	–	–	0.004	–	–
D	2.88	3.00	3.12	0.113	0.118	0.123	–
D1	1.58	–	1.83	0.062	–	0.072	3
E	4.88	5.00	5.12	0.192	0.197	0.202	–
E1	4.75	–	4.85	0.187	–	0.190	3
e	–	0.73	–	–	0.029	–	4
L	0.33	–	0.52	0.013	–	0.020	3

NOTES:

1. CONTROLLING DIMENSIONS: MILLIMETERS
2. UNLESS SPECIFIED TOLERANCE=±0.076[0.003].
3. PADS (INCLUDING CENTER) SHOWN UNIFORM SIZE FOR REFERENCE ONLY. ACTUAL PAD SIZE AND LOCATION WILL VARY WITHIN MIN. AND MAX. DIMENSIONS ACCORDING TO SPECIFIC LAMINATE DESIGN.
4. PITCH MEASUREMENT (e) TAKEN CENTERLINE TO CENTERLINE OF SOLDER MASK OPENINGS.
5. UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.

Figure 4: Package Outline - 14 Pin 3 mm x 5 mm x 1 mm Surface Mount Module

NOTES:

1. ANADIGICS LOGO SIZE: NONE
2. PART NUMBER: FOUR DIGIT NUMERICAL
3. WAFER LOT NUMBER: LLLL = LOT NUMBER
   NN = WAFER I.D.
4. PIN 1 INDICATOR: LASER DOT
5. B.O.M. # BBBB
6. COUNTRY CODE: CC = TH–for–THAILAND, TW–for–TAIWAN
   CC = PH–for–PHILIPPINES, CH–for–CHINA
7. TYPE : ARIAL
   SIZE : 1.5–POINT
   COLOR : LASER

Figure 5: Branding Specification

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
AWC6313RM28Q7	-30 °C to +85 °C	RoHS Compliant 14 Pin 3 mm x 5 mm x 1 mm Surface Mount Module	Tape and Reel, 2500 pieces per Reel
AWC6313RM28P9	-30 °C to +85 °C	RoHS Compliant 14 Pin 3 mm x 5 mm x 1 mm Surface Mount Module	Partial Tape and Reel

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