ABRIDGED VERSION

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SSI 33P3733A
8-26.5 Mbit/s Read Channel w/Pit Mark Pulse Qualifier

February 1996

DESCRIPTION

The SSI 33P3733A device is a high performance BiCMOS single chip read channel IC that contains all the functions needed to implement a complete zoned recording read channel for magneto-optical (MO) drive systems. Functional blocks include the pulse detector, programmable filter, time base generator, and data synchronizer. MO data rates from 8 to 26.5 Mbit/s for (1,7) code, 6 to 20 Mbit/s for (2,7) code can be programmed using an internal DAC whose reference current is set by a single external resistor.

Programmable functions of the SSI 33P3733A device are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The SSI 33P3733A utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption.

FEATURES

- **Programmable MO data rate of 8 to 26.5 Mbit/s for (1,7) code, 6 to 20 Mbit/s for (2,7) code, internal DAC controlled**
- **Complete zoned recording application support**
- **Low-power operation (375 mW typical @ 5V)**
- **Bi-directional serial port for register access**
- **Register programmable power management (sleep mode <5 mW)**
- **Power supply range (4.5 to 5.5 volts)**
- **Small footprint 64-lead TQFP package**

PULSE DETECTOR

- **Fast attack/decay modes for rapid AGC *recovery***
- **Dual rate charge pump for fast transient recovery**
- **Low Drift AGC hold circuitry**
- **Temperature compensated, exponential control AGC**
- **Wide bandwidth, high precision full-wave rectifier**
- **Programmable LEVEL pin time constant with separate MO data and emboss registers**
- **Separate MO data and emboss AGC levels (4-bit DAC)**
- **Pulse qualification circuitry is provided for Pit Mark detection**
- **Internal fast decay timing**
- **External $\overline{LOW\_Z}$ control pin**
- **0.5 ns max. pulse pairing with sine wave input**

PROGRAMMABLE FILTER

- **Programmable cutoff frequency of 4 to 12 MHz**
- **Programmable boost/equalization of 0 to 13 dB**
- **Matched normal and differentiated outputs**
- **± 15% *fc* accuracy**
- **± 3% maximum group delay variation**
- **Less than 1.5% total harmonic distortion**
- ***Low-Z input switch controlled by $\overline{LOW\_Z}$ pin***
- **No external filter components required**

TIME BASE GENERATOR

- **Better than 1% frequency resolution**
- ***Up to 75 MHz frequency output***
- **Independent divide-by M and N registers**
- **VCO center frequency matched to data synchronizer VCO**
- **VCO (FOUT) output available independent of the mode**

DATA SEPARATOR

- **Fast acquisition phase lock loop with zero *phase restart technique***
- **Fully integrated data separator**
  - **No external delay lines, active devices, or active PLL components required**
- **Programmable decode window symmetry control via serial port**
  - **Window shift control ± 30% (4-bit)**
  - **Includes delayed read MO data and VCO *clock monitor points***

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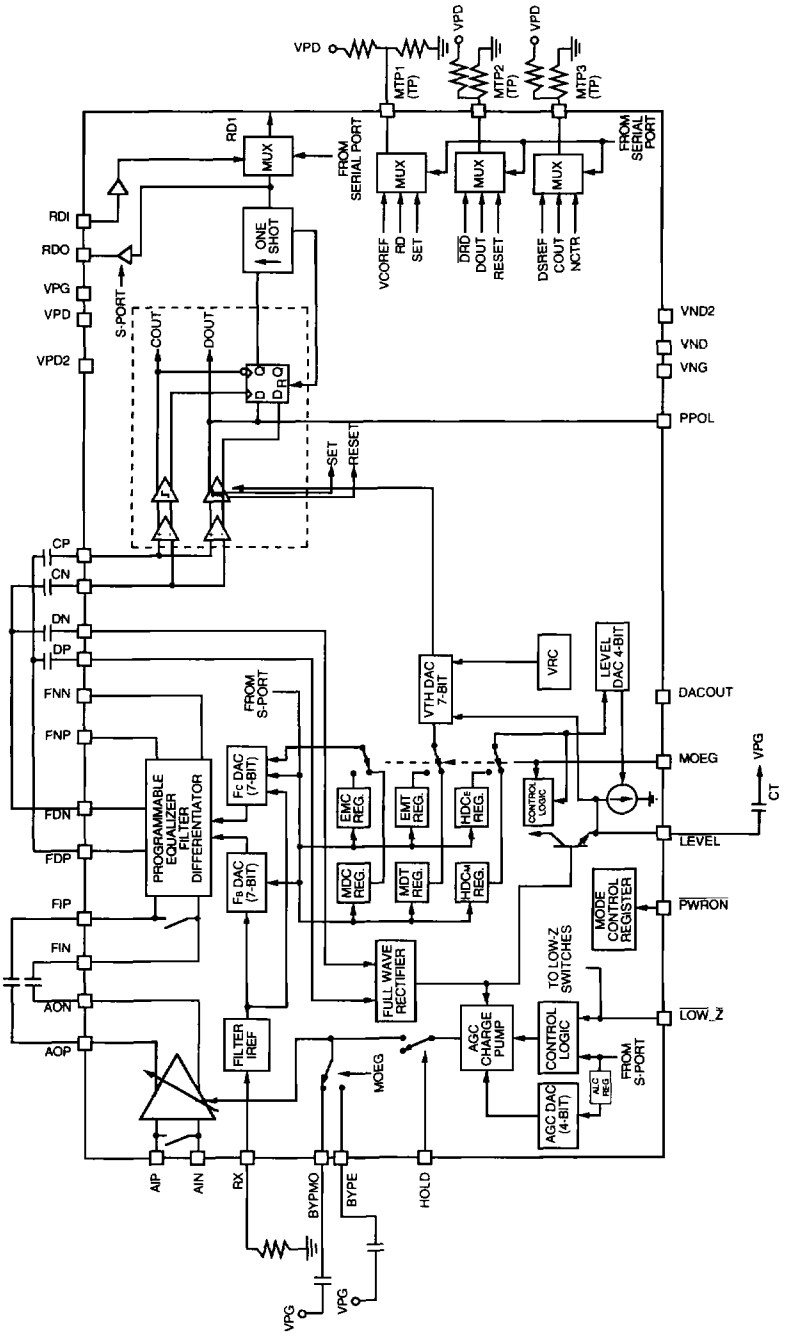

FIGURE 1A: Block Diagram, Front End

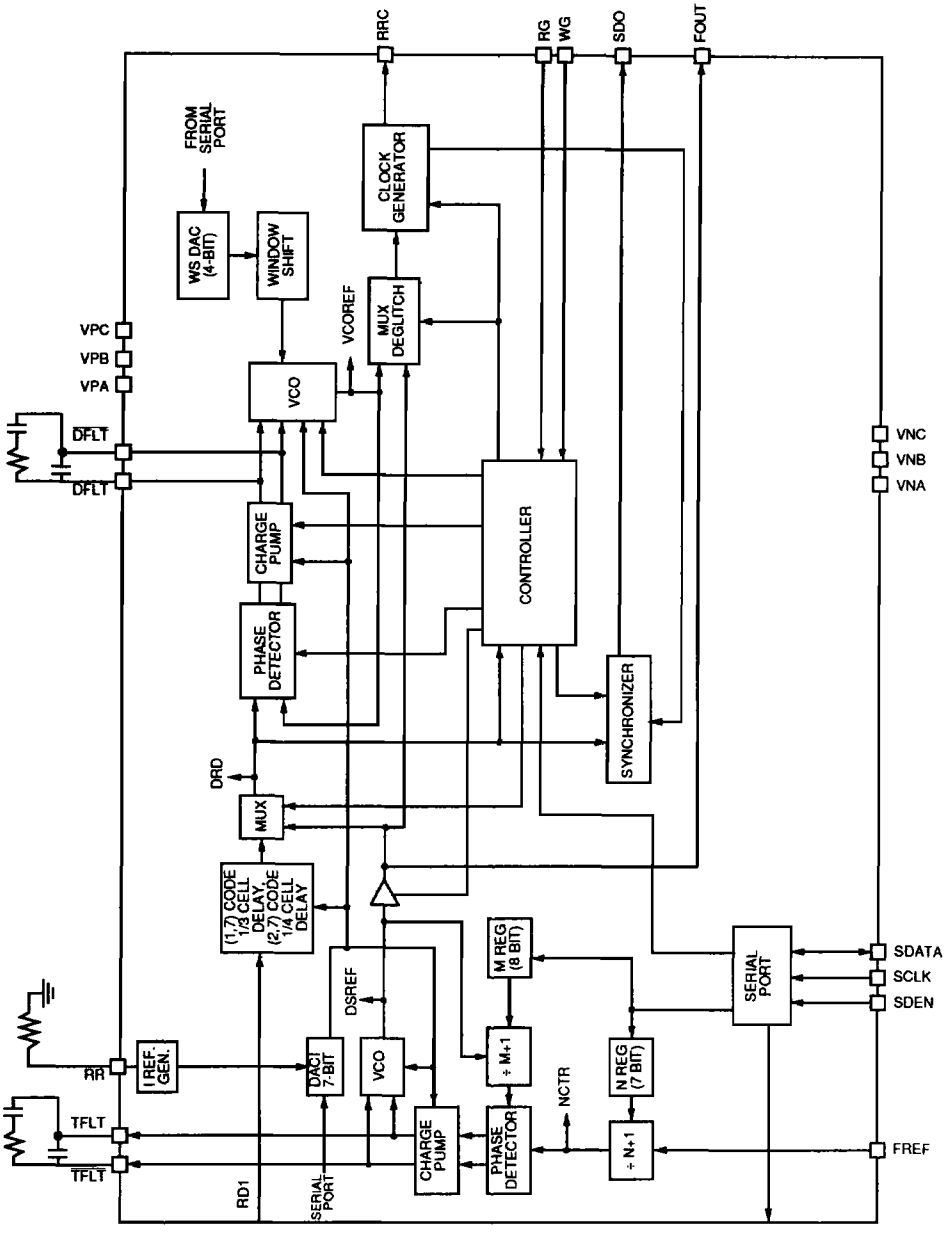

FIGURE 1B: Block Diagram, Back End

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FUNCTIONAL DESCRIPTION

The SSI 33P3733A implements a high performance complete read channel, including pulse detector, programmable active filter, time base generator, and data synchronizer, at MO data rates up to 26.5 Mbit/s for (1,7) code, 20 Mbit/s for (2,7) code. A circuit block diagram is shown in Figure 1.

PULSE DETECTOR CIRCUIT DESCRIPTION

The pulse detector, in conjunction with the programmable filter, provides all the MO data processing functions necessary for detection and qualification of encoded read signals. The signal processing circuits include a wide bandwidth variable gain amplifier, a precision wide bandwidth fullwave rectifier, and a dual rate charge pump. The entire signal path is fully-differential to minimize external noise pick up.

AGC CIRCUIT

The gain of the AGC amplifier is controlled by the voltage (V_{BYPx}) stored on the BYPx hold capacitor (C_{BYPx}). A dual rate charge pump drives C_{BYPx} with currents that depend on the instantaneous differential voltage at the DP/DN pins. Attack currents lower V_{BYPx} which reduces the amplifier gain, while decay currents increase V_{BYPx} which increases the amplifier gain. When the signal at DP/DN is greater than 100% of the programmed AGC level, the nominal attack current of approximately 0.17 mA is used to reduce the amplifier gain. If the signal is greater than 125% of the programmed AGC level, a fast attack current of eight (8) times nominal is used to reduce the gain. This dual rate approach allows AGC gain to be quickly decreased when it is too high/low yet minimizes distortion when the proper AGC level has been acquired.

A constant decay current of approximately 4 µA acts to increases the amplifier gain when the signal at DP/DN is less than the programmed AGC level. The large ratio (0.17 mA:4 µA) of the nominal attack and nominal decay currents enable the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. A fast decay Current mode is provided to allow the AGC gain to be rapidly increased, if required. In fast decay mode, the decay current is increased by a factor of 21.

In read mode and write mode, the reference voltage for the AGC charge pump is a nominal 1.0V. When MOEG is high, the reference voltage for the AGC charge pump is set by a 4-bit AGC level DAC (DACA) controlled by the serial port. The DAC output voltage is offset so that "1111" results in a 0.78V output, and "0000" results in a 1.00V output:

$$V_{AGC} = 1.00 - (DACA \times 0.01467)\ Vpp$$

where DACA is the decimal value of the AGC level control register (ALCR).

When the chip is in power down mode, the AGC dual rate charge pump is disabled.

Upon power up, the Low-Z/fast decay sequence should be executed to rapidly recover from any transients or drift which may have occurred on the BYPx hold capacitors.

BYPMO AND BYPE CONTROL VOLTAGE

The BYPMO capacitor voltage will be held constant (subject to leakage currents) during sleep mode, emboss mode (MOEG = high), write mode, LOW_Z mode, or when the HOLD signal is high. Upon the transition of $\overline{PWRON}$ from high to low, there is a 1 µs delay inserted before the AGC loop is allowed to drive the BYPMO capacitor. When MOEG is high, the charge pump drives the BYPE capacitor. When MOEG is low, the BYPE capacitor voltage will be held constant (subject to leakage currents). When MOEG is high, the BYPMO capacitor voltage will be held contstant (subject to leakage currents).

AGC MODE CONTROL

When write gate ($\overline{WG}$) is driven low, the dual rate charge pump is disabled causing the AGC amplifier gain to be held constant. When the $\overline{WG}$ pin transitions from low to high, the LOW_Z mode can be entered using the $\overline{LOW\_Z}$ control pin. When this pin is brought low, the input impedance at both the AGC amplifier and the programmable filter are reduced to allow for quick recovery of the AC coupling capacitors. When the $\overline{LOW\_Z}$ pin goes high, the fast decay mode is triggered on BYPMO if in idle or read mode, or on BYPE if in emboss mode, allowing rapid acquisition of the proper AGC level. The duration of the fast decay mode is internally set at a nominal 1 µs. fast decay mode is also triggered by a transition of the MO/emboss gate (MOEG) pin as follows: when MOEG goes low, fast decay mode is initiated on BYPMO, when MOEG goes high, fast decay mode is initiated on BYPE. When the pulse detector is powered-down, V_{BYPx} will be held constant subject to leakage currents only.

AGC MODE CONTROL (continued)

External control for enabling the dual rate charge pump is also provided. Driving the HOLD pin high forces the dual rate charge pump output current to zero. In this mode, V_{BYPX} will be held constant subject to leakage currents only.

RDO OUTPUT PIN

A CMOS compatible, 5 ns wide (min), Raw Data Output (RDO) signal is provided. This pin is controlled by CBR bit 0 (RDO register bit). When CBR bit 0 goes high, RDO will be held High-Z. The rising edge of RDO indicates the presence of a valid read data pulse.

RDI INPUT PIN

A TTL compatible pin read data input (RDI) is provided as a read data input to the data synchronizer from an external qualification circuit. RDI is available when CBR bit 2 (RDI register bit) goes high.

HYSTERESIS COMPARATOR QUALIFICATION

The SSI 33P3733A provides a hysteresis comparator pulse qualification circuit for Pit Mark detection. This circuit uses only the differentiated signal for qualification. The differentiated signal is connected to both the hysteresis and zero cross comparators. A positive peak that clears the established threshold level will set the hysteresis comparator. A peak of the opposite polarity must clear the negative threshold level to reset the hysteresis comparator. A differential comparator with programmable hysteresis threshold allows differential signal qualification for noise rejection. The floating hysteresis threshold, V_{TH}, is driven by a multiplying DAC which is driven by LEVEL and referenced to VRC (internal reference voltage, VCC-2.4V). Hysteresis threshold from 10 to 80% may be set with a resolution of 1%. The internal current sink LEVEL DAC (DACL) and external capacitor CT set the hysteresis time constant. DACL is switched between two 4-bit registers by MO/emboss gate (MOEG) to determine the sink current magnitude in MO and emboss mode. In MO mode, the four LSBs of the Hysteresis Decay Register (HDCR) determine the value of the pull down current. In emboss mode, the four MSBs are selected. The LSB value of DACL is 3.0 µA, and DACL is offset by LSB such that "0000" corresponds to 3.0 µA, and "1111" results in 48 µA. A positive edge of the hysteresis comparator output is connected to the D-input of the D-Flip-Flop which is triggered by the negative edge of the zero cross comparator output. This output triggers the one-shot. Timing for the hysteresis comparator is shown in Figure 2.

PROGRAMMABLE FILTER CIRCUIT DESCRIPTION

The SSI 33P3733A programmable filter consists of an electronically controlled low-pass filter with a separate differentiated low-pass output. A seven-pole, low-pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. Programmable bandwidth and boost/equalization is provided by internal 7-bit control DACs. The programmable characteristics are automatically switched during emboss mode to improve signal to noise ratio. Differentiation pulse slimming equalization is accomplished by a two-pole,

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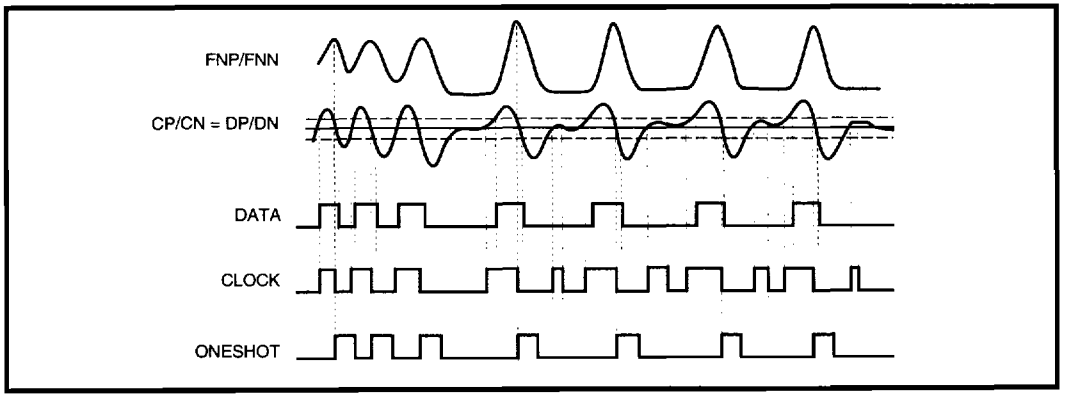


FIGURE 2: Hysteresis Comparator Timing Diagram

PROGRAMMABLE FILTER CIRCUIT DESCRIPTION (continued)

low-pass with a two-pole, high-pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The filter implements a 0.05 degree equiripple linear phase response. The normalized transfer functions (i.e., Wc = 2 πfc = 1) are:

Vnorm/Vi = [(-Ks2 + 17.98016)/D(s)] x A_N

and

Vdiff/Vi = (Vnorm/Vi) x (s/0.86133) x A_D

where D (s)=

$(S^2 + 1.68495s + 1.31703)(S^2 + 1.54203s + 2.95139)(S^2 + 1.14558s + 5.37034)(s + 0.86133)$,

A_N and A_D are adjusted for a gain of 2 at fs = (2/3)fc.

FILTER OPERATION

AC coupled differential signals from the AGC are applied to the FIP/FIN inputs of the filter. To improve settling time of the coupling capacitors, the FIP/FIN inputs are placed into a Low-Z state when the $\overline{LOW\_Z}$ pin is brought low. The programmable bandwidth and boost/equalization features are controlled by internal DACs and the registers programmed through the serial port. The current reference for both DACs is set using a single 12.1 kΩ external resistor connected from pin RX to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current.

BANDWIDTH CONTROL

The programmable bandwidth is set by the filter cutoff DAC. This DAC has two separate 7-bit registers that can program the DAC value as follows:

fc = (0.097 x FC DAC) -0.381 (MHz)
where FCDAC = MDCR or EMCR value

In the MO data mode, the MO Data Cutoff Register (MDCR) is used to determine the filter's 3 dB cutoff frequency. In the emboss mode, the emboss Mode Cutoff Register (EMCR) is used. Switching of the registers is controlled by the MO/emboss gate (MOEG) pin. The filter cutoff set by the internal DAC is the unboosted 3 dB frequency. When boost/equalization is added, the actual 3 dB point will move out. Table 1 provides information on boost verses 3 dB frequency.

TABLE 1: 3 dB Cutoff Frequency vs Boost Magnitude

BOOST (dB)	fc (3 dB)	BOOST (dB)	fc (3 dB)
0	1.00	7	2.42
1	1.21	8	2.51
2	1.50	9	2.59
3	1.80	10	2.66
4	2.04	11	2.73
5	2.20	12	2.80
6	2.32	13	2.86

BOOST/EQUALIZATION CONTROL

The programmable equalization is also controlled by an internal DAC. The 7-bit Filter Boost Control Register (FBCR) determines the amount of equalization that will be added to the 3 dB cutoff frequency, as follows:

Boost = 20 log[(0.02583 x FBDAC) + (5.4×10^{-5} x FBDAC x FC DAC) + 1] (dB)
where FBDAC = FBCR value

For example, with the DAC set for maximum output (FBCR = 7 Fh or 127) there will be 13 dB of boost added at the 3 dB frequency. This will result in +10 dB of signal boost above the 0 dB baseline. When MOEG is active the boost can be disabled by setting bit 7 in Control A register (CAR). When bit 7 is "0" and MOEG is active the boost will automatically be set to 0 dB. If bit 7 is "1" the boost will remain at its programmed value regardless of the state of MOEG.

TIME BASE GENERATOR CIRCUIT DESCRIPTION

The time base generator, which is a PLL based circuit, provides a programmable frequency reference for constant density recording applications. The frequency can be programmed with an accuracy better than 1%. An external passive loop filter is required to control the PLL locking characteristics. The filter is fully-differential and balanced in order to suppress common mode noise generated, for example, from the data synchronizer's PLL.

TIME BASE GENERATOR CIRCUIT DESCRIPTION (continued)

In read, write and idle modes, the time base generator is programmed to provide a stable reference frequency for the data synchronizer. In read mode the internal reference clock is disabled after the data synchronizer has achieved lock and switched over to read MO data as the source for the RRC. This minimizes jitter in the data synchronizer PLL. The reference frequency is programmed using the M and N registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

Reference Frequency = ((M+1)/(N+1))FREF

The VCO center frequency and the phase detector gain of the time base generator are controlled by an internal DAC addressed through the MO data recovery control register (DRCR). This DAC also sets the 1/3 cell delay for (1,7) code or 1/4 cell delay for (2,7) code, VCO center frequency, and phase detector gain for the data synchronizer circuitry. When changing frequencies, the M and N registers must be loaded first, followed by the DRCR register. A frequency change is initiated only when the DRCR register has been changed.

$$Fvco = [12.5/(RR + 0.4)] \times [(0.622 \times DACI) + 4.27] \text{ MHz};$$

for Fvco < 24 MHz

$$Fvco = [12.5/(RR + 0.4)] \times [(0.7 \times DACI) + 1.4] \text{ MHz}$$

Where DACI is the value in the DRCR and RR is the value (kΩ) of the external RR resistor, typically 12.1 kΩ.

DATA SYNCHRONIZER CIRCUIT DESCRIPTION

In the read mode, the data synchronizer performs sync field search and data synchronization. Data rate is established by the time base generator and the internal reference DACI controlled by the DRCR. The DAC generates a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 or 1/4 cell delay.

PHASE LOCKED LOOP

The circuit employs a dual mode phase detector; harmonic in the read mode and non-harmonic in idle mode. In the read mode the harmonic phase detector updates the PLL with each occurrence of a $\overline{DRD}$ pulse. In idle mode the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock onto the reference frequency of the internal time base generator. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, the VCO transient is minimized and false lock to DLYD DATA is eliminated. The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The data synchronizer also requires an external passive loop filter to control its PLL locking characteristics. The filter is again fully-differential and balanced in order to suppress common mode noise which may be generated from the time base generator's PLL.

MODE CONTROL

The read gate (RG) and write gate ($\overline{WG}$) inputs control the Device Operating mode. RG is an asynchronous input and may be initiated or terminated at any position on the disk. $\overline{WG}$ is also an asynchronous input. See Table 2.

READ MODE

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read gate (RG) initiates the PLL locking sequence and selects the PLL reference input; a high level (read mode) selects the internal RD input and a low level selects the reference clock. In the read mode the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of the VCO reference (VCOR). $\overline{DRD}$ is a 1/3 (for (1,7) code or 1/4 for (2,7) code) cell wide (TVCO) pulse whose leading edge is defined by the falling edge of RD. A decode window is developed from the VCOR clock.

FUNCTIONAL DESCRIPTION (continued)

PREAMBLE SEARCH

When RG is asserted, an internal counter is triggered to count positive transitions of the incoming read MO/emboss data, RD. Once the counter reaches a count of 3, the internal read gate is enabled. This switches the phase detector reference from the internal time base to the delayed read data ($\overline{DRD}$) signal. At the same time an internal zero phase restart signal restarts the VCO in phase with the $\overline{DRD}$. This prepares the VCO to be synchronized to MO/emboss data.

VCO LOCK

One of two VCO locking modes will be entered depending on the state of the gain shift (GS) bit, or bit 1, in the Control B register. If GS = "1," the phase detector will enter a gain shift mode of operation. The phase detector starts out in a high gain mode of operation to support fast phase acquisition. After an internal counter counts the first 11 transitions of the internal $\overline{DRD}$ signal, the gain is reduced by a factor of 3. This reduces the bandwidth and damping factor of the loop by $\sqrt{3}$ which provides improved jitter performance in the MO data which follows. The counter continues to count the next 5 $\overline{DRD}$ transitions (a total of 19 pulses from assertion of RG) and then asserts an internal VCO lock signal.

When the VCO lock signal is asserted, the internal RRC source is also switched from the time base generator to the VCO clock signal that is phase locked to $\overline{DRD}$. During the internal RRC switching period the external RRC signal may be held for a maximum of 2 VCO clock periods, however no short duration glitches will occur.

When the GS bit is set to "0" the phase detector gain shift function is disabled. The VCO lock sequence is identical to that of the gain shift mode explained above, except that no gain shift is made after the first 11 transitions.

WINDOW SHIFT

Shifting the phase of the VCO clock effectively shifts the relative position of the $\overline{DRD}$ pulse within the decode window. Decode window control is provided via the WS control bits of the Window Shift Control Register (WSCR). Further description of the WSCR is provided in the window shift control section.

NON-READ MODE

In the non-read modes, the PLL is locked to the reference clock. This forces the VCO to run at a frequency which is very close to that required for tracking actual MO data. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment error in this manner, the acquisition time is substantially reduced.

OPERATING MODES AND CONTROL

The SSI 33P3733A has several operating modes that support read, and power management functions. Mode selection is accomplished by controlling the read gate (RG), write gate ($\overline{WG}$), MO/emboss gate (MOEG), and $\overline{PWRON}$ pins. Additional modes are also controlled by programming the Power Down Control Register (PDCR), the Control A register (CAR), and the Control B register (CBR) via the serial port.

EXTERNAL MODE CONTROL

All operating modes of the device are controlled by driving the read gate (RG), write gate ($\overline{WG}$), MO/emboss gate (MOEG), and $\overline{PWRON}$ pins with TTL compatible signals. For normal operation the $\overline{PWRON}$ pin is driven low. During normal operation the SSI 33P3733A is controlled by the read gate (RG), write gate ($\overline{WG}$), and MO/emboss gate (MOEG) pins. When RG is high and $\overline{WG}$ is high the device is in read mode. When RG is low the device is in idle mode.

POWER DOWN CONTROL

For power management, the $\overline{\text{PWRON}}$ pin can be used in conjunction with the Power Down Control Register (PDCR) to set the operating mode of the device. The PDCR provides a control bit for each of the functional blocks. When the $\overline{\text{PWRON}}$ pin is brought high ("1") the device is placed into sleep mode (<5 mW) and all circuits are powered down except the serial port. This allows the user to program the serial port registers while still conserving power. Register information is retained during the sleep mode so it is not necessary to reprogram the serial port registers after returning to an active mode. When the $\overline{\text{PWRON}}$ pin is driven low ("0"), the contents of the PDCR determine which blocks will be active. Register mapping for the PDCR is shown in Table 3. To improve recovery time from the sleep mode, the $\overline{\text{LOW\_Z}}$ pin should be asserted following power down to initiate the AGC recovery sequence.

SERIAL INTERFACE OPERATION

The serial interface is a CMOS bi-directional port for reading and writing programming data from/to the internal registers of the SSI 33P3733A. The serial port data transfer format is shown in Figure 3. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining 7-bits determine the internal register to be accessed. Table 3 provides register mapping information. The second byte contains the programming data. In serial port read mode (R/W=1) the SSI 33P3733A will output the register contents of the selected address. In serial port write mode the device will load the selected register with data presented on the SDATA pin. At initial power-up, the contents of the internal registers will be in an unknown state and must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained. Detailed timing information is provided in Figure 4.

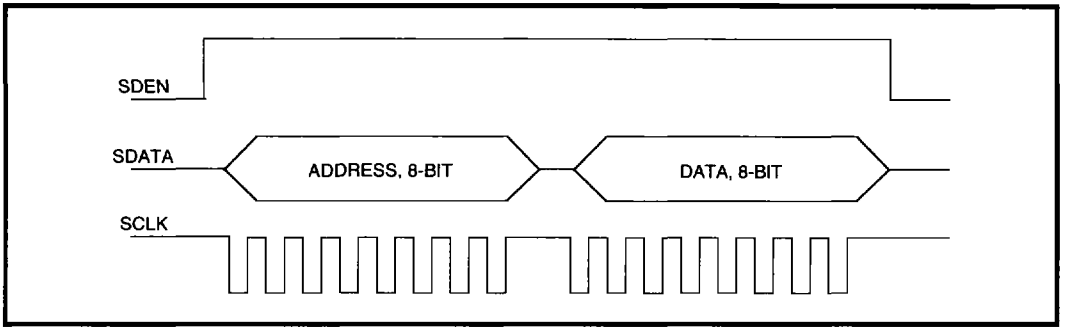


FIGURE 3: Serial Port Data Transfer Format

TABLE 2: MODE CONTROL

CONTROL LINE				DEVICE MODE	DAC CONTROL				
$\overline{PWRON}$	RG	MOEG	$\overline{WG}$		VTH	FC	BOOST	HYSTERESIS	LEVEL
1	X	X	X	**SLEEP MODE:** All functions are powered down. The serial port registers remain active and register programming data is saved.	off	off	off	off	off
0	1	0	1	**MO READ MODE:** The pulse detector is active. The data synchronizer begins the preamble lock sequence. RDO is active	MR	MR	MR	MR	MR
0	1	1	1	**EMBOSS MODE:** The pulse detector is active and the emboss control registers are enabled for the fc DAC, the VTH DAC, and the LEVEL DAC.	ER	ER	MR	ER	ER
0 (0	0 0	0 1	X X)	**IDLE MODE:** The contents of the PDCR determine which blocks are powered-up. In normal operation with all blocks powered-up, the pulse detector is active, the data synchronizer VCO is locked to the time base generator, and the MO data (emboss) control registers are used for VTH and fc.	MR (ER	MR ER	MR MR	MR ER	MR ER)
-	-	-	-	All other states are illegal. If an illegal state is programmed, the chip function will be in an indeterminable state, but no damage will occur.					

DAC Control Key: MR = MO data register, ER = emboss register, off = disabled

REGISTER NAME		A6			ADDRESS			A0	R/W	D7	DATA BIT MAP						D0
POWER DOWN CONTROL	(PDCR)	0	0	0	0	0	1	0	0	--	--	--	TBG 1=DISABLE 0=ENABLE	DATA SEP 1=DISABLE 0=ENABLE	FILTER 1=DISABLE 0=ENABLE	--	PD 1=DISABLE 0=ENABLE
MO DATA MODE CUTOFF	(MDCR)	0	0	0	0	0	1	1	0	--	F_{CM} DAC BIT 6	F_{CM} DAC BIT 5	F_{CM} DAC BIT 4	F_{CM} DAC BIT 3	F_{CM} DAC BIT 2	F_{CM} DAC BIT 1	F_{CM} DAC BIT 0
EMBOSS MODE CUTOFF	(EMCR)	0	0	1	0	0	1	1	0	--	F_{CE} DAC BIT 6	F_{CE} DAC BIT 5	F_{CE} DAC BIT 4	F_{CE} DAC BIT 3	F_{CE} DAC BIT 2	F_{CE} DAC BIT 1	F_{CE} DAC BIT 0
FILTER BOOST	(FBCR)	0	0	0	1	0	1	1	0	EMBOSS BOOST 1=ENABLE 0=DISABLE	F_B DAC BIT 6	F_B DAC BIT 5	F_B DAC BIT 4	F_B DAC BIT 3	F_B DAC BIT 2	F_B DAC BIT 1	F_B DAC BIT 0
MO DATA THRESHOLD	(MDTR)	0	0	0	1	0	1	0	0	--	T_M DAC BIT 6	T_M DAC BIT 5	T_M DAC BIT 4	T_M DAC BIT 3	T_M DAC BIT 2	T_M DAC BIT 1	T_M DAC BIT 0
EMBOSS THRESHOLD	(EMTR)	0	0	1	0	0	1	0	0	--	T_E DAC BIT 6	T_E DAC BIT 5	T_E DAC BIT 4	T_E DAC BIT 3	T_E DAC BIT 2	T_E DAC BIT 1	T_E DAC BIT 0
CONTROL A	(CAR)	0	0	1	1	0	1	0	0	Fast Decay test mode 0=ENABLE	TMS1	TMS0	TBG 1=BYPASS 0=NORMAL	MTP3 TEST POINT ENABLE	PUMP DWN 1=TP ON 0=TP OFF	PUMP UP 1=TP ON 0=TP OFF	PHASE DET 1=ENABLE 0=DISABLE
CONTROL B	(CBR)	0	0	0	1	1	0	0	0	--	MTPE 1=ENABLE 0=DISABLE	PUMP DWN 1=TP ON 0=TP OFF	PUMP UP 1=TP ON 0=TP OFF	PHASE DET 1=ENABLE 0=DISABLE	RDI 1 = RDI INPUT 0 = RDI DISABLE	GAIN SHFT 1 = ON 0 = OFF	RDO 1=RDO HI-Z 0=Enable
N COUNTER	(NCR)	0	0	0	0	1	1	0	0	--	N COUNT BIT 6	N COUNT BIT 5	N COUNT BIT 4	N COUNT BIT 3	N COUNT BIT 2	N COUNT BIT 1	N COUNT BIT 0
M COUNTER	(MCR)	0	0	0	1	1	1	0	0	M COUNT BIT 7	M COUNT BIT 6	M COUNT BIT 5	M COUNT BIT 4	M COUNT BIT 3	M COUNT BIT 2	M COUNT BIT 1	M COUNT BIT 0
DATA RECOVERY	(DRCR)	0	0	0	0	1	0	0	0	--	DACI BIT 6	DACI BIT 5	DACI BIT 4	DACI BIT 3	DACI BIT 2	DACI BIT 1	DACI BIT 0
WINDOW SHIFT	(WSCR)	0	0	0	0	1	0	1	0	TDAC 1	TDAC 0	WIN SHFT 1=ENABLE 0=DISABLE	WS DIR 1=LATE 0=EARLY	WS3*	WS2*	WS1*	WS0*
AGC LEVEL	(ALCR)	0	1	0	0	0	1	0	0	--	--	--	--	DACA BIT 3	DACA BIT 2	DACA BIT 1	DACA BIT 0
HYSTERESIS DECAY	(HDCR)	0	1	0	1	0	1	0	0	DACL EMBOSS BIT 3	DACL EMBOSS BIT 2	DACL EMBOSS BIT 1	DACL EMBOSS BIT 0	DACL MO BIT 3	DACL MO BIT 2	DACL MO BIT 1	DACL MO BIT 0

TABLE 3: Serial Port Register Mapping

FUNCTIONAL DESCRIPTION (continued)

CONTROL REGISTERS

Control registers CAR and CBR allow the user to configure the SSI 33P3733A test points for evaluation of different internal signals and also control other device functions. CAR controls functions of the pulse detector, filter, and time base generator. CBR controls test points and functions of the data separator. The bits of the CA and CB registers are defined as follows:

CONTROL REGISTER CA

BIT	NAME	FUNCTION
0	EPDT	Enable Phase Detector (Time Base Generator)
1	UT	Pump Up (TFLT sources current, $\overline{\text{TFLT}}$ sinks Current)
2	DT	Pump Down (TFLT sinks current, $\overline{\text{TFLT}}$ sources Current)
3	ET	Enable MTP3 Test Point Output
4	BYPT	Bypass Time Base Generator Circuit Function
5	TMS0	Control bit for selecting test point source (see Table 4)
6	TMS1	Control bit for selecting test point source (see Table 4)
7	FDTM	Constant fast decay current test mode

CONTROL REGISTER CB

0	-	Not Used
1	GS	Enable Phase Detector Gain Switching
2	RDI/O	RDI and RDO pins control
3	EPDD	Enable Phase Detector (Data Separator)
4	UD	Pump Up (DFLT sources current, $\overline{\text{DFLT}}$ sinks current)
5	DD	Pump Down (DFLT sinks current, $\overline{\text{DFLT}}$ sources current)
6	MTPE	Enable Test Points MTP1, 2, 3 (see Table 4)
7	-	Not used

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VPA	-	Data separator PLL analog power supply pin
VPB	-	Time base generator PLL analog power supply pin
VPC	-	Internal ECL, CMOS logic power supply pin
VPD, VPD2	-	CMOS buffer I/O digital power supply pin
VPG	-	Pulse detector, filter, analog power supply pin
VNA	-	Data separator PLL analog ground pin
VNB	-	Time base generator PLL analog ground pin
VNC	-	Internal ECL, CMOS logic ground pin
VND, VND2	-	CMOS buffer I/O digital ground pin
VNG	-	Pulse detector, filter, analog ground pin

INPUT PINS

AIP, AIN	I	AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins.
DP, DN	I	ANALOG INPUTS FOR MO DATA PATH: Differential analog inputs to full-wave rectifier.
CP, CN	I	ANALOG INPUTS FOR CLOCK PATH: Differential analog inputs to the clock comparator, and data comparators.
$\overline{\text{LOW\_Z}}$	I	LOW IMPEDANCE ENABLE: TTL compatible input pin that activates the Low-Z switches. A low level activates the switches and the falling edge of the internal LOW_Z triggers the fast decay circuit.
$\overline{\text{PWRON}}$	I	POWER ENABLE: CMOS compatible power control input. A low level TTL input enables power to circuitry according to the contents of the PDCR. A high level CMOS input shuts down all circuitry.
HOLD	I	HOLD CONTROL: TTL compatible control pin which, when pulled high, disables the AGC charge pump and holds the AGC amplifier gain at its present value.
FIP, FIN	I	FILTER SIGNAL INPUTS: The AGC output signals must be AC coupled into these pins.
FREF	I	REFERENCE FREQUENCY INPUT: Frequency reference input for the time base generator. FREF may be driven either by a direct coupled TTL signal or by an AC coupled ECL signal. Pin FREF has an internal pull down resistor.
RDI	I	READ DATA INPUT: TTL compatible input. RDI is provided as a read data input to the data synchronizer from an external qualification circuit. RDI is available when CBR bit 2 goes high. The minimum RDI input pulse width is 10 ns.

INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
RG	I	READ GATE: TTL compatible read gate input. A high level TTL input selects the RD input and enables the read mode/address detect sequences. A low level selects the FREF input.
MOEG	I	MO/emboss GATE: TTL compatible MO/emboss gate input. A high level TTL input activates the emboss mode by selecting the emboss control registers and the BYPE capacitor.
$\overline{WG}$	I	WRITE GATE: TTL compatible write gate input.

OUTPUT PINS

MTP1-3	O	MULTIPLEXED TEST POINTS: Open emitter ECL output test points. Internal test signals are routed to these test points as determined by the CAR and CBR. External resistors are required to use these pins. They should be removed during normal operation to reduce power dissipation.
SDO	O	SYNCHRONIZED READ DATA: CMOS output pin. Read MO data output when RG is high.
FDP, FDN	O	DIFFERENTIAL DIFFERENTIATED OUTPUTS: Filter differentiated outputs. These outputs are AC coupled into the CP/CN inputs and DP/DN inputs.
FNP, FNN	O	DIFFERENTIAL NORMAL OUTPUTS: Filter normal low pass output signals.
RDO	O	RAW DATA OUTPUT: CMOS output pin. The rising edge of RDO indicates the presence of a valid MO data pulse. RDO is enabled when CBR bit 0 is low. When CBR bit 0 goes high, RDO will be held High-Z.
RRC	O	READ REFERENCE CLOCK: Read clock CMOS output. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When RG goes high, RRC initially remains synchronized to the reference clock. When the Sync Bits are detected, RRC is synchronized to the read MO Data. When RG goes low, RRC is synchronized back to the reference clock.
AOP, AON	O	AGC AMPLIFIER OUTPUT: Differential AGC amplifier output pins. These outputs are AC coupled into the filter inputs (FIP/FIN).
FOUT	O	TIME BASE GENERATOR VCO OUTPUT: CMOS output pin. This clock signal is the data separator PLL reference. This output is independent of the RG and $\overline{WG}$ pins.
PPOL	O	PULSE POLARITY: Pulse polarity CMOS output pin. The output is high when the pulse being qualified is positive and it is low when the pulse being qualified is negative. PPOL is active when RG is low.

ANALOG PINS

NAME	TYPE	DESCRIPTION
BYPMO	-	The AGC read mode integration capacitor CBYPMO, is connected between BYPMO and VPG.
BYPE	-	The AGC emboss mode integration capacitor CBYPE, is connected between BYPE and VPG.
DACOUT	-	DAC VOLTAGE TEST POINT: This test point monitors the outputs of the internal DACs. The source DAC is selected by programming the two MSBs of the WSCR register (see Table 5).
TFLT, $\overline{\text{TFLT}}$	-	PLL LOOP FILTER: These pins are the connection points for the time base generator loop filter.
DFLT, $\overline{\text{DFLT}}$	-	PLL LOOP FILTER: These pins are the connection points for the data separator loop filter.
LEVEL	-	An NPN emitter output that provides a full-wave rectified signal from the DP, DN inputs. An external capacitor should be connected from LEVEL to VPG to set the hysteresis threshold time constant in conjunction with the internal current DAC, (DACL).
RR	-	REFERENCE RESISTOR INPUT: An external 12.1 kΩ, 1% resistor is connected from this pin to VNA to establish a precise internal reference current for the data separator and time base generator.
RX	-	REFERENCE RESISTOR INPUT: An external 12.1 kΩ, 1% resistor is connected from this pin to VNG to establish a precise PTAT (proportional to absolute temperature) reference current for the filter.

SERIAL PORT PINS

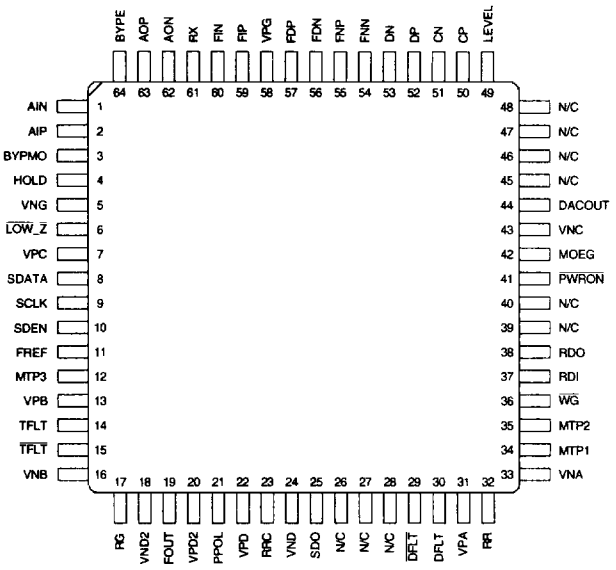
SDEN	I	SERIAL DATA ENABLE: Serial enable TTL compatible CMOS input. A high level TTL input enables the serial port.
SDATA	I/O	SERIAL DATA: Serial data TTL compatible bi-directional CMOS pin. NRZ programming data for internal registers is applied to this input when the first bit is 0. When the first bit is 1, the address register data will be clocked out on the rising edge of SCLK.
SCLK	I	SERIAL CLOCK: Serial clock TTL compatible CMOS input. The clock applied to this pin is synchronized with the data applied to SDATA.

SSI 33P3733A
8-26.5 Mbit/s Read Channel w/Pit Mark Pulse Qualifier

PACKAGE PIN DESIGNATIONS
(Top View)

Thermal Characteristics: θjA

64-lead TQFP	75° C/W



64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 33P3733A 64-Lead TQFP	33P3733A-CGT	33P3733A-CGT

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