

## RICMOS™ SOI GATE ARRAYS

## HX2000 HX2000r FAMILY

### FEATURES

- Fabricated on Honeywell's Radiation Hardened
  - 0.65  $\mu\text{m}_{\text{Leff}}$  RICMOS™ IV SOI Process, HX2000
  - 0.55  $\mu\text{m}_{\text{Leff}}$  RICMOS™ IV SOI Process, HX2000r
- Array Sizes from 40K to 390K Available Gates (Raw)
- HX2000 Supports 5V Core Operation
- HX2000r Supports 3.3V Core Operation
- HX2000r Supports Mixed Voltage I/O Buffers
- TTL (5V) or CMOS (5V/3.3V) Compatible I/O
- Configurable Multi-Port Gate Array SRAM
- Single or Dual Port Custom SRAM Drop-In Capability
- Supports Chip Level Power Down for Cold Sparring
- Supports System Speeds Beyond 100 MHz
- Total Dose Hardness  $\geq 1 \times 10^6$  rad(SiO<sub>2</sub>)
- Dose Rate Upset Hardness:
  - $\geq 1 \times 10^{10}$  rad(Si)/sec, HX2000\*
  - $\geq 1 \times 10^9$  rad(Si)/sec, HX2000r\*Option Available for:
  - $\geq 1 \times 10^{11}$  rad(Si)/sec, HX2000\*
  - $\geq 1 \times 10^{10}$  rad(Si)/sec, HX2000r\*
- Dose Rate Survivability  $\geq 1 \times 10^{12}$  rad(Si)/sec\*
- Soft Error Rate
  - $\leq 1 \times 10^{-11}$  Errors/Bit/Day, HX2000
  - $\leq 1 \times 10^{-10}$  Errors/Bit/Day, HX2000r
- Neutron Fluence Hardness to  $1 \times 10^{14}$ /cm<sup>2</sup>
- No Latchup

\*Projected

### GENERAL DESCRIPTION

The HX2000 and HX2000r gate arrays are performance oriented sea-of-transistor arrays, fabricated on Honeywell's RICMOS™ IV Silicon On Insulator (SOI) process. The HX2000 arrays are for 5V designs only. The HX2000r arrays support 5V and 3.3V operation. High density is achieved with the standard 3-layer metal or optional 4-layer metal process, providing up to 290,000 usable gates. The high density and performance characteristics of the RICMOS (Radiation Insensitive CMOS) SOI process make possible device operation beyond 100 MHz over the full military temperature range, even after exposure to ionizing radiation exceeding  $1 \times 10^6$  rad(SiO<sub>2</sub>). Flip-Flops have been designed for a Soft Error Rate (SER) of less than  $1 \times 10^{-11}$  errors/bit/day in the Adams 90% worst case environment.

Each HX2000/HX2000r design is founded on our proven RICMOS ASIC library of SSI and MSI logic elements, configurable RAM cells, and selectable I/O pads. The gate arrays feature a global clock network capable of handling multiple clock signals with low clock skew between registers. This family is fully compatible with Honeywell's high reliability screening procedures and consistent with QML Class Q and V requirements.

Designers can choose from a wide variety of I/O types. Output buffer options include 8 drive strengths, CMOS/TTL levels, IEEE 1149.1 boundary scan, pull-up/pull-down resistors, and three-state capability. Input buffers can be selected for CMOS/TTL/Schmitt trigger levels, IEEE 1149.1 boundary scan and pull-up/pull-down resistors. Bi-directional buffers are also available.

An important feature of HX2000r is the dual voltage I/O capability in which the designer has complete flexibility in terms of placement of I/O buffers. This feature allows adjacent I/O buffers with different supply voltages.

The HX2000/HX2000r families provide options for configurable multi-port SRAMs. Word widths can be selected in single bit increments. A variety of SRAM read and write port options are available to serve most applications. Custom drop-in macrocells can also be implemented to further increase chip density. Word widths can be selected in two bit increments. Single port and two port options are available.

The HX2000/HX2000r families have a special feature to allow a chip level power down mode, in which the associated buses connected to the chip can remain active. This

# HX2000/HX2000r

HX2000 Characteristics		HX2040*	HX2080	HX2160	HX2300	HX2400
Total Core Gate Count		40K	85K	160K	295K	390K
Usable Gate Count	3-Layer Metal	27K	53K	91K	156K	200K
	4-Layer Metal (1)	36K	71K	132K	226K	290K
Maximum Die I/O		132	176	240	336	372
Maximum Package I/O (2)		TBD	176	240	320	320
Typical Delay—2 Input NAND		270 ps at 5.0V, 290 ps at 3.3V				
Selectable I/O		Driver, Receiver, Bi-Directional, Three-State				
I/O Interface Levels		CMOS, TTL, Schmitt Trigger				
Typical Power Dissipation, $\mu$ W/Gate/MHz		0.6 @ 5.0V, 0.22 @ 3.3V				
Operating Voltage	HX2000	5.0V $\pm$ 10%				
	HX2000r	3.3V $\pm$ 10% (Core & I/O) and/or 5.0V $\pm$ 10% (I/O)				
Operating Temperature		-55° C to 125° C				
Process Technology		RICMOS™ IV SOI				
Minimum Geometry	HX2000	0.65 $\mu$ m $L_{eff}$ / 0.8 $\mu$ m Drawn (5V)				
	HX2000r	0.55 $\mu$ m $L_{eff}$ / 0.7 $\mu$ m Drawn (3.3V)				

(1) Projected

(2) Design and package dependent.

\* Planned Array

high impedance off-state buffer feature allows users to power down portions of their system for power savings or for cold sparing.

Logic designers need not have prior experience in radiation hardening. Honeywell's VDS™ Toolkit and RICMOS IV SOI libraries provide the necessary guidance to achieve first pass design success. The VDS Toolkit supports industry standard platforms including those offered by Mentor Graphics and Synopsys.

Honeywell can perform design translations to the HX2000 arrays from other CAD platforms. Our synthesis capabilities allow customers to use familiar CAD tools and libraries to map existing designs to Honeywell library components.

The HX2000 family of gate arrays is the right choice for your high reliability applications demanding high density and radiation performance. To learn more about Honeywell's variety of space components, call us at 612-954-2888.

**To learn more about Honeywell Solid State Electronics Center, visit our web site at <http://www.ssec.honeywell.com>**

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