MV1442

HDB3 ENCODER/DECODER/CLOCK REGENERATOR

(Supersedes June 1993 edition)

The MV1442, along with other devices in the GPS 2Mbit PCM signalling series comprise a group of circuits which will perform the common channel signalling and error detection functions for a 2.048Mbit PCM transmission link operating in accordance with the appropriate CCITT recommendations. The circuits are fabricated in CMOS and operate from a single +5V supply with all inputs and outputs being TTL compatible.

The MV1442 is an encoder/decoder for the HDB3 pseudo–ternary transmission code, described in Annex A of CCITT Recommendation G. 703. The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of the HDB3 coding, all ones detection and loss of input (all zeros detection). In addition a loop back function is provided for terminal testing. The MV1442 may be selected to function in either internal or external clock recovery modes. Internal clock recovery mode may be selected for either 1.544MHz or 2.048MHz operation and in this mode an external 16.384MHz crystal (12.352MHz for 1.544MHz Operation) is required. External clock recovery mode may be selected for 1.544MHz, 2.048MHz or 8.448MHz operation.

FEATURES

- On–chip Digital Clock Regenerator
- HDB3 Encoding and Decoding to CCITT Recommendation G.703
- Asynchronous operation
- Simultaneous Encoding and Decoding
- Clock Recovery signal allows Off–chip Clock Regeneration
- Loop Back Control
- HDB3 Error Monitor
- 'All Ones' Error Monitor
- Loss of Input Alarm
- Low Power Operation
- 2.048MHz or 1.544MHz Operation in External or Internal Clock Recovery mode
- 8.448MHz Operation in External Clock Recovery mode

ORDERING INFORMATION

MV1442/IG/DPAS DIL plastic package
MV1442/IG/DGAS DIL cerdip package
MV1442/IG/MPES Minature plastic package

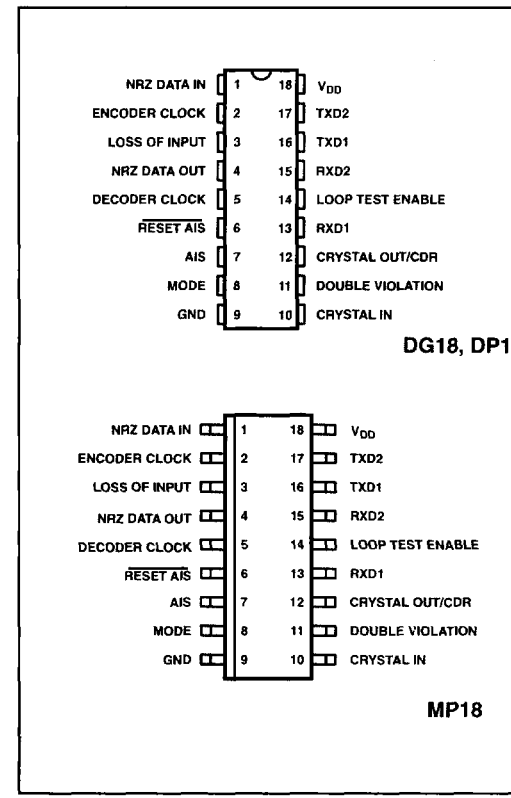

Fig. 1: Pin connections – top view

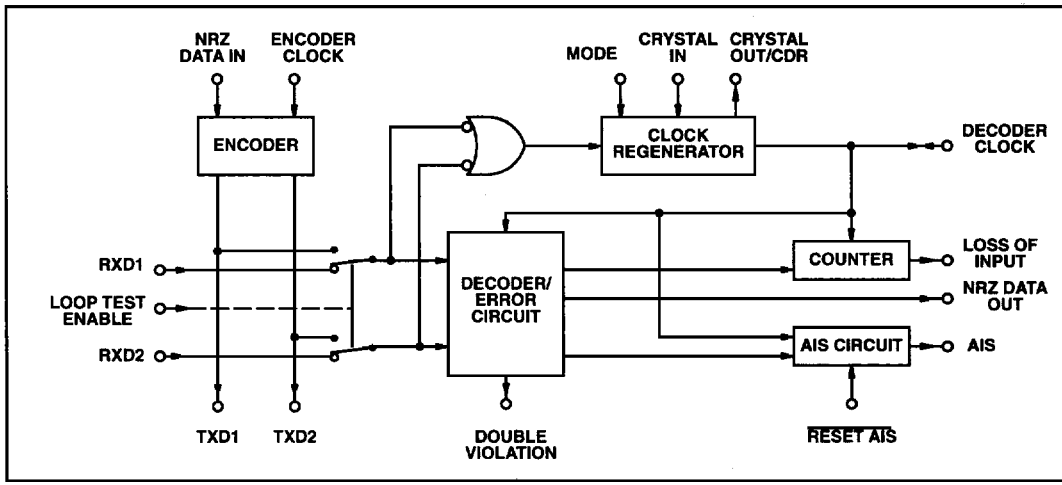

Fig. 2: Block diagram

FUNCTIONAL DESCRIPTION

High Density Bipolar 3 (HDB3) is a pseudo–ternary transmission code in which the number of consecutive zeros which may occur is restricted to three, to allow adequate clock recovery at the receiver. In any sequence of four consecutive binary zeros, the last zero is substituted by a mark of the same polarity as the previous mark, thus breaking the Alternate Mark Inversion (AMI) code. This mark is termed a violation. In addition, the first zero may also be substituted by a mark if the last mark and last violation are of the same polarity. This mark does not violate the AMI code, and ensures that successive violations alternate in polarity and as such introduce no DC component to the HDB3 signal.

The MV1442 consists of three main blocks, the HBD3 Encoder, the HDB3 Decoder and the Clock Regenerator. The function of each block is now described separately.

HDB3 ENCODER

The HDB3 Encoder is responsible for converting the incoming NRZ data into pseudo–ternary form for transmission over a PCM link. This conversion is carried out in accordance with the HDB3 coding laws specified in CCITT Recommendation G.703. The data to be encoded is input on the NRZ DATA IN pin and the encoding process is synchronised to the clock signal being input on the ENCODER CLOCK pin. The two TXD outputs, TXD1 and TXD2, represent the HDB3 data in pseudo–ternary form. If a mark is to be transmitted the output goes high after the rising edge of the clock. The length of the pulse is set by the positive clock pulse width. The timing diagram of the HDB3 Encoder is shown in Fig.3.

HDB3 DECODER

The HDB3 Decoder is responsible for decoding the HDB3 pseudo–ternary data on its inputs RXD1 and RXD2, into NRZ form to be output on the NRZ DATA OUT pin. In addition to this the decoder circuit provides three alarm outputs. The first of these alarms is DOUBLE VIOLATION. As its name suggests, a logic high on this output denotes that two successive violations have been received with the same polarity, thus violating the HDB3 coding laws. The second alarm, LOSS OF INPUT, is used to denote that 11 consecutive zeros have been received on the RXD inputs. The final alarm output is AIS (All ones). This alarm goes high if less than 3 decoded zeros have been detected in the preceding RESET AIS = 1 period (i.e. between RESET AIS = 0 pulses) and as such this alarm can be used as an all ones' detector. The decoding process and all the alarm circuitry is synchronised to the clock signal being input to this block on the DECODER CLOCK pin. This clock signal may be asynchronous with the ENCODER CLOCK signal. The timing diagrams of the HDB3 Decoder and alarm circuitry are shown in Figs. 4 to 7.

In addition to the normal mode of operation, a loop test mode is available for terminal testing. This mode is selected by taking the LOOP TEST ENABLE input high. In this mode, the HDB3 encoded pseudo–ternary data outputs of the Encoder block are fed back as the inputs to the Decoder block, which in turn decodes this data and outputs it in NRZ form.

CLOCK REGENERATOR

The Clock Regenerator block has two possible modes of operation. With the MODE pin high, internal crystal controlled clock regeneration is selected whilst with the MODE pin low, external clock regeneration is selected, using, for example, a tuned circuit.

In external clock regeneration mode, a logically 'OR'ed version of the HDB3 data, from the RXD inputs, is output to the external clock regeneration circuitry on the CRYSTAL OUT/CDR pin. The regenerated clock is then fed back into the MV1442 on the DECODER CLOCK pin. External clock regeneration may be used for operation with data rates of 1.544Mbits, 2.048Mbits or 8.448Mbits.

In internal clock regeneration mode, the logically 'OR'ed data is input to a digital regenerator, which constantly resynchronises a divide–by–8 counter to the incoming data stream. The clock thus regenerated is output to the decoder circuitry and to any external circuitry on the DECODER CLOCK pin. A crystal of frequency 8 times the required data rate must be connected between the CRYSTAL IN and CRYSTAL OUT/CDR pins. Thus the crystal frequency needs to be 16.384MHz or 12.352MHz for data rates of 2.048Mbits or 1.544Mbits respectively. Internal clock regeneration may not be used for operation at a data rate of 8.448Mbits.

The MV1442 is capable of withstanding up to 0.25UI of peak to peak input jitter at a jitter frequency of 2.048MHz without introducing errors into the decoded data. At lower jitter frequencies, the MV1442 is capable of withstanding much larger values of peak to peak input jitter. In the absence of input jitter, the MV1442 will produce an output jitter waveform in the form of a sawtooth ramping between 0UI and 0.125UI. The period of this waveform will be dependent upon the difference

in frequencies between the remote transmitters clock and the crystal controlled clock of the MV1442.

The MV1442 was originally designed as a pin compatible replacement for the MV1441 with a much improved internal clock recovery circuit and allowing operation at 8.448MHz with external clock recovery selected. However, there are certain minor differences between the two circuits which are described in a separate Applications Brief (AB33).

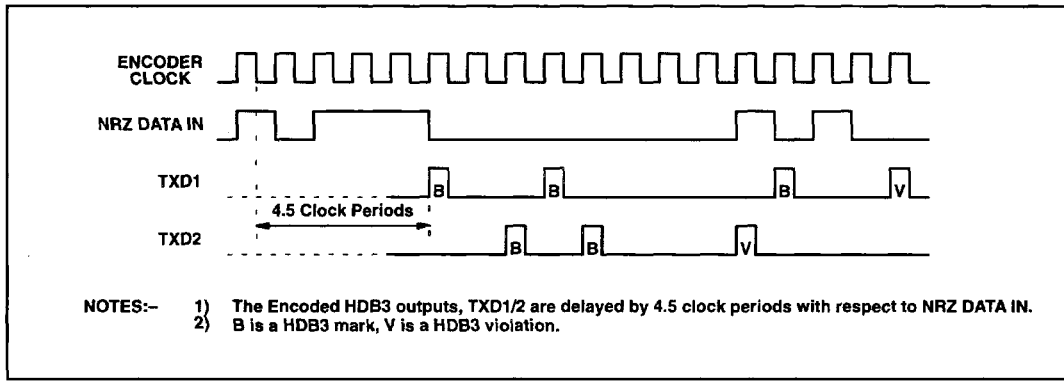

Fig. 3: Encoder waveforms

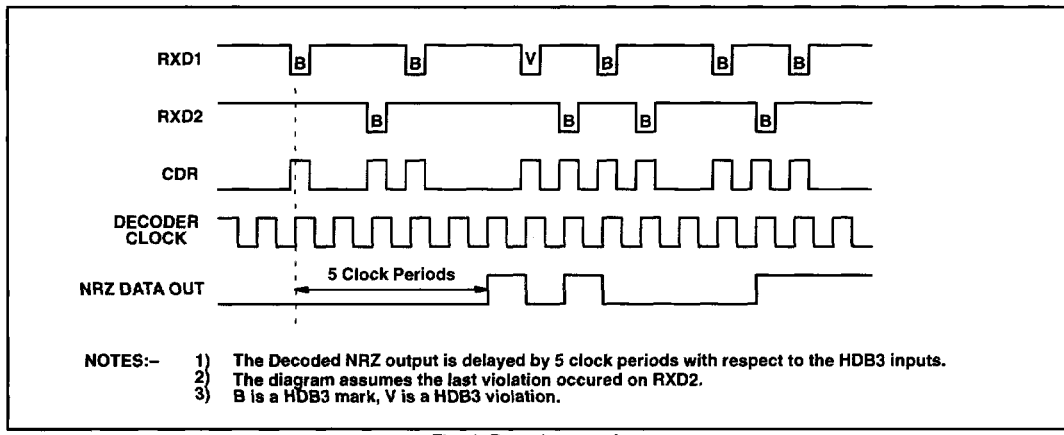

Fig. 4: Decoder waveforms

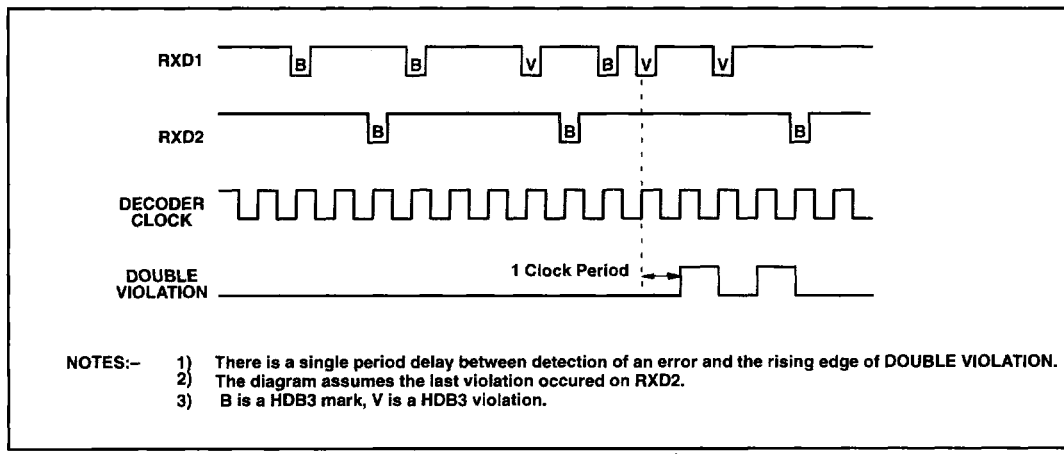

Fig. 5: HDB3 double violation waveforms

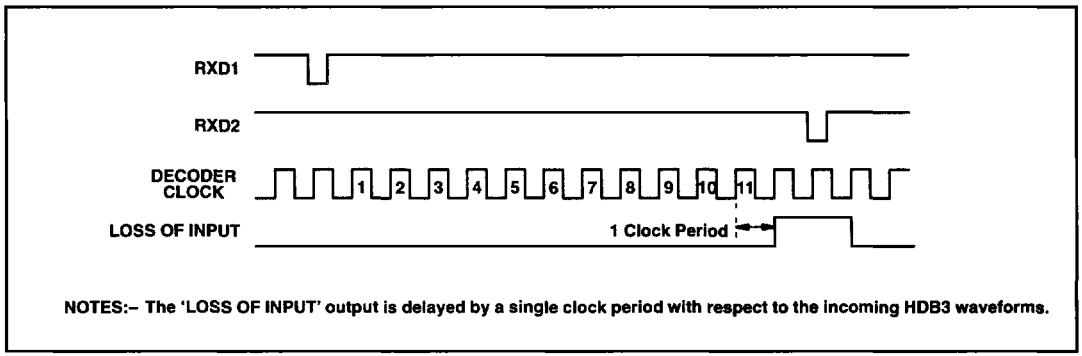

Fig. 6: Loss of input waveforms

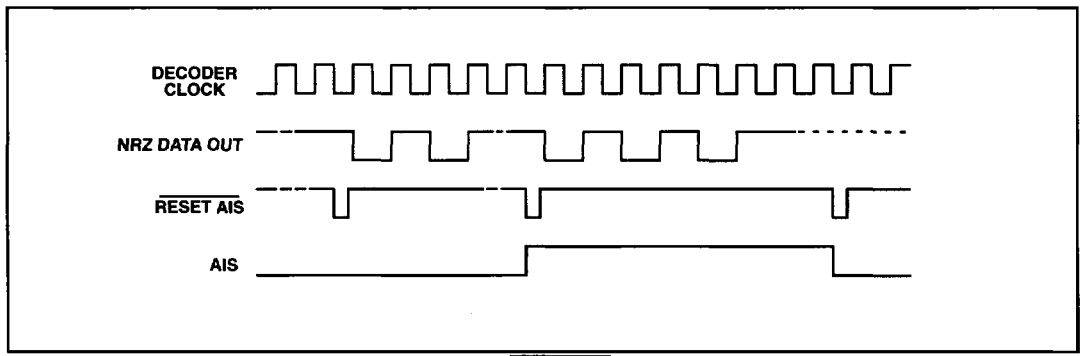

Fig. 7: AIS and RESET AIS waveforms

PIN DESCRIPTION

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	NRZ DATA IN	Input pin for data to be encoded into pseudo–ternary HDB3 form. This data is clocked into the Encoder block by the falling edge of ENCODER CLOCK.
2	ENCODER CLOCK	Clock input for the encoding of data on pin 1.
3	LOSS OF INPUT	Output from the loss of input circuit. This output goes high one clock period after the detection of eleven consecutive zeros on the decoder inputs. Any logic '1' at the input (RXD1 or RXD2 = 0) resets this count after a single clock period delay.
4	NRZ DATA OUT	NRZ data output obtained from the decoding of the pseudo–ternary inputs to the Decoder block.
5	DECODER CLOCK	Clock input to the Decoder block, for decoding data on RXD1 and RXD2, or TXD1 and TXD2 in loop test mode. In internal clock regeneration mode, this pin is used to output the regenerated clock to external circuitry. In external clock regeneration mode, this pin is used to input the externally regenerated clock signal direct to the Decoder block.
6	$\overline{\text{RESET AIS}}$	Reset input to the decoded zero counter. A logic '0' on this input resets a decoded zero counter. It will also reset the AIS output to '0' provided 3 or more zeros have been decoded in the preceding $\overline{\text{RESET AIS}}$ = 1 period, or set AIS to '1' if less than 3 zeros have been decoded in the preceding $\overline{\text{RESET AIS}}$ = 1 period. This may be used to indicate loss of timeslot zero. A logic '1' on this pin enables the decoded zero counter.
7	AIS	Output from AIS circuit (see description for pin 6).

8	MODE	Input pin for selection of clock regeneration mode. A logic high on this input selects internal crystal controlled clock regeneration whilst a logic low selects external clock regeneration.
9	GND	Digital ground. 0 Volts.
10	CRYSTAL IN	Input to crystal oscillator amplifier when in internal clock regeneration mode, with the crystal connected between pins 10 and 12. Alternatively, this pin may be used as the 16.384/12.352MHz input to the internal clock regeneration circuitry if one oscillator is shared between several decoders. This pin has no function when external clock regeneration is selected and should be tied to GND.
11	DOUBLE VIOLATION	Output from the error detector circuit. This output goes high for one period of Decoder clock, one period after the detection of a HDB3 violation of the same polarity as the previous HDB3 violation.
12	CRYSTAL OUT/CDR	In external clock regeneration mode, this pin is used to output the OR function of the two HDB3 inputs, RXD1 and RXD2 (or TXD1 and TXD2 if loop test mode is selected), to an external clock regeneration circuit. In internal clock regeneration mode, this is the output which forms the crystal oscillator with pin 10.
13	RXD1	HDB3 input 1 to Decoder block. This input asynchronously latches the incoming HDB3 encoded data and is falling edge sensitive.
14	LOOP TEST ENABLE	Input pin for selection of normal or loop back operation. A logic low on this pin selects normal operation, with encoder and decoder being independant and asynchronous. A logic high on this pin internally connects TXD1 to RXD1 and TXD2 to RXD2. Note that in loop back mode, a decoder clock must be supplied (or regenerated from pin 12) along with the encoder clock.
15	RXD2	HDB3 input 2 to Decoder block. See pin 13 description.
16	TXD1	HDB3 Encoded output 1 from Encoder block. This output goes high after the rising edge of clock if a mark is to be transmitted. The length of the pulse is set by the positive clock pulse width.
17	TXD2	HDB3 Encoded output 2. See pin 16 description.
18	VDD	Digital supply voltage. 5Volt ±10%.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{DD} = 5V ± 0.5V Ambient Temperature T_{amb} = −40°C to +85°C

STATIC CHARACTERISTICS

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Low Level Input Voltage	V_{IL}	0		0.8	Volts	
High Level Input Voltage	V_{IH}	2.0		V_{DD}	Volts	
Low Level Output Voltage	V_{OL}			0.4	Volts	I_{SINK} = 2mA
High Level Output Voltage	V_{OHT} V_{OHC}	2.4 V_{DD} −1.0			Volts Volts	I_{SOURCE} = 2mA I_{SOURCE} =1mA
Input Leakage Current	I_{IN}	−10		+200	µAmp	V_{IN} = V_{DD} or GND
Supply Current	I_S			15	mAmps	1.544/2.048MHz Operation with Internal clock regeneration, Note 1.
				5	mAmps	1.544/2.048MHz Operation with External clock regeneration, Note 1.
				15	mAmps	8.448MHz Operation, Note 1.
Input Capacitance	C_{IN}		5		pF	All Inputs
Output Capacitance	C_{OUT}		5		pF	All Outputs

Notes:− 1. All supply currents specified with outputs unloaded. These currents are not tested but are guaranteed by characterisation and a static current test.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{DD} = 5V ± 0.5V Ambient Temperature T_{amb} = –0°C to +70°C

DYNAMIC CHARACTERISTICS

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Clock Period	T_{CP}	100			nS	Refer Fig. 8
Clock Rise/Fall Time	T_{CR}/T_{CF}			20	nS	Refer Fig. 8
Clock High/Low time	T_{CH}/T_{CL}	30			nS	Refer Fig. 8
Encoder Data Setup Time	T_{EDS}	10			nS	Refer Fig. 9
Encoder Data Hold Time	T_{EDH}	10			nS	Refer Fig. 9
TXD1/TXD2 Output Propagation Delay	T_{EPDR}/ T_{EPDF}			45	nS	Note 1, refer Fig. 9
CDR Propagation Delay	T_{CPDR}/ T_{CPDF}			40	nS	Note 1, refer Fig. 10
RXD1/2 Data Setup Time	T_{RS}	15			nS	Refer Fig. 10
RXD1/2 Pulse Width	T_{RW}	20			nS	Refer Fig. 10
Decoder Output Propagation Delay	T_{OPD}			45	nS	Notes 1 and 2, refer Fig. 10
$\overline{\text{RESET AIS}}$ Hold Off Time	T_{RAHO}	10			nS	Refer Fig. 10
$\overline{\text{RESET AIS}}$ Pulse Width	T_{RAW}	15			nS	Refer Fig.10
$\overline{\text{RESET AIS}}$ Setup Time	T_{RAS}	10			nS	Refer Fig. 10
AIS Output Propagation Delay	T_{APD}			45	nS	Note 1, refer Fig. 10

Notes:– 1. All propagation delays are measured with the relevant output loaded with a 50pF capacitor.
2. T_{OPD} applies to outputs NRZ DATA OUT, LOSS OF INPUT and DOUBLE VIOLATION, but does not apply to AIS.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{DD} = 5V ± 0.5V Ambient Temperature T_{amb} = –40°C to +85°C

DYNAMIC CHARACTERISTICS

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Clock Period	T_{CP}	100			nS	Refer Fig. 8
Clock Rise/Fall Time	T_{CR}/T_{CF}			20	nS	Refer Fig. 8
Clock High/Low time	T_{CH}/T_{CL}	35			nS	Refer Fig. 8
Encoder Data Setup Time	T_{EDS}	20			nS	Refer Fig. 9
Encoder Data Hold Time	T_{EDH}	20			nS	Refer Fig. 9
TXD1/TXD2 Output Propagation Delay	T_{EPDR}/ T_{EPDF}			50	nS	Note 1, refer Fig. 9
CDR Propagation Delay	T_{CPDR}/ T_{CPDF}			45	nS	Note 1, refer Fig. 10
RXD1/2 Data Setup Time	T_{RS}	20			nS	Refer Fig. 10
RXD1/2 Pulse Width	T_{RW}	25			nS	Refer Fig. 10

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Decoder Output Propagation Delay	T_{OPD}			50	nS	Notes 1 and 2, refer Fig. 10
$\overline{\text{RESET AIS}}$ Hold Off Time	T_{RAHO}	15			nS	Refer Fig. 10
$\overline{\text{RESET AIS}}$ Pulse Width	T_{RAW}	20			nS	Refer Fig.10
$\overline{\text{RESET AIS}}$ Setup Time	T_{RAS}	15			nS	Refer Fig. 10
AIS Output Propagation Delay	T_{APD}			55	nS	Note 1, refer Fig. 10

Notes:– 1. All propagation delays are measured with the relevant output loaded with a 50pF capacitor.
2. T_{OPD} applies to outputs NRZ DATA OUT, LOSS OF INPUT and DOUBLE VIOLATION, but does not apply to AIS.

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

$+V_{DD}$	–0.5 to +7V
Inputs	V_{DD} + 0.5V to GND –0.5V
Outputs	V_{DD} +0.5V to GND –0.5V
Storage temperature	Plastic –55 to +125°C
	Ceramic –65 to +150°C

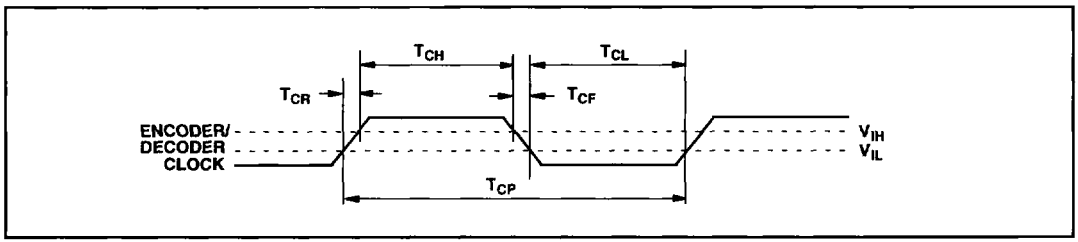

Fig. 8: Clock timing parameters

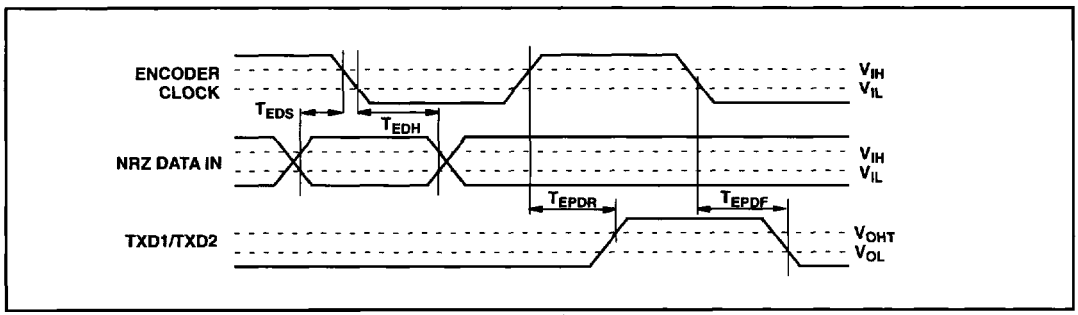

Fig. 9: Encoder timing parameters

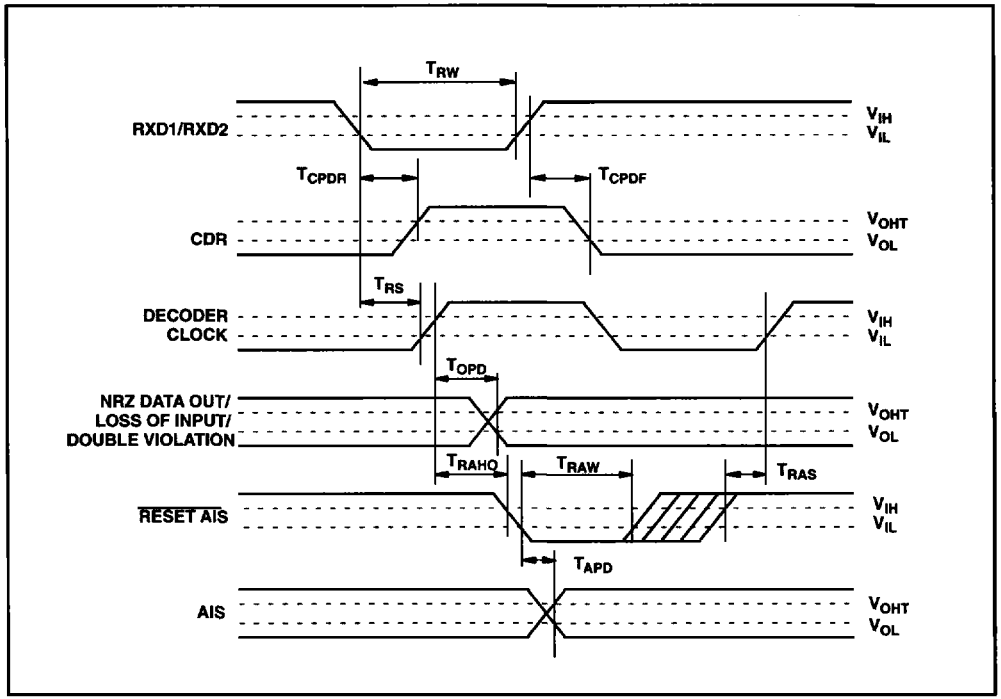

Fig. 10: Decoder timing parameters