

## TEST AND MEASUREMENT PRODUCTS

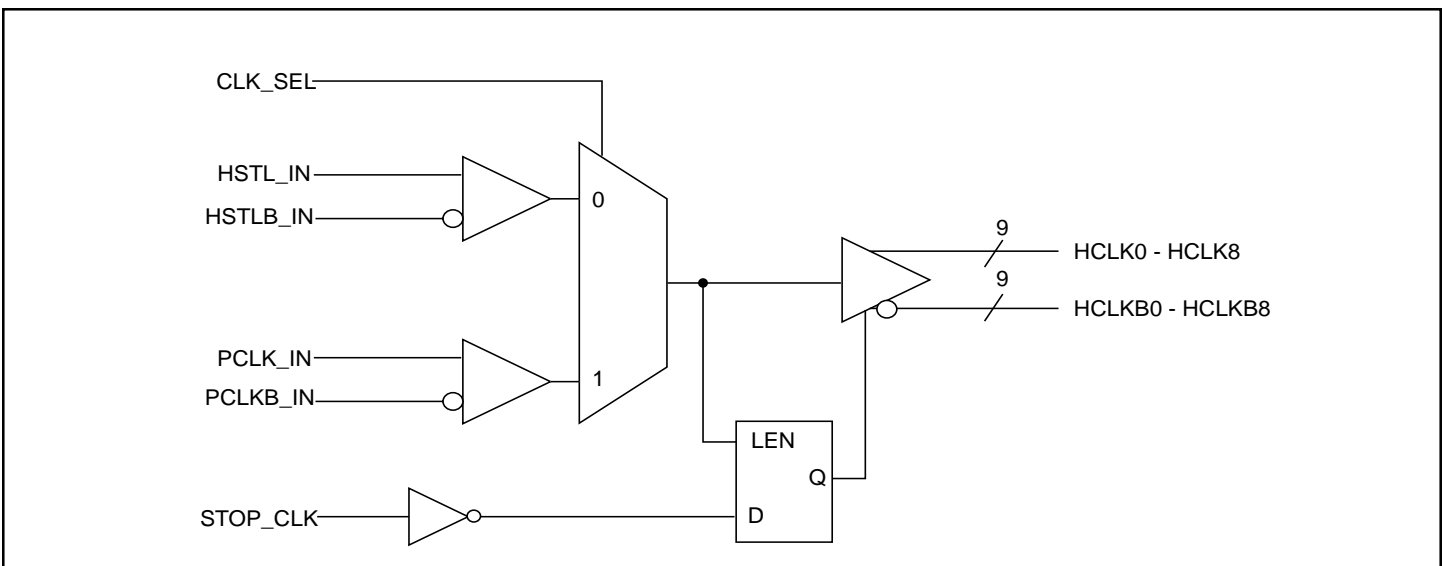
Description	Features
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The SK2200 is a high performance bus clock driver with 9 differential HSTL (High Speed Transceiver Logic) outputs. It can receive either HSTL or LVPECL type signals at its inputs; this feature makes this device ideal for applications where clock distribution, low output-to-output and within device skew are of utmost importance.

The input is multiplexed from either HSTL or LVPECL by the CLK\_SEL. The STOP\_CLK input is synchronous so that the outputs will only be enabled/disabled when they are already in the low state. This feature prevents generating any runt clocks. The HSTL outputs can be terminated using 50Ω resistor to ground without offset voltage.

- HSTL and LVPECL Inputs
- 500 MHz Maximum Clock Frequency
- 35 ps Output-to-Output Skew
- 1:9 Fanout Buffer
- Low Voltage HSTL Output Buffer (VOH = 1.2V)
- Stop Clock Function
- 9 Differential HSTL (Low Voltage Swing) Output Pairs
- 50Ω to GND Termination with no offset voltage
- Low Part-to-Part Skew (200 ps MAX.)
- New Differential Input Common Mode Range
- ESD Protection of >4000V
- Temperature Range: 0°C to +70°C
- 32 Pin LQFP Package (7mm x 7mm x 1.4mm)

## Functional Block Diagram

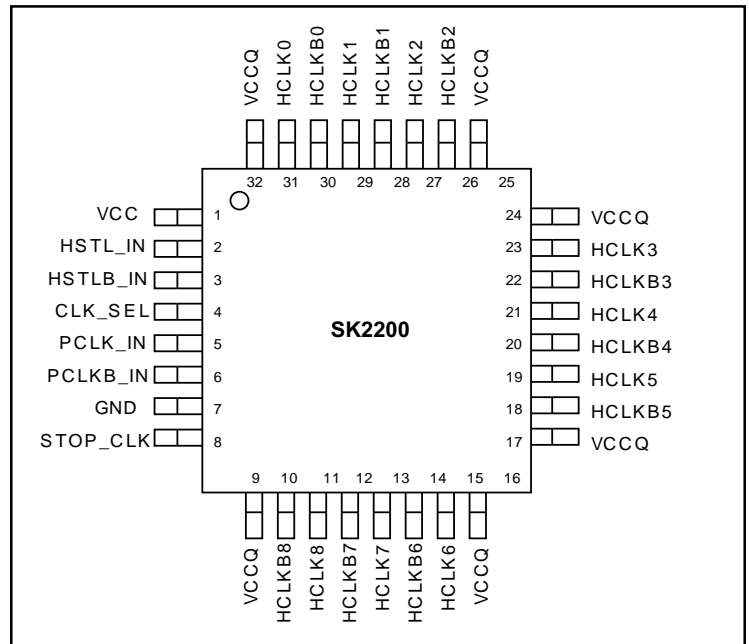


TEST AND MEASUREMENT PRODUCTS

Pin Description

Pin	Function
HSTL_IN, HSTLB_IN	Differential HSTL Inputs
PCLK_IN, PCLKB_IN	Differential LVPECL Inputs
CLK_SEL	Input Clock Select LVTTTL
STOP_CLK	Stop Clock Input LVTTTL
HCLK0 - HCLK8, HCLKB0 - HCLKB8	Diff HSTL Outputs
GND	Ground
VCC	Power Supply
VCCQ	Power Supply

Pin Names



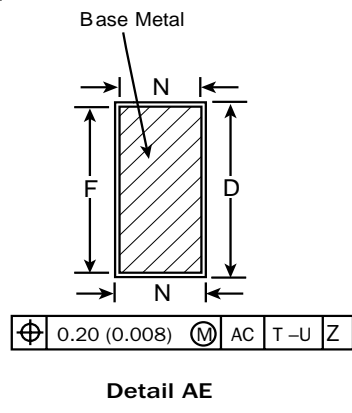
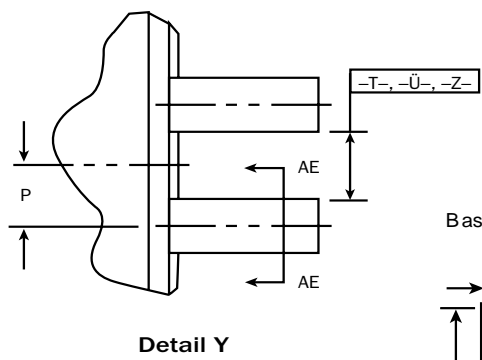
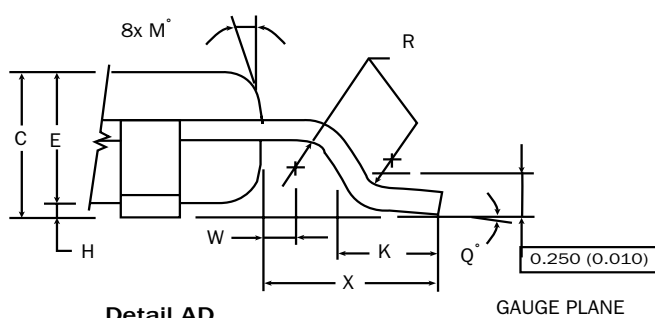
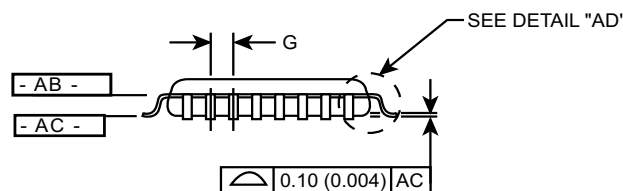
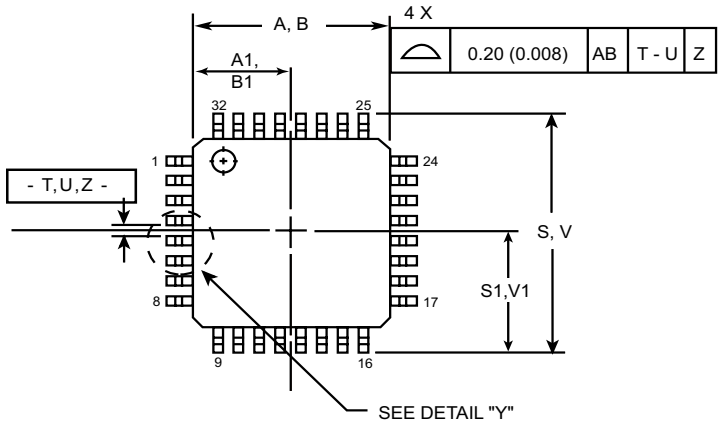
Pinout

STOP_CLK	CLK_SEL	HCLK[0:8]	HCLKB[0:8]
0	0	LOW	HIGH
0	1	LOW	HIGH
1	0	HSTL_IN	HSTLB_IN
1	1	PCLK_IN	PCLKB_IN

Truth Table

TEST AND MEASUREMENT PRODUCTS

Package Information



NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling Dimension: Millimeter
3. Datum Plane -AB- is located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
4. Datums -T-, -U-, and -Z- to be determined at Datum Plane -AB-.
5. Dimensions S and V to be determined at Seating Plane -AC-.
6. Dimensions A and B do not include mold protrusion. Allowable protrusion is 0.250 (0.010) per side. Dimensions A and B do not include mold mismatch and are determined at Datum Plane -AB-.
7. Dimension D does not include Dambar protrusion. Dambar protrusion shall not cause the D dimension to exceed 0.520 (0.020).
8. Minimum solder plate thickness shall be 0.0075 (0.0003).
9. Exact shape of each corner may vary from depiction.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

**TEST AND MEASUREMENT PRODUCTS**
**Absolute Maximum Ratings\***

Symbol	Parameter	Value	Unit
V <sub>CCQ</sub>	Output Power Supply	-0.5 to 4.0	V
V <sub>CC</sub>	Power Supply (3.3V Supply Voltage)	-0.5 to 4.0	V
V <sub>IH</sub> <sup>3</sup>	3.3V LVTTTL Input High Voltage	-0.5 to V <sub>CC</sub>	V
V <sub>IL</sub> <sup>3</sup>	3.3V LVTTTL Input Low Voltage	-0.5	V
T <sub>A</sub>	Ambient Temperature Range	0 to +70	°C
θ <sub>JA</sub> for LQFP	Thermal Resistance (Junction-to-Ambient) at still air	59.5	°C/W
θ <sub>JC</sub> for LQFP	Thermal Resistance (Junction-to-Case) at still air	14.5	°C/W
T <sub>STORE</sub>	Storage Temperature Range	-65 to +150	°C

\* Maximum Ratings are those values beyond which damage to the device may occur.

**DC Electrical Characteristics**
**Power Supply (Note 4)**

Symbol	Characteristic	T <sub>A</sub> = 0°C			T <sub>A</sub> = +25°C			T <sub>A</sub> = +70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	Core Supply Voltage	3.135		3.465	3.135		3.465	3.135		3.465	V
V <sub>CCQ</sub>	Output Supply Voltage	1.6		2.0	1.6		2.0	1.6		2.0	V
I <sub>CCQ</sub>	Output Supply Current			275			275			275	mA
I <sub>CC</sub>	Core Supply Current	50	68	88	50	68	88	50	68	88	mA

**SK2200 HSTL I/O DC Electrical Characteristics**

(V<sub>CC</sub> = 3.3V ± 5%; V<sub>CCQ</sub> = 1.8 ± 0.2V; GND = 0V; Outputs loaded with 50 Ω to GND)

Symbol	Characteristic	T <sub>A</sub> = 0°C			T <sub>A</sub> = +25°C			T <sub>A</sub> = +70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V <sub>OH</sub> <sup>1</sup>	Output HIGH Voltage	1.0		1.2	1.0		1.2	1.0		1.2	V
V <sub>OL</sub> <sup>1</sup>	Output LOW Voltage	0		0.4	0		0.4	0		0.4	V
V <sub>IH</sub>	Input HIGH Voltage	V <sub>x</sub> + 0.1		1.6	V <sub>x</sub> + 0.1		1.6	V <sub>x</sub> + 0.1		1.6	V
V <sub>IL</sub>	Input LOW Voltage	-0.3		V <sub>x</sub> - 0.1	-0.3		V <sub>x</sub> - 0.1	-0.3		V <sub>x</sub> - 0.1	V
V <sub>X</sub>	Input Crossover Voltage	0.68		0.9	0.68		0.9	0.68		0.9	V
I <sub>IH</sub>	Input HIGH Current			-400			-400			-400	mA
I <sub>IL</sub>	Input LOW Current	-600		0	-600		0	-600		0	mA

**TEST AND MEASUREMENT PRODUCTS**
**DC Characteristics (continued)**
**SK2200 LVPECL Input DC Electrical Characteristics**
 $(V_{CC} = 3.3V \pm 5\%; V_{CCQ} = 1.8 \pm 0.2V; GND = 0V)$ 

Symbol	Characteristic	TA = 0°C			TA = +25°C			TA = +70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{IH}^2$	Input HIGH Voltage	2.135		2.42	2.135		2.42	2.135		2.42	V
$V_{IL}^2$	Input LOW Voltage	1.49		1.825	1.49		1.825	1.49		1.825	V
$I_{IN}$	Input Current	-150		150	-150		150	-150		150	mA
$V_{PP}$	Minimum Input Swing	200	600	1000	200	600	1000	200	600	1000	mV
$V_{CMR}^7$	Common Mode Range	GND + 1.5V		$V_{CC}$	GND + 1.5V		$V_{CC}$	GND + 1.5V		$V_{CC}$	V

**SK2200 LVTTTL Input DC Characteristics (Note 2)**
 $(V_{CC}=3.3V \pm 5\%; V_{CCQ} = 1.8 \pm 0.2V; GND = 0V)$ 

Symbol	Characteristic	TA = 0°C			TA = +25°C			TA = +70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{IH}$	Input HIGH Voltage	2.0			2.0			2.0			V
$V_{IL}$	Input LOW Voltage			0.8			0.8			0.8	V
$I_{IH}$	Input HIGH Current	-40		40	-40		40	-40		40	μA
$I_{IL}$	Input LOW Current	-80		0	-80		0	-80		0	μA

**TEST AND MEASUREMENT PRODUCTS**
**AC Characteristics**

## SK2200 AC Electrical Characteristics

 (V<sub>CC</sub> = 3.3V ± 5%; V<sub>CCQ</sub> = 1.8 ± 0.2V; GND = 0V )

Symbol	Characteristic	TA = 0°C			TA = +25°C			TA = +70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
F <sub>MAX</sub>	Maximum Toggle Frequency	500			500			500			MHz
T <sub>PLH</sub> <sup>3</sup> T <sub>PHL</sub>	Input-to-Output Delay	860	930	1000	880	940	1000	930	1040	1100	ps
T <sub>SKEW</sub> <sup>5</sup>	Output-to-Output Skew (Diff) Part-to-Part Skew			35 200			35 200			35 200	ps ps
t <sub>r</sub> , t <sub>f</sub>	Output Rise/Fall Times (20% to 80%)	410		570	420		560	430		550	ps
t <sub>s</sub> <sup>8</sup>	STOP_CLK Setup Time	1000			1000			1000			ps
t <sub>H</sub>	STOP_CLK HOLD Time	500			500			500			ps
DCD <sup>9</sup>	Output Duty Cycle Distortion	48		52	48		52	48		52	%

**NOTES:**

1. Parametric values are specified at V<sub>CCQ</sub> = 1.8V.
2. Parametric values are specified at V<sub>CC</sub> = 3.3V.
3. Measured from the differential input crossing point to differential output crossing point.
4. No power sequencing allowed in the system.
5. Measured from output differential crossing point to output differential crossing point.
6. For part ordering description, see TMD Part Ordering Information Data Sheet.
7. CMR range is referenced to the most positive side of the differential LVPECL input signal. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between V<sub>PP</sub> (min) and 1V. The lower end of the CMR range varies 1:1 with GND and is equal to GND + 1.5V. V<sub>CMR</sub> is referenced to VCC (LVPECL input supply).
8. Setup time measuring point is defined at 1.5V of the STOP\_CLK and the crossing point of the differential input clock. The setup is measured between the edge rate of the STOP\_CLK and the next rising edge of the true output of the differential input clock.
9. Measured with duty cycle of input clock ([PCLK\_IN, PCLKB\_IN] or [HCLK\_IN, HCLKB\_IN]) at 50%.

**TEST AND MEASUREMENT PRODUCTS****Ordering Information<sup>6</sup>**

Ordering Code	Package ID
SK2200LF	32-LQFP
SK2200LFT	32-LQFP

**Application Notes**

- AN1003 - Termination Techniques for ECL/LVECL/PECL/LVPECL Devices
- AN1004 - Interfacing Between LVDS and ECL/LVECL/PECL/LVPECL
- AN1008 - Interfacing With CML

**Contact Information**

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