OKI Semiconductor

MSM5416273

Preliminary

262,144 -Word x 16 Bits Multiport DRAM

Rev.1.0

GENERAL DESCRIPTION

The MSM5416273 is a 4-Mbit CMOS multiport DRAM composed of a 262,144-word by 16-bit dynamic RAM and a 512-words by 16-bits SAM. Its RAM and SAM operate independently and asynchronously.

The MSM5416273 supports three types of operations : random access to RAM port , high speed serial access to SAM port and bidirectional transfer of data between any selected row in the RAM port and the SAM port . In addition to the conventional multiport DRAM operating modes, the MSM5416273 features the block write , flash write functions and extended page mode on the RAM port and a split data transfer capability ,programmable stops on the SAM port. The SAM port requires no refresh operation because it uses static CMOS flip-flops.

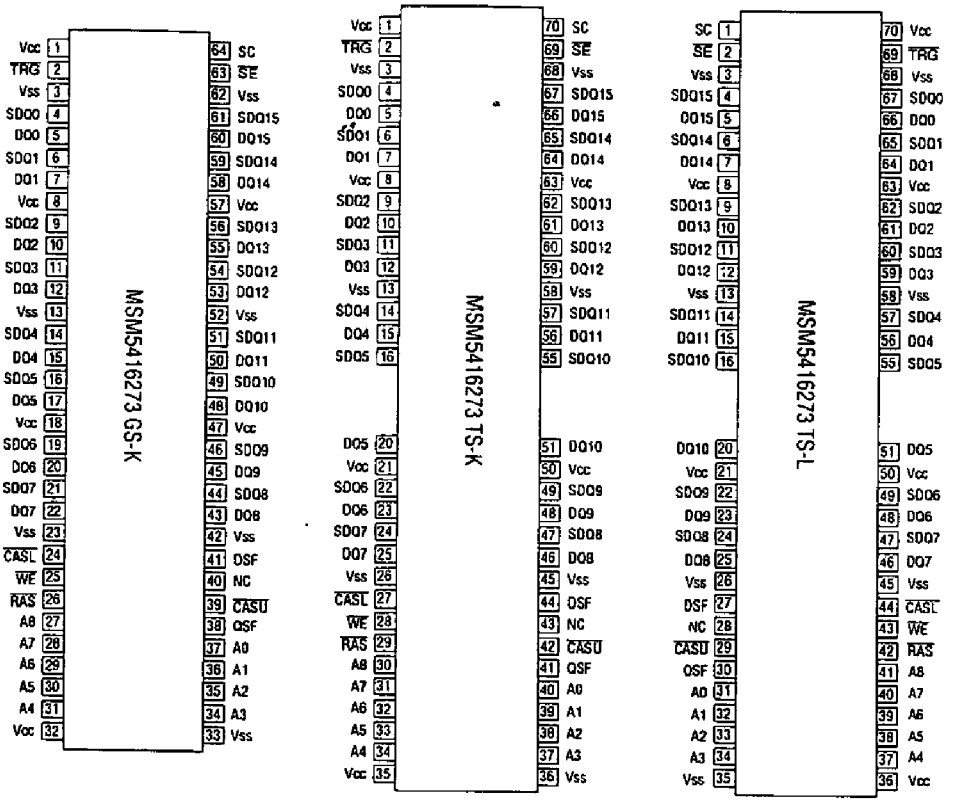
FEATURES

- Single power suply : 5V ± 10%
- Full TTL compatibility
- Multiport organization
  RAM : 256K word x 16 bits
  SAM : 512 word x 16 bits
- Extended page mode
- Write per bit
- Persistent write per bit
- Byte read/write
- Masked flash write
- Masked block write (8column)
- $\overline{RAS}$ only refresh
- $\overline{CAS}$ before $\overline{RAS}$ refresh
- Hidden refresh
- Serial read/write
- 512 tap location
- Programmable stops
- Bidirectional data transfer
- Split transfer
- Masked write transfer
- Refresh : 512 cycles/8ms
- Package : 525 mil 64 pin SSOP
  (SSOP64-P-525-K)
  : 400 mil 70/64 pin TSOP II
  (TSOP70/64-P-400/0.65-K,-L)

PRODUCT FAMILY

Family	Access Time		Cycle Time		Power Dissipation	
	RAM	SAM	RAM	SAM	Operating	Standby
MSM5416273-50	50ns	17ns	110ns	20ns	160mA	8mA
MSM5416273-60	60ns	18ns	120ns	22ns	150mA	8mA
MSM5416273-70	70ns	20ns	140ns	22ns	140mA	8mA

PIN CONFIGURATION (TOP VIEW)



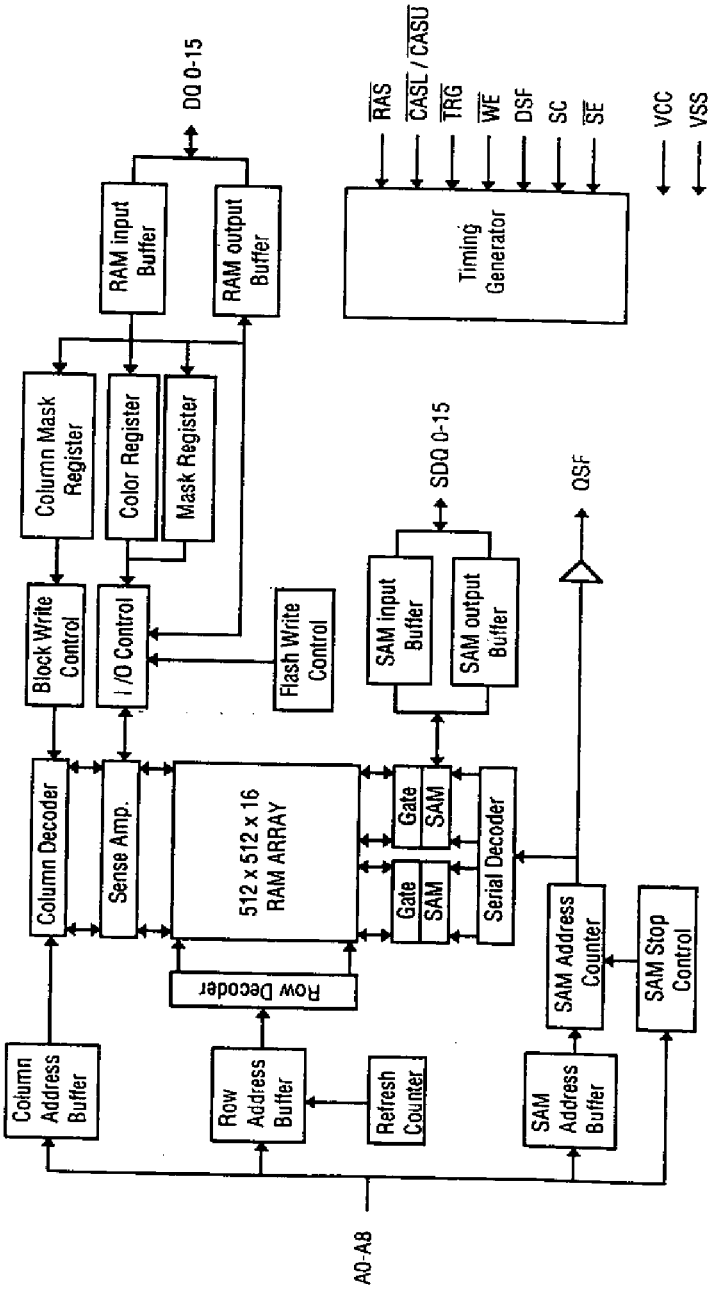
64-PIN SSOP

70/64-PIN TSOP II
NORMAL

70/64-PIN TSOP II
REVERSE

Pin Name	Function	Pin Name	Function
A0 - A8	Address Inputs	SC	Serial Clock
DQ0 - DQ15	RAM Inputs / Outputs	$\overline{SE}$	SAM Port Enable
SDQ0 - SDQ15	SAM Inputs / Outputs	DSF	Special Function Input
$\overline{RAS}$	Row Address Strobe	QSF	Special Function Output
$\overline{CASL}$	Column Address Strobe Lower	Vcc	Power Supply (3.3V)
$\overline{CASU}$	Column Address Strobe Upper	Vss	Ground (0V)
$\overline{WE}$	Write Enable	NC	No Connection
$\overline{TRG}$	Transfer / Output Enable		

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(Note : 1)

Parameter	Symbol	Conditions	Ratings	Unit
Input Output Voltage	V_T	Ta = 25 ℃	- 1.0 to 7.0	V
Output Current	I_{OS}	Ta = 25 ℃	50	mA
Power Dissipation	P_D	Ta = 25 ℃	1	W
Operating Temparature	Topr	-	0 to 70	℃
Strage Temparature	Tstg	-	- 55 to 150	℃

Recommended Operating Conditions

(Ta = 0 to 70 ℃) (Note : 2)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	-	6.5	V
Input Low Voltage	V_{IL}	- 1.0	-	0.8	V

Capacitance

(Vcc = 5.0V, f = 1MHz, Ta = 25℃)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance	Ci	-	6	pF
Input / Output Capacitance	Cio	-	7	pF
Output Capacitance	Co (QSF)	-	7	pF

Note : This parameter is periodically sampled and is not 100% tested

DC Characteristics 1

Parameter	Symbol	Conditions	Min.	Max.	Unit
Output "H" Level Voltage	V_{OH}	I_{OH} = - 2mA	2.4	-	V
Output "L" Level Voltage	V_{OL}	I_{OL} = + 2mA	-	0.4	V
Input Leakage Current	I_{IL}	0 < V_{IN} < Vcc All other pins not under test = 0V	- 10	10	μA
Output Leakage Current	I_{OL}	0 < V_{OUT} < Vcc Output Disable	- 10	10	μA

DC Characteristics 2

(Vcc=5.0V± 10% , Ta=0 to 70 ℃)

ITEM (RAM)	SAM	Symbol	- 50	- 60	- 70	Unit	Note
			MAX.	MAX.	MAX.		
Operating Current ($\overline{RAS}$,$\overline{CAS}$ Cycling t_{RC}=t_{RC} min.)	Standby	I_{CC1}	125	115	105	mA	3, 4
	Active	I_{CC1A}	160	150	140		17
Standby Current ($\overline{RAS}$,$\overline{CAS}$ = V_{IH})	Standby	I_{CC2}	8	8	8		
	Active	I_{CC2A}	55	50	50		3, 4
$\overline{RAS}$ Only Refresh Current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH} t_{RC} = t_{RC} min.)	Standby	I_{CC3}	125	115	105		3, 4
	Active	I_{CC3A}	160	150	140		17
Page Mode Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling t_{PC} = t_{PC} min.)	Standby	I_{CC4}	125	115	105		3, 4
	Active	I_{CC4A}	160	150	140		18
$\overline{CAS}$ before $\overline{RAS}$ Refresh Current ($\overline{RAS}$ Cycling, $\overline{CAS}$ before $\overline{RAS}$ t_{RC} = t_{RC} min.)	Standby	I_{CC5}	125	115	105		3, 4
	Active	I_{CC5A}	160	150	140		3, 4
Data Transfer Current ($\overline{RAS}$,$\overline{CAS}$ Cycling t_{RC}=t_{RC} min.)	Standby	I_{CC6}	125	115	105		3, 4
	Active	I_{CC6A}	160	150	140		17
Flash Write Current ($\overline{RAS}$,$\overline{CAS}$ Cycling t_{RC}=t_{RC} min.)	Standby	I_{CC7}	125	115	105		3, 4
	Active	I_{CC7A}	160	150	140		3, 4
Block Write Current ($\overline{RAS}$,$\overline{CAS}$ Cycling t_{RC}=t_{RC} min.)	Standby	I_{CC8}	125	115	105		3, 4
	Active	I_{CC8A}	160	150	140		3, 4

AC Characteristics (1/3)

Parameter	Symbol	-50		-60		-70		Unit.	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	tRC	110	—	120	—	140	—	ns	
Read Modify Write Cycle Time	tRMW	145	—	170	—	185	—	ns	
Fast Page Mode Cycle Time	tHPC	28	—	30	—	35	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	tPRMW	80	—	85	—	90	—	ns	
Access Time from $\overline{RAS}$	tRAC	—	50	—	60	—	70	ns	8,14
Access Time from Column Address	tAA	—	25	—	30	—	35	ns	8,14
Access Time from $\overline{CAS}$	tCAC	—	15	—	18	—	20	ns	8,15
Access Time from $\overline{CAS}$ Precharge	tCPA	—	30	—	35	—	40	ns	8,15
Output Buffer Turn-Off Delay Time	tOFF	0	12	0	15	0	17	ns	10
Transition Time(Rise and Fall)	tT	3	35	3	35	3	35	ns	7
$\overline{RAS}$ Precharge Time	tRP	40	—	50	—	60	—	ns	
$\overline{RAS}$ Pulse Width	tRAS	50	10k	60	10k	70	10k	ns	
$\overline{RAS}$ Pulse Width(Hyper Page Mode Only)	tRASP	50	100k	60	100k	70	100k	ns	
$\overline{RAS}$ Hold Time	tRSH	15	—	15	—	20	—	ns	
$\overline{CAS}$ Hold Time	tCSH	50	—	60	—	70	—	ns	
$\overline{CAS}$ Pulse Width	tCAS	12	10k	15	10k	20	10k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	18	35	20	42	20	50	ns	14
$\overline{RAS}$ to Column Address Delay Time	tRAD	13	25	15	30	15	35	ns	14
Column Address to $\overline{RAS}$ Lead Time	tRAL	25	—	30	—	35	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	5	—	5	—	10	—	ns	
$\overline{CAS}$ Precharge Time(Hyper Page Mode)	tCP	8	—	10	—	10	—	ns	
Row Address Set-Up Time	tASR	0	—	0	—	0	—	ns	
Row Address Hold Time	tRAH	8	—	10	—	10	—	ns	
Column Address Set-Up Time	tASC	0	—	0	—	0	—	ns	
Column Address Hold Time	tCAH	10	—	10	—	10	—	ns	
Column Address Hold Time referenced to $\overline{RAS}$	tAR	40	—	50	—	55	—	ns	
Read Command Set-Up Time	tRCS	0	—	0	—	0	—	ns	
Read Command Hold Time	tRCH	0	—	0	—	0	—	ns	11
Read Command Hold Time referenced to $\overline{RAS}$	tRRH	0	—	0	—	0	—	ns	11
$\overline{CAS}$ "H" to $\overline{RAS}$ "H" Lead Time	tCRL	0	—	0	—	0	—	ns	
$\overline{RAS}$ "H" to $\overline{CAS}$ "H" Lead Time	tRCL	0	—	0	—	0	—	ns	
Data Output Hold After $\overline{CAS}$ Low	tCOH	5	—	5	—	5	—	ns	19
Write Command Set-Up Time	tWCS	0	—	0	—	0	—	ns	13
Write Command Hold Time	tWCH	8	—	10	—	12	—	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	tWCR	40	—	50	—	55	—	ns	
Write Command Pulse Width	tWP	8	—	10	—	12	—	ns	
Write Command to $\overline{RAS}$ Lead Time	tRWL	12	—	15	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	tCWL	12	—	15	—	20	—	ns	

AC Characteristics (2/3)

Parameter	Symbol	-50		-60		-70		Unit.	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Data Set-Up Time	tDS	0	—	0	—	0	—	ns	12
Data Hold Time	tDH	10	—	10	—	12	—	ns	12
Data Hold Time referenced to $\overline{RAS}$	tDHR	40	—	50	—	55	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	tRWD	70	—	80	—	90	—	ns	13
Column Address to $\overline{WE}$ Delay Time	tAWD	45	—	50	—	55	—	ns	13
$\overline{CAS}$ to $\overline{WE}$ Delay Time	tCWD	30	—	35	—	40	—	ns	13
Data to $\overline{CAS}$ Delay Time	tDZC	0	—	0	—	0	—	ns	
Data to $\overline{OE}$ Delay Time	tDZO	0	—	0	—	0	—	ns	
Access Time from $\overline{OE}$	tOEA	—	15	—	18	—	20	ns	
Output Buffer Turn-Off Delay Time from $\overline{OE}$	tOEZ	0	12	0	15	0	17	ns	
$\overline{OE}$ Command Hold Time	tOEH	8	—	10	—	10	—	ns	
$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	tROH	10	—	10	—	15	—	ns	
$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	tCSR	8	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	tCHR	8	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	tRPC	0	—	0	—	0	—	ns	
Refresh Period	tREF	—	8	—	8	—	8	ms	
$\overline{WB}$ Set-Up Time	tWSR	0	—	0	—	0	—	ns	
$\overline{WB}$ Hold Time	tRWH	10	—	10	—	10	—	ns	
DSF Set-up Time Referenced to $\overline{RAS}$	tFSR	0	—	0	—	0	—	ns	
DSF Hold Time Referenced to $\overline{RAS}$ (1)	tRFH	10	—	10	—	10	—	ns	
DSF Hold Time Referenced to $\overline{RAS}$ (2)	tFHR	40	—	50	—	55	—	ns	
DSF Set-up Time Referenced to $\overline{CAS}$	tFSC	0	—	0	—	0	—	ns	
DSF Hold Time Referenced to $\overline{CAS}$	tCFH	10	—	10	—	10	—	ns	
Write-Per-Bit Mask Data Set-Up Time	tMS	0		0		0		ns	
Write-Per-Bit Mask Data Hold Time	tMH	10	—	10	—	10	—	ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self-refresh)	tRASS	100	—	100	—	100	—	μs	
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self-refresh)	tRPS	110	—	120	—	140	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self-refresh)	tCHS	0	—	0	—	0	—	ns	
$\overline{TRG}$ High Set-Up Time	tTHS	0	—	0	—	0	—	ns	
$\overline{TRG}$ High Hold Time	tTHH	10	—	10	—	10	—	ns	
$\overline{TRG}$ Low Set-Up Time	tTLS	0	—	0	—	0	—	ns	
$\overline{TRG}$ Low Hold Time	tTLH	10	10k	10	10k	10	10k	ns	
$\overline{TRG}$ Low Hold Time Referenced to $\overline{RAS}$	tRTH	40	10k	50	10k	60	10k	ns	
$\overline{TRG}$ Low Hold Time Referenced to Column Address	tATH	20	—	20	—	25	—	ns	
$\overline{TRG}$ Low Hold Time Referenced to $\overline{CAS}$	tCTH	15	—	15	—	20	—	ns	
$\overline{TRG}$ to $\overline{RAS}$ Precharge Time	tTRP	40	—	50	—	60	—	ns	
$\overline{TRG}$ Precharge Time	tTP	15	—	20	—	20	—	ns	
$\overline{RAS}$ to First SC Delay Time (Read Transfer)	tRSD	50	—	60	—	70	—	ns	

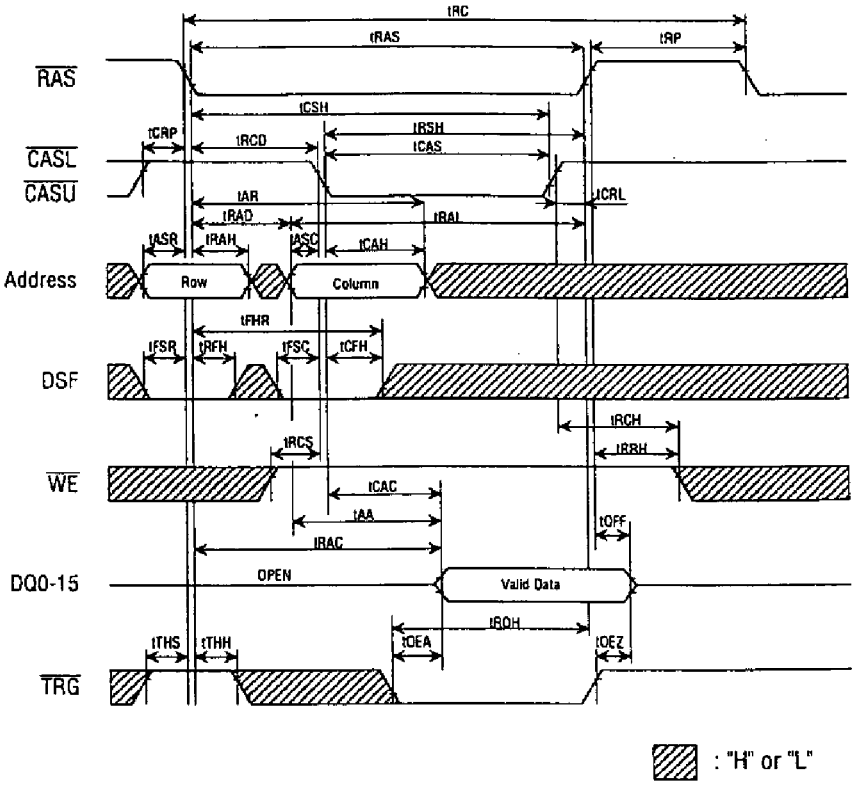
AC Characteristics (3/3)

Parameter	Symbol	-50		-60		-70		Unit.	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Column Address to First SC Delay Time	tASD	35	—	40	—	45	—	ns	
$\overline{CAS}$ to First SC Delay Time (Read Transfer)	tCSD	20	—	20	—	20	—	ns	
Last SC to $\overline{TRG}$ Lead Time	tTSL	5		5		5		ns	
$\overline{TRG}$ to First SC Delay Time (Read Transfer)	tTSD	15	—	15	—	15	—	ns	
Last SC to $\overline{RAS}$ Set-up Time (Serial Input)	tSRS	20	—	20	—	25	—	ns	
Serial Output Buffer Turn-off Delay Time from $\overline{RAS}$	tSDZ	10	30	10	30	10	40	ns	10
SC Cycle Time	tSCC	20	—	22	—	22	—	ns	
SC Pulse Width (SC High Time)	tSC	5	—	5	—	5	—	ns	
SC Precharge Time (SC Low Time)	tSCP	5	—	5	—	5	—	ns	
Access Time from SC	tSCA	—	17	—	18	—	20	ns	9
Serial Output Hold Time from SC	tSOH	5	—	5	—	5	—	ns	19
Access Time from $\overline{SE}$	tSEA	—	17	—	18	—	20	ns	9
$\overline{SE}$ Pulse Width	tSE	10	—	10	—	10	—	ns	
$\overline{SE}$ Precharge Time	tSEP	10	—	10	—	10	—	ns	
Serial Output Buffer Turn-off Delay Time from $\overline{SE}$	tSEZ	0	14	0	15	0	17	ns	10
Split Transfer Set-up Time	tSTS	25	—	25	—	25	—	ns	
Split Transfer Hold Time	tSTH	25	—	25	—	25	—	ns	
SC-QSF Delay Time	tSQD	—	25	—	25	—	25	ns	
$\overline{TRG}$-QSF Delay Time	tTQD	—	25	—	25	—	25	ns	
$\overline{CAS}$-QSF Delay Time	tCQD	—	30	—	30	—	35	ns	
$\overline{RAS}$-QSF Delay Time	tRQD	—	70	—	70	—	75	ns	
$\overline{RAS}$ to Serial Input Delay Time	tSDD	30	—	30	—	40	—	ns	
Serial Input Set-up Time	tSDS	0	—	0	—	0	—	ns	
Serial Input Hold Time	tSDH	8	—	10	—	10	—	ns	
Serial Input to $\overline{SE}$ Delay Time	tSZE	0	—	0	—	0	—	ns	
Serial Input to First SC Delay Time	tSZS	0	—	0	—	0	—	ns	
Serial Write Enable Set-up Time	tSWS	0	—	0	—	0	—	ns	
Serial Write Enable Hold Time	tSWH	8	—	10	—	10	—	ns	
Serial Write Disable Set-up Time	tSWIS	0	—	0	—	0	—	ns	
Serial Write Disable Hold Time	tSWIH	8	—	10	—	10	—	ns	

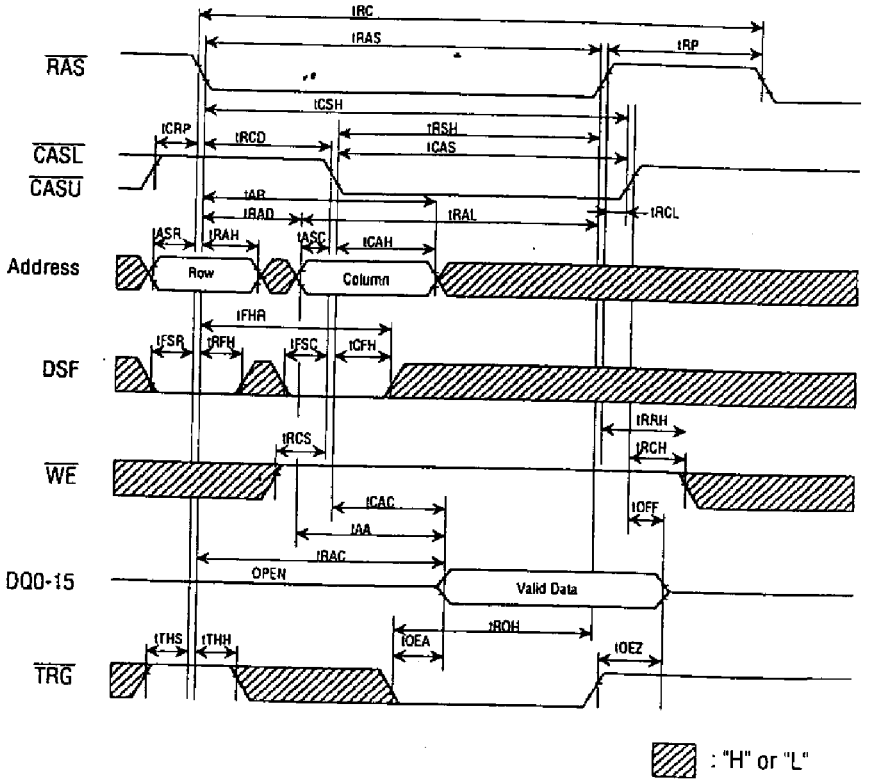
Notes: 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damege to the device.
2. All voltage are referenced to Vss.
3. These parameters depend on cycle rate.
4. These parameters depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200 μs is required after power up followed by any 8 $\overline{RAS}$ cycles ($\overline{TRG}$ = "high") and any 8 SC cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC mesurements assume t_T = 5ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for mesuring timing of input signals. Also, transition times are mesured between V_{IH} and V_{IL}.
8. RAM port outputs are mesured with a load equivalent to 1 TTL load and 50pF. DOUT reference levels : V_{OH}/V_{OL} = 2.0V/0.8V.
9. SAM port outputs are mesured with a load equivalent to 1 TTL load and 30pF. DOUT reference levels : V_{OH}/V_{OL} = 2.0V/0.8V.
10. t_{OFF}(max.), t_{OEZ}(max.), t_{SDZ}(max.) and t_{SEZ}(max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.This parameter is sampled and not 100% tested.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
12. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WE}$ leading edge in $\overline{TRG}$ controlled write cycles and read modify write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are inculuded in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$(min.), the cycle is an early write cycles and the data out pin will remain open circuit throughout the entire cycles ; If $t_{RWD} > t_{RWD}$(min.), $t_{CWD} > t_{CWD}$(min.) and $t_{AWD} > t_{AWD}$(min.) the cycle is a read modify write cycle and the data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condistion of the data out is indeterminate.
14. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
16. Input levels at the AC testing are 3.0V/0V.
17. Address(A0-A8) may be changed two times or less while $\overline{RAS}$ = V_{IL}.
18. Address(A0-A8) may be changed once or less while $\overline{CAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.
19. This is guaranteed by design. ($t_{SOH}/t_{COH} = t_{SCA}/t_{CAC}$ - output transition time) This parameter is not 100% tested.

TIMING WAVEFORM

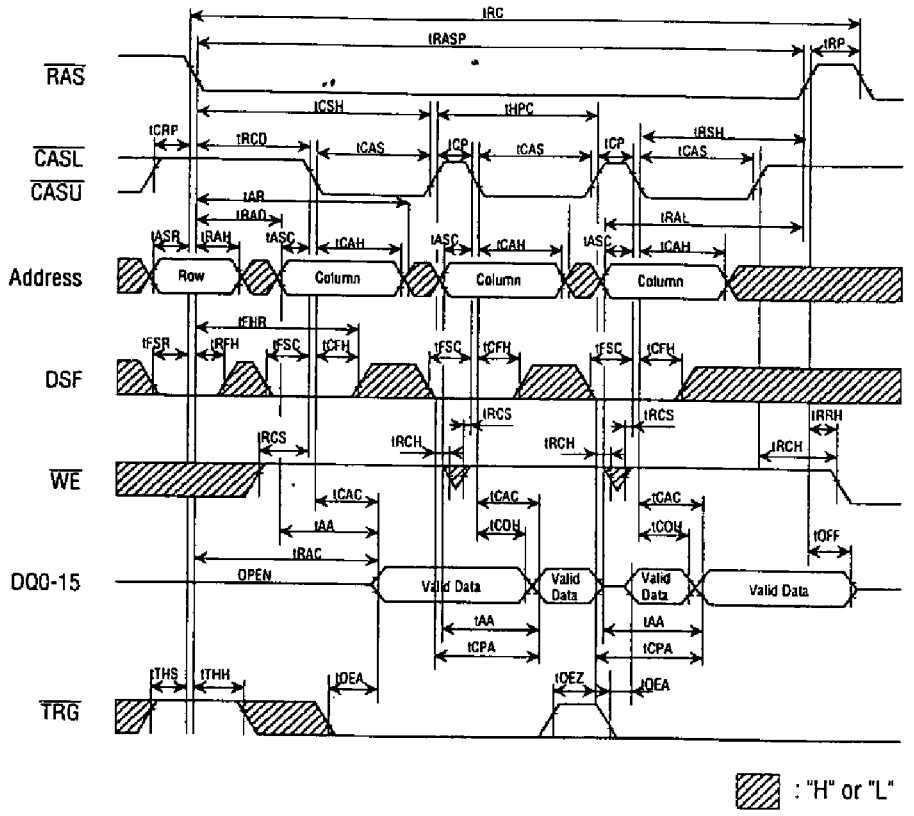
Read Cycle (Outputs Controlled by $\overline{RAS}$)



Read Cycle (Outputs Controlled by $\overline{CAS}$)



Extended Page Mode Read Cycle



Write Cycle Function Table

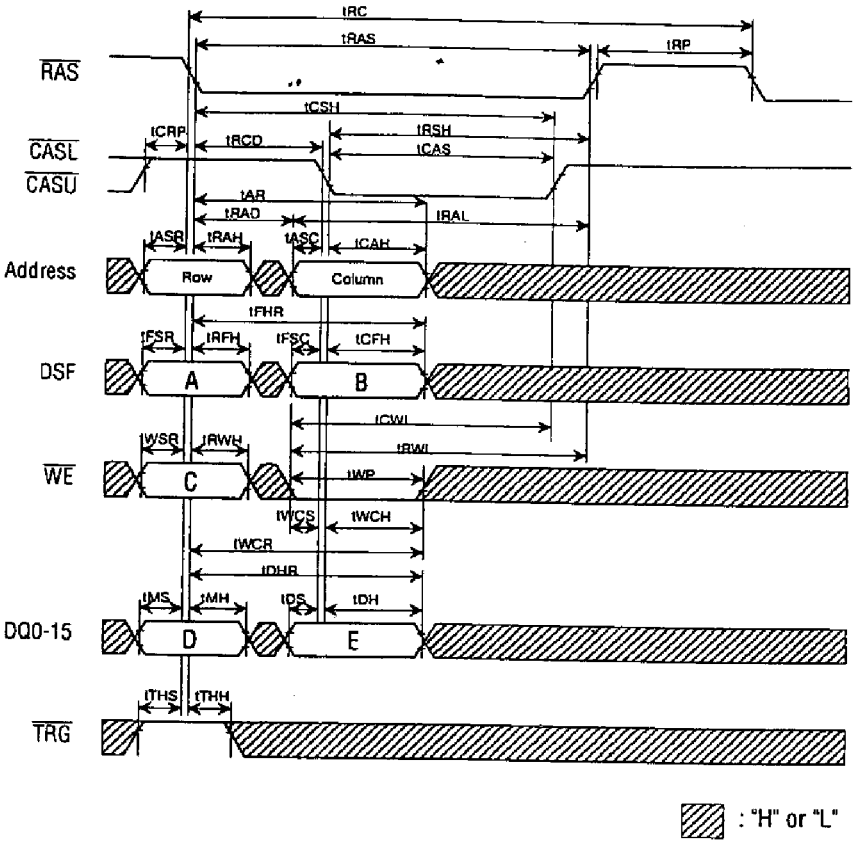
CODE	RAS Falling Edge			CAS Falling Edge		FUNCTION
	A	C	D	B	E	
	DSF	$\overline{WE}$	DQ	DSF	DQ	
RWM	0	0	Write Mask	0	Valid Data	Masked Write (New/Old)
BWM	0	0	Write Mask	1	Column Mask	Masked Block Write (New/Old)
FWM	1	0	Write Mask	X	X	Masked Flash Write (New/Old)
RW	0	1	X	0	Valid Data	Normal Write
BW	0	1	X	1	Column Mask	Block Write
LMR	1	1	X	0	Write Mask Data	Load Mask Register
LCR	1	1	X	1	Color Data	Load Color Register

Write Mask Data: Low=Mask, High=No Mask

Column Mask Data

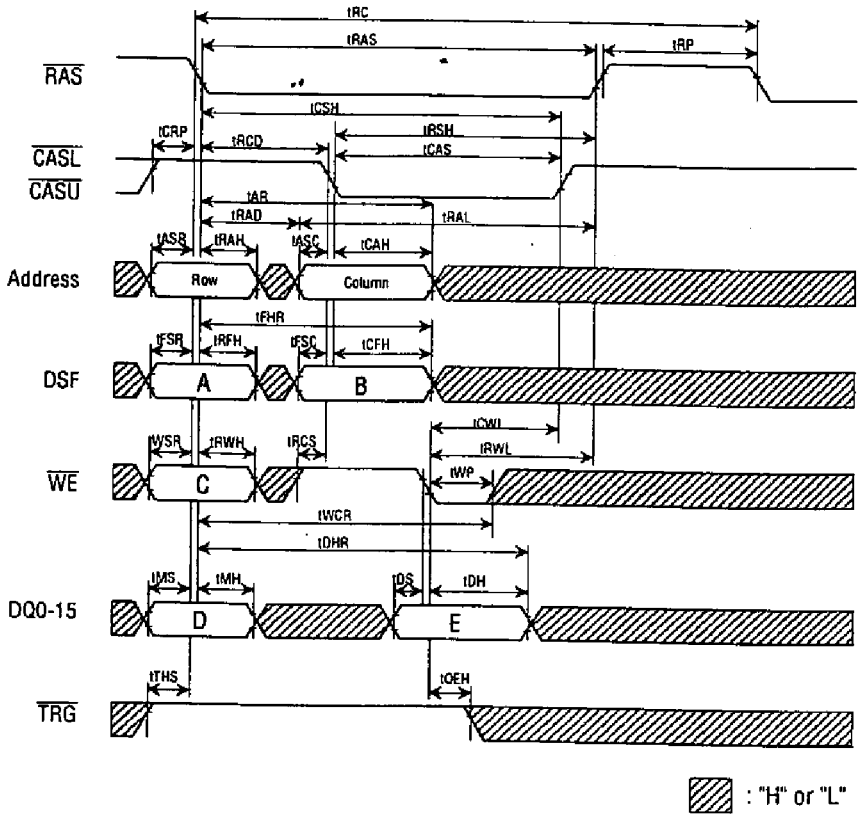
	DQ 0-16	Column Mask Data	
Lower Byte	DQ 0	Column 0 (A0=0, A1=0, A2=0)	Low : Mask High : No Mask
	DQ 1	Column 1 (A0=1, A1=0, A2=0)	
	DQ 2	Column 2 (A0=0, A1=1, A2=0)	
	DQ 3	Column 3 (A0=1, A1=1, A2=0)	
	DQ 4	Column 4 (A0=0, A1=0, A2=1)	
	DQ 5	Column 5 (A0=1, A1=0, A2=1)	
	DQ 6	Column 6 (A0=0, A1=1, A2=1)	
	DQ 7	Column 7 (A0=1, A1=1, A2=1)	
Upper Byte	DQ 8	Column 0 (A0=0, A1=0, A2=0)	Low : Mask High : No Mask
	DQ 9	Column 1 (A0=1, A1=0, A2=0)	
	DQ 10	Column 2 (A0=0, A1=1, A2=0)	
	DQ 11	Column 3 (A0=1, A1=1, A2=0)	
	DQ 12	Column 4 (A0=0, A1=0, A2=1)	
	DQ 13	Column 5 (A0=1, A1=0, A2=1)	
	DQ 14	Column 6 (A0=0, A1=1, A2=1)	
	DQ 15	Column 7 (A0=1, A1=1, A2=1)	

Early Write Cycle

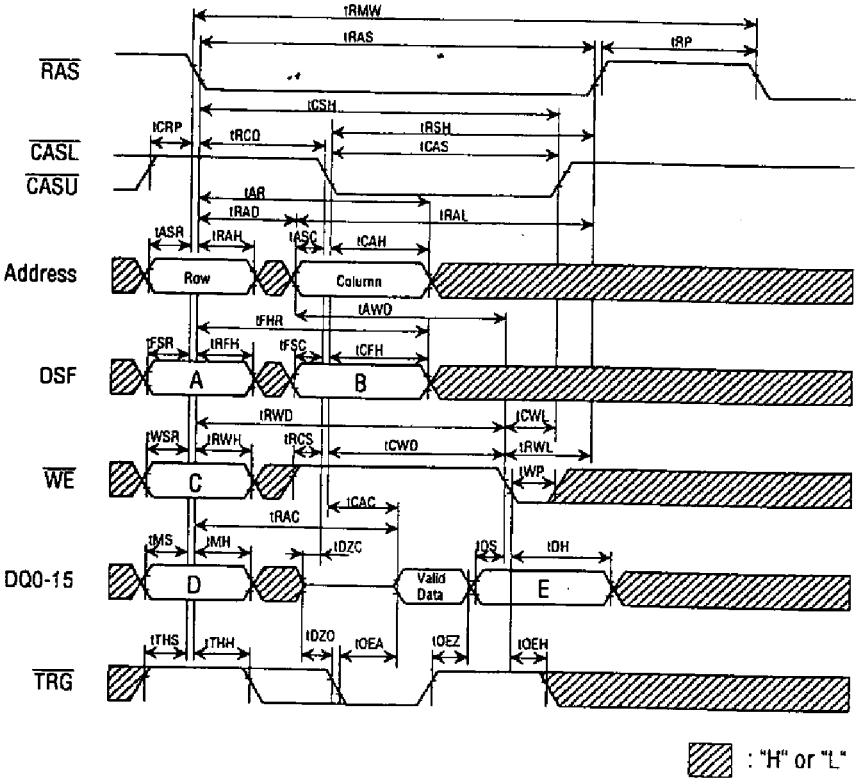


: "H" or "L"

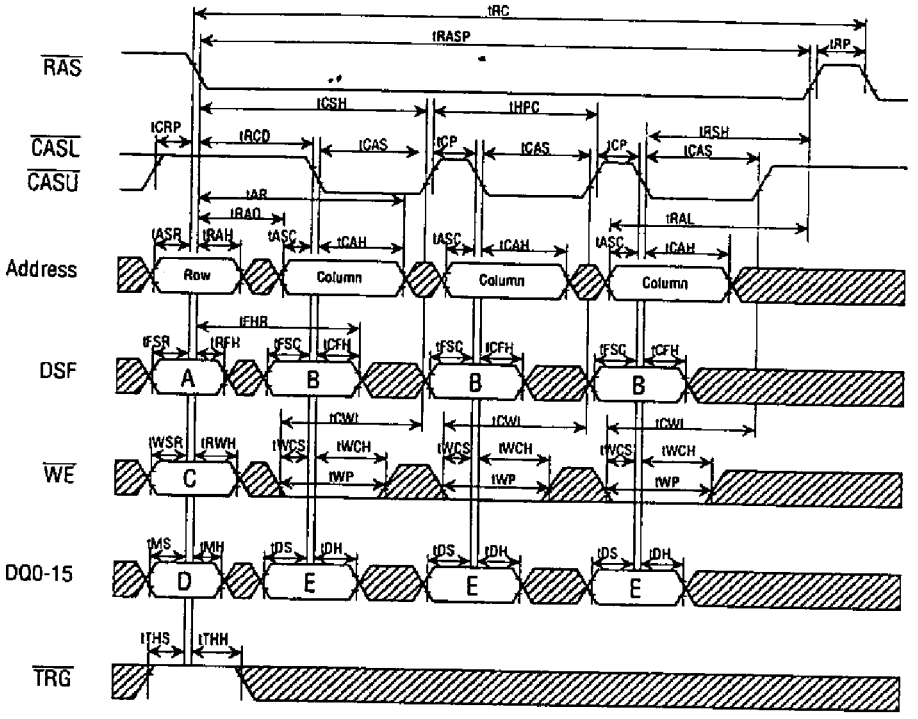
Late Write Cycle



Read Modify Write Cycle

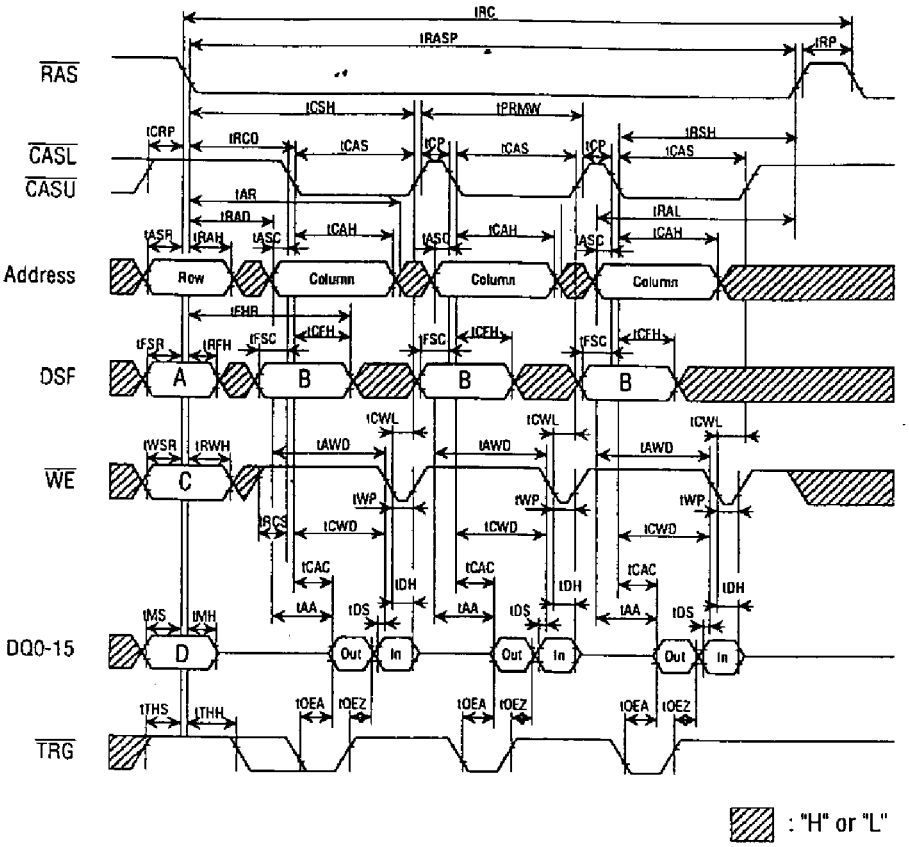


Fast Page Mode Early Write Cycle

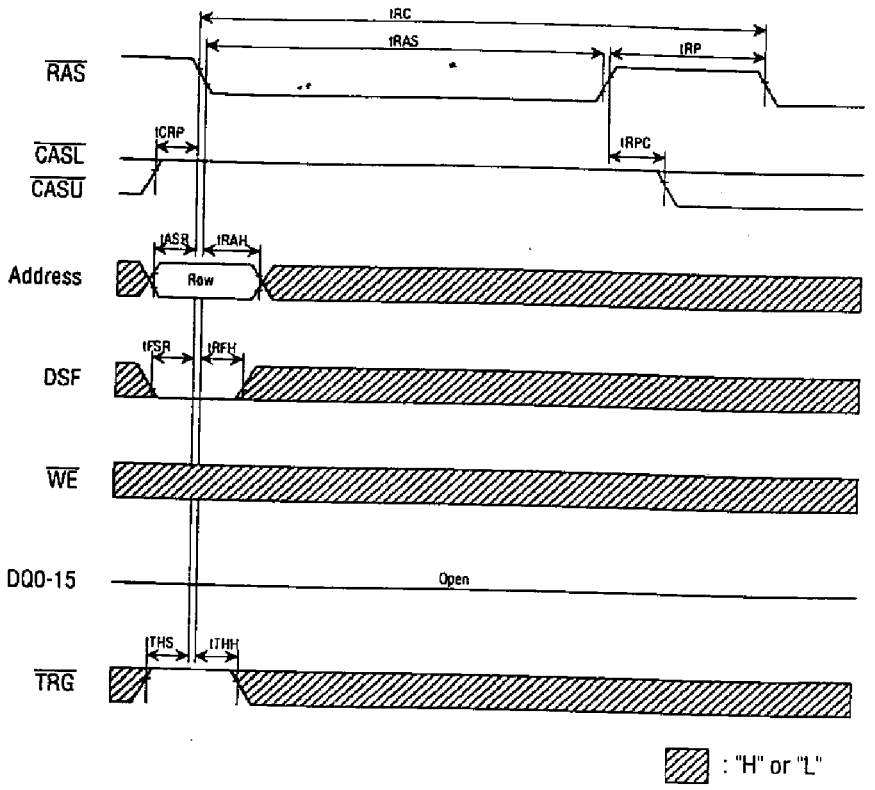


: "H" or "L"

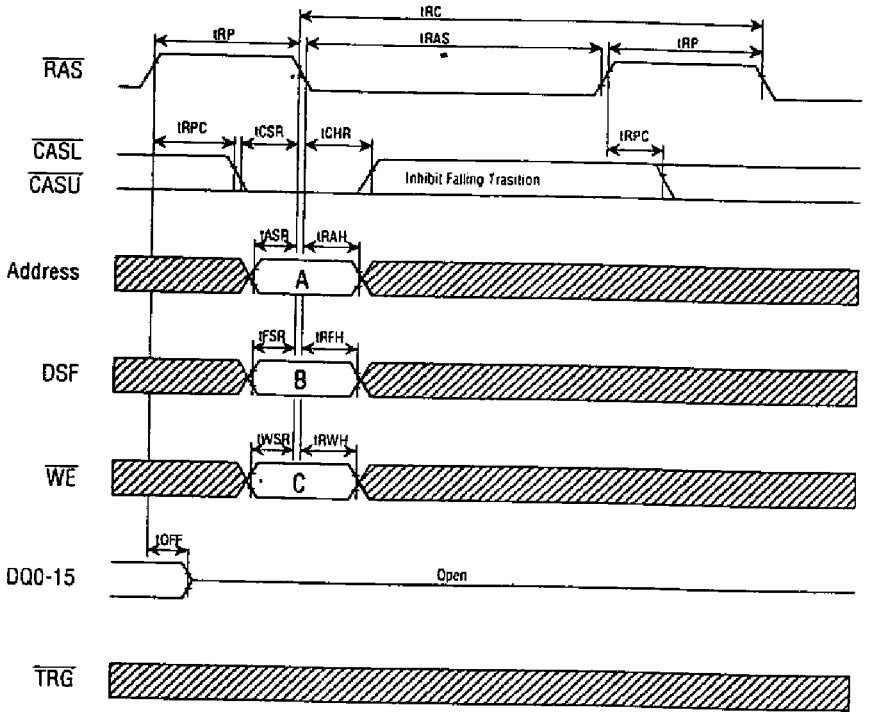
Fast Page Mode Read Modify Write Cycle



$\overline{\text{RAS}}$ Only Refresh Cycle



CAS Before RAS Refresh Cycle

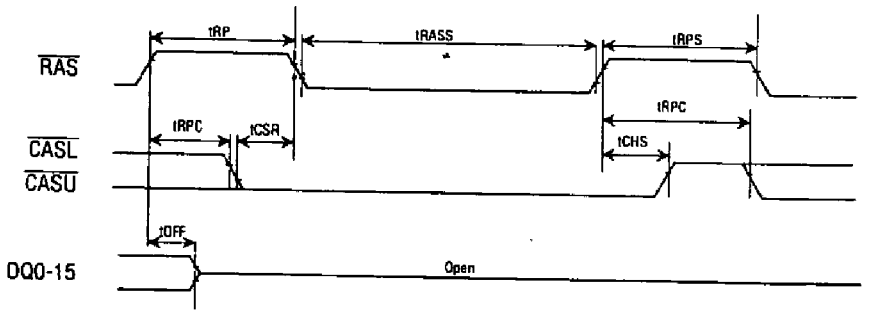


Note: The type of CBR operations are determined by the logic states of "A", "B" and "C".

CBR Cycle Function Table

Code	RAS Falling Edge			Function
	A	B	C	
CBRR	X	0	1	CBR Refresh (Reset All Options)
CBRS	STOP Address	1	0	CBR Refresh (Set STOP Address)
CBRN	X	1	1	CBR Refresh (No Reset Options)

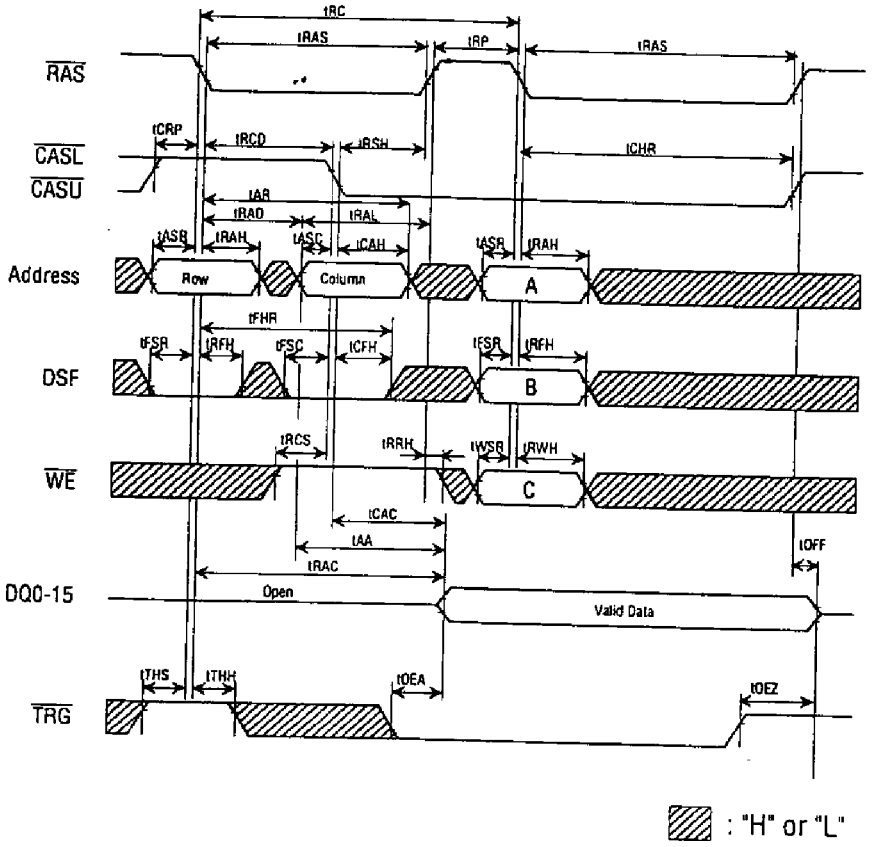
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self-Refresh Cycle



Note: Address, DSF, $\overline{\text{WE}}$, $\overline{\text{TRG}}$ = "H" or "L"

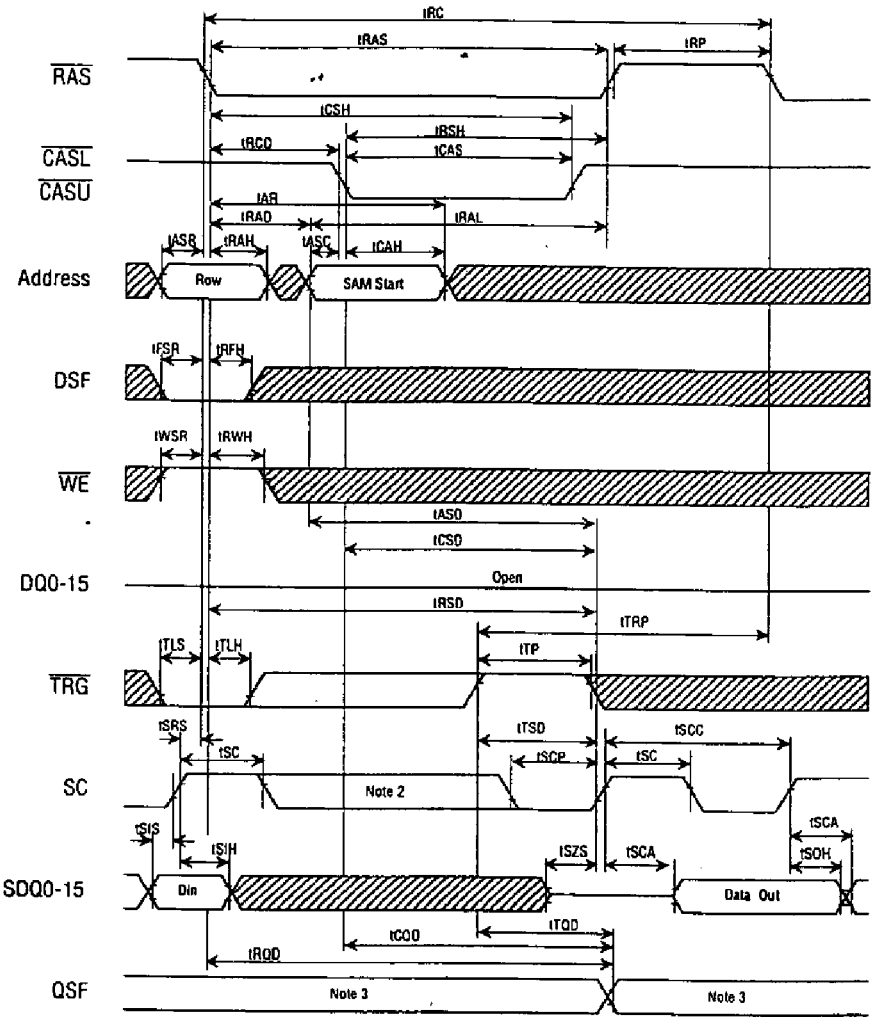
: "H" or "L"

Hidden Refresh Cycle



NOTE: The type of CBR operations are determined by the logic states of "A", "B" and "C".

Read Transfer Cycle

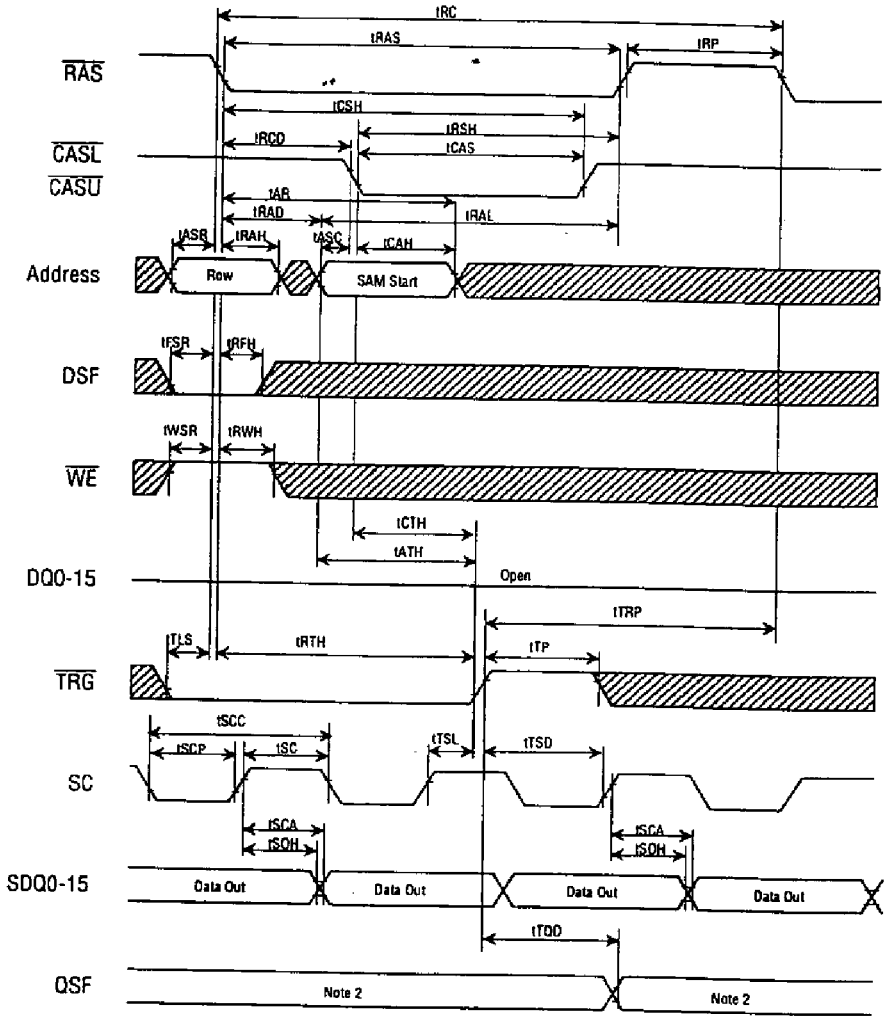


Note 1: $\overline{SE}$="L"

Note 2: There must be no rising transitions

Note 3: QSF="L" -- Lower SAM (0-255) is active
QSF="H" -- Upper SAM (256-511) is active

Real Time Read Transfer Cycle

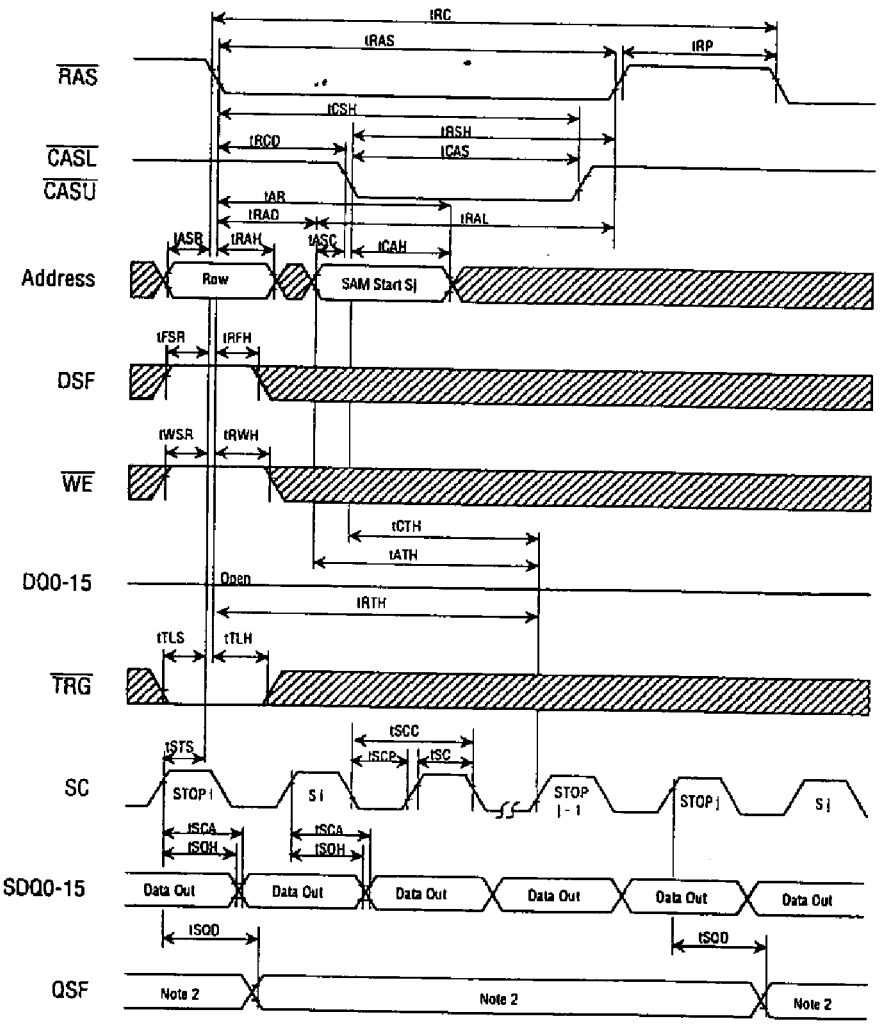


: "H" or "L"

Note 1: $\overline{SE}$="L"

Note 2: QSF="L" -- Lower SAM (0-255) is active
QSF="H" -- Upper SAM (256-511) is active

Split Read Transfer Cycle



: "H" or "L"

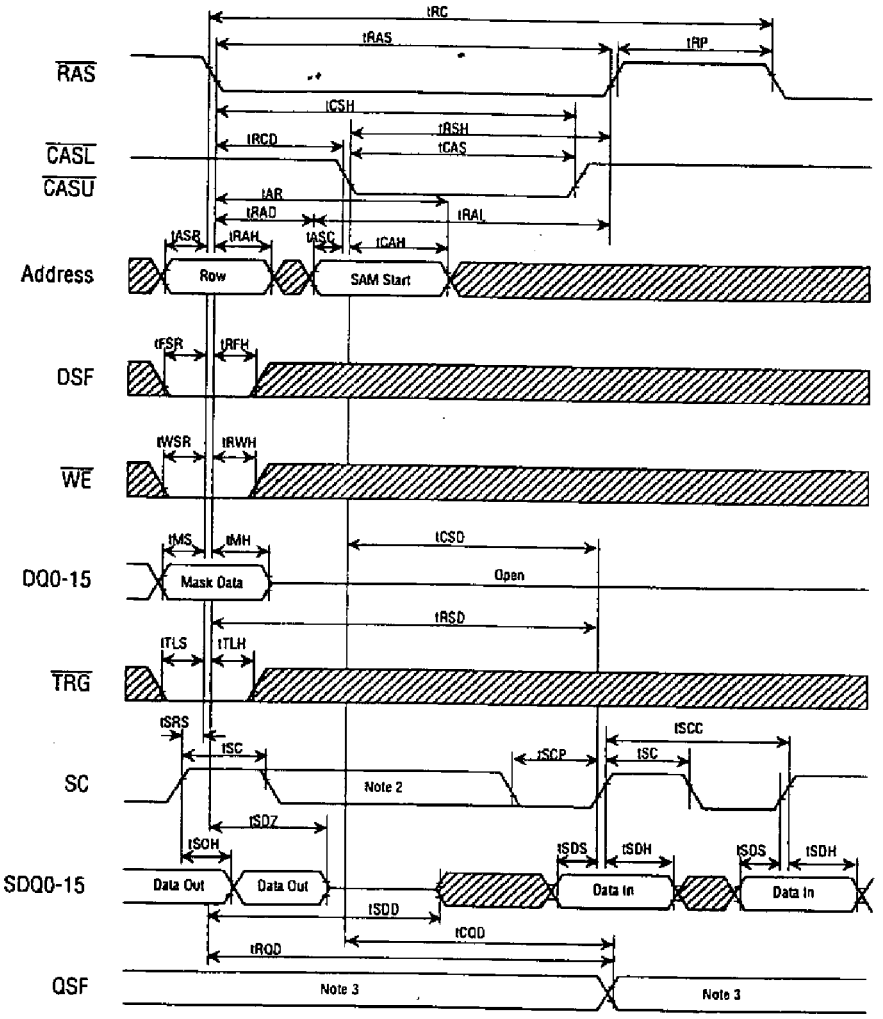
Note 1: $\overline{SE}$="L"

Note 2: QSF="L" -- Lower SAM (0-255) is active
QSF="H" -- Upper SAM (256-511) is active

Note 3: Si is the SAM start address in before SRT

Note 4: STOP i and STOP j are programmable stop address

Masked Write Transfer Cycle

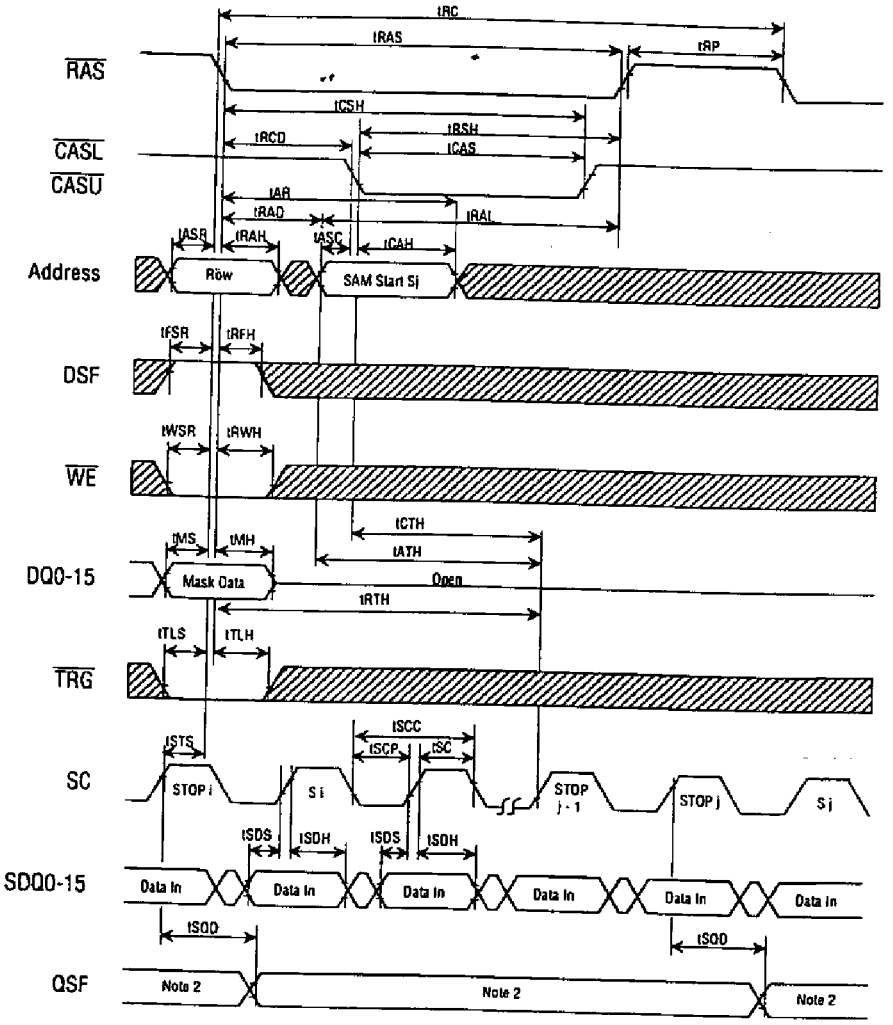


Note 1: $\overline{SE}$="L"

Note 2: There must be no rising transitions

Note 3: QSF="L" -- Lower SAM (0-255) is active
QSF="H" -- Upper SAM (256-511) is active

Masked Split Write Transfer Cycle



: "H" or "L"

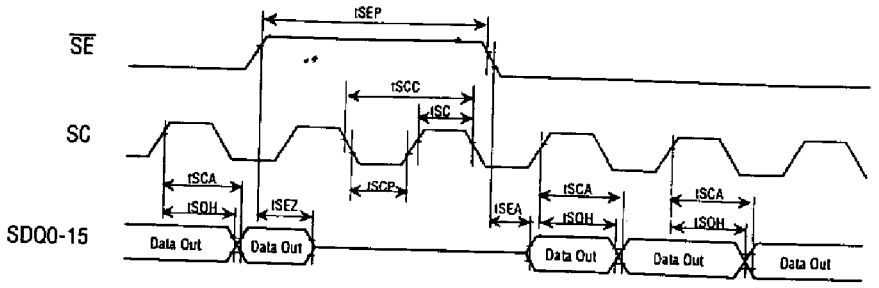
Note 1: $\overline{SE}$="L"

Note 2: QSF="L" -- Lower SAM (0-255) is active
QSF="H" -- Upper SAM (256-511) is active

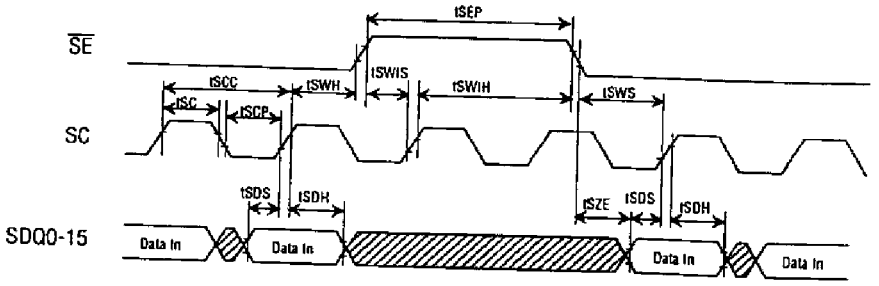
Note 3: Si is the SAM start address in before SWT

Note 4: STOP *i* and STOP j are programmable stop address

Serial Read Cycle



Serial Write Cycle



: "H" or "L"

PIN FUNCTION

Address Input : A0 - A8

The 18 address bits decodes 16-bit of the 4,194,304 locations in the MSM5416273 memory array. The address bits are multiplexed to 9 address inputpins (A0 - A8) as standard DRAM. 9 row address bits are latched at the falling edge of $\overline{RAS}$. The following 9 column address bits are latched at the falling edge of $\overline{CAS}$.

Row Address Strobe : $\overline{RAS}$

$\overline{RAS}$ is a basic RAM control signal. The RAM port is in standby mode when the $\overline{RAS}$ level is "high". As the standard DRAM's $\overline{RAS}$ signal function, $\overline{RAS}$ is control input that latches the row address bits and a random access cycle begin at the falling edge of $\overline{RAS}$. In addition to the conventional $\overline{RAS}$ signal function, the level of the inputsignals , $\overline{CAS}$, $\overline{TRG}$,$\overline{WE}$ and DSF at the falling edge of $\overline{RAS}$, determines the MSM5416273 operation modes.

Column Address Strobe : $\overline{CASL}$, $\overline{CASU}$

As the standard DRAM's $\overline{CAS}$ signal function, $\overline{CASL}$ and $\overline{CASU}$ are the control input signal that latches the column address input and the state of the special function input DSF to select , inconjunction with the $\overline{RAS}$ control, either read/write operations or the special block write feature on the RAM port when the DSF is held "low" at the falling edge of $\overline{RAS}$.
$\overline{CASL}$ and $\overline{CASU}$ also act as a RAM port output enable signal.

Data Transfer , Output Enable : $\overline{TRG}$

$\overline{TRG}$ is also a control input signal having multifunction. As the standard DRAM's $\overline{OE}$ signal function, $\overline{TRG}$ is used as an output enable control when $\overline{TRG}$ is "high" at the falling edge of $\overline{RAS}$.
In addition to the conventional $\overline{OE}$ signal function, a data transfer operation is started between the RAM port and the SAM port when $\overline{TRG}$ is "low" at the falling edge of $\overline{RAS}$.

Write per Bit , Write Enable : $\overline{WE}$

$\overline{WE}$ is control input signals having multifunction. As the standard DRAM's $\overline{WE}$ signal function, these are used to write data into the memory on the RAM port when $\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$.
In addition to the conventional $\overline{WE}$ signal function, the $\overline{WE}$ determines the write-per-bit function when $\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, during RAM port operations.
The $\overline{WE}$ also determines the direction of data transfer between the RAM and SAM. When $\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$, the data is transferred from RAM to SAM (read transfer). When $\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, the data is transferred SAM to RAM (write transfer).

Write Mask Data , Data Input and Output: DQ0 - DQ15

In conventional write-per bit mode, DQ pins function as mask data at the falling edge of $\overline{RAS}$. Data are written only to high DQ pins. Data on low DQ pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.
In persistent write-per-bit mode, DQ pins are don't care at the falling edge of $\overline{RAS}$. The mask data are determined in the mask register load cycle.

Serial Clock: SC

SC is a main serial cycle control input signal. All operations of SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read cycle, the output data becomes valid on the SDQ pins after the maximum specified serial access time tSCA from the rising edge of SC.
In a serial write cycle, data on SDQ pins at the rising edge of SC are fetched into the SAM register.

Serial Enable: $\overline{SE}$

The $\overline{SE}$ is a serial access enable control and serial read/write control signal. In a serial read cycle, $\overline{SE}$ is used as an output control. In a serial write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is "high", serial access is disable, however, the serial address pointer location is still incremented when SC is clocked even When $\overline{SE}$ is "high".

Special Function Input: DSF

The DSF is latched at the falling edge of $\overline{RAS}$ and $\overline{CAS}$ and allows for the sellection of several RAM port and transfer operating modes. In addition to the conventional multiport DRAM, the special function consisting of flash write, block write, load/read color register and split read/write transfer can be invoked.

Special Function Output: QSF

QSF is an output signal which, during split register mode, indicates which half of the split SAM is being accessed. QSF "low" indicates that the lower split SAM (0 - 255) is being accessed. QSF "high" indicates that the upper SAM (256 - 511) is being accessed.

Serial Input/Output: SDQ0-SDQ15

Serial input/output mode is determined by the most recent read, write or pseudo write transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a write or pseudo write transfer cycle is performed, the SAM port is swiched from output mode to input mode.

OPERATION MODE

The Table-1 shows the function truth table for a listing of all available RAM port and transfer operation of MSM5416273.

The RAM port and data transfer operating are determined by the state of $\overline{CAS}$, $\overline{TRG}$, $\overline{WE}$, and DSF at the falling edge of $\overline{RAS}$ and by the state of DSF at the falling edge of $\overline{CAS}$.

Table-1 Function Truth Table

CODE	RAS↓				CAS↓	ADDRESS		W/IO		Write	Pers.	Register		Function
	CAS	TRG	WE	DSF	DSF	RAS↓	CAS↓	RAS↓	CAS/WE↓	Mask	W.M.	WM	Color	
CBRR	0	*	1	0	-	*	*	*	*	-	Reset	Reset	-	CBR refresh with register reset
CBRS	0	-	0	1	-	STOP	-	-	-	-	-	-	-	CBR refresh with stop register set
CBRN	0	-	1	1	-	-	-	-	-	-	-	-	-	CBR refresh (No reset)
ROR	1	1	-	0	-	Row	-	-	-	-	-	-	-	RAS only refresh
MWT	1	0	0	0	-	Row	TAP	WM1	-	Yes	No/Yes	Load Use	-	Masked Write Transfer
MSWT	1	0	0	1	-	Row	TAP	WM1	-	Yes	No/Yes	Load Use	-	Masked Split Write Transfer
RT	1	0	1	0	-	Row	TAP	-	-	-	-	-	-	Read Transfer
SRT	1	0	1	1	-	Row	TAP	-	-	-	-	-	-	Split Read Transfer
RWM	1	1	0	0	0	Row	Column	WM1	Din,Dout	Yes	No/Yes	Load Use	-	Read / Write (New/old mask)
BWM	1	1	0	0	1	Row	Column A3c-8c	WM1	Column Select	Yes	No/Yes	Load Use	Use	Masked Block Write (New/old)
FWM	1	1	0	1	-	Row	-	WM1	-	Yes	No/Yes	Load Use	Use	Masked Flash Write (New/old)
RW	1	1	1	0	0	Row	Column	-	Din,Dout	No	No	-	-	Read / Write (no mask)
BW	1	1	1	0	1	Row	Column A3c-8c	-	Column Select	No	No	-	Use	Block Write (no mask)
LMR	1	1	1	1	0	Row	*	*	Mask Data	-	Set	Load	-	Load mask register (Old mask set)
LCR	1	1	1	1	1	Row	*	*	Color Data	-	-	-	Load	Load color register

Notes : 1. With CBRS, SAM operations use stop register
2. After LMR, RWM, BWM, FWM, and MSWT, use old mask which can be reset by CBRR.

If the DSF is "high" at the falling edge of $\overline{RAS}$, special function such as split transfer, flash write, load mask register, load color register, CBRS and CBRN can be invoked.
If the DSF is "low" at the falling edge of $\overline{RAS}$ and "high" at the falling edge of $\overline{CAS}$, the block write feature can be invoked.

RAM PORT OPERATION

Extended RAM Read Cycle : $\overline{RAS}$ falling edge --- $\overline{TRG}$=$\overline{CAS}$="H" , DSF="L"
$\overline{CAS}$ falling edge --- DSF="L"

The MSM5416273 offers an accelerated page mode cycle (EXTENDED PAGE MODE) by eliminating output disable from $\overline{CAS}$ "high", and it allows $\overline{CAS}$ precharge time (tCP) to occur without the output data going invalid. This new data out operates (Extended data out) as any RAM read or Page Mode Read,except data will be held valid after $\overline{CAS}$ goes "high" ,as long as $\overline{RAS}$ is "low".
Byte read occurs if only one of $\overline{CASL}$ or $\overline{CASU}$ falls during the cycle.

RAM Write Cycle : $\overline{RAS}$ falling edge --- $\overline{TRG}$=$\overline{CAS}$="H" , DSF="L"
$\overline{CAS}$ falling edge --- DSF="L

1) Write cycle with no mask : $\overline{RAS}$ falling edge -- $\overline{WE}$="H"

At the falling edge of $\overline{CAS}$, $\overline{WE}$ is set "low" after $\overline{RAS}$ gose "low", a write cycle is excuted. If $\overline{WE}$ is set "low" before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and all DQ pins become in high impedance.

If $\overline{WE}$ is set "low" after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle and all 16 data are latched on the falling edge of $\overline{WE}$.
Byte write occures if only one of $\overline{CASL}$ or $\overline{CASU}$ falls during the cycle. DQ pins don't become high impedance in this cycle, so data should be entered with $\overline{TRG}$ in "high".

2) Write cycle with mask : $\overline{RAS}$ falling edge -- $\overline{WE}$="L"

At the falling edge of $\overline{RAS}$, if $\overline{WE}$ is set "low", two modes of mask write can be invoked.

#1 In new mask mode, mask data is loaded and used. Whether or not a DQ is written depends on DQ level at the falling edge of $\overline{RAS}$. The data is written in "high" level DQs, and the data is masked and retained in "low" level DQs. This mask data is effective during the $\overline{RAS}$ cycle. In page mode cycles, the mask data is retained during the page access.

#2 If a load mask register cycle (LMR) has been performed, the mask data is not loaded from DQ pins and the mask data stored in mask register persistently are used. This operation is known as persistent write mask, set by LMR and reset by CBRR.

Load / Read Color Register : $\overline{RAS}$ falling edge --- $\overline{CAS}$=$\overline{TRG}$=$\overline{WE}$=DSF="H"
$\overline{CAS}$ falling edge --- DSF="H"

The MSM5416273 is provided with an on-chip 16bits color register for use during the flash write or block write operation. Each bit of the color register corresponds to one of the DRAM I/O blocks.
The data presented on the DQi lines is subsequently latched into the color register at the falling edge of either $\overline{CAS}$ or $\overline{WE}$ whichever occurs later.
The read color register cycle is activated by holding $\overline{WE}$ "high" at the falling edge of $\overline{CAS}$ and throughout the remainder of the cycle. The data in the color register becomes valid on the DQi lines after the specified access times from $\overline{RAS}$ and $\overline{TRG}$ are satisfied.
During the load/read color register cycle, the memory cells on the row address latched at the falling edge of $\overline{RAS}$ are refreshed.

Load / Read Mask Register : $\overline{RAS}$ falling edge --- $\overline{CAS}$=$\overline{TRG}$=$\overline{WE}$=DSF="H"
$\overline{CAS}$ falling edge --- DSF="L"

The MSM5416273 is provided with an on-chip 16bits mask register for use during the mask write cycle, flash write cycle, block write cycle, masked write transfer and masked split write transfer. Each bit of the mask register corresponds to one of the DRAM I/O blocks.
The data presented on the DQi lines is subsequently lached into the mask register at the falling edge of either $\overline{CAS}$ or $\overline{WE}$ whichever occurs later.
The read mask register cycle is activated by holding $\overline{WE}$ "high" at the falling edge of $\overline{CAS}$ and throughout the remainder of the cycle. The data in the mask register becomes valid on the DQi lines after the specified access times from $\overline{RAS}$ and $\overline{TRG}$ are satisfied.
During the load/read mask register cycle, the memory cells on the row address latched at the falling edge of $\overline{RAS}$ are refreshed.

Flash Write : $\overline{RAS}$ falling edge --- $\overline{CAS}$=$\overline{TRG}$=DSF="H", $\overline{WE}$="L"

Flash write allows for the data in the color register to be written into all the memory locations of a selected row.
Each bit of the color register corresponds to one of the DRAM I/O blocks and the flash write operation can be selectively controlled on an I/O basis in the same manner as the write per bit operation. The mask data is as same as that of a RAM write cycle.

Block Write : $\overline{RAS}$ falling edge --- $\overline{CAS}$=$\overline{TRG}$="H", DSF="L"
$\overline{CAS}$ falling edge --- DSF="H", $\overline{WE}$="L"

Block write allows for the data in the color register to be written into 8 consecutive column address locations starting from a selected column address in a selected row.
The block write operation can be selectively controlled on an I/O basis and a column mask capability is also available. During a block write cycle, the 3 least significant colum address locations (A0C -A2C) are internally controlled and only the 6 most significant column address (A3C - A8C) are latched at the falling edge of $\overline{CAS}$.

1) No masked block write : $\overline{WE}$ "high" at the falling edg of $\overline{RAS}$
   The data on 16 DQ pins are all cleared by data of color register.
2) Masked block write : $\overline{WE}$ "low" at the faling edge of $\overline{RAS}$
   The mask data is the same as that of a RAM write cycle (new mask or persistent mask).

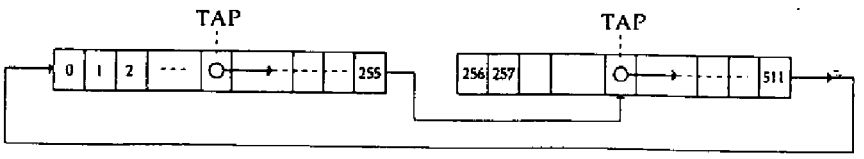
SAM PORT OPERATION

Single Register Mode

High speed serial read or write operation can be performed through the SAM port independent of the RAM port operation, except during read/write transfer cycles.
The preceding transfer operation determines the direction of data flow through the SAM port. If the preceding transfer is a read transfer, the SAM port is in the output mode. If the preceding transfer is write transfer , the SAM port is in the input mode.
Serial data can be read out of the SAM after a read transfer has been performed. The data is shifted out of the SAM starting at any of the 512 bits locations.
The TAP location corresponds to the column address selected at the falling edge of $\overline{CAS}$ during the read or write transfer cycle. The SAM registers are configured as circular data register. The data is shifted out sequentially starting from the selected TAP location to the most significant bit (511) and then wraps around to the least significant bit (0).

Split Register Mode

In split register mode, data can be shifted into or out of one half of the SAM while a split read or split write transfer is being performed on the other half of the SAM.
Conventional (non split) read, or write transfer cycle must precede any split read or split write transfers. The split read and write transfers will not change the SAM port mode set by preceding conventional transfer operation. In the split register mode, serial data can be shifted in or out of one of the split SAM registers starting from any at the 256 TAP locations, excluding the last address of each split SAM, data is shifted in or out sequentially starting from the selected TAP location to the most significant bit (255 or 511) of the first split SAM and then the SAM pointer moves to the TAP location selected for the second split SAM to shift data in or out sequentially starting from this TAP location to the most significant bit (511 or 255) and finally wraps arround to the least significant bit.

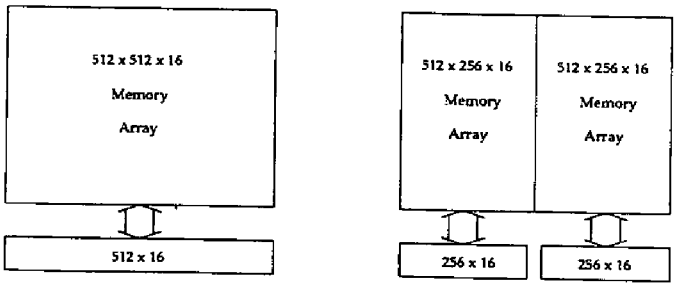


DATA TRANSFER OPERATION

The MSM5416273 features two types of bidirectional data transfer capability between RAM and SAM, as shown in Figure 1 below.

1) Conventional (non split) transfer : 512 words by 16 bits of data can be loaded from RAM to SAM (Read transfer) or from SAM to RAM (Write transfer).
2) Split transfer : 256 words by 16 bits of data can be loaded from the lower/upper half of the RAM to the lower/upper half of the SAM (Split read transfer) or from the lower /upper half of SAM to the lower/upper half of RAM (Split write transfer).

The conventional transfer and split transfer modes are controlled by the DSF input signal.



1) Conventional Transfer 2) Split Transfer

Figure 1.

The MSM5416273 supports 4 types of transfer operation : Read transfer, Split read transfer, Write transfer and Split write transfer as shown in truth table. Data transfer are invoked by holding the $\overline{TRG}$ signal "low" at the falling edge of $\overline{RAS}$. The type of transfer operation is determined by the state of $\overline{CAS}$, $\overline{WE}$ and DSF latched at the falling edge of $\overline{RAS}$. During conventional transfer operations, the SAM port is swiched from input to output mode (Read transfer) or output to input mode (Write transfer) whereas it remains unchanged during split transfer operation (Split read transfer or Split write transfer).

Read Transfer : $\overline{RAS}$ falling edge --- $\overline{CAS}$=$\overline{WE}$="H" , $\overline{TRG}$=DSF="L"

Read transfer consists of loading a selected row of data from the RAM into the SAM register. A read transfer is invoked by holding $\overline{CAS}$ "high" , $\overline{TRG}$ "low" , $\overline{WE}$ "high" and DSF "low" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM. The transfer cycle is completed at the rising edge of $\overline{TRG}$. When the transfer is completed, the SAM port is set into the output mode. In a read / real time read transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{TRG}$ and this data becomes valid on the SDQ lines after the specified access time tSCA from the rising edge of the subsequent SC cycles. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$. In a read transfer cycle (which is preceded by a write transfer cycle), SC clock must be held at a constant VIL or VIH, after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay tTSD from the rising edge of $\overline{TRG}$.

In a real time read transfer cycle (which is preceded by another read transfer cycle), the previous row data appears on the SDQ lines until the $\overline{TRG}$ signal goes "high" and the serial access time tSCA for the following serial clock is satisfied. This feature allows for the first bit of the new row of data to appear on the serial output as soon as the last bit of the previous row has been strobed without any timing loss. To make this continuous data flow possible, the rising edge of $\overline{TRG}$ must be syncronized with $\overline{RAS}$, $\overline{CAS}$ and the subsequent rising edge of SC (tRTH, tCTH, and tTSL/tTSD must be satisfied).

Masked write Transfer : $\overline{RAS}$ falling edge --- $\overline{CAS}$="H", $\overline{WE}$=$\overline{TRG}$=DSF="L"

Write transfer cycle consist of loading the content of the SAM register into a selected row of the RAM. This write transfer is the same as a mask write operation in RAM, so new and persistent (old) mask mode can be supported (Masked write transfer).
If the SAM data to be transferred must first be loaded through the SAM, a Masked write transfer operation (all DQ pins "low" at falling edge of $\overline{RAS}$) must precede the write transfer cycles. A masked write transfer is invoked by holding $\overline{CAS}$ "high" , $\overline{TRG}$ "low" , $\overline{WE}$ "low" and DSF "low" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling ege of $\overline{CAS}$ determines the start address of the serial pointer of the SAM. After the write transfer is completed, the SDQ lines are set in the input mode so that serial data synchronized with the SC clock can be loaded.
When consecutive write transfer operation are performed, new data must not be written into the serial register until the $\overline{RAS}$ cycle of the preceding write transfer is completed. Consequently, the SC clock must be held at a constant VIL or VIH during the $\overline{RAS}$ cycle. A rising edge of the SC clock is only allowed after the specified delay tCSD from the falling edge of the $\overline{CAS}$, at which time a new row of data can be written in the serial register.
Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other address of RAM by write transfer cycle. However, the address to write data must be the same as that of the read transfer cycle (row address AX8).

Split Data Transfer and QSF

The MSM5416273 features a bi-directional split data transfer capability between the RAM and SAM. During split data transfer operation, the serial register is split into two halves which can be controlled independently. Split read or split write transfer operation can be performed to or from one half of the serial register while serial data can be shifted into or out of the other half of the serial register. The most significant column address location (A8C) is controlled internally to determines which half of the serial register will be reloaded from the RAM. QSF is an output in which indicates which half of the serial register is in an active state. QSF changes state when the last SC clock is applied to active split SAM.

Split Read Transfer : $\overline{RAS}$ falling edge --- $\overline{CAS}$=$\overline{WE}$=DSF="H" , $\overline{TRG}$="L"

The MSM5416273 supports two types of split register operation.
#1 Normal split register operation
#2 Boundary split register operation using programmable SAM stops described later.
Normal split read transfer consists of loading 256 words by 16bits of data from a selected row of the split RAM into the corresponding non-active split SAM register. Serial data can be shifted out from the other half of the split SAM register simultaneously. During split read transfer operation, the RAM port input clocks do not have to be synchronized with the serial clock SC, thus eliminating timing restrictions as in the case of real time read transfers. A split read transfer can be performed after a delay of tSTS, from the change of state of the QSF output, is satisfied.
Conventional (non-split) read transfer operation must precede split read transfer cycles.

Masked Split Write Transfer : $\overline{RAS}$ falling edge --- $\overline{CAS}$=DSF="H", $\overline{TRG}$=$\overline{WE}$="L"

Split write transfer consists of loading 256 words by 16bits of data from the non-active split SAM register into a selected row of the corresponding split RAM. Serial data can be shifted into the other half of the split SAM register simultaneously. During split write transfer operation, the RAM port input clocks do not have to be synchronized with the serial clock SC, thus allowing for real time transfer. This operation is the same as a mask write operation in RAM , so new and persistent mode can be supported.
A split write transfer can be performed after a delay of tSTS, from the change of state of the QSF output, is satisfied.
A masked write transfer operation must precede split write transfer, the purpose is to swich the SAM port from output mode to input mode and to set the initial TAP location prior to split write transfer operations.

Programmable SAM Stops in Split Transfer Cycle

The MSM5416273 has the boundary split register operation using programmable stops. If a CBRS cycle has been performed,split transfer cycle performs the boundary operation. Figure 2 shows an example of boundary split register (4 stop points). The stop points defines a SAM location at which the access will change from one half of the SAM to the other half (at the TAP address).

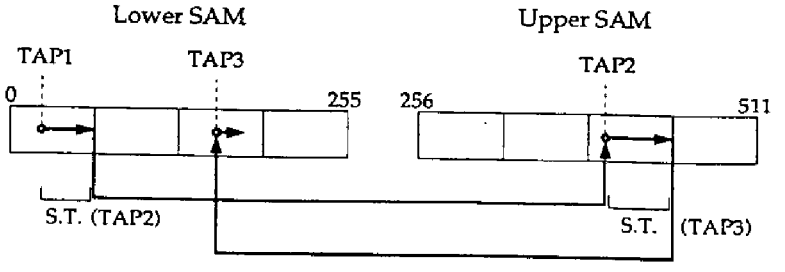


Figure 1. Example of Boundary Split Register

SAM Stop Set Cycle (CBRS): $\overline{RAS}$ falling edge --- $\overline{CAS}$=$\overline{WE}$="L" , DSF="H"

SAM Stop location data (boundaries) are latched from address inputs at the falling edge of $\overline{RAS}$. To determine the boundary, A4 -A7 can be used and don't care A0 -A3, and A8. Once CBRS is executed, the programmable SAM stop operation continues until CBRR.

SAM Stop Boundary Table

Number of Stop points	ADDRESS				Size of partition
	A4	A5	A6	A7	
1	1	1	1	1	256
2	1	1	1	0	128
4	1	1	0	X	64
8	1	0	X	X	32
16	0	X	X	X	16

Register Reset Cycle (CBRR): $\overline{RAS}$ falling edge --- $\overline{CAS}$=DSF="L", $\overline{WE}$="H"

A CBRR can reset the programmable SAM stop operation and persistent mask write operation. The CBRR will take effect immediately ; it does't require a split transfer cycle.

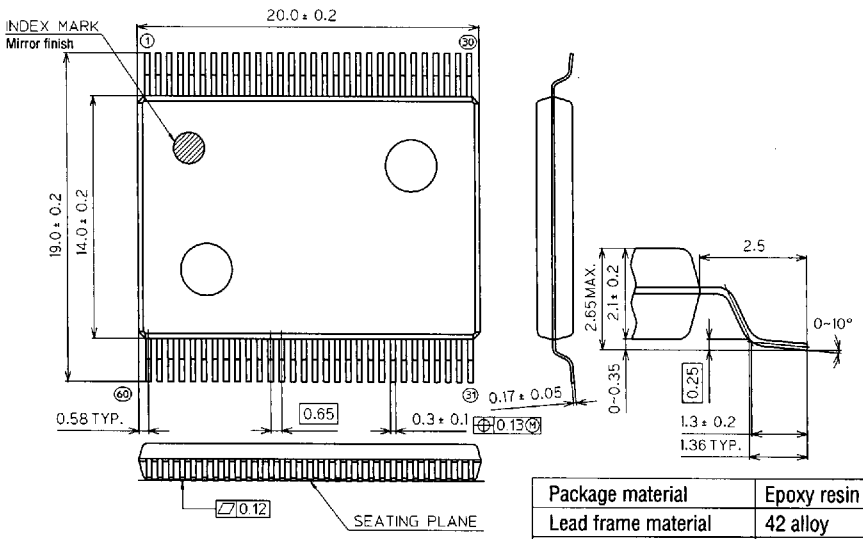
POWER UP

Power must be applied to the $\overline{RAS}$ and $\overline{TRG}$ input signals to pull them "high" before or at the same time as the Vcc supply is turned on. After power-up, a pause of 200 us minimum is required with $\overline{RAS}$ and $\overline{TRG}$ held "high". After the pause, a minimum of 8 $\overline{RAS}$ and 8 SC dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{TRG}$ signal must be held "high". If the internal refresh counter is used, a minimum 8 $\overline{CAS}$ before $\overline{RAS}$ cycles are required instead of 8 $\overline{RAS}$ cycles.

(1) PLASTIC SOP (cont.)

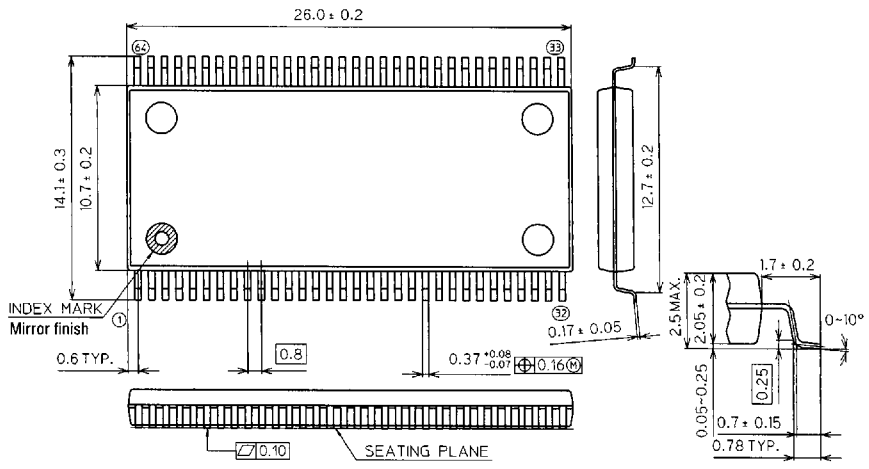
(Unit: mm)

SSOP60-P-700-0.65-L



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5μm or more
Package weight (g)	1.21 TYP.

SSOP64-P-525-0.80-K



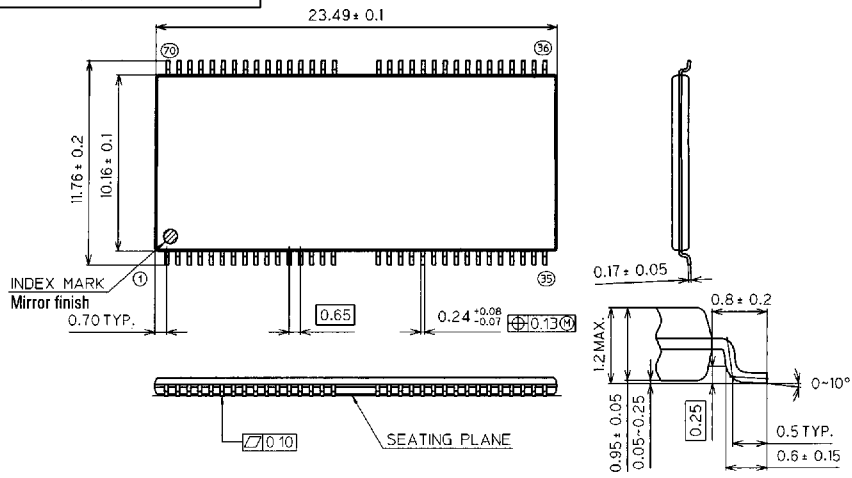
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5μm or more
Package weight (g)	1.34 TYP.

2. PACKAGE OUTLINES AND DIMENSIONS

(1) PLASTIC TSOP(Type II)(cont.)

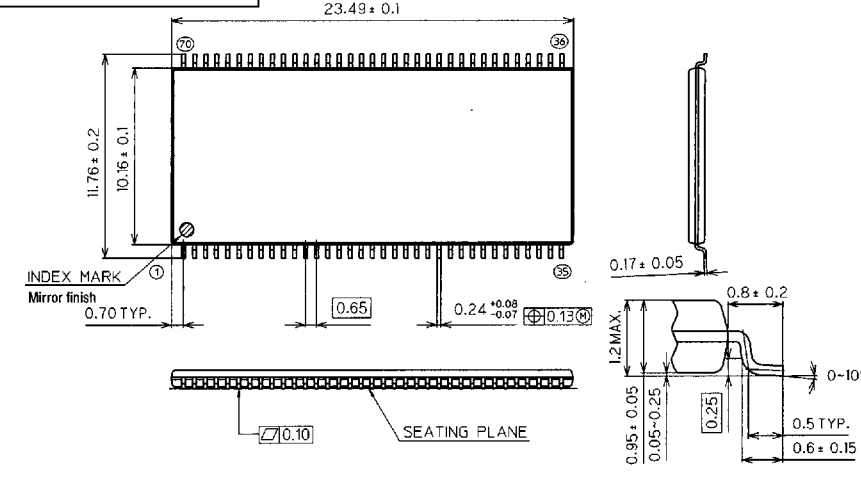
(Unit: mm)

TSOPII70/64-P-400-0.65-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5μm or more
Package weight (g)	TYP

TSOPII70-P-400-0.65-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5μm or more
Package weight (g)	TYP