

DESCRIPTION

This family is a 16M bit dynamic RAM organized 2,097,152 x 8-bit configuration with Fast Page mode CMOS DRAMs. Fast Page mode offers high speed random access of memory cells within the same row. The circuit and process design allow this device to achieve high performance and low power dissipation. Optional features are access time(60,70 or 80ns) and refresh cycle(2K Ref. or 4K Ref.) and package type (SOJ or TSOP-II) and power consumption (Normal or Low power with self refresh).

Hyundai's advanced circuit design and process technology allow this device to achieve high bandwidth, low power consumption and high reliability.

ORDERING INFORMATION

Part Number	Ref.	Power	Pkg.
HY5117800BJ	2K		SOJ
HY5117800BSLJ	2K	SL-part	SOJ
HY5117800BT	2K		TSOP-II
HY5117800BSLT	2K	SL-part	TSOP-II
HY5116800BJ	4K		SOJ
HY5116800BSLJ	4K	SL-part	SOJ
HY5116800BT	4K		TSOP-II
HY5116800BSLT	4K	SL-part	TSOP-II

* Reverse TSOP-II packages are also available

FEATURES

- Part Number Information
 - HY5117800B: 2K Ref.
 - HY5116800B: 4K Ref.

- Max. Active Power Dissipation

Speed	2K	4K
60	660 mW	550 mW
70	550 mW	495 mW
80	495 mW	440 mW

- Fast access time and cycle time

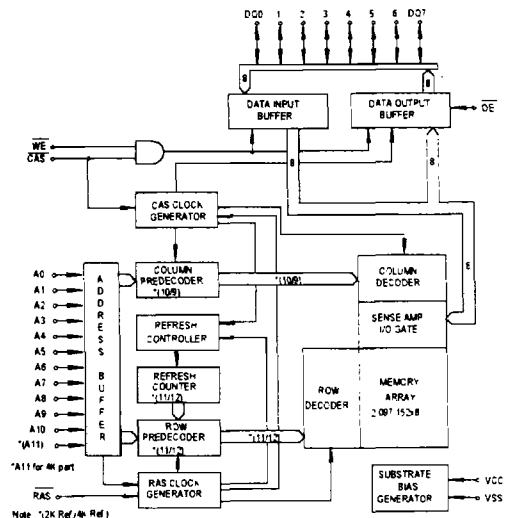
Speed	tRAC	tCAC	tPC
60ns	60ns	15ns	40ns
70ns	70ns	20ns	45ns
80ns	80ns	20ns	50ns

- Fast Page Mode Operation
- Single power supply of 5.0V ± 10%
- Read-Modify-Write Capability
- Early Write or Output Enable controlled write
- TTL compatible inputs and outputs
- /CAS-before-/RAS, /RAS-only, Hidden and Self Refresh Capability
- Refresh cycles

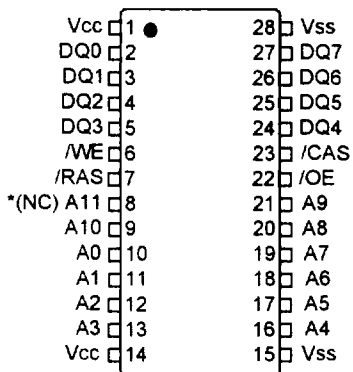
Part No.	Ref.	Normal	SL-part
HY5117800B	2K	32ms	256ms
HY5116800B	4K	64ms	

- JEDEC standard pinout
 - 28-pin Plastic SOJ (300 mil)
 - 28-pin Plastic TSOP-II (300mil)

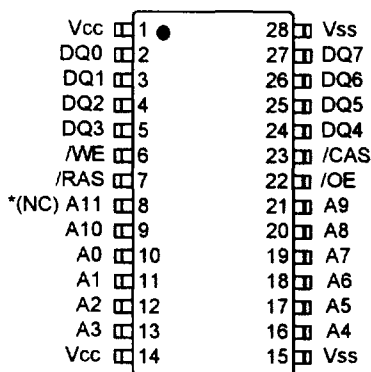
BLOCK DIAGRAM



PIN CONFIGURATION (Marking Side)



28-pin Plastic SOJ (300mil)



28-pin Plastic TSOP-II (300mil)

*.(N.C) : For 2K Refresh product

PIN DESCRIPTION

/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
/OE	Output Enable
A0-A11	Address Inputs (4K Product)
A0-A10	Address Inputs (2K Product)
DQ0-DQ7	Data Input/Output
Vcc	Power (+5.0V)
Vss	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin relative to VSS	-1.0 to 7.0	V
VCC	Voltage on Vcc relative to VSS	-1.0 to 7.0	V
Ios	Short Circuit Output Current	50	mA
Pd	Power Dissipation	1.0	W
TSOLDER	Soldering Temperature · Time	260 · 10	°C · sec

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Power Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	VCC+1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

Note: All voltages are referenced to VSS.

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DC CHARACTERISTICS

($T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5.0\text{V} \pm 10\%$ and $V_{SS}=0\text{V}$, unless otherwise noted.)

Symbol	Parameter	Test Condition	Speed/ Power	Max. Current		UNIT
				2K Ref	4K Ref	
I _{CC1}	Operating Current	/RAS and /CAS cycling t _{RC} =t _{RC} (min.)	60 70 80	120 100 90	100 90 80	mA
I _{CC2}	TTL Standby Current	/RAS=/CAS ≥ V _{IH} other inputs ≥ V _{SS}	SL-part	2 1	2 1	mA
I _{CC3}	/RAS-only Refresh Current	/CAS=V _{IH} , /RAS cycling t _{RC} =t _{RC} (min.)	60 70 80	120 100 90	100 90 80	mA
I _{CC4}	Fast Page mode Current	/RAS=V _{IL} , /CAS, Address cycling t _{PC} =t _{PC} (min.)	60 70 80	80 70 60	70 60 50	mA
I _{CC5}	CMOS Standby Current	/RAS = /CAS ≥ V _{CC} -0.2V	SL-part	1 300	1 300	mA μA
I _{CC6}	/CAS-before- /RAS Refresh Current	/RAS and /CAS cycling t _{RC} =t _{RC} (min.)	60 70 80	120 100 90	100 90 80	mA
I _{CC7}	Battery Back-up Current (SL-part)	t _{RC} =125 μs(2K Ref), 62.5 μs(4K Ref) /CAS = CBR cycling or 0.2V /OE & /WE=V _{CC} - 0.2V Address =V _{CC} -0.2V or 0.2V DQ0-DQ7=V _{CC} -0.2V, 0.2V or open	t _{RAS} ≤ 300ns	300	300	μA
			t _{RAS} ≤ 1 μs	400	400	μA
I _{CC8}	Self Refresh Current (SL-part)	/RAS & /CAS = 0.2V Other pins are same as I _{CC7}		300	300	μA

Symbol	Parameter	Test condition	Min.	Max.	UNIT
I _I	Input Leakage current (Any Input Pin)	V _{SS} ≤ V _{IN} ≤ V _{CC} + 1.0 All other pins not under test=V _{SS}	-10	10	μA
I _O	Output Leakage current (Any Input Pin)	V _{SS} ≤ V _{OUT} ≤ V _{CC} /RAS & /CAS at V _{IH}	-10	10	μA
V _{OL}	Output Low Voltage	I _{OL} = 4.2mA	-	0.4	V
V _{OH}	Output High Voltage	I _{OH} = -5.0mA	2.4	-	V

NOTE

- I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on output loading and cycle rates(t_{RC} and t_{PC}).
- Specified values are obtained with outputs unloaded.
- I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, I_{CC6}, address can be changed only once while /RAS=V_{IL}. In I_{CC4}, address can be changed maximum once while /CAS=V_{IH} within one Fast Page mode cycle time t_{PC}.
- Only /RAS(max.) = 1 μs is applied to refresh of battery backup but t_{RAS}(max.) = 10 μs is to applied to normal functional operation.
- I_{CC5}(max.) = 300 μA, I_{CC7} and I_{CC8} are applied to SL-part only

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{cc}=5.0V ± 10% and V_{ss}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY5117800B / HY5116800B						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t _{RC}	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	t _{RWC}	Read-Modify-Write Cycle Time	155	-	170	-	200	-	ns	
3	t _{PC}	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
4	t _{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	80	-	95	-	105	-	ns	
5	t _{RAC}	Access Time from /RAS	-	60	-	70	-	80	ns	4,5,6
6	t _{CAC}	Access Time from /CAS	-	15	-	20	-	20	ns	4,5
7	t _{AA}	Access Time from Column Address	-	30	-	35	-	40	ns	4,6
8	t _{CPA}	Access Time from Column Precharge	-	35	-	40	-	45	ns	4
9	t _{CLZ}	/CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	t _{OFF}	Out Buffer Turn-Off Delay Time	0	15	0	15	0	15	ns	7
11	t _T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	2
12	t _{RP}	/RAS Precharge Time	40	-	50	-	60	-	ns	
13	t _{RAS}	/RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	t _{RASP}	/RAS Pulse Width (Fast Page Cycle)	60	100K	70	100K	80	100K	ns	
15	t _{RSH}	/RAS Hold Time	15	-	20	-	20	-	ns	
16	t _{CSH}	/CAS Hold Time	60	-	70	-	80	-	ns	
17	t _{CAS}	/CAS Pulse Width	15	10K	15	10K	20	10K	ns	
18	t _{RCD}	/RAS to /CAS Delay Time	20	45	20	50	20	60	ns	5
19	t _{RAD}	/RAS to Column Address Delay Time	15	30	15	35	15	40	ns	6
20	t _{CRP}	/CAS to /RAS Precharge Time	5	-	5	-	5	-	ns	10
21	t _{CP}	/CAS Precharge Time	10	-	10	-	10	-	ns	14
22	t _{ASR}	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	t _{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
24	t _{ASC}	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	t _{CAH}	Column Address Hold Time	10	-	15	-	15	-	ns	
26	t _{RAL}	Column Address to /RAS Lead Time	30	-	35	-	40	-	ns	
27	t _{RCS}	Read Command Set-up Time	0	-	0	-	0	-	ns	
28	t _{RCH}	Read Command Hold Time Referenced to /CAS	0	-	0	-	0	-	ns	8
29	t _{RRH}	Read Command Hold Time Referenced to /RAS	0	-	0	-	0	-	ns	8
30	t _{WCH}	Write Command Hold Time	15	-	15	-	15	-	ns	
31	t _{WP}	Write Command Pulse Width	10	-	10	-	10	-	ns	
32	t _{RWL}	Write Command to /RAS Lead Time	20	-	20	-	20	-	ns	
33	t _{CWL}	Write Command to /CAS Lead Time	20	-	20	-	20	-	ns	14
34	t _{DS}	Data-In Set-up Time	0	-	0	-	0	-	ns	9
35	t _{DH}	Data-In Hold Time	15	-	15	-	15	-	ns	9

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AC CHARACTERISTICS

(Continued)

#	SYMBOL	PARAMETER	HY5117800B / HY5116800B						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
36	tREF	Refresh Period (2048 cycles)	32	-	32	-	32	-	ms	
		Refresh Period (4096 cycles)	64	-	64	-	64	-	ms	
		Refresh Period (SL-part)	256	-	256	-	256	-	ms	
37	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	10
38	tCWD	/CAS to /WE Delay Time	45	-	50	-	50	-	ns	10,13
39	tRWD	/RAS to /WE Delay Time	85	-	95	-	105	-	ns	10
40	tAWD	Column Address to /WE Delay Time	55	-	60	-	65	-	ns	10
41	tCSR	/CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	15
42	tCHR	/CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	16
43	tRPC	/RAS to /CAS Precharge Time	5	-	5	-	5	-	ns	
44	tCPT	/CAS Precharge Time (CBR Counter Test)	30	-	35	-	40	-	ns	12
45	tROH	/RAS Hold Time Reference to /OE	10	-	10	-	10	-	ns	
46	tOEA	/OE Access Time	-	15	-	20	-	20	ns	
47	tOED	/OE to Data Delay Time	15	-	20	-	20	-	ns	
48	tOEZ	Output Buffer Turn Off Delay Time from /OE	0	15	0	15	0	15	ns	7
49	tOEH	/OE Command Hold Time	15	-	20	-	20	-	ns	
50	tCPWD	/WE Delay Time from /CAS Precharge	55	-	65	-	75	-	ns	10
51	tRHCP	/RAS Hold Time from /CAS Precharge	40	-	40	-	50	-	ns	
52	tWRP	/WE to /RAS Precharge Time(CBR cycle)	10	-	10	-	10	-	ns	
53	tWRH	/WE to /RAS Hold Time (CBR cycle)	10	-	10	-	10	-	ns	
54	tRASS	/RAS Pulse Width (Self Refresh)	100	-	100	-	100	-	μs	
55	tRPS	/RAS Precharge Time (Self Refresh)	110	-	130	-	150	-	ns	
56	tCHS	/CAS Hold Time (Self Refresh)	-50	-	-50	-	-50	-	ns	

NOTE

1. An initial pause of 200 μs is required after power-up followed by 8 /RAS only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CBR refresh cycles instead of 8 /RAS only refresh cycles are required.
2. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min.) and VIL(max.)
3. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (TA = 0 to 70 °C) is assured.
4. Measured at VOH=2.4V and VOL=0.4V with a load equivalent to 2 TTL loads and 100pF.
5. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC
6. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA
7. tOFF(max.) and tOEZ(max.) define the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referred to /CAS leading edge in early write cycles and to /WE leading edge in Read-Modify-Write cycles.
10. tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS ≥ tWCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If tCWD ≥ tCWD(min.), tRWD ≥ tRWD(min.) and tCPWD ≥ tCPWD(min.), then the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
11. tASC and tCAH are referred to the earlier /CAS falling edge.
12. tCP and tCPT are measured when /CAS is high state.
13. tCWD is referred to the later /CAS falling edge at Read-Modify-Write cycle.
14. tCWL must be satisfied by /CAS for 8-bit access cycles.
15. tCSR is referred to the earlier /CAS falling low before /RAS transition low.
16. tCHR is referred to the later /CAS rising high after /RAS transition low.

CAPACITANCE

(TA=25 °C, Vcc=5.0V ± 10%, Vss=0V and f = 1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0 - A11)	-	5	pF
CIN2	Input Capacitance (/RAS, /CAS, /WE, /OE)	-	7	pF
CDQ	Data Input /Output Capacitance (DQ0 - DQ7)	-	7	pF

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