DC Brushless Motor Driver Series

Built-in Speed Control, 3 Hall Sensors Three-Phase Brushless Motor Driver

BM62380MUV

General Description

BM62380MUV is sine wave driver IC for three-phase brushless motor driver with 40 V power supply voltage rating and 2.0 A output current rating. It detects the rotor position by 3 Hall sensors. In addition, it has a speed feedback control function, and controls output PWM Duty by adjusting the rotational frequency characteristics for the input PWM signal and the rotational frequency affected from motor.

Features

- Speed Control on PWM Duty Input
- Low ON Resistance DMOS Output
- Built-in Boost Voltage Circuit
- 3 Hall Sine Wave Drive
- Automatic Lead Angle Control
- Motor Pole Select Function
- Soft Start Function
- Current Limit Function
- Power Save Function
- Direction of Rotation Setting
- Short Brake Control
- Speed Feedback Control
- Able to set Motor Rotation Speed Table and Various Parameters with the built-in OTP
- Built-in Several Protection Functions (Motor Lock Protection [MLP], High Speed Rotation Protection, Over Voltage Lock Out [OVLO], Under Voltage Lock Out [UVLO], Thermal Shutdown [TSD], Over Current Protection [OCP])

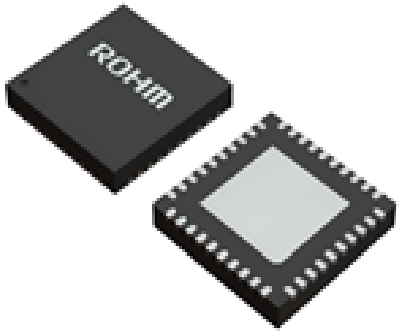
Application

- Fan Motor
- Other General Consumer Equipment

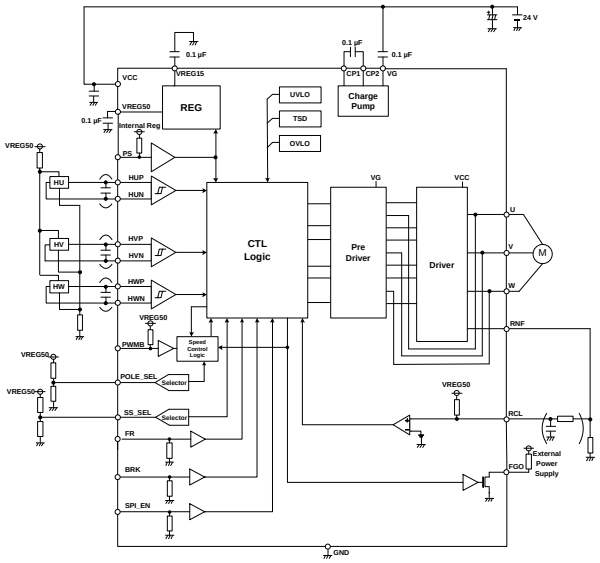
Key Specifications

- Operating Supply Voltage Range: 8 V to 28 V
- Output current rating: 2.0 A
- Output ON Resistance (top & bottom total): 0.6 Ω (Typ)
- Output PWM Frequency: 40 kHz (Typ)
- Standby Current: 0.6 mA (Typ)
- Operating Temperature Range: -40 °C to +85 °C

Package	W (Typ) x D (Typ) x H (Max)
VQFN040V6060	6.00 mm x 6.00 mm x 1.00 mm



Typical Application Circuit

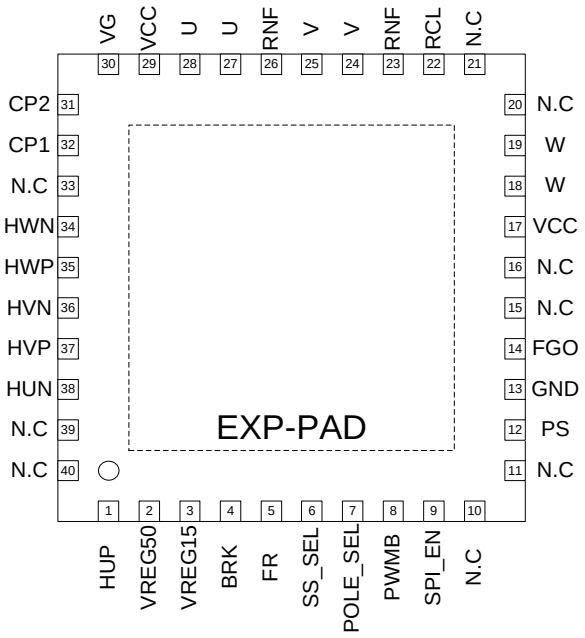


○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays

Contents

Pin Configurations

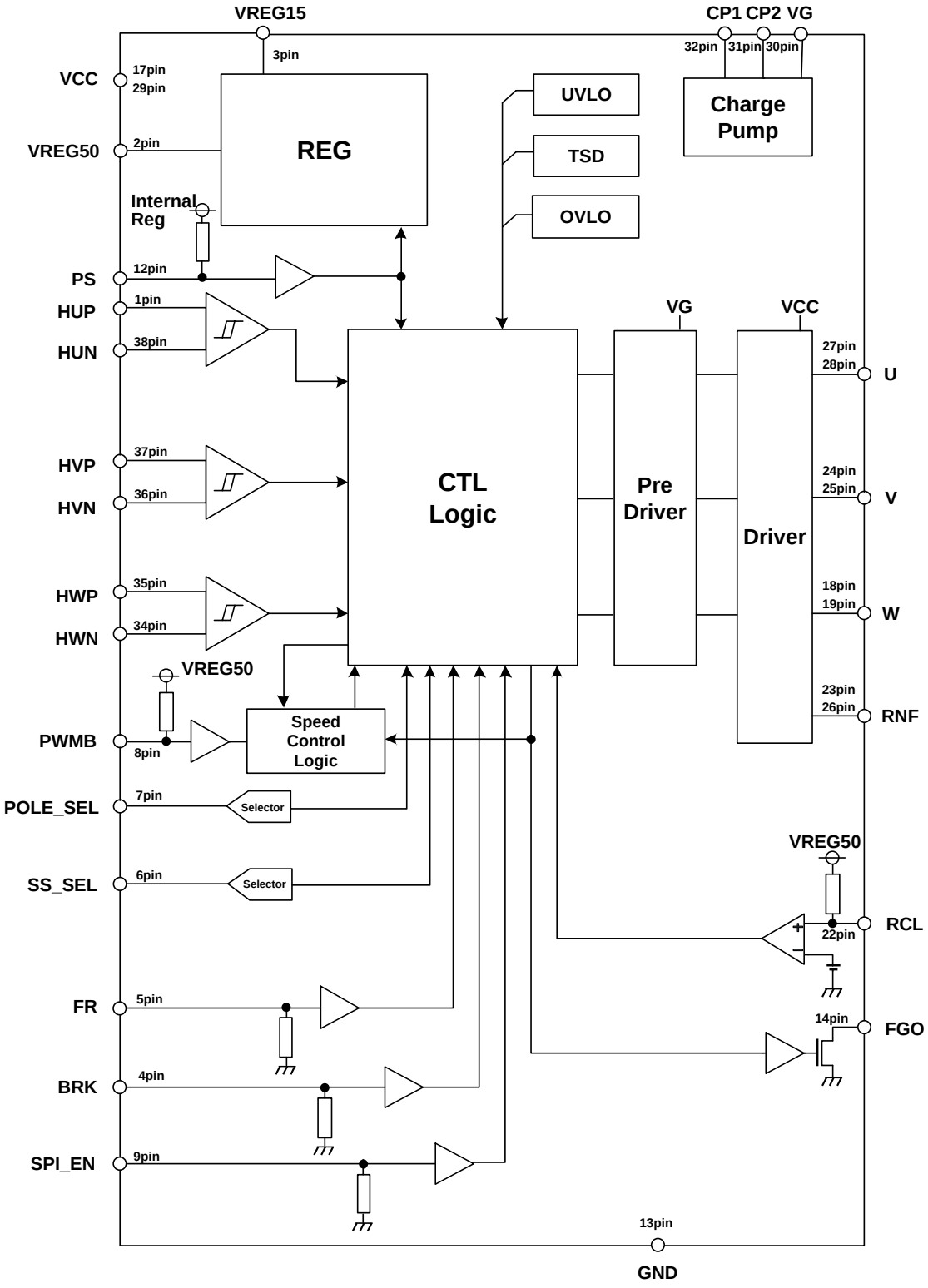
(TOP VIEW)



Pin Description

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	HUP	U phase hall input +	21	N.C.	N.C. (OPEN)
2	VREG50	Standard voltage output	22	RCL	Output current detection voltage input
3	VREG15	Internal power supply output for logic circuit	23	RNF	Pin for connecting the current sense resistor.
4	BRK	Brake control / SPI communication data input-output	24	V	V Phase output
5	FR	Rotation direction setting	25	V	V Phase output
6	SS_SEL	Soft Start setting	26	RNF	Pin for connecting the current sense resistor.
7	POLE_SEL	Motor Pole setting	27	U	U Phase output
8	PWMB	PWM input (negative logic) / SPI communication clock input	28	U	U Phase output
9	SPI_EN	SPI communication setting	29	VCC	Power supply
10	N.C.	N.C. (OPEN)	30	VG	Boost output
11	N.C.	N.C. (OPEN)	31	CP2	Capacitor connection for boost circuit 2
12	PS	Power Save input	32	CP1	Capacitor connection for boost circuit 1
13	GND	Ground	33	N.C	N.C. (OPEN)
14	FGO	Rotating speed pulse signal output	34	HWN	W phase hall input -
15	N.C.	N.C. (OPEN)	35	HWP	W phase hall input +
16	N.C.	N.C. (OPEN)	36	HVN	V phase hall input -
17	VCC	Power supply	37	HVP	V phase hall input +
18	W	W Phase output	38	HUN	U phase hall input -
19	W	W Phase output	39	N.C.	N.C. (OPEN)
20	N.C.	N.C (OPEN)	40	N.C.	N.C. (OPEN)
Back Side	EXP-PAD	Connect the EXP-PAD to the GND.			

Block Diagram



Absolute Maximum Ratings (Ta= 25 °C)

Parameters	Symbol	Rating	Unit
Power Supply Voltage (VCC)	V_{CC}	40	V
VG Voltage	V_G	40	V
Driver Output Current (U, V, W)	I_{OMAX}	2.0	A
Output Voltage (U, V, W)	V_{OMAX}	40	V
RNF Pin Voltage	V_{RNF}	0.7	V
FGO Pin Voltage	V_{FGO}	30	V
FGO Pin Current	I_{FGO}	10	mA
VREG50 Pin Current	I_{VREG50}	-30	mA
RCL Pin Voltage	V_{RCL}	4.5	V
Control Input Pin Voltage*(Note 1)*	V_{IN1}	7	V
Hall Input Pin Voltage*(Note 2)*	V_{IN2}	7	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) The SS_SEL, POLE_SEL, PWMB, PS, BRK, FR, SPI_EN pins.

(Note 2) The HUP, HUN, HVP, HVN, HWP, HWN pins.

Thermal Resistance*(Note 3)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 5)*	2s2p*(Note 6)*	
VQFN040V6060				
Junction to Ambient	θ_{JA}	101.4	23.7	°C/W
Junction to Top Characterization Parameter*(Note 4)*	Ψ_{JT}	5.0	3.0	°C/W

(Note 3) Based on JESD51-2A(Still-Air).
(Note 4) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 5) Using a PCB board based on JESD51-3.
(Note 6) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 7)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 7) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Operation Temperature	Topr	-40	+25	+85	°C
Operating Supply Voltage (VCC)	V_{CC}	8.0	24.0	28.0	V
Control Input Pin Voltage*(Note 8)*	V_{IN1}	0	-	V_{VREG50}	V

(Note 8) The SS_SEL, POLE_SEL, PWMB, BRK, FR, SPI_EN pins.

Electrical Characteristics (Unless otherwise specified V_{CC}=24 V Ta=25 °C)

Parameters	Symbol	Min	Typ	Max	Unit	Conditions
<Whole>						
Circuit Current	I_{CC}	-	14	28	mA	PS=0 V
Standby Current	I_{STBY}	-	0.6	1.2	mA	PS=5 V
VREG50 Voltage	V_{VREG50}	4.5	5.0	5.5	V	I_{OUT}=-10 mA
VREG15 Voltage	V_{VREG15}	1.35	1.50	1.65	V	
< Boost Circuit >						
VG Voltage	V_G	V_{CC}+4.5	V_{CC}+5.5	V_{CC}+6.5	V	
< Driver Output >						
Output On Resistance	R_{ON}	-	0.6	0.9	Ω	I_{OUT}=±1.0 A (Upper+Lower)
Output PWM Frequency	f_{PWM}	36	40	44	kHz	
<Hall Input>						
Input Bias Current	I_{HALL}	-2.0	-0.1	+2.0	μA	HUP=0 V, HUN=0 V HVP=0 V, HVN=0 V HWP=0 V, HWN=0 V
Common Mode Input Voltage Range	V_{HALLCM}	0	-	V_{VREG50}-1.7	V	
Input Voltage Range	$V_{HALLRNG}$	0	-	V_{VREG50}	V	
Minimum Input Voltage	$V_{HALLMIN}$	50	-	-	mV_{P-P}	
Hall Input Hysteresis Level+	V_{HYSP}	2	12	22	mV	
Hall Input Hysteresis Level-	V_{HYSN}	-22	-12	-2	mV	
<PS>						
Input Current	I_{PS}	-82.5	-55.0	-27.5	μA	PS=0 V
Input High Voltage	V_{STBY}	3.8	-	5.0	V	Power Save
Input Low Voltage	V_{ENA}	0	-	0.5	V	Drive
<FR>						
Input Current	I_{FR}	25	50	75	μA	FR=V_{VREG50}
Input High Voltage	V_{FRH}	V_{VREG50}-1.2	-	V_{VREG50}	V	U→V→W
Input Low Voltage	V_{FRL}	0	-	0.8	V	U→W→V
<BRK>						
Input Current	I_{BRK}	25	50	75	μA	BRK=V_{VREG50}
Input High Voltage	V_{BRKH}	V_{VREG50}-1.2	-	V_{VREG50}	V	Short brake
Input Low Voltage	V_{BRKL}	0	-	0.8	V	Drive
<SPI_EN>						
Input High Voltage	V_{SPI_ENH}	V_{VREG50}-1.0	-	V_{VREG50}	V	OTP write mode
Input Low Voltage	V_{SPI_ENL}	0	-	0.8	V	Drive mode

For parameters involving current, positive notation means inflow of current to the IC while negative notation means outflow of current from the IC

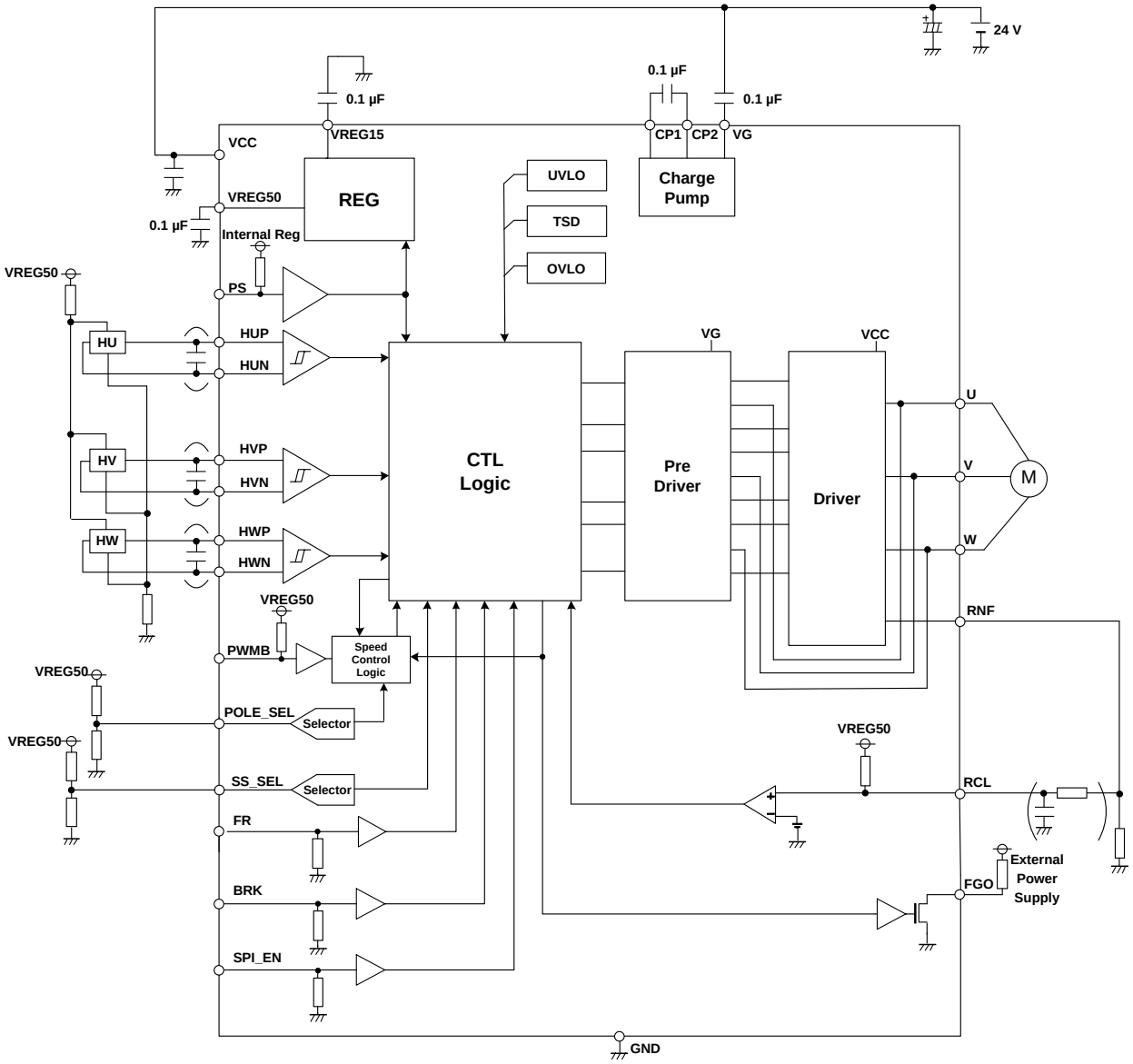
Electrical Characteristics - Continued (Unless otherwise specified V_{CC}=24 V Ta=25 °C)

Parameters	Symbol	Min	Typ	Max	Unit	Conditions
< Control Input: SS_SEL, POLE_SEL>						
Input Current	I_{IN}	-1.2	-	+1.2	μA	
<Speed Control Input: PWMB>						
Input Current	I_{PWMB}	-75	-50	-25	μA	PWMB=0 V
Input High Voltage	V_{PWMBH}	V_{VREG50}-1.2	-	V_{VREG50}	V	
Input Low Voltage	V_{PWMBL}	0	-	0.8	V	
Input Frequency Range	f_{PWMB}	1	-	50	kHz	
<FGO Output>						
Output Low Voltage	V_{FGOL}	0	0.1	0.3	V	I_{FGO}=+3 mA
Output Leak Current	I_{FGLEAK}	-	-	1	μA	FGO=30 V
<Current limit: RCL>						
Input Current	I_{RCL}	-70	-40	-20	μA	RCL=0 V
Current Limit Detect Voltage	V_{CL}	0.18	0.20	0.22	V	
<UVLO>						
VCC UVLO Release Voltage	V_{UVH}	6.5	7.0	7.5	V	
VCC UVLO Lockout Voltage	V_{UVL}	5.5	6.0	6.5	V	
VG UVLO Voltage	V_{UVVG}	V_{CC}+2.0	V_{CC}+3.0	V_{CC}+4.0	V	
<OVLO>						
OVLO Release Voltage	V_{OVL}	28.5	30.0	31.5	V	
OVLO Lockout Voltage	V_{OVH}	29.5	31.0	32.5	V	
<Motor Lock Protection, Several Protections>						
Motor Lock Protection Detect Time	t_{LK_DET}	0.45	0.50	0.55	s	
Protect Time	t_{LK_PRT}	4.5	5.0	5.5	s	Several Protections *(Note 9)*

For parameters involving current, positive notation means inflow of current to the IC while negative notation means outflow of current from the IC.

(Note 9) Motor Lock Protection (MLP), High Speed Rotation Protection, Over Voltage Lock Out (OVLO), Thermal Shutdown (TSD), Over Current Protection (OCP).

Application Example



Board Design Note

1. The IC power, the IC ground, the motor outputs, and the motor ground (RNF) lines are made as wide as possible.
2. The IC ground is arranged to the ground connector of PCB as close as possible.
3. The bypass capacitor connected to the VCC pin is placed as close as possible to the VCC pin.

Description of Pin Functions

1. Power Supply Pin (VCC)
   - In order to decrease the AC impedance in wide frequency bandwidth, place a ceramic capacitor (0.01 µF to 0.1 µF) in parallel with the electrolytic capacitor.
   - The motor's Back EMF and PWM switching noise may affect the VCC pin voltage. To regulate or stabilize the V_{CC} voltage supply, place the bypass capacitor to the IC pin as close as possible. Increase the value of the bypass capacitor if the IC needs to drive higher current or if it is experiencing higher Back EMF. V_{CC} must not exceed the absolute maximum ratings. It is effective to add a zener diode not exceeding the absolute maximum ratings. Take note that reversing the voltages of the VCC and the GND may destroy the IC.

2. Ground Pin (GND)
   The GND must have impedance as low as possible and must always be maintained as the lowest voltage potential. This is to reduce the noise caused by the switching current, and to make the internal voltages stable. Avoid having common impedance with other devices GND line.

3. Boost Pins (CP1, CP2, VG)
   Built-in charge pump circuit (for High side FET drive) generates boost voltage VG=V_{CC}+5.5 V (Typ) by connecting capacitor between the CP1 pin and the CP2 pin and between the VG pin and the VCC pin. It is recommended to use capacitor of 0.1 µF or more.

4. Driver Output Pins (U, V, W)
   When driver output converts "L"→"H" or "H"→"L", for example when synchronous rectification PWM is operating, a dead time (1µs [Typ]) will be set to prevent simultaneous ON of output top and bottom MOS. Please be careful about the following points in using driver output.
   - Wiring should be thick, short, and low impedance due to motor drive current.
   - In applying steep pulse signal or voltage like as surge more than the ratings, it might cause destruction of IC. Do not exceed ratings.
   - When using large current, in case that driver current changes considerably toward positive and negative (when Back EMF is large), malfunction or destruction of IC might occur. Please add Schottky diode to the driver output pin. To reduce the noise by switching current and to stabilize the reference voltage of inside the IC, make wiring impedance from this pin as low as possible and set potential the lowest at any operating condition. Also, do not hold common impedance with other GND pattern.

5. Regulator Output Pins (VREG50, VREG15)
   The VREG50 pin is 5.0 V (Typ) for standard voltage output, and the VREG15 pin is 1.5 V (Typ) for internal power supply output for logic circuit. It is recommended to connect 0.1 µF to 1 µF capacitor to each pin. When using the VREG50 pin as power supply for Hall device bias, be careful that the drain current from the VREG50 pin does not exceed the absolute maximum ratings. And connect nothing to the VREG15 pin except a capacitor.

6. Power Save Pin (PS)
   The PS pin controls ON/OFF state on each phase output. The Power Save state has a preference to other control input signal and it turns off regulator output (VREG50, VREG15). Furthermore, the PS pin is pulled up to internal power supply by 101 kΩ (Typ) resistor.

Table 1. PS Pin Setting Table

PS pin Setting	Function
Low	Drive
High / Open	Power Save

7. Motor Pole Setting Pin (POLE_SEL)
   Motor Pole can be set at the POLE_SEL pin by applying the appropriate voltage via resistive voltage dividers from VREG50 (5 V [Typ]). High accuracy is needed for setting, and it is recommended to use 5 % or less precision resistors. Refer to P. 17 regarding the Motor Pole setting method.

8. Soft Start Setting Pin (SS_SEL)
   This IC sets Soft Start step time at the SS_SEL pin by applying the appropriate voltage via resistive voltage dividers from VREG50 (5 V [Typ]). High accuracy is needed for setting, and it is recommended to use 1 % or less precision resistors. Refer to P. 16 regarding the time setting method of Soft Start.

9. Speed Control Input Pin (PWMB)
   The PWM signal Duty for the PWMB pin can control motor speed (Negative logic). The PMWB pin is pulled up to VREG50 by 100 kΩ (Typ) resistor. Refer to P. 19 regarding the rotation speed setting of Speed feedback control.

Description of Pin Functions – continued

10. Hall Input Pins (HUP, HUN, HVP, HVN, HWP, HWN)
    - Hall comparator is designed with hysteresis (±12 mV [Typ]) in order to prevent malfunction due to noise.
    - Case of Hall element: Set the bias current for the Hall element so that the amplitude of Hall input voltage is the minimum input voltage ($V_{HALLMIN}$) or more. It is recommended to connect a ceramic capacitor with about 100 pF to 0.01 µF value between the differential input pins of the Hall comparator. Hall comparator has common mode input voltage range (V_{HALLCM}). Set the bias voltage within the V_{HALLCM}.
    - Case of Hall IC: Connect the HUP pin, the HVP pin and the HWP pin to each output of Hall ICs and input within the input voltage range ($V_{HALLRNG}$). If the output of the Hall IC is an open drain, pull up it to VREG50 voltage by external resistance. Input a reference voltage within V_{HALLCM} into the HUN pin, the HVN pin and the HWN pin (e.g., input a half voltage of VREG50 voltage).

11. Resistor Connection Terminal for Detecting Output Current Pin (RNF)
    Insert resistor for detecting current 0.12 Ω to 0.50 Ω between the RNF pin and GND. When deciding resistor value, it should be careful that consumption electricity of resistor for detecting current I_{OUT}^2 x R[W] does not exceed rating of resistor. In addition, please do not have common impedance with other GND patterns by using low impedance wiring, since motor drive current flows into pattern of the RNF pin to resistor for detecting current to GND. In case that RNF voltage goes over rating (0.7 V), circuit malfunction might occur. Therefore, please do not exceed rating. When the RNF pin is shorted to GND, big current flows due to a lack of normal current limit operation. Please be careful that OCP or TSD might operate in that case.

12. Output Current Detect Pin (RCL)
    The RCL pin is an input pin for the current limit comparator. Take into consideration the wiring pattern on the PCB to reduce noise when designing PCB layout. Note that the RCL pin is pulled up to VREG50 by 250 kΩ (Typ) resistor. Additionally, when the RCL pin is shorted to GND, big current might flow due to a lack of normal current limit operation. Please be careful that OCP or TSD might operate in that case.

13. FG Output Pin (FGO)
    The FGO pin outputs FG signal that is generated by Hall signal. No output in Power Save mode. The FGO pin is open drain output, so this pin must be pulled up to external voltage by 10 kΩ to 100 kΩ resistor. Note that FGO voltage and current should not exceed the maximum absolute ratings.

14. SPI Communication Setting Pin (SPI_EN)
    When the SPI_EN pin is connected to VREG50, the BRK pin and the PWMB pin are switched to SPI communication pins. Refer to the Application Note about OTP Writing Application Circuit using SPI communication. When you do not use SPI communication, connect the SPI_EN pin to the GND. The SPI_EN pin is pulled down by 61.5 kΩ (Typ) resistor.

15. Rotation Direction Setting Pin (FR)
    The FR pin controls rotational direction change. Phase driving sequence is U→V→W when FR=High, and U→W→V when FR=Low or Open. Changing the rotational direction during motor rotation is not recommended. If the rotational direction is changed, outputs will shift to short brake mode until the rotational speed becomes 500 rpm or less. The FR pin is pulled down by 100 kΩ (Typ) resistor.

Table 2. FR Pin Setting Table

FR pin Setting	Function
Low / Open	U→W→V
High	U→V→W

16. Brake Control Pin (BRK)
    - The BRK pin can stop a rotation. It enters short brake mode with BRK=High, wherein all outputs are "L". It cancels short brake mode when BRK=Low or Open. The BRK pin is pulled down by 100 kΩ (Typ) resistor.
    - Short brake has higher priority than other protection functions. That is why the protection function is cancelled and short brake operation is enabled when the short brake starts operation during other protection function is operating.

Table 3. BRK Pin Setting Table

BRK pin Setting	Function
Low / Open	Drive
High	Short Brake

17. Non Connection Pin (N.C.)
    No electrical connection with IC internal circuit.

Description of Operations

1. Timing Chart
It detects the rotor position by 3 Hall sensors. In addition, silent and low vibration are implemented by making the output current a sine waveform.

1.1 Timing chart of the sine wave drive on 3 Hall sensors
The timing chart of the 3 Hall sensor signals and output signals are shown below.

FR=High (U→V→W, lead angle 0°)

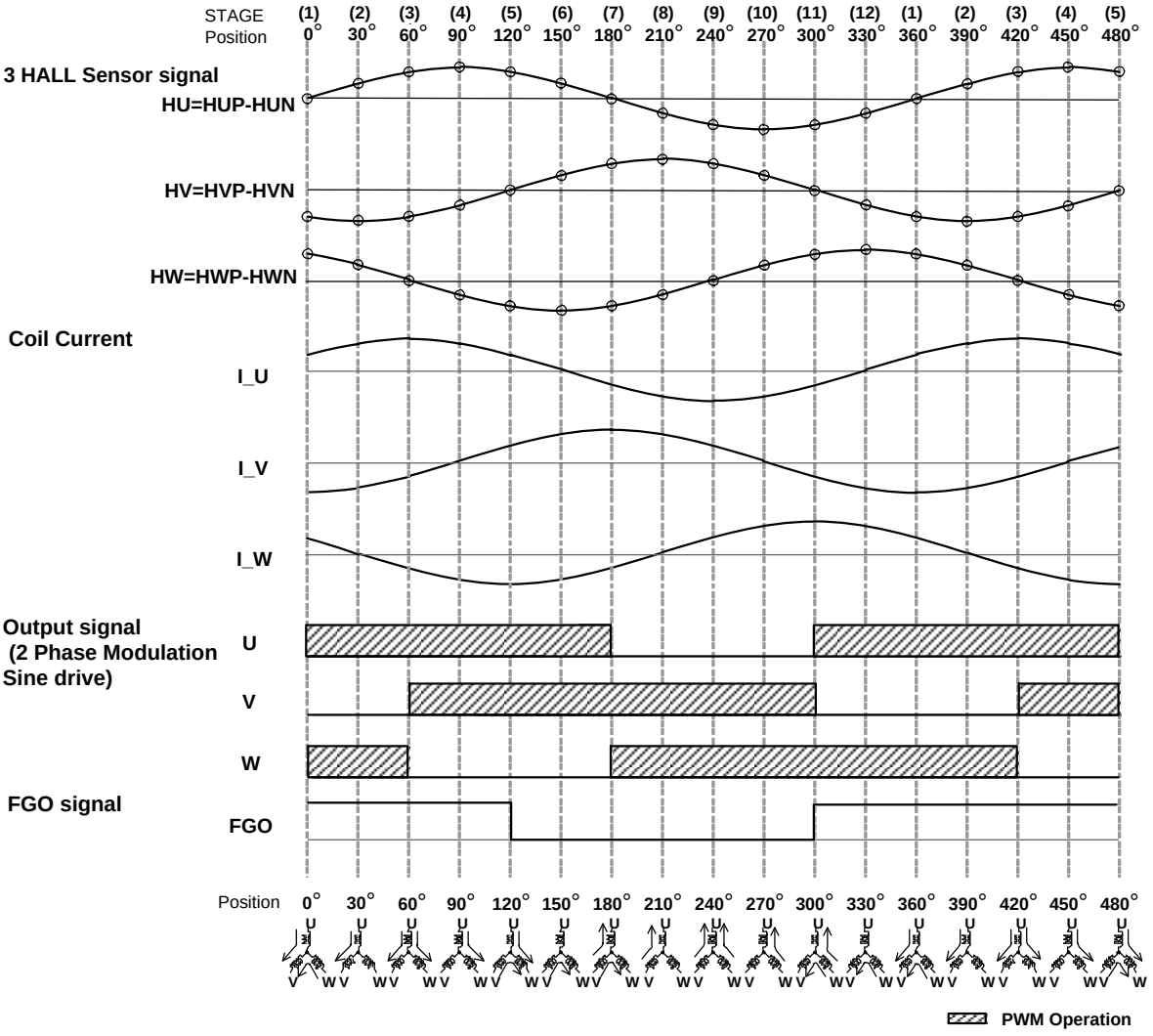


Figure 1. Timing Chart for Sine Wave Drive (FR=High)

1.1 Timing chart of the sine wave drive on 3 Hall sensors – continued

FR=Low (U→W→V, lead angle 0°)

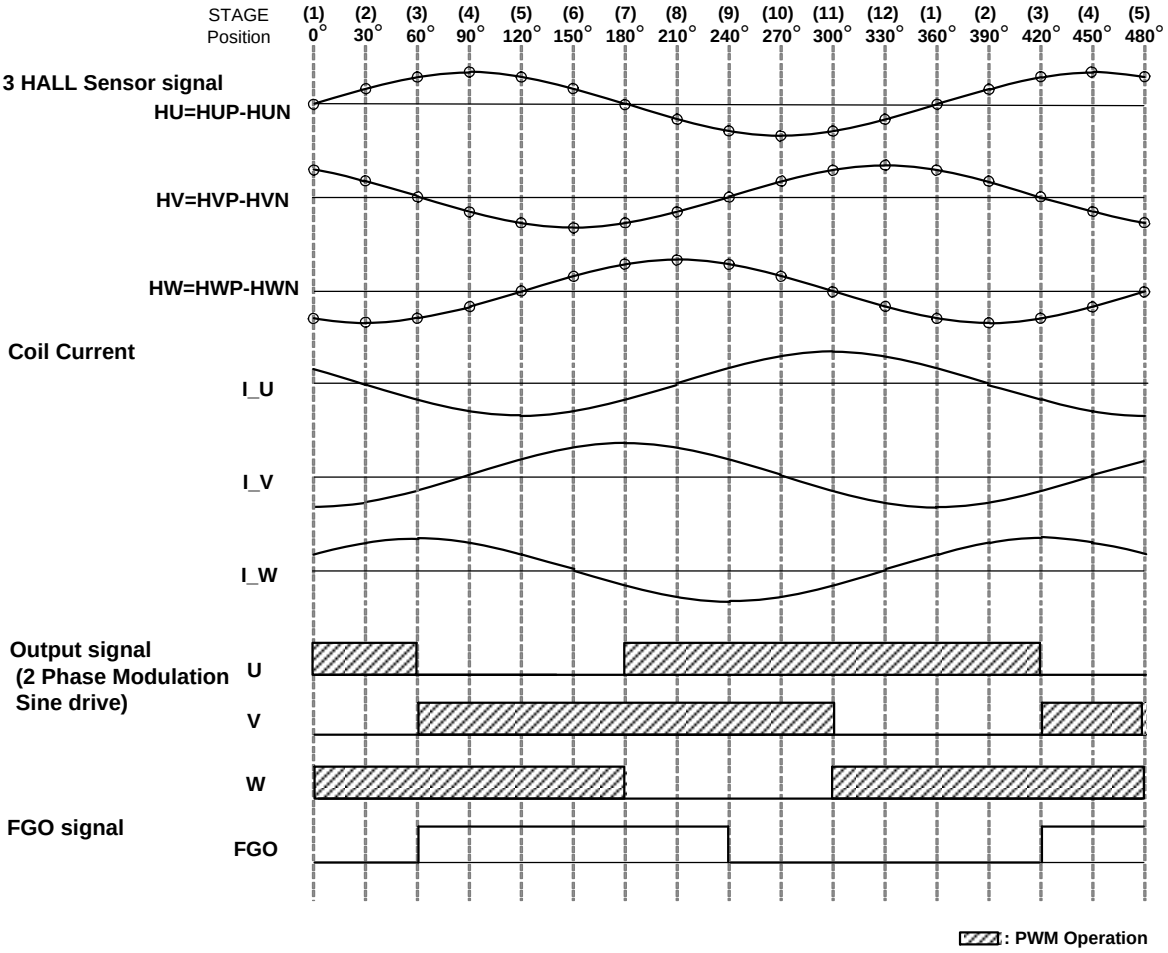


Figure 2. Timing Chart for Sine Wave Drive (FR=Low)

Adjustment of the Hall Sensor

When the Hall sensor is used, the amplitude adjustment of the Hall signal is important for a stable drive. It is necessary to detect the correct position of a motor that the amplitude of Hall signal is larger enough than the Hall input hysteresis level+ (V_{HYSP}) and Hall input hysteresis level- (V_{HYSN}). About Selections of Hall element or Hall IC, it is necessary to fully consider the sensitivity and temperature characteristics.

1. Timing Chart – continued

1.2 Energizing Logic

FR=High (U→V→W, lead angle 0°)

Table 4. Energizing Logic Table

	Input Condition			Output State		
STAGE	HU =(HUP)-(HUN)	HV =(HVP)-(HVN)	HW =(HWP)-(HWN)	U	V	W
1	Middle	Low	High	PWM	Low	PWM
2	High	Low	High	PWM	Low	PWM
3	High	Low	Middle	PWM	Low to PWM	PWM to Low
4	High	Low	Low	PWM	PWM	Low
5	High	Middle	Low	PWM	PWM	Low
6	High	High	Low	PWM	PWM	Low
7	Middle	High	Low	PWM to Low	PWM	Low to PWM
8	Low	High	Low	Low	PWM	PWM
9	Low	High	Middle	Low	PWM	PWM
10	Low	High	High	Low	PWM	PWM
11	Low	Middle	High	Low to PWM	PWM to Low	PWM
12	Low	Low	High	PWM	Low	PWM

2. Lock Protection Function (MLP: Motor Lock Protection)
When the motor is locked due to disturbance factors, the IC has a protection function that turns off all outputs for a certain period (lock protection time t_{LK_PRT}: 5.0 s [Typ]) so that the current will not continue to flow in the coil current. In addition, it has a function that automatically restarts after lock protection time. Hall signal transitions are detected as the motor rotates. But when the motor is locked, they are not detected. When they are not detected for a certain period (lock protection detect time t_{LK_DET}: 0.5 s [Typ]), the IC judges as the motor is locked. The timing chart of the Hall signal and each output phase during lock protection is shown in Figure 3.

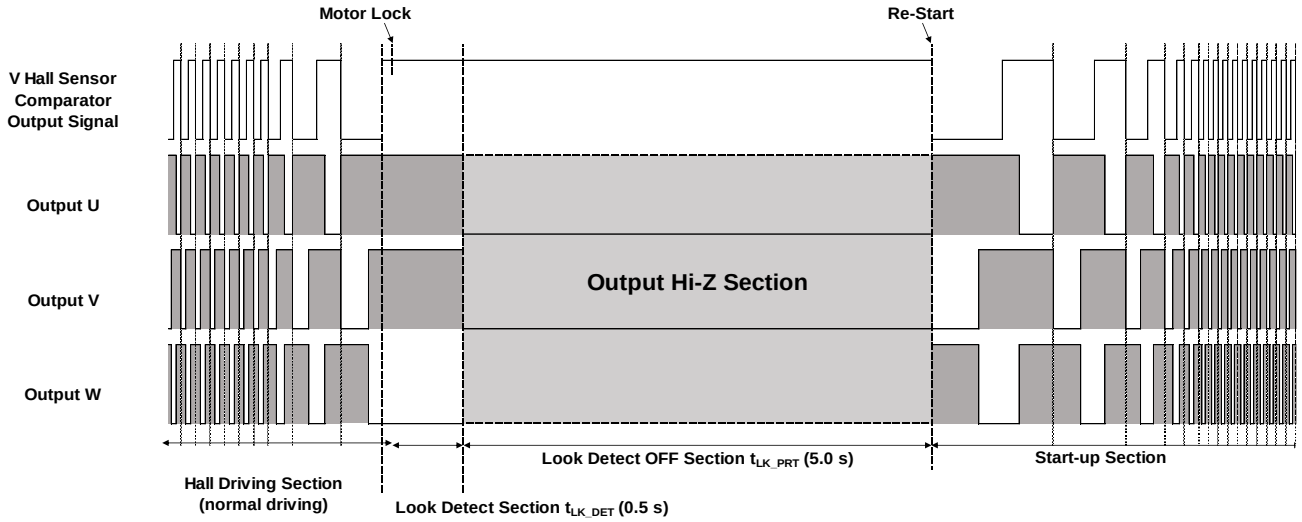


Figure 3. Timing Chart during Lock Protection

Description of Operations – continued

3. Current Limit Setting (the RCL pin)
When the IC detects the coil current is the current setting value or more, all high side FETs are turned off and cut off the current. When the current is less than the current value setting in the timing of next PWM (ON) after that, it returns to normal drive. Setting current value I_O that operates the current limit is determined on the current limit setting voltage (V_{CL}) 0.2 V (Typ) in the IC and the resistance R_1 to use for the coil current detection. Please refer to the formula shown below in the case of R_1=0.2 Ω.

$$I_O[\mathrm{A}] = V_{CL}[\mathrm{V}] / R_1[\Omega] = 0.2 / 0.2 = 1.0\ \mathrm{A}$$

$$P_C\ [W] = V_{CL}[\mathrm{V}] \times Io[\mathrm{A}] = 0.2 \times 1.0 = 0.2\ \mathrm{W}$$

When the current limit function is not used, short the RCL pin with the GND. A large current flows through the resistor R_1 to detect the coil current. Because the power consumption P_C is calculated with the formula shown above, please pay attention to the power dissipation.

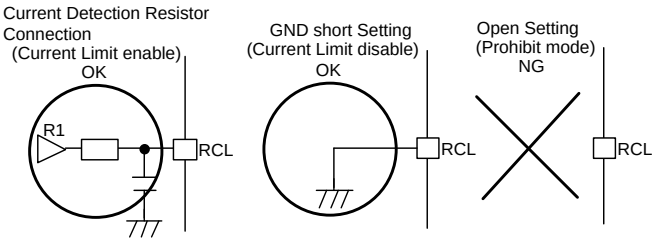


Figure 4. RCL Pin Process

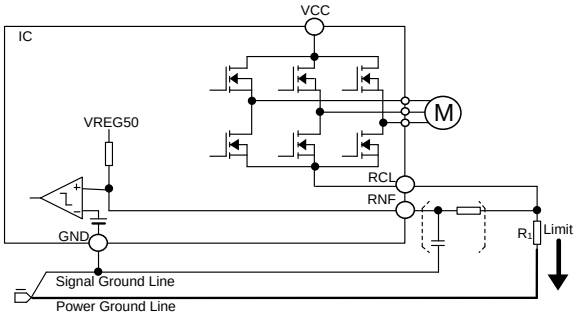


Figure 5. Small Signal and Large Current GND Line Separation

When design a PCB layout, separate the IC small signal GND line from the motor large current GND line connected to R_1 as shown in Figure 5.

4. Soft Start Time Setting (the SS_SEL pin)
When it starts from a motor stop state, there is a function to increase the VCC current gradually (Soft Start function) for controlling the inrush current. In the start-up command to start from the motor stop state, there are the start by the power supply injection, the start by the torque input (the PWMB pin), the start by the power save cancellation (the PS pin), the return from lock protection, the return from the short brake mode at the time of the rotational direction change (the FR pin), and the return from the motor stop state by each protection function (High Speed Rotation Protection, Over Voltage Lock Out, Under Voltage Lock Out and Thermal Shutdown). About the current limit during Soft Start, it maintains the sine wave drive by gradually increasing the output duty.

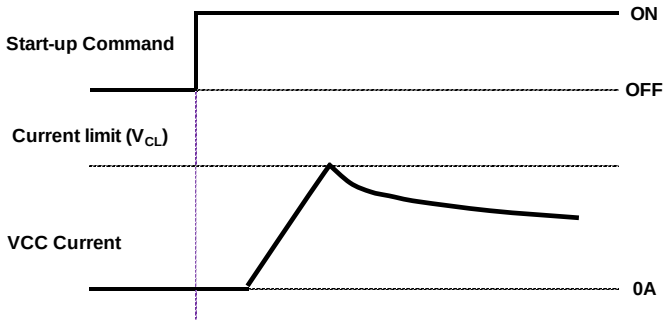


Figure 6. Timing Chart of the Coil Current Waveform at Soft Start

4. Soft Start Time Setting (the SS_SEL pin) – continued

The Soft Start function can gradually increase the current limit setting voltage in the IC. The Time for 1 step is set on the voltage of the SS_SEL pin as shown in Table 5. In addition, set it in consideration of ±10 % tolerance of the Time for 1 step. The current limit setting voltage in the IC increases for 1 step voltage 5.16 mV (Typ). Therefore, the soft start time can be calculated as follows.

$$Soft\ Start\ time\ =\ Time\ for\ 1\ step \times (V_{CL} - 51.6\ \text{mV}) / 5.16\ \text{mV}$$

For example, when SS_SEL=0 V, it is calculated as below.

$$Soft\ Start\ time\ =\ 49\ \text{ms} \times (200\ \text{mV} - 51.6\ \text{mV}) / 5.16\ \text{mV}\ =\ 1.4\ \text{s}$$

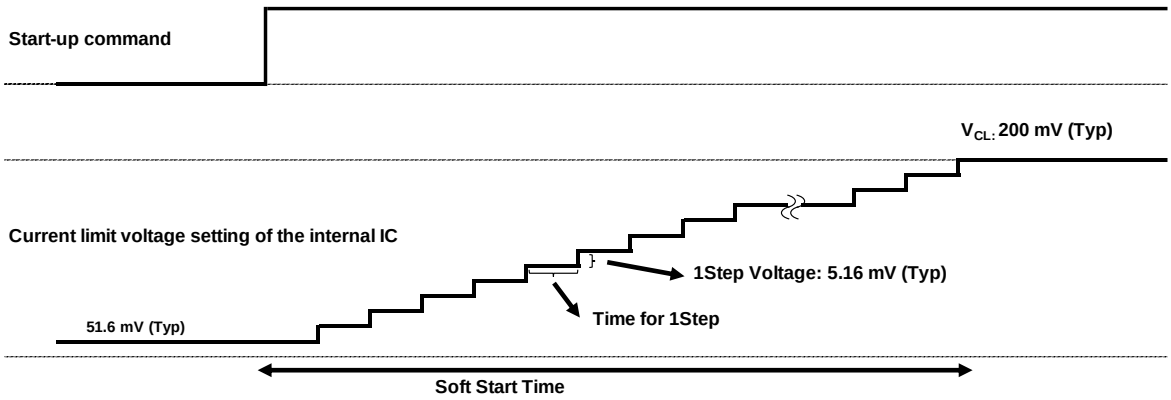


Figure 7. Timing Chart of the Current Limit Voltage Setting during Soft Start

Table 5. SS_SEL Pin Setting Table

SS_SEL pin Setting							Time for 1 step (Typ)
0.000	x	V_{VREG50}	to	0.056	x	V_{VREG50}	49 ms
0.069	x	V_{VREG50}	to	0.119	x	V_{VREG50}	98 ms
0.131	x	V_{VREG50}	to	0.181	x	V_{VREG50}	147 ms
0.194	x	V_{VREG50}	to	0.244	x	V_{VREG50}	197 ms
0.256	x	V_{VREG50}	to	0.306	x	V_{VREG50}	246 ms
0.319	x	V_{VREG50}	to	0.369	x	V_{VREG50}	295 ms
0.381	x	V_{VREG50}	to	0.431	x	V_{VREG50}	344 ms
0.444	x	V_{VREG50}	to	0.494	x	V_{VREG50}	393 ms
0.506	x	V_{VREG50}	to	0.556	x	V_{VREG50}	442 ms
0.569	x	V_{VREG50}	to	0.619	x	V_{VREG50}	491 ms
0.631	x	V_{VREG50}	to	0.681	x	V_{VREG50}	541 ms
0.694	x	V_{VREG50}	to	0.744	x	V_{VREG50}	590 ms
0.756	x	V_{VREG50}	to	0.806	x	V_{VREG50}	639 ms
0.819	x	V_{VREG50}	to	0.869	x	V_{VREG50}	688 ms
0.881	x	V_{VREG50}	to	0.931	x	V_{VREG50}	737 ms
0.944	x	V_{VREG50}	to	1.000	x	V_{VREG50}	786 ms

Description of Operations – continued

5. Motor Pole Setting (the POLE_SEL pin)
Set the POLE_SEL pin voltage based on the motor poles. Refer to Table 6 for setting. For other motor poles setting, refer to the Application Note.

Table 6. POLE_SEL Pin Setting Table

POLE_SEL pin Setting							Motor Pole (poles)
0.00	x	V_{VREG50}	to	0.13	x	V_{VREG50}	4
0.16	x	V_{VREG50}	to	0.27	x	V_{VREG50}	6
0.30	x	V_{VREG50}	to	0.41	x	V_{VREG50}	8
0.44	x	V_{VREG50}	to	0.56	x	V_{VREG50}	2
0.59	x	V_{VREG50}	to	0.70	x	V_{VREG50}	12
0.73	x	V_{VREG50}	to	0.84	x	V_{VREG50}	14
0.87	x	V_{VREG50}	to	1.00	x	V_{VREG50}	10

6. Under Voltage Lock Out (UVLO)
In extremely low supply voltage domain deviating from normal operation, it is a protection function that prevents the unexpected operations such as large current flow in drive FET by turning off all outputs intentionally. UVLO works and all outputs are turned off when V_{CC} reaches 6 V (Typ) or less in the domain less than 8 V of the recommended operating minimum voltage. And the regulator outputs (VREG50, VREG15) are turned off. UVLO circuit has hysteresis of 1 V (Typ), and UVLO is cancelled when V_{CC} reaches 7 V (Typ) or more.

7. VG Under Voltage Lock Out (VG UVLO)
When V_G reaches V_{CC}+3.0 V (Typ) or less, VG UVLO works and all outputs are turned off. VG UVLO circuit has no hysteresis.

8. Over Voltage Lock Out (OVLO)
When V_{CC} reaches 31 V (Typ) or more, OVLO works and it enters short brake mode, wherein all outputs become Low for a certain period (protect time t_{LK_PRT}: 5.0 s [Typ]). In addition, the boost function for VG voltage is turned off. OVLO circuit has hysteresis of 1 V (Typ), and OVLO is cancelled when V_{CC} reaches 30 V (Typ) or less after the protect time. This circuit has mask time of 4 µs (Typ) to prevent malfunctions.

9. High Speed Rotation Protection
When a rotating speed reaches 40,300 rpm (Typ) or more due to boost up by uncontrollable motor, it has the protection function which turn off all outputs for a certain period (protect time t_{LK_PRT}: 5.0 s [Typ]). After the Protect time, the High Speed Rotation Protection is cancelled when a rotating speed reaches less than 40,300 rpm (Typ).

10. Thermal Shutdown (TSD)
When the chip temperature reaches 175 °C (Typ) or more, TSD works and all outputs are turned off for a certain period (protect time t_{LK_PRT}: 5.0 s [Typ]). TSD circuit has hysteresis of 25 °C (Typ), and TSD is cancelled when the chip temperature drops after the protect time. Moreover, the purpose of the TSD circuit is to protect driver IC from thermal breakdown, therefore, temperature of this circuit will be over working temperature when it is started up. Thus, thermal design should have sufficient margin, so do not take continuous use and action of the circuit as a precondition.

Description of Operations – continued

11. Over Current Protection (OCP)
Over current protection is built-in in order to prevent from destruction when being shorted between output pins and also being VCC or GND shorted. Therefore, over current protection operates when the specified current or more is detected, and all outputs are turned off for a certain period (protect time t_{LK_PRT}: 5.0 s [Typ]). When it is not detected after the protect time, OCP is canceled. However, output current rating is exceeded when this circuit operates. Thus, please design sufficient margin not to take continuous use and action of the circuit as a precondition.

12. Hall input error protection (Hall Error)
When Hall input is abnormal, the Hall input error protection works and all outputs are turned off. This protection has the mask time of 1.0 ms (Typ). Once protection is operated, it continues until it is cancelled by restart from the operation of Power Save, Speed Control Non-input or V_{CC} off.

13. Priority of Protection
This IC has a priority order in each protection operation as shown below. The protection with higher priority will be activated during the protection with lower priority.

Table 7. Priority Order of Protect Operation

Priority Order	Protection
1st	VCC UVLO,
2nd	OCP
3rd	TSD
4th	OVLO
5th	MLP, High Speed Rotation Protection, Hall Error Protection, VG UVLO

14. Auto Lead Angle Control
It has the auto lead angle function which enables a high efficiency drive by matching the phase of the coil current to the phase of the Back EMF voltage generated to the coil automatically while driving the motor. To do that, place Hall sensors in reference to Figure 8 so that the timing of the Hall sensor signal and the coil current at the lead angle 0° becomes Figure 1 (U→V→W) or Figure 2 (U→W→V). The lead angle adjustment range is from 0° to 45°.

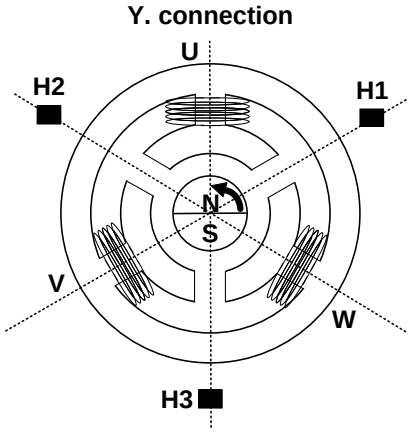


Figure 8. The Placement of Hall sensors

Description of Operations – continued

15. Speed Feedback Control

It has a speed feedback control to keep the motor rotation speed constant. It controls a drive duty so that the target motor rotation speed that set by an input PWMB signal and the frequency of internal FG signal are equal. It sets various parameters that are most suitable for the target rotation speed and characteristics of the motor. These setting parameters can be written to the OTP. The data written on the OTP are set to registers when the IC is powered on. If the data is not written on the OTP, registers are set default value shown in the register map. Refer to the Application Note about OTP setting. In this document, default value is described. The block diagram of speed feedback control is shown in Figure 9.

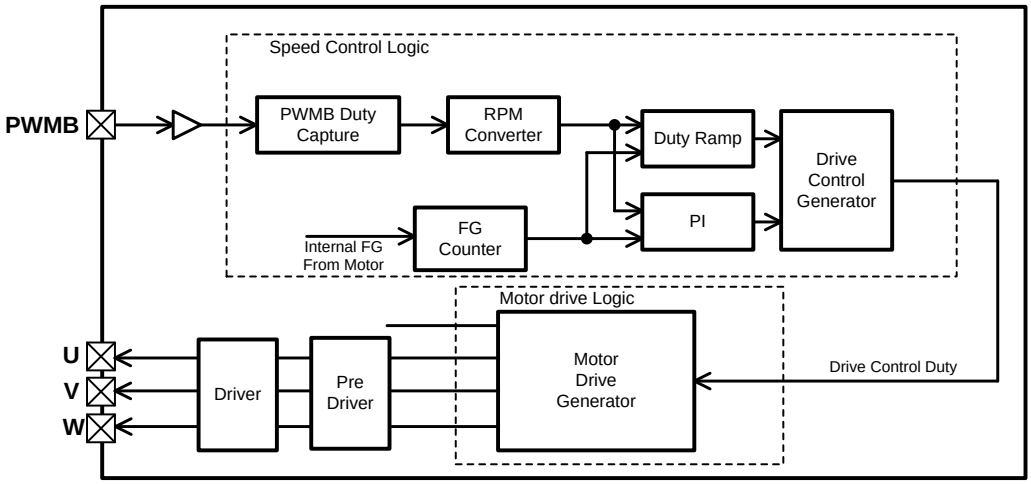


Figure 9. The Block Diagram of Speed Feedback Control

15.1 Relations of the Input PWMB Duty and the Target RPM

In the case that the POLE_SEL pin setting is 10 poles, the relations of the input PWMB Duty and the Target RPM become like Figure 10. The relation of the maximum Target RPM when input PWMB Duty=0 % (Note that this is negative logic) and the motor poles is calculated below.

$$Target\ RPM\ (Max) = 1{,}024 \times (80 + 1) \times 0.256 \times \frac{4}{poles}$$

Where poles=10, then,

$$Target\ RPM\ (Max) = 1{,}024 \times (80 + 1) \times 0.256 \times \frac{4}{10}$$
$$= 8493\ \text{rpm}$$

In addition, it is equipped with a function that can perform Drive Off judgment and stops (Hi-z output) the motor when the Target RPM is 84.9 rpm or less (PWMB Duty is 99 % or more). And it restarts the motor in a timing that the Target RPM is 424.6 rpm or more (PWMB Duty is 95 % or less).

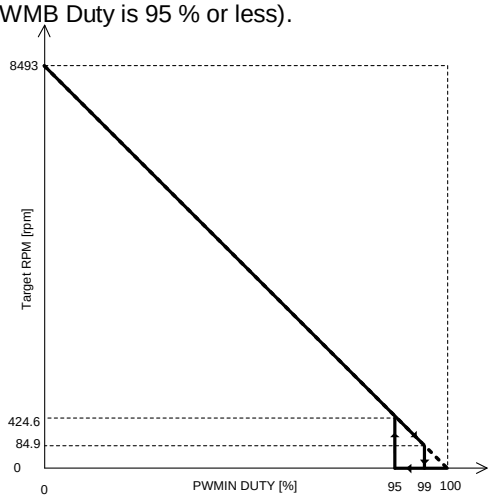


Figure 10. PWMB Duty and Target RPM (10 poles Setting)

15. Speed Feedback Control – continued

15.2 Motor RPM Measurement

For the motor RPM, a half period of the internal FG signal is measured. This measured value is compared with a half target period which is calculated from the Target RPM. And this difference is the speed error value. When the half period of the internal FG signal is longer (the motor rotation speed is slow), the speed error value becomes minus. On the other hand, when it is shorter (the motor rotation speed is fast), the speed error value becomes plus.

15.3 Setting of Motor Speed control

Built-in RAMP control drive and PI control drive. The setting method is shown in Table 8.

Table 8. The Motor Speed Control Setting

Start and Acceleration / Deceleration Operation	Stable Operation
RAMP control drive	PI control drive

15.4 PI Control

It drives the closed-loop speed feedback control using the PI control. The Drive Control Duty (Drive Control) is calculated from the proportional gain (KP=1.0) and the integral gain (KI=0.0117) regarding the speed error value (Error Value) measured in Internal FG Signal Period Measurement. The PI control block diagram is shown in Figure 11.

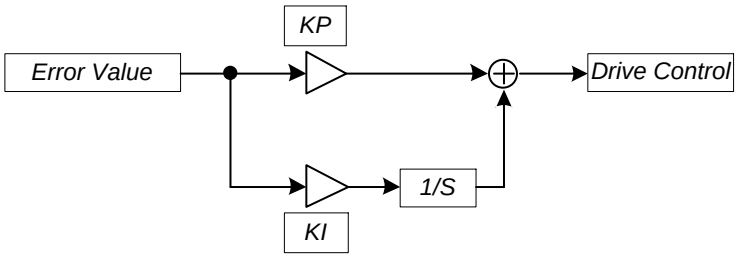


Figure 11. The PI Control Block Diagram

15. Speed Feedback Control – continued

15.5 RAMP Control

The Drive Control Duty increases gradually when the speed error value is minus (the motor rotation speed is slow), and decreases gradually when the speed error value is plus (the motor rotation speed is fast). So the real motor rotation speed approaches the target motor rotation speed. An increase/decrease step width of the Drive Control Duty is 0.49 % every 41.6 ms as shown in Figure 13.

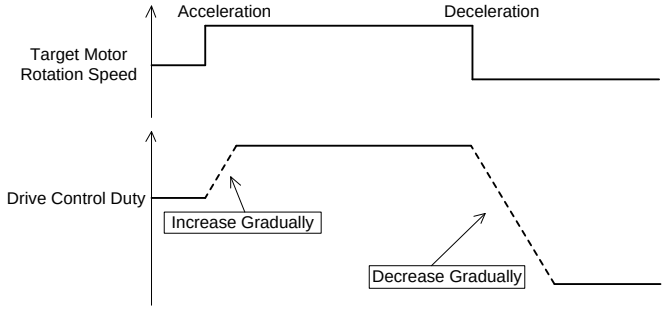


Figure 12. The RAMP Control Function Summary

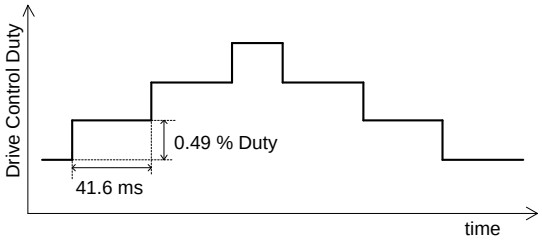


Figure 13. The RAMP Step

About shifting from the RAMP control to the PI control, the state shifts to the PI control when the speed error value is settled with 1.57 % or less. In the large domain of the speed error value, the real motor rotation speed approaches the target motor rotation speed operating the RAMP control. So the speed error value becomes small, it starts the PI control. It facilitates parameter adjustment.

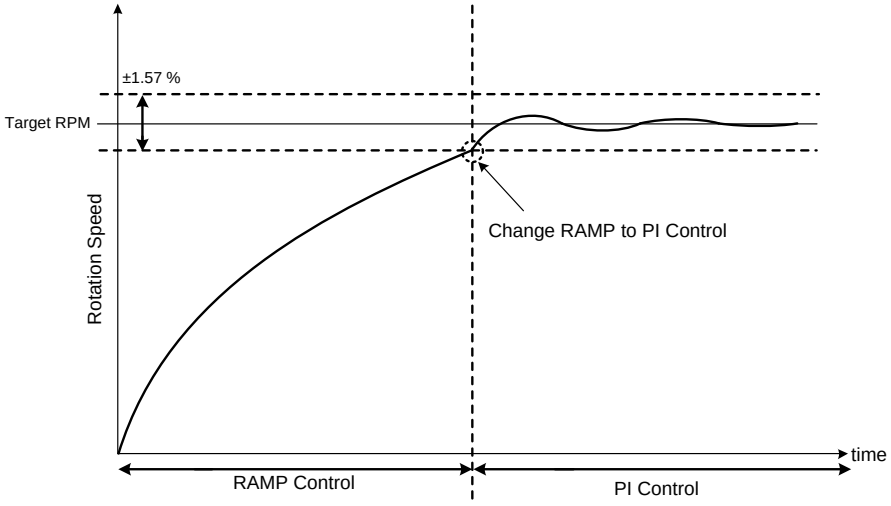


Figure 14. The State Switch from the RAMP Control to the PI Control

Thermal Resistance Model

Heat generated by consumed power of IC is radiated from the mold resin or lead frame of package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called thermal resistance. Thermal resistance from the chip junction to the ambient is represented in θ_{JA} (°C/W), and thermal characterization parameter from junction to the top center of the outside surface of the component package is represented in Ψ_{JT} (°C/W). Thermal resistance is divided into the package part and the substrate part. Thermal resistance in the package part depends on the composition materials such as the mold resins and the lead frames. On the other hand, thermal resistance in the substrate part depends on the substrate heat dissipation capability of the material, the size, and the copper foil area etc. Therefore, thermal resistance can be decreased by the heat radiation measures like installing a heat sink etc. in the mounting substrate. The equations are shown below and the thermal resistance model is shown in Figure 15.

Equation

$$\theta_{JA} = \frac{Tj - Ta}{P} \text{ [°C/W]}$$

$$\psi_{JT} = \frac{Tj - Tt}{P} \text{ [°C/W]}$$

Where:

θ_{JA} is the thermal resistance from junction to ambient (°C/W)
ψ_{JT} is the thermal characterization parameter from junction to the top center of the outside surface of the component package (°C/W)
Tj is the junction temperature (°C)
Ta is the ambient temperature (°C)
Tt is the package outside surface (top center) temperature (°C)
P is the power consumption (W)

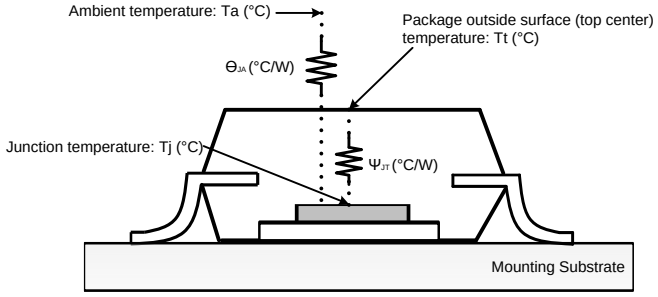
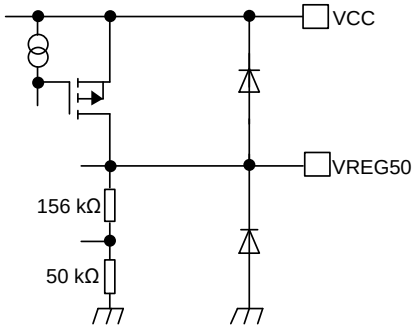


Figure 15. Thermal Resistance Model of Surface Mount

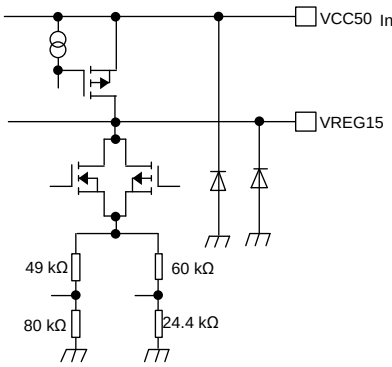
Even if it uses the same package, θ_{JA} and Ψ_{JT} are changed depending on the chip size, power consumption and the measurement environments of the ambient temperature, the mounting condition and the wind velocity, etc.

I/O Equivalence Circuits

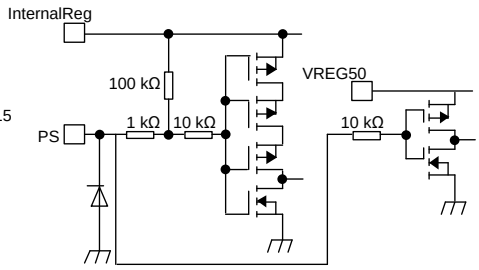
1) VREG50 pin



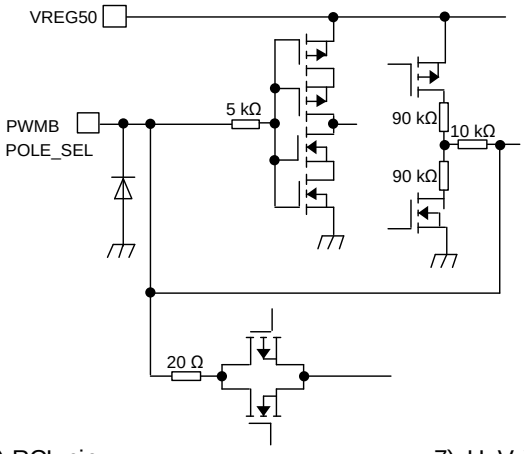
2) VREG15 pin



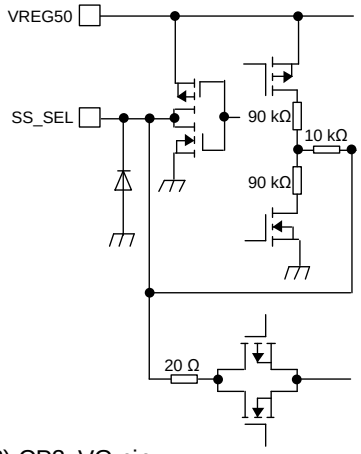
3) PS pin



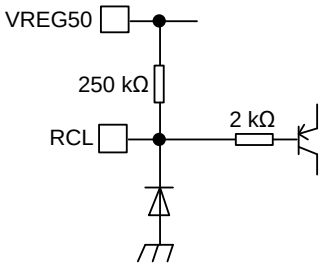
4) PWMB, POLE_SEL pin



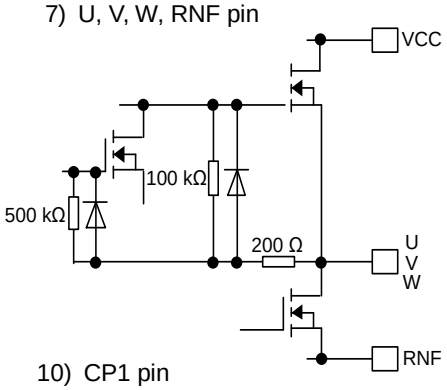
5) SS_SEL pin



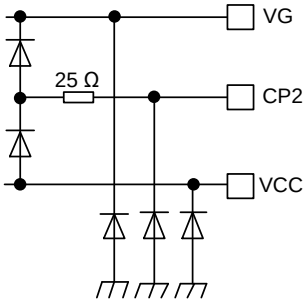
6) RCL pin



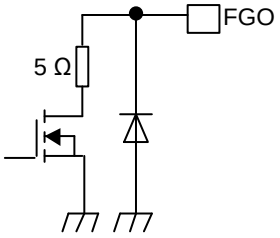
7) U, V, W, RNF pin



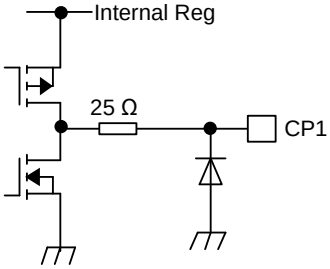
8) CP2, VG pin



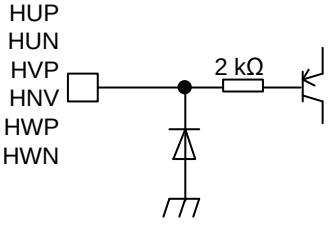
9) FGO pin



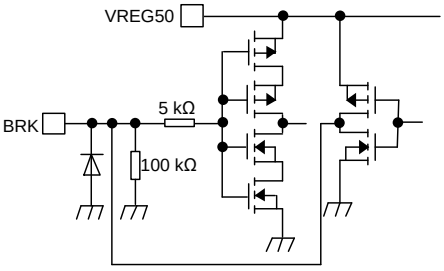
10) CP1 pin



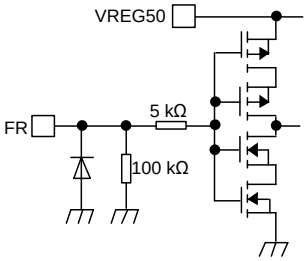
11) HUP, HUN, HVP, HVN, HWP, HWN



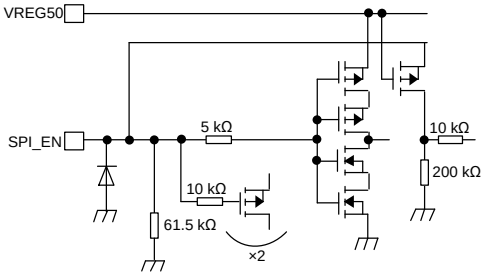
12) BRK pin



13) FR pin



14) SPI_EN pin



Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

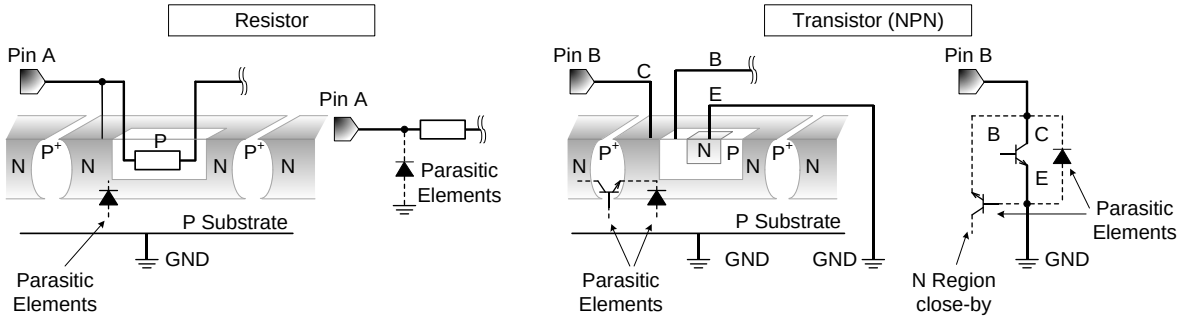


Figure 16. Example of IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

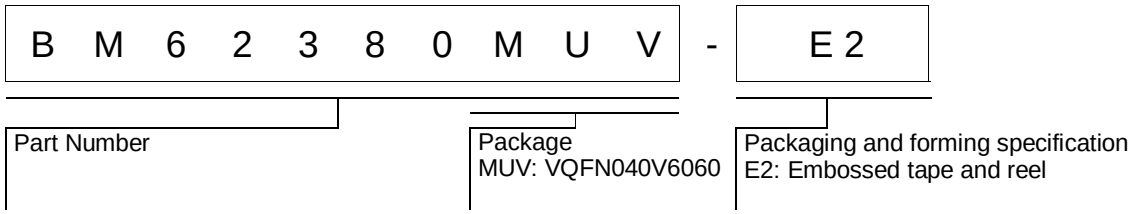
12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

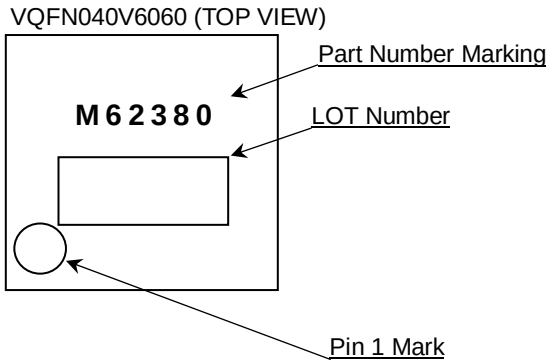
13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

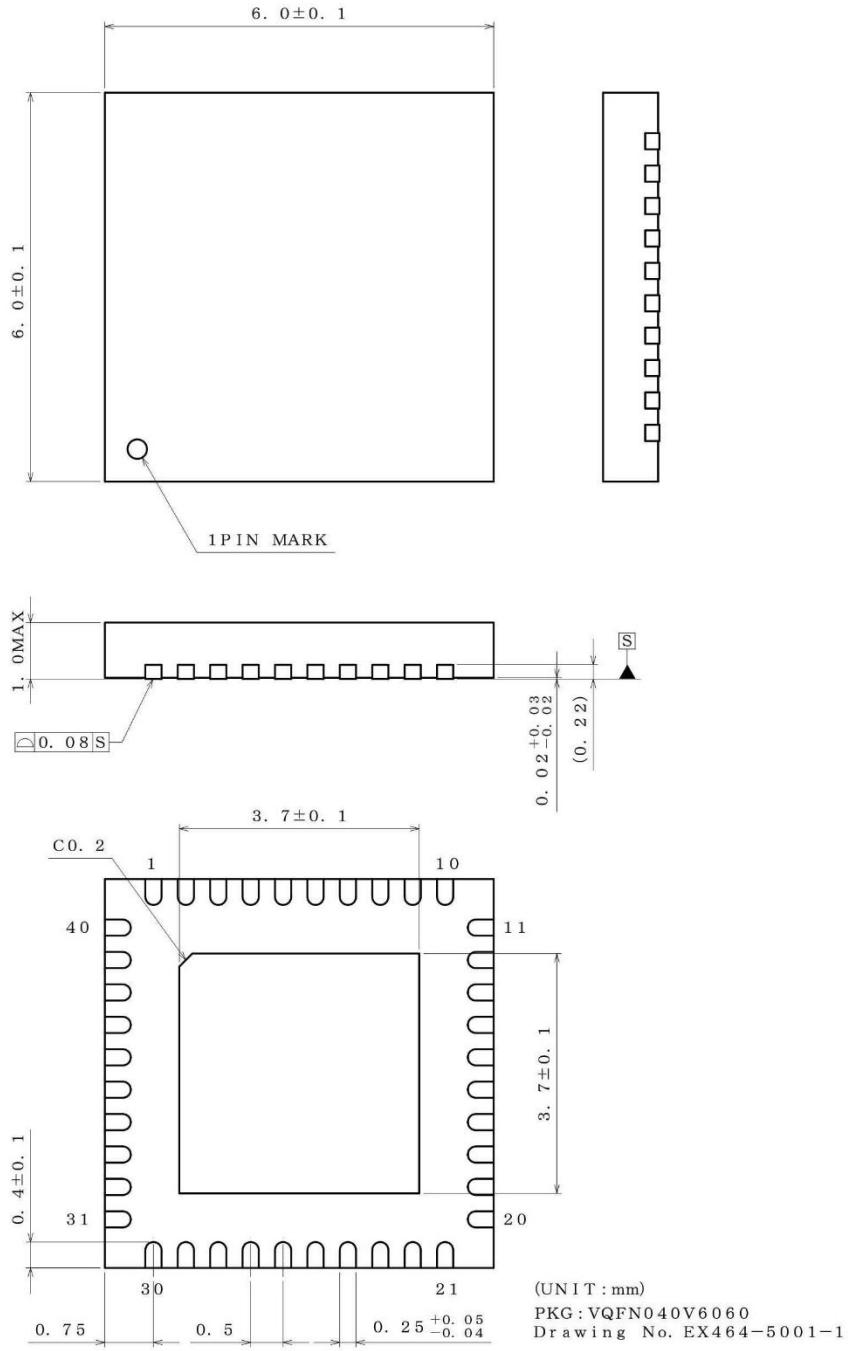


Marking Diagram



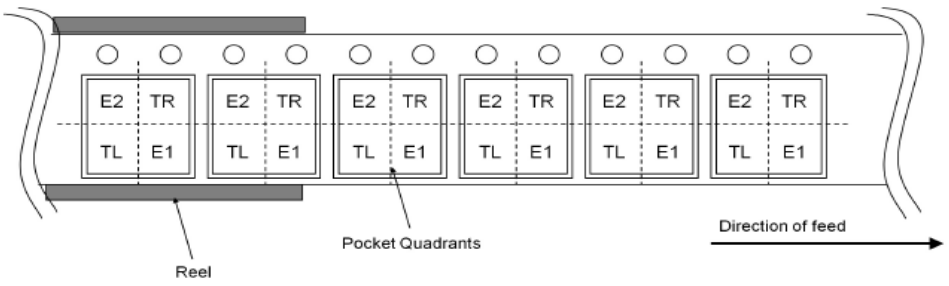
Physical Dimension and Packing Information

Package Name	VQFN040V6060



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



Revision History

Date	Revision	Changes
18.Mar.2019	001	New Release

ご注意

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日本	USA	EU	中国
CLASSⅢ	CLASSⅢ	CLASSⅡb	Ⅲ類
CLASSⅣ		CLASSⅢ	

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   ②直射日光・屋外暴露、塵埃中でのご使用
   ③潮風、Cl_2、H_2S、NH_3、SO_2、NO_2 等の腐食性ガスの多い場所でのご使用
   ④静電気や電磁波の強い環境でのご使用
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   ③直射日光や結露する場所での保管
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