

JAN. 1998

SPECIFICATION

for KS5520

**SYSTEM LSI BUSINESS
SAMSUNG ELECTRONICS CO.**



SPECIFICATION for KS5520

Important Notice

Copyright 1998 by SAMSUNG

The information in this publication has been carefully checked and is believed to be accurate at the time of publication. Samsung assumes no responsibility, however, for possible errors or omissions, or for any consequences resulting from the use of the information contained herein.

Samsung reserves the right to make changes in its products or product specifications with the intent to improve function or design at any time and without notice and is not required to update this documentation to reflect such changes.

This publication does not convey to a purchaser of semiconductor devices described herein any license under the patent rights of Samsung or others.

Samsung makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Samsung assume any liability arising out of the application or use of any product or circuit and specifically disclaims any liability, including without limitation any consequence or incidental damages.

Typical parameters can and do vary in different applications. All operating parameters, including *Typicals,* must be validated for each customer application by the customer's technical experts.

Samsung products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, for other applications intended to support or sustain life, or for any other application in which the failure of the Samsung product could cause personal injury or death.

Should the buyer purchase or use a Samsung product for any such unintended or unauthorized application, the buyer shall indemnify and hold Samsung and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, expenses, and reasonable attorney fees arising out of, either directly or indirectly, any claim of personal injury or death that may be associated with such unintended or unauthorized use, even if such claim alleges that Samsung was negligent regarding the design or manufacture or manufacture of said product.

CONTENTS

• OUTLINE OF PRODUCT	3
• FUNCTIONS	3
• FEATURES	3
• OPTION CODE	3
• ORDERING INFORMATION	3
• BLOCK DIAGRAM	4
• PIN CONFIGURATION	4
• ABSOLUTE MAXIMUM RATING --	6
• ELECTRICAL CHARACTERISTICS -	7
• TIMING DIAGRAM	8
• MEMORY STRUCTURE	9
• SCREEN STRUCTURE	15
• BLANK MODE	15
• SCROLL/HALF-TONE FUNCTION -	16
• BOX DRAWING FUNCTION	17
• APPLICATION CIRCUIT	18
• PACKAGE DIMENSIONS	20

1. OUTLINE OF PRODUCT

The KS5520 is a single chip VLSI device which performs the on screen display function with sync separation of video composite signal and AFC is proposed.

It can choose total 256 characters and display up to 360 characters in a screen.

It can also select various built-in functions such as character color select, inverse, etc. These functions are compatible with all video systems including NTSC, PAL, SECAM.

2. FUNCTIONS

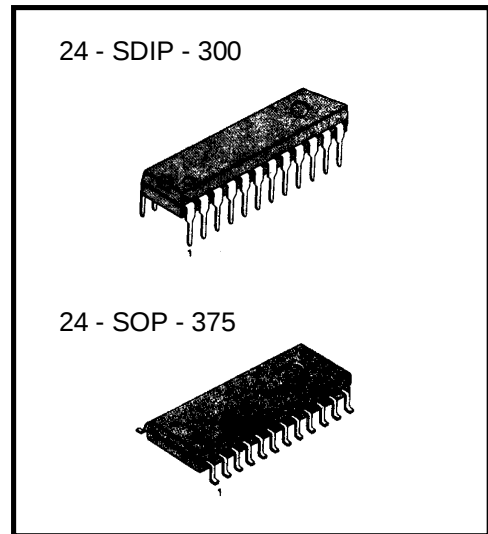
- On screen display
- Sync separator and sync detector
- AFC

3. FEATURES

- Screen structure : 360 (30 columns × 12 rows)
- Character structure : 12 × 18 dots
- Character types : 256 kinds of color characters
- Display position : 62 horizontal position
64 vertical position
- Character size : 4 × 4 times of normal in both vertical and horizontal directions
- Blinking : controllable in character unit, blinking time also controllable
- Blanking : controllable in line units, blanking mode change possible
Blank color fill possible in character units (8 colors)
- Background coloring : 8 colors
- Character coloring : coloring of characters possible in blank mode
- Inverse character display : controllable in character units
- Synchronous ways : automatic selection of internal or external synchronization via MICOM control
- Built-in clamp, horizontal/vertical sync separator & sync detector circuit
- Sync detection sensitivity can be adjusted via MICOM control.
- Built-in analog horizontal/vertical sync PLL circuit
- Scroll & Box Drawing ability
- Half-Tone function ability
- NTSC / PAL / SECAM mode via MICOM control

4.2 ORDERING INFORMATION

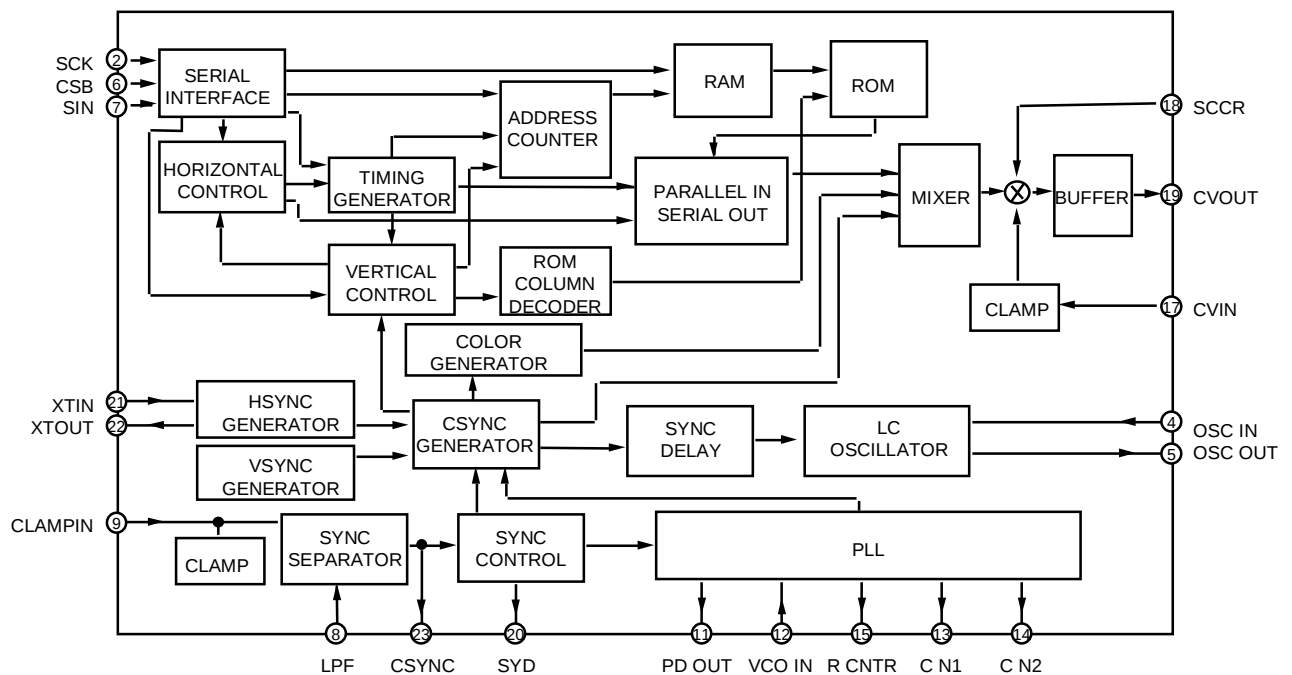
Device	Package	Operating Temperature
KS5520-XX	24-SDIP-300	- 20 ~ + 70℃
KS5520D-XX	24-SOP-375	- 20 ~ + 70℃



4.1 OPTION CODE

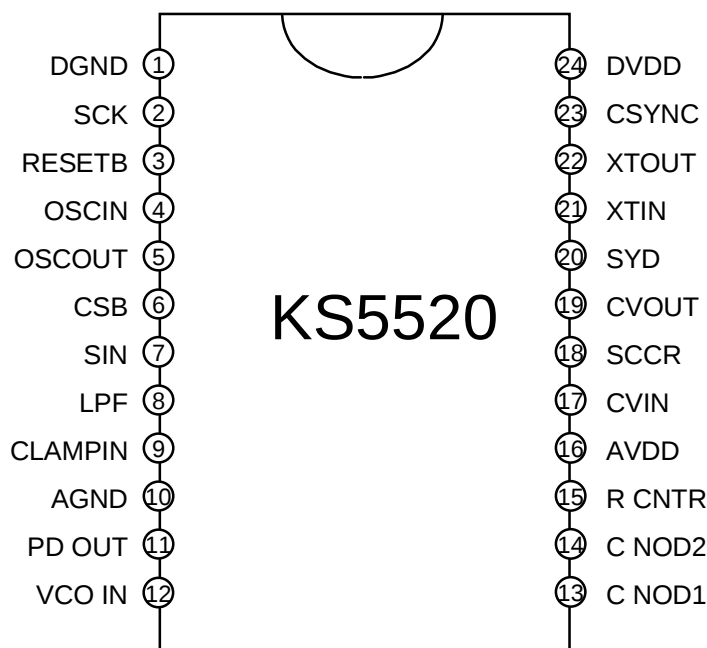
Code No.	Remark
KS5520-01	English, Russian, German, French, Spanish, Italian, Polish, Portuguese, Swedish, Danish, Dutch, Esperanto, Vietnamese, Indonesian, Czechoslovak
KS5520D-04	English, Russian, German, French, Spanish, Italian, Polish, Portuguese, Swedish, Danish, Dutch, Esperanto, Vietnamese, Indonesian, Czechoslovak, Greek

5. BLOCK DIAGRAM



6. PIN CONFIGURATION & DESCRIPTION

6.1 PIN CONFIGURATION



6.2 PIN DESCRIPTION

Pin No.	Symbol	I/O	Function
1	DGND	-	Digital Ground
2	SCK	I	Serial clock input. When CSB pin is low, then 16-bit serial data is inputted by controlling micom. Built-in pull-up resistor.
3	RESETB	I	Auto clear pin. If low, then all circuit is reset. Built-in pull-up resistor.
4	OSCIN	I	LC oscillation pin. Standard frequency is 9MHz & the horizontal start position and the horizontal size are controlled by the clock of oscillation block.
5	OSCOUT	O	
6	CSB	I	While pin 6 is low, serial data input is active. Built - in pull-up resistor
7	SIN	I	Serial data input pin. Built-in pull-up resistor
8	LPF	I	LPF gets rid of the color signal in a video input signal.
9	CLAMPIN	I	Clamp input pin of composite video signal of 2Vpp
10	AGND	-	Analog ground
11	PD OUT	O	Phase detect output of analog PLL. Loop filter is formed by PD OUT and VCO IN.
12	VCO IN	I	VCO input pin of PLL
13	C NOD1	O	Capacitor node 1 of PLL VCO
14	C NOD2	O	Capacitor node 2 of PLL VCO
15	R CNTR	O	Resistor node of PLL VCO
16	AVDD	-	5V Analog VDD
17	CVIN	I	Composite video input pin
18	SCCR	I	When SECAM mode, color signal is mixed in the character level.
19	CVOUT	O	Composite video output pin

6.2 PIN DESCRIPTION (Continued)

Pin No.	Symbol	I/O	Function
20	SYD	O	H-sync detect output pin. If sync exists, then high if not, low
21	XTIN	I	X-tal input / output pin NTSC : 14.31818 MHz, PAL : 17.734475MHz
22	XTOUT	O	
23	CSYNC	O	When external, C-sync separator output is out, when internal, then internal C-sync is outputted.
24	DVDD	-	5V Digital VDD

7. ABSOLUTE MAXIMUM RATINGS (Ta = 25℃)

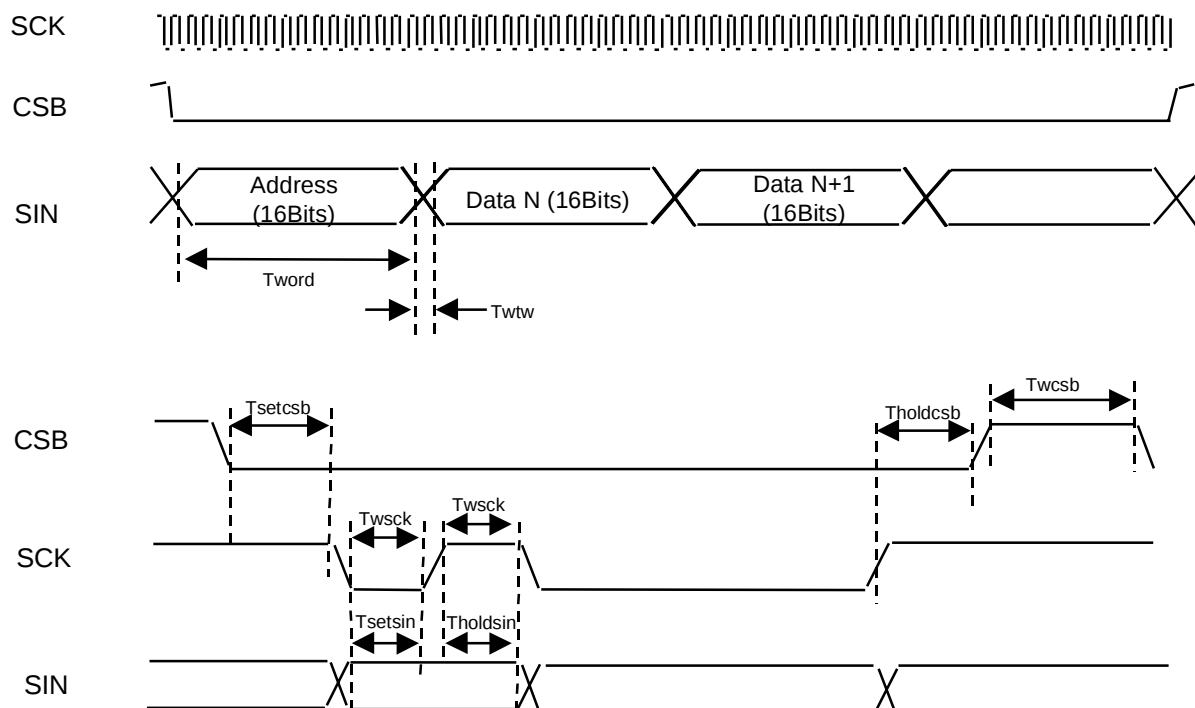
Characteristics	Symbol	Value	Unit
Supply Voltage	VDD	3.0 ~ 7.0	V
Input Voltage	VIN	$V_{SS} - 0.3 \leq V_{IN} \leq V_{DD} + 0.3$	V
Power Dissipation	PD	200	mW
Operating Temperature	Topr	- 20 ~ + 70	℃
Storage Temperature	Tstg	- 40 ~ + 125	℃

8. ELECTRICAL CHARACTERISTICS (Ta = 25℃, AVDD = DVDD = 5V)

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Voltage	VDD	4.75	5.00	5.25	V
Operating Current	Icc	20	40	60	mA
Input High Voltage	VIH	0.8VDD	-	-	V
Input Low Voltage	VIL	-	-	0.2VDD	V
Output High Voltage (2mA drive)	VOH	0.7VDD	-	-	V
Output Low Voltage (2mA drive)	VOL	-	-	0.3VDD	V
Pin8 LPF Voltage	Vp8	2.15	2.35	2.55	V
Pin9 Clamp Voltage	Vp9	1.25	1.45	1.65	V
Pin15 R_CNTR Voltage	Vp15	2.35	2.50	2.65	V
Pin17 Clamp Voltage	Vp17	0.60	0.80	1.00	V
Buffer Gain	Vp19G	1.80	2.00	2.20	V
LC Oscillation Frequency	Fosc	8.0	9.0	10.0	MHz
Hsync Duty	Fh_duty	250	550	850	nS
Hsync Frequency	H_fre	15.5	15.7	15.9	KHz
X-tal Oscillation Frequency	Fp22	14.1	14.3	14.5	MHz
Sync Separation Voltage	Vse	0.10	0.25	0.40	V
Blueback Sync Tip Level	Vbst	0.50	0.80	1.10	V
Blueback Pedestal Level	Vbpd	1.10	1.40	1.70	V
Blueback Color Burst Level High	Vcbh	1.40	1.70	2.00	V
Blueback Color Burst Level Low	Vcbl	0.80	1.10	1.40	V
Blueback Color Level High	Vbch	2.30	2.60	2.90	V
Blueback Color Level Low	Vbcl	1.30	1.60	1.90	V
Blueback Blank Level High	Vblkh	1.40	1.70	2.00	V
Blueback Blank Level Low	Vblk1	1.10	1.40	1.70	V
Blueback Character Level High	Vchh	2.40	2.70	3.00	V
Blank Color Off Level	Vbcof	1.10	1.40	1.70	V
Box White Level	Vbwl	2.20	2.50	2.80	V
Box Black Level	Vbbl	1.10	1.40	1.70	V
HalfTone Level	Vhalf	1.80	2.10	2.40	V
VCO Input Voltage	Vvco	2.30	2.50	2.70	V
AFC Freerun Frequency	Ffr	15.5	15.7	15.9	KHz
AFC Lock Range High	Falh	200	300	400	Hz
AFC Lock Range Low	Fall	-	-	-500	Hz

Note 1 : Specifications are subject to change without notice.

9. TIMING DIAGRAM



ITEM	SYMBOL	LIMITS			UNIT
		MIN	TYP	MAX	
SCK Width	T_{wsck}	200	-	-	nsec
CSB Width	T_{wcsb}	1	-	-	usec
CSB Setup Time	T_{setcsb}	200	-	-	nsec
CSB Hold Time	$T_{holdcsb}$	2	-	-	usec
SIN Setup Time	T_{setsin}	200	-	-	nsec
SIN Hold Time	$T_{holdsin}$	200	-	-	nsec
1 Word Write Time	T_{word}	10	-	-	usec
Word To Word Time	T_{wtw}	1	-	-	usec

10. MEMORY STRUCTURE

It consists of 360*16 bits SRAM, 256 font ROM and 5 mode control register.

	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0	Box_ Inv	Box 1	Box 0	R	G	B	Invert	Blink	C7	C6	C5	C4	C3	C2	C1	C0
1	*	* (Note)	* (Note)	* (Note)	*	*	(Note)	(Note)	Character Code (ROM Address)							
2																
3																
.																
.																
.																
.																
.																
.																
357																
358																
359	Box_ Inv	Box 1	Box 0	R	G	B	Invert	Blink	C7	C6	C5	C4	C3	C2	C1	C0
360	0	0	Half_ Tone	Blink 1	Blink 0	Blink_ Time	HZ 21	HZ 20	HZ 11	HZ 10	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
361	0	Ext_ fsc	Blank_ Level	Scroll_ Time	Scroll_ On	Inter_ -nal	VZ 21	VZ 20	VZ 11	VZ 10	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0
362	0	RAM_ Erase	Disp_ On	P626/ P628	Inlace /Non-	Secam	NTSC/ PAL	Blk 1	Blk 0	Blk Col	C_ Level	R_ Lev1	R_ Lev0	R_ Cntr2	R_ Cntr1	R_ Cntr0
363	0	0	0	All_ Blank	DSP B	DSP A	DSP 9	DSP 8	DSP 7	DSP 6	DSP 5	DSP 4	DSP 3	DSP 2	DSP 1	DSP 0
364	0	Fil2	Fil1	Fil0	Fih3	Fih2	Fih1	Fih0	Fcl3	Fcl2	Fcl1	Fcl0	Fch3	Fch2	Fch1	Fch0

* (Note) : same as above.

< Raster Color Level Control > (Control Register 362 (16AH))

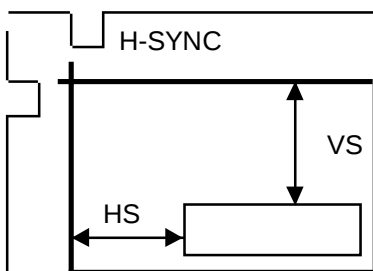
DA4(Lev 1)	DA3(Lev 0)	Raster Color Level `H`	Raster Color Level `L`	Remark
0	0	2.6V	1.6V	Level 0
0	1	2.2V	1.4V	Level 1
1	0	2.2V	1.4V	Level 1
1	1	2.0V	1.3V	Level 2

CONTROL REGISTER

1) Register 360 (168H)

DA0 ~ DAD	Register	ContentSs		Remark																	
		State	Functions																		
0	HP0	0	$HS = Tc * \{ 4 * \sum_{n=0}^5 (HPn * 2^n) + N \}$$Tc : \text{osc. period (} 1/9 \text{ MHz} = 111 \text{ nsec)}$<table><tr><td>HSZ11</td><td>HSZ10</td><td rowspan="2">N</td></tr><tr><td>HSZ21</td><td>HSZ20</td></tr><tr><td>0</td><td>0</td><td>9</td></tr><tr><td>0</td><td>1</td><td>10</td></tr><tr><td>1</td><td>0</td><td>11</td></tr><tr><td>1</td><td>1</td><td>12</td></tr></table>	HSZ11	HSZ10	N	HSZ21	HSZ20	0	0	9	0	1	10	1	0	11	1	1	12	Horizontal Start Position
HSZ11	HSZ10	N																			
HSZ21	HSZ20																				
0	0	9																			
0	1	10																			
1	0	11																			
1	1	12																			
	1																				
1	0																				
	1																				
2	0																				
	1																				
3	0																				
	1																				
4	0																				
	1																				
5	0																				
	1																				
6	HZ10	0	<table><tr><td> HZ10 HZ11 </td><td>0</td><td>1</td></tr><tr><td>0</td><td>1X</td><td>2X</td></tr><tr><td>1</td><td>3X</td><td>4X</td></tr></table>	HZ10 HZ11	0	1	0	1X	2X	1	3X	4X	1st line horizontal character size control								
HZ10 HZ11	0	1																			
0	1X	2X																			
1	3X	4X																			
	1																				
7	HZ11	0																			
	1																				
8	HZ20	0	<table><tr><td> HZ20 HZ21 </td><td>0</td><td>1</td></tr><tr><td>0</td><td>1X</td><td>2X</td></tr><tr><td>1</td><td>3X</td><td>4X</td></tr></table>	HZ20 HZ21	0	1	0	1X	2X	1	3X	4X	2nd ~ 12th line horizontal character size control								
HZ20 HZ21	0	1																			
0	1X	2X																			
1	3X	4X																			
	1																				
9	HZ21	0																			
	1																				
A	Blink	0	Blink Time = 1 sec	Blink Time Control																	
	Time	1	Blink Time = 0.5 sec																		
B	Blink 0	0	<table><tr><td> Blink0 Blink1 </td><td>0</td><td>1</td></tr><tr><td>0</td><td>Off</td><td>Duty 25%</td></tr><tr><td>1</td><td>Duty 50%</td><td>Duty 75%</td></tr></table>	Blink0 Blink1	0	1	0	Off	Duty 25%	1	Duty 50%	Duty 75%	Blinking Duty Control								
Blink0 Blink1	0	1																			
0	Off	Duty 25%																			
1	Duty 50%	Duty 75%																			
	1																				
C	Blink 1	0																			
	1																				
D	Half-tone	0	Half-tone Off	Half-tone On/Off																	
		1	Half-tone On																		

2) Register 361(169H)

DA0 ~ DAE	Register	Contents		Remark									
		State	Functions										
0	VP0	0	$VS = H * \{ 4 * \sum_{n=0}^5 (VPn * 2^n) + 3 \}$ H : horizontal synchronous pulse time 	Vertical Start Position									
	1												
1	VP1	0											
	1												
2	VP2	0											
	1												
3	VP3	0											
	1												
4	VP4	0											
	1												
5	VP5	0											
	1												
6	VZ10	0	<table><tr><td> VZ11 \ VZ10 </td><td>0</td><td>1</td></tr><tr><td>0</td><td>1X</td><td>2X</td></tr><tr><td>1</td><td>3X</td><td>4X</td></tr></table>	VZ11 \ VZ10	0	1	0	1X	2X	1	3X	4X	1st line vertical character size control
VZ11 \ VZ10	0	1											
0	1X	2X											
1	3X	4X											
	1												
7	VZ11	0	<table><tr><td> VZ21 \ VZ20 </td><td>0</td><td>1</td></tr><tr><td>0</td><td>1X</td><td>2X</td></tr><tr><td>1</td><td>3X</td><td>4X</td></tr></table>	VZ21 \ VZ20	0	1	0	1X	2X	1	3X	4X	2nd ~ 12th line vertical character size control
VZ21 \ VZ20	0	1											
0	1X	2X											
1	3X	4X											
	1												
8	VZ20	0	<table><tr><td> VZ21 \ VZ20 </td><td>0</td><td>1</td></tr><tr><td>0</td><td>1X</td><td>2X</td></tr><tr><td>1</td><td>3X</td><td>4X</td></tr></table>	VZ21 \ VZ20	0	1	0	1X	2X	1	3X	4X	
VZ21 \ VZ20	0	1											
0	1X	2X											
1	3X	4X											
	1												
9	VZ21	0	<table><tr><td> VZ21 \ VZ20 </td><td>0</td><td>1</td></tr><tr><td>0</td><td>1X</td><td>2X</td></tr><tr><td>1</td><td>3X</td><td>4X</td></tr></table>	VZ21 \ VZ20	0	1	0	1X	2X	1	3X	4X	
VZ21 \ VZ20	0	1											
0	1X	2X											
1	3X	4X											
	1												
A	Internal	0	External SYNC	External / Internal Mode									
		1	Internal SYNC										
B	Scroll	0	Scroll Off	Scroll Display Control									
	On	1	Scroll On										
C	Scroll	0	Scroll Time 0.5 sec	Scroll Time Control									
	Time	1	Scroll Time 1 sec										
D	Blank	0	Blank Low Level 0 (1.4V)	Blank Color Low Level Control									
	L Level	1	Blank Low Level 1 (1.8V)										
E	Ext	0	External 4fsc X-TAL (Pin 21,22)	External fsc Clock Input									
	fsc	1	External fsc input to Pin 21(*Only for IC Test)										

3) Register 362 (16AH)

DA0 ~ DAE	Register	Contents					Remark													
		State	Functions																	
0	R_cntr0	0	Cntr2	Cntr1	Cntr0	NTSC	PAL	Raster Color Control												
		1	0	0	0	Red	Red													
1	R_cntr1	0	0	0	1	Blue	G + Y													
		1	0	1	0	B + G	B + G													
		1	0	1	1	Yellow	Blue													
2	R_cntr2	0	1	0	0	Orange	Magenta													
		1	1	0	1	Magenta	Yellow													
		1	1	1	0	Cyan	Green													
		1	1	1	1	Gray	Gray													
3	R_lev0	0	<table><tr><td>Lev 0</td><td>0</td><td>1</td></tr><tr><td>Lev 1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>Level 0</td><td>Level 1</td></tr><tr><td>1</td><td>Level 1</td><td>Level 2</td></tr></table>						Lev 0	0	1	Lev 1	0	1	0	Level 0	Level 1	1	Level 1	Level 2
		Lev 0						0	1											
Lev 1	0	1																		
0	Level 0	Level 1																		
1	Level 1	Level 2																		
1																				
4	R_lev1	0																		
		1																		
5	C_level	0	Character Level 1 (2.7V)					Character Level Control												
		1	Character Level 2 (2.5V)																	
6	Blank Color	0	Blank Color Off					When SECAM, Blank Color Off is not used.												
		1	Blank Color On																	
7	BLK0	0	Blank Mode Select by Controlling the Data of Register 363 (16BH)																	
		1																		
8	BLK1	0																		
		1																		
9	NTSC /PAL	0	NTSC					Color System Select												
		1	PAL																	
A	SECAM	0	NTSC or PAL																	
		1	SECAM																	
B	Interlace /Non-I	0	Interlace					Scanning Type Control												
		1	Non-Interlace																	
C	P626/ P628	0	PAL 1 Field = 626H					PAL Mode 1 Field Control												
		1	PAL 1 Field = 628H																	
D	DSP ON	0	Display Off					Character Display Control												
		1	Display On																	
E	RAM ERS	0	RAM is not erased.																	
		1	RAM is erased.																	

4) Register 363 (16BH)

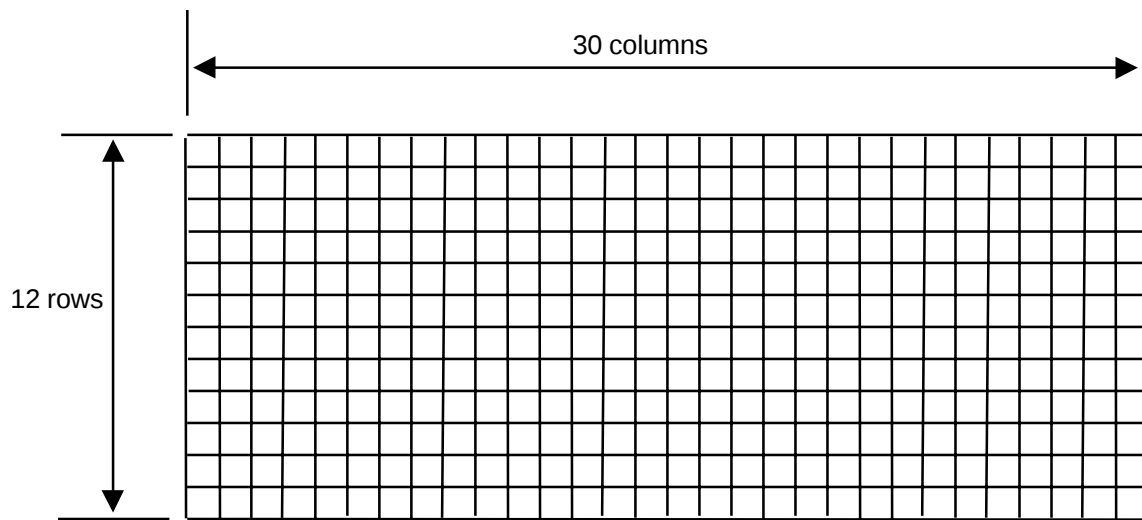
DA0 ~ DAC	Register	Contents		Remark																														
		State	Functions																															
0	DSP0	0	1st line BLANK mode select	<table><tr><th>BLK1</th><th>BLK0</th><th>DSP</th><th>Blank Mode</th></tr><tr><td rowspan="4">0</td><td rowspan="2">0</td><td>0</td><td>Blank Off</td></tr><tr><td>1</td><td>O*</td></tr><tr><td rowspan="2">1</td><td>0</td><td>C*</td></tr><tr><td>1</td><td>O*</td></tr><tr><td rowspan="4">1</td><td rowspan="2">0</td><td>0</td><td>O*</td></tr><tr><td>1</td><td>R*</td></tr><tr><td rowspan="2">1</td><td>0</td><td>R*</td></tr><tr><td>1</td><td>C*</td></tr><tr><td colspan="2">ALL BLK = 1</td><td colspan="2">All Blank</td></tr></table>	BLK1	BLK0	DSP	Blank Mode	0	0	0	Blank Off	1	O*	1	0	C*	1	O*	1	0	0	O*	1	R*	1	0	R*	1	C*	ALL BLK = 1		All Blank	
		BLK1			BLK0	DSP	Blank Mode																											
0	0	0	Blank Off																															
		1	O*																															
	1	0	C*																															
		1	O*																															
1	0	0	O*																															
		1	R*																															
	1	0	R*																															
		1	C*																															
ALL BLK = 1		All Blank																																
1	DSP1	0	2nd line BLANK mode select																															
		1																																
2	DSP2	0	3th line BLANK mode select																															
		1																																
3	DSP3	0	4th line BLANK mode select																															
		1																																
4	DSP4	0	5th line BLANK mode select																															
		1																																
5	DSP5	0	6th line BLANK mode select																															
		1																																
6	DSP6	0	7th line BLANK mode select																															
		1																																
7	DSP7	0	8th line BLANK mode select																															
		1																																
8	DSP8	0	9th line BLANK mode select																															
		1																																
9	DSP9	0	10th line BLANK mode select																															
		1																																
A	DSPA	0	11th line BLANK mode select																															
		1																																
B	DSPB	0	12th line BLANK mode select																															
		1																																
C	All	0	Depend on BLK0, BLK1																															
	BLK	1	All screen blank except character																															

C*	Character Blank
O*	Outline Blank
R*	Raster Blank

5) Register 364 (16CH)

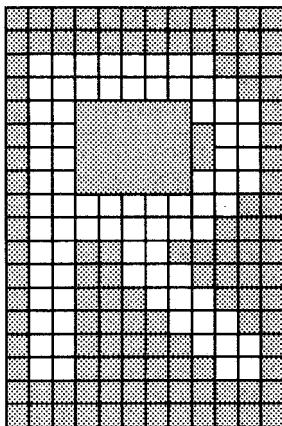
DA0 ~ DAE	Register	Contents		Remark
		State	Functions	
0	Fch0	0	$Fch = 30 * \left\{ \sum_{n=0}^3 Fchn * 512 * 2^n \right\} \text{ Hz}$ Capture Range `H` = 15.36 kHz ~ 230.4 kHz	Sync Detect Capture Range High Sensitivity Control
		1		
1	Fch1	0		
		1		
2	Fch2	0		
		1		
3	Fch3	0		
		1		
4	Fcl0	0	$Fcl = 30 * \left\{ \sum_{n=0}^3 Fchn * 64 * 2^n \right\} \text{ Hz}$ Capture Range `L` = 1.92 kHz ~ 28.8 kHz	Sync Detect Capture Range Low Sensitivity Control
		1		
5	Fcl1	0		
		1		
6	Fcl2	0		
		1		
7	Fcl3	0		
		1		
8	Flh0	0	$Flh = 30 * \left\{ \sum_{n=0}^3 Fchn * 512 * 2^n \right\} \text{ Hz}$ Locking Range `H` = 15.36 kHz ~ 230.4 kHz	Sync Detect Locking Range High Sensitivity Control
		1		
9	Flh1	0		
		1		
A	Flh2	0		
		1		
B	Flh3	0		
		1		
C	Fll0	0	$Fll = 30 * \left\{ \sum_{n=0}^2 Fchn * 64 * 2^n \right\} \text{ Hz}$ Locking Range `L` = 1.92 kHz ~ 13.44 kHz	Sync Detect Locking Range Low Sensitivity Control
		1		
D	Fll1	0		
		1		
E	Fll2	0		
		1		

11. SCREEN STRUCTURE

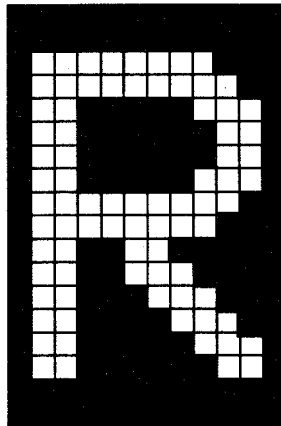


TV Screen

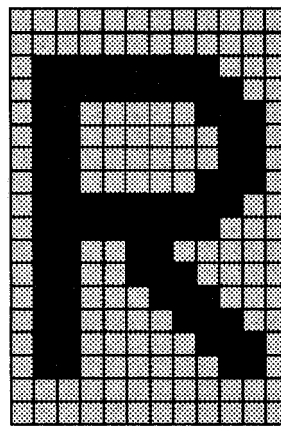
12. BLANK MODE



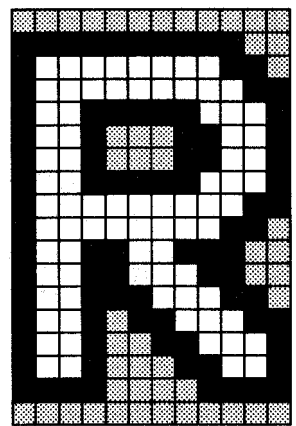
Blank Off



Raster Blank

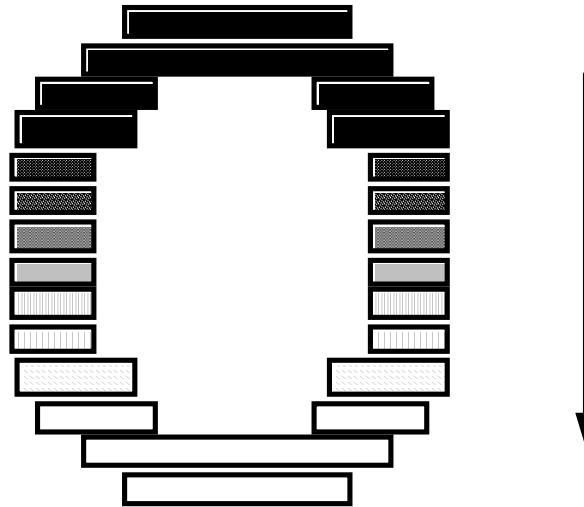


Character Blank



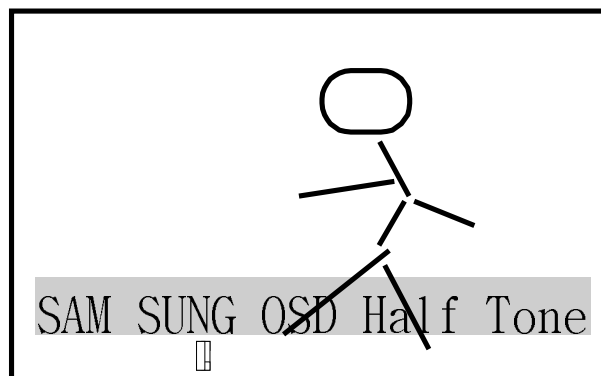
Outline Blank

13. SCROLL FUNCTION



When control register 361, scroll bit (DAB bit) is high, character display on/off from top to down slowly about 0.5 sec or 1 sec. (also controlled by register setting)

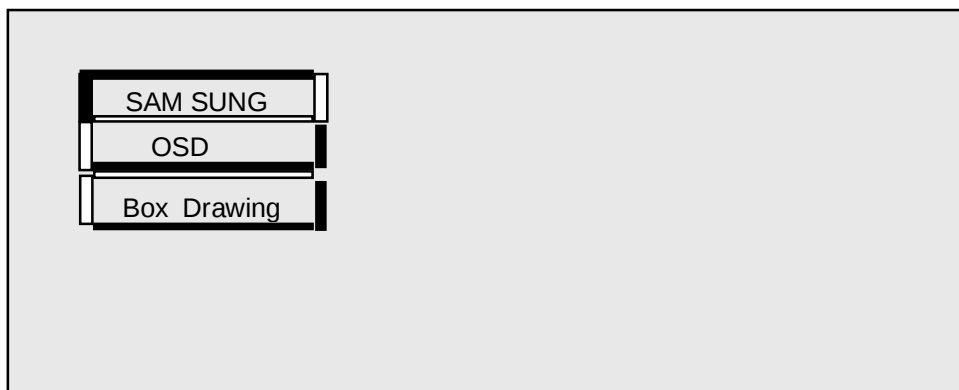
14. HALF-TONE FUNCTION



TV Screen

When control register 360, half tone bit (DAD bit) is high, character display with half luminance level and also display background screen.

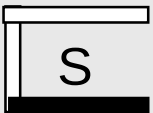
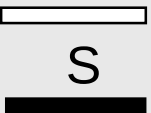
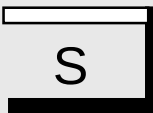
15. BOX DRAWING FUNCTION



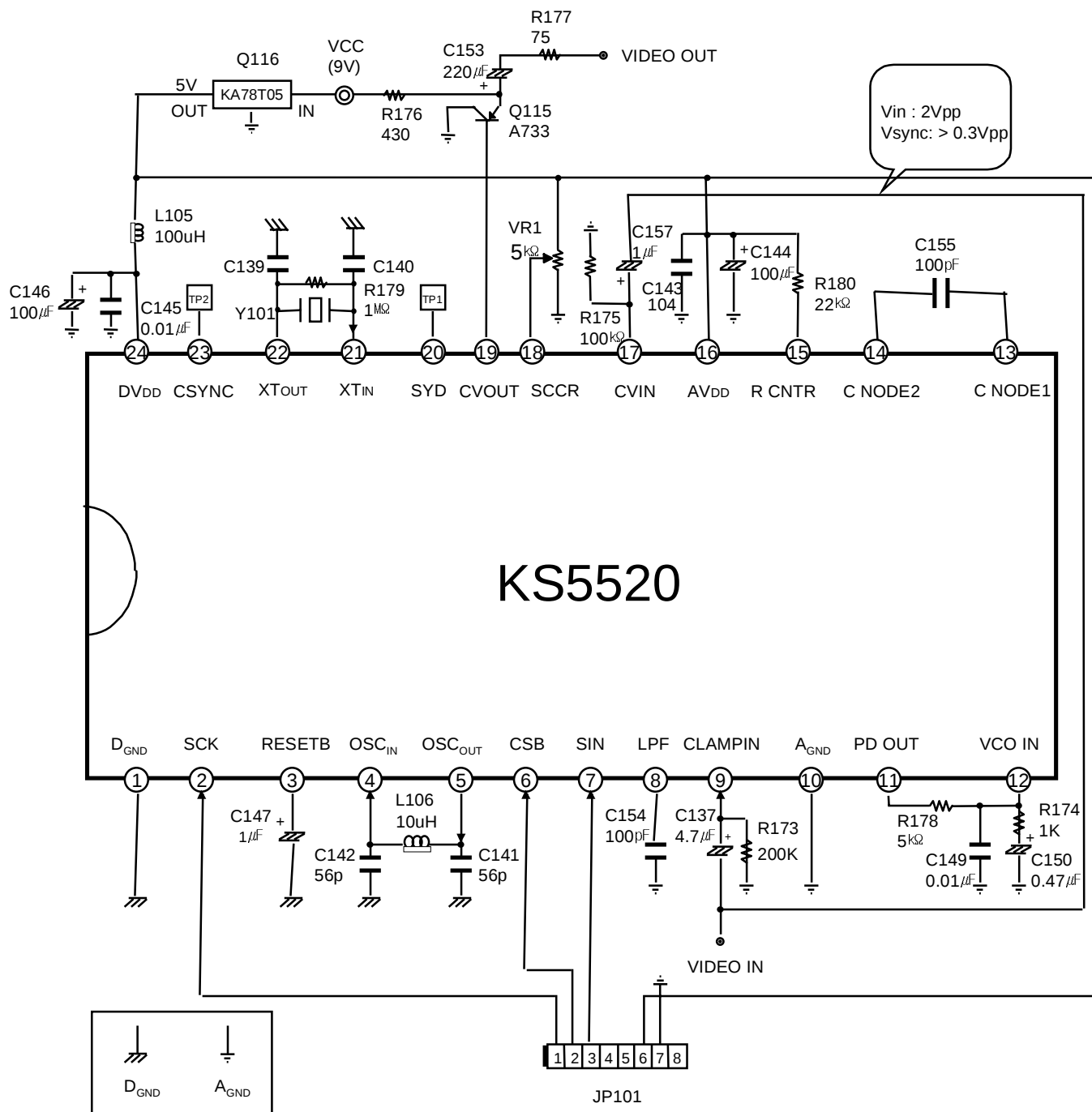
TV Screen

It can draw rectangle box. If you want to concave display, top and left side of characters are drawn black color, bottom and right side of characters are drawn white color and also want to convex display, character colors are vice versa.

It is all controlled by each RAM attribution bit, that is box1 (DAE), box0 (DAD) and box_inv (DAF).

		box0	
		0	1
box1	0	BOX OFF	
	1		

16-1. APPLICATION CIRCUIT (OSD BLOCK)

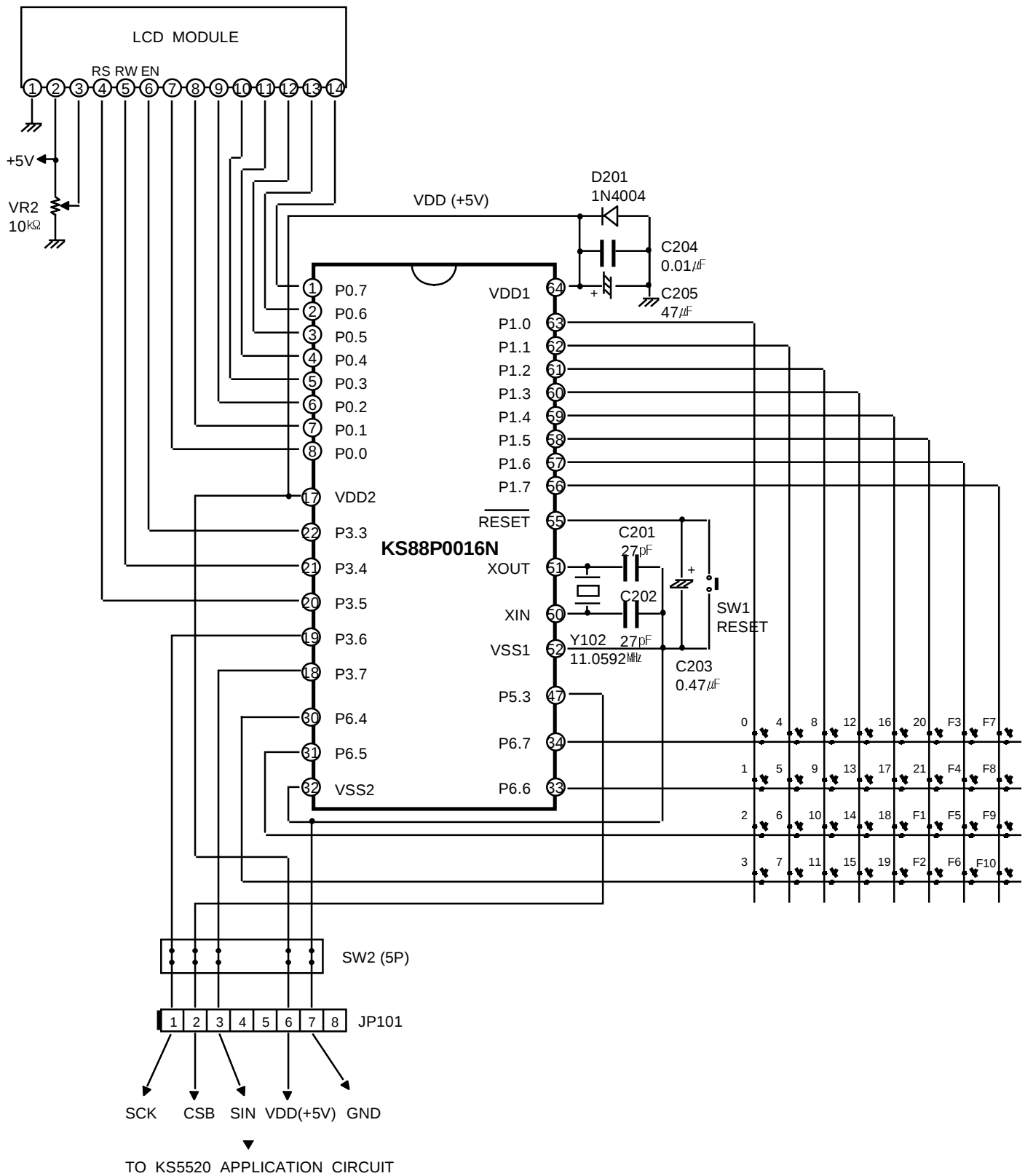


TO MICOM APPLICATION CIRCUIT
or PC PARALLEL PORT

The circuit drawn above is for Demo Board.

- Y101 (4fsc X-TAL) → NTSC : 14.31818MHz
PAL : 17.734475MHz
- C139 / C140 : The load CAP of X-TAL Y101 has a difference each according to its manufactures.
27pF typical (NTSC), 47pF typical (PAL)

16-2. APPLICATION CIRCUIT (CONTROLLER BLOCK)



MEMO

SAMSUNG ELECTRONICS CO., LTD.
SEMICONDUCTOR BUSINESS BEIJING OFFICE
15FL., BRIGHT CHINA CHANG AN BLDG.,
NO.7, JIANGUOMEN, NEI AVENUE,
BEIJING, CHINA 100005
TEL 8610 - 6510 - 1234(0)
FAX 8610 - 6510 - 1545

HEAD OFFICE :

8/11FL., SAMSUNG MAIN BLDG.
250, 2 - KA. TAEPYUNG - RO,
CHUNG - KU, SEOUL, KOREA
TEL 2 - 727 - 7114
FAX 2 - 753 - 0967

SEMICONDUCTOR BUSINESS

SALES & MARKETING DIVISION :

15/16 FL., SEVERANCE BLDG., 84 - 11,
5 - KA, NAMDAEMOON - RO, CHUNG - KU
SEOUL, KOREA
TEL 2 - 259 - 1114
FAX 2 - 259 - 2468

SAMSUNG SEMICONDUCTOR INC.

3655 NORTH FIRST STREET,
SAN JOSE, CA 95134, U.S.A
TEL 408 - 954 - 7000
FAX 408 - 954 - 7873

SAMSUNG SEMICONDUCTOR EUROPE GMBH

SAMSUNG HOUSE,
AM KRONBERGER HANG 6,
65824 SCHWALBACH/TS
TEL 49 - 6196 - 663300
FAX 49 - 6196 - 663311

SAMSUNG SEMICONDUCTOR EUROPE LTD.

GREAT WEST HOUSE
GREAT WEST ROAD, BRENTFORD,
MIDDLESEX TW8 9DQ
TEL 181 - 380 - 7132
FAX 181 - 380 - 7220

SAMSUNG ELECTRONICS JAPAN CO., LTD.

HAMACHO CENTER BLDG.,
31 - 1, NIHONBASHI - HAMACHO, 2 - CHOME,
CHUO - KU, TOKYO 103, JAPAN
TEL 3 - 5641 - 9850
FAX 3 - 5641 - 9851

SAMSUNG ELECTRONICS HONGKONG CO., LTD.

65TH FL., CENTRAL PLAZA,
18 HARBOUR ROAD,
WANCHAI, HONG KONG
TEL 852 - 2862 - 6900
FAX 852 - 2866 - 1343

SAMSUNG ELECTRONICS TAIWAN CO., LTD.

30FL., NO.333, KEELUNG RD.,
SEC1, TAIPEI, TAIWAN, R.O.C
TEL 886 - 2 - 757 - 7292
FAX 886 - 2 - 757-7311

SAMSUNG ASIA PRIVATE LIMITED

80. ROBINSON ROAD, #20 - 01
SINGAPORE 068898
TEL 65 - 535 - 2808
FAX 65 - 227 - 2792

SAMSUNG ELECTRONICS CO., LTD.

SHANGHAI OFFICE

9F, SHANGHAI INTERNATIONAL TRADE CENTRE,
NO.2200 YANAN(W) RD.,
SHANGHAI, CHINA 200335
TEL 8621 - 6270 - 4168
FAX 8621 - 6275 - 2975