General Description

Silicon Image's SiI2020A is a serializer/deserializer (SerDes) capable of transmitting and receiving data at 1.0625 and 2.125 gigabits-per-second (Gbps) targeting Fibre Channel applications. Designed for power, performance and price, the SiI 2020A SerDes makes use of a robust, low-power, low-cost, low-jitter, single-PLL CMOS design that comes in compact 64-pin, 14 mm MQFP and 10 mm TQFP packages. The SiI2020A supports selectable transmit and receive data rates for automatic speed negotiation and a narrow 10-bit SSTL_2-compatible interface for parallel data input/output. The innovative digital, fast-locking, single-PLL design enables high data reliability and ease-of-design while eliminating the need for external PLL capacitors and multiple PLLs.

The SiI2020A leverages much of the circuit innovation at the physical layer of Silicon Image's proprietary reduced overhead Multi-layer Serial Link (MSL™) architecture, which was pioneered and proven with our market-leading PanelLink® products. Silicon Image has shipped over 20 million units of PanelLink products for host systems and displays in the PC and the CE markets, notable for their noisy operating conditions. The MSL technology is a multi-layered approach to providing cost-effective, multi-gigabit semiconductor solutions on a single chip for high-bandwidth applications.

SiI 2020A Pin Diagram

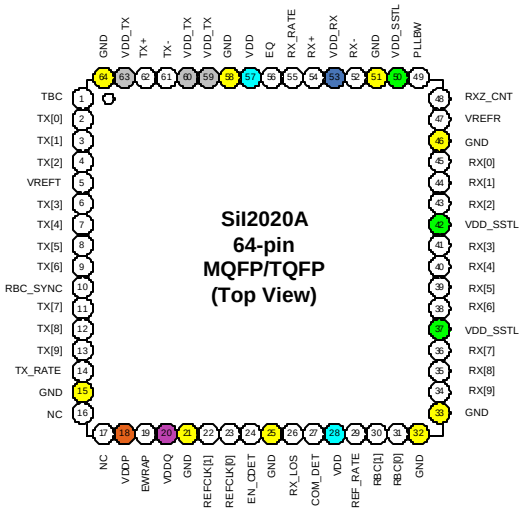


Figure 1. SiI2020A Pin Diagram

Features

General

- Fibre Channel-compliant
- Multi-rate: 1.0625 Gbps and 2.125 Gbps

Low Power

- Single 2.5V supply for core circuits and high-speed I/O
- Power dissipation at 2.125 Gbps: 425mW (typical), 665mW (maximum)

Cost Effective

- Standard CMOS technology
- Compact 64-pin, 14 x 14mm MQFP package
- Compact 64-pin, 10 x 10mm TQFP package

Narrow parallel I/O Interface

- 10-bit interface with DDR for 2.125 Gbps mode
- SSTL_2 and High-Speed Parallel Interface (HSPI)-compliant
- Separate transmit byte clock (TBC) for latching parallel input data

Highly Reliable Serial Interface

- Separately selectable Tx and Rx data rates
- Single, digital PLL architecture
- Very-low-jitter PLL: 2.7 ps (random jitter), 24.6 ps (deterministic jitter)
- Adjustable PLL filter bandwidth
- Variable pre-emphasis control
- Variable on-chip termination resistor
- Full ESD tolerance to 2kV

Proven Technology

- MSL™-based technology proven with PanelLink® ICs for the PC and the CE markets (2-5 Gbps, over 20M units shipped)
- Robust design for "noisy" environments

Functional Block Diagram

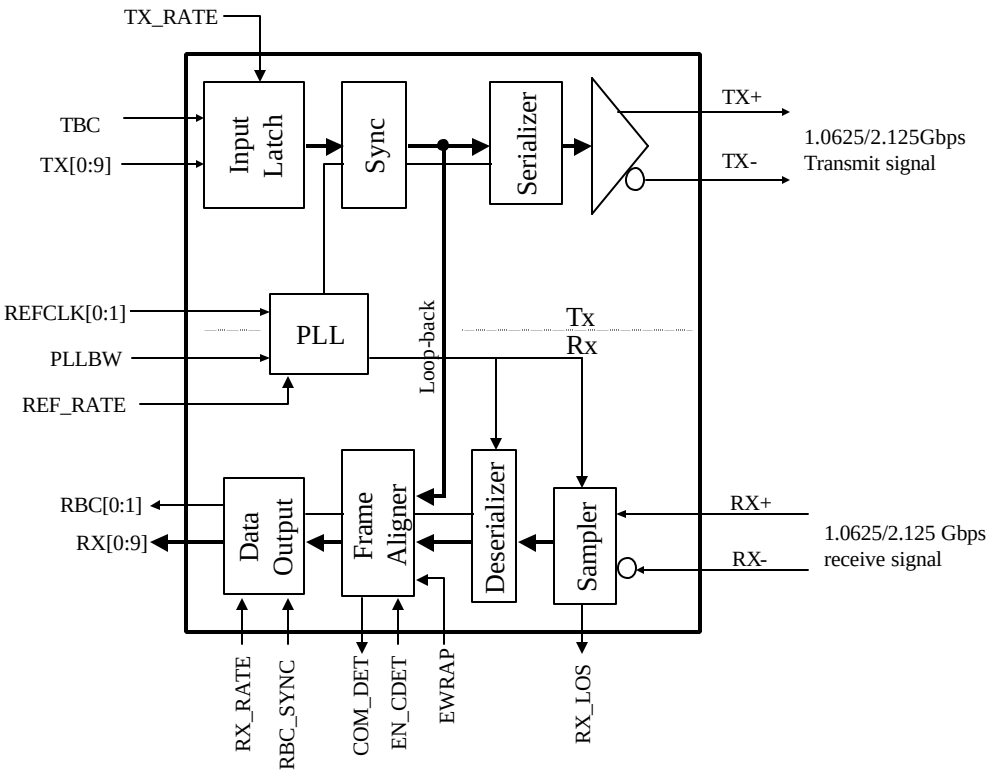


Figure 2. Functional Block Diagram

Single PLL: Only one PLL is used in the SiI 2020A SerDes. The internal PLL generates multiple phases from an external reference (REFCLK[0:1]) to not only transmit but also to receive serial data. For data reception, multiple phases are used to extract the incoming data and clock via oversampling. By eliminating one PLL, the SerDes consumes less power and is easier to design even in noisy environments. Hence, issues such as injection locking and interference between the transmission and reception clocks that are common to multiple-PLL architectures are eliminated.

10-bit Input Latch and Sync: SiI 2020A latches 10-bit parallel data on the falling edge of TBC in 1.0625 Gbps mode (TX_RATE = 0) and on both edges of TBC in 2.125 Gbps mode (TX_RATE = 1). After the data is captured using TBC, the data is synced with an internal clock generated from the PLL, which is generated from REFCLK[0:1]. Therefore, REFCLK and TBC must be synchronous with each other.

Serializer: The 10-bit parallel data are converted to high-speed serial data by the serializer. TX[0] is transmitted first and TX[9] is transmitted last. Pre-emphasis can be optionally added to the output streams. The amount of pre-emphasis is controlled by an external resistor.

R-Term: The termination value is controlled by the RXZ_CNT pin. When RXZ_CNT is high, the termination value is 75 Ohms and when RXZ_CNT is low, the termination value is 50 Ohms.

Sampler: The sampler oversamples the input data by a multiple factor of the input rate. This oversampled information is used to determine the correct sampling point of the incoming data.

Frame Aligner: If EN_CDET is high, the frame aligner finds the special characters (“0011111xxx”). If a special character is detected, the frame aligner aligns the incoming data so that the next comma or data character will start at RX[0]. The Comma character will be aligned at the rising edge of RBC1 in SiI2020A. If the first Comma is detected at the rising edge of RBC0, which is the misaligned case, the RBC1 will be stretched by a half clock , but never slivered, after the first Comma misalignment detection. During this realignment after the first Comma

misalignment detection, some data (less than 3 bytes after the first misaligned Comma) and possibly the first misaligned Comma may be lost or misaligned. However, the second Comma character and the subsequent data will be output correctly and properly aligned.

Loop-back: Loop-back mode can be used for diagnostic testing. When loop-back mode is enabled (EWRAP set high), the TX[0:9] input data are synced to the internal clock, realigned, and sent out as the RX[0:9] output. The TX+/- outputs are disabled and set to a DC logic state of 1; the RX+/- inputs are ignored. For normal operation, EWRAP should be low.

Electrical Specifications

Absolute Maximum Conditions

Symbol	Description	Min	Typ	Max	Units
V_{DD}	Supply Voltage 2.5V	-0.3		4.0	V
V_I	Input Voltage	-0.3		V_{DD}+ 0.3	V
T_{STG}	Storage Temperature	-65		150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)		33		°C/W

Notes: Permanent device damage may occur if absolute maximum conditions are exceeded.
Functional operation should be restricted to the conditions described under Normal Operating Conditions below.

Normal Operating Conditions

Symbol	Description	Min	Typ	Max	Units
V_{DD}	Supply Voltage	2.375	2.5	2.625	V
T_A	Ambient Temperature (with power applied)	0	25	70	°C

DC Digital I/O Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
VREFT	Input reference voltage	1.15	1.25	1.35	V
V_{IH}	High level input Voltage	V_{REFT}+0.35		V_{DD}+0.30	V
V_{IL}	Low level input Voltage	-0.3		V_{REFT}-0.35V	V
V_{IHPECL}	High level LVPECL input Voltage for REFCLK[0:1]	V_{DD} -0.4		V_{DD} +0.4	V
V_{ILPECL}	Low level LVPECL input Voltage for REFCLK[0:1]	-0.3		V_{DD}-0.7	V
$V_{IHLVTTL}$	High level LVTTL input Voltage for REFCLK[0:1]	2.0			V
$V_{ILLVTTL}$	Low level LVTTL input Voltage for REFCLK[0:1]			0.80	V
V_{OH}	High level output voltage	1.9			V
V_{OL}	Low level output voltage	GND		0.6	V

DC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{SOUT75}	TX+/TX- differential peak-to-peak voltage swing.	Terminated by 75 Ohms	1100	1500	1800	mV
V_{SOUT50}	TX+/TX- differential peak-to-peak voltage swing.	Terminated by 50 Ohms.	800	1100	1500	mV
V_{IN}	RX+/RX- differential peak-to-peak input sensitivity		200		2000	mV
V_{DIH}	RX+/RX- differential Input common-mode voltage [3]			V_{DD}		V
V_{DOH}	TX+/TX- differential Output common-mode voltage [3]			1.2		V
P_{CC}	Power dissipation	C_{LOAD}=5pF 2.125 Gbps rate TX+/- = 50ohms terminated		425[1]	665[2]	mW

[1] Sending/Receiving Random Pattern

[2] Sending/Receiving Worst Case (maximum transitions) Pattern

[3] Self biased

REFCLK[0:1], TBC Parameters

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
T_{REF_FREQ}	Nominal Frequency		106.25		MHz
T_{REF_J}	REFCLK[0:1] frequency tolerance	-100		100	ppm
T_{REF_DUTY}	REFCLK[0:1] duty cycle	40%		60%	
T_{RT_SKEW}	REFCLK to TBC skew (REFCLK and TBC must be synchronous with each other)	-2		2	ns

Transmit Function AC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
T_{TXS}	TX[0:9] setup time to the falling edge of TBC (TX_RATE=0)	1400			ps
T_{TXH}	TX[0:9] hold time from the falling edge of TBC (TX_RATE=0)	1400			ps
T_{TCT}	TX[0:9], TBC transition time (TX_RATE=1)			1880	ps
T_{TCV}	TX[0:9], TBC valid/stable time (TX_RATE=1)	2820			ps
T_{RISE}	TX+/TX- rise time into 50 Ohms. Measured from 20% and 80% of full swing.		200		ps
T_{FALL}	TX+/TX- fall time into 50 Ohms. Measured from 20% and 80% of full swing.		200		ps
T_{TXLAT}	Latency from TX[0:9] parallel input to TX+/TX- serial output		18		ns
T_{TRJ}	TX+/TX- output random RMS jitter[4] [5]		2.7		ps
T_{TDJ}	TX+/TX- output deterministic jitter[6]		24.6		ps

[4] Random jitter was measured according to "Fibre Channel Specification X3.230-1994 FC-PH, Annex A, Section A.4.4 (oscilloscope method)".

[5] Histogram for random jitter is shown in Figure 11.

[6] Deterministic jitter was measured according to "Fibre Channel Specification X3.230-1994 FC-PH, Annex A, Section A.4.3"

Conditions:

All parameters are measure to 50% of full swing except where noted.

Receiver Function AC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
T_{AXS}	**Mode A**, RX[0:9] setup time to the rising edge of RBC[0:1]	3			ns
T_{AXH}	**Mode A**, RX[0:9] hold time to the rising edge of RBC[0:1]	2.5			ns
T_{ARR}	**Mode A**, RBC[1] to RBC[0] rising edge skew	8.8		9.9	ns
T_{BXS}	**Mode B**, RX[0:9] setup time to the rising edge of RBC[0] , or falling edge of RBC[1]	3			ns
T_{BXH}	**Mode B**, RX[0:9] hold time to the rising edge of RBC[0] , or falling edge of RBC[1]	3			ns
T_{CXS}	**Mode C**, RX[0:9] setup time to the rising edge of RBC[0:1]	1.4			ns
T_{CXH}	**Mode C**, RX[0:9] hold time to the rising edge of RBC[0:1]	1.4			ns
T_{CRR}	**Mode C**, RBC[1] to RBC[0] rising edge skew	4.5		4.9	ns
T_{DCT}	**Mode D**, RX[0:9] transition time			1.5	ns
T_{DCV}	**Mode D**, RX[0:9] valid/stable time	3			ns
T_{RRISE}, T_{RFALL}	Parallel output rise/fall. Measured from 20% and 80% of full swing.			2	ns
T_{RDUTY}	Duty cycle of RBC[0:1]. Measured from 20% and 80% of full swing.	40%		60%	
T_{RXLAT}	Latency from RX+/RX- serial input to RX[0:9] parallel output		32		ns
T_{JUMP}	RCLKP/RCLKN cycle to cycle period variation. Phase jump of synthesized clock.			1/3	RX0+/- bit time

Conditions:

1. RBC[1] /RBC[0] and RX[0:9] are loaded by 10pF to ground for these measurements.
2. All parameters are measure to 50% of full swing except where noted.

PLL Parameters

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
$T_{PLLLOCK}$	PLL Locking time			200	µs
T_{BSYNC}	Bit sync time		200	2500	bits

AC Timing

Transmit Timing

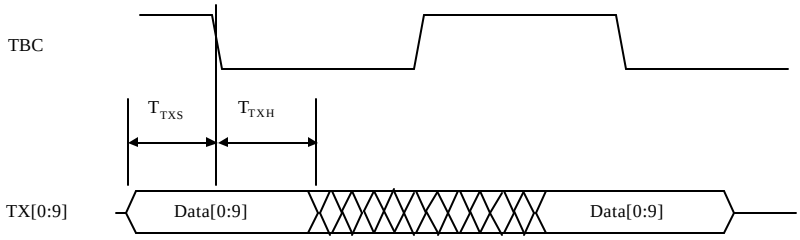


Figure 3. Input Timing for TX_RATE = 0 (1.0625 Gbps mode)

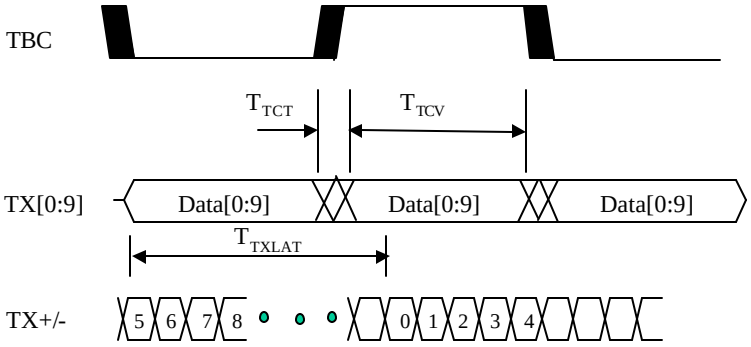


Figure 4. Input Timing for TX_RATE = 1 (2.125 Gbps mode)

Receive Timing

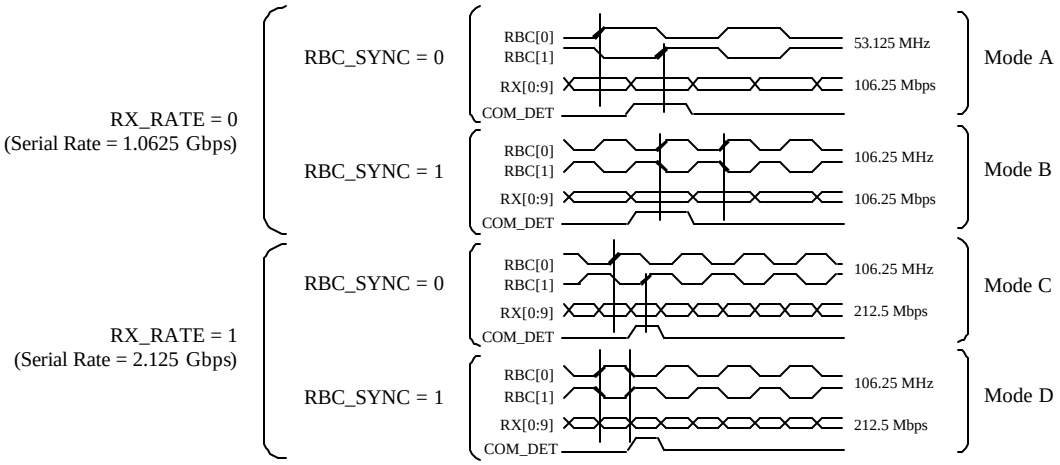


Figure 5. Parallel Output Modes

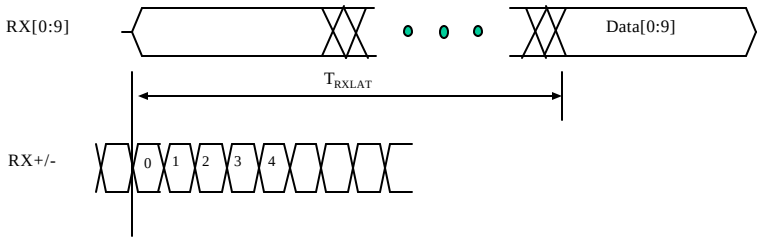


Figure 6. RX Latency

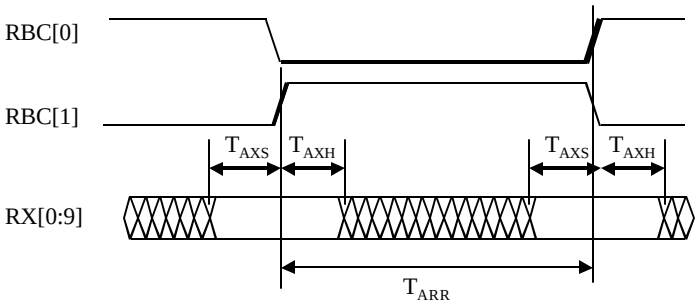


Figure 7. Mode A Timing Diagram (RX_RATE=0, RBC_SYNC=0)

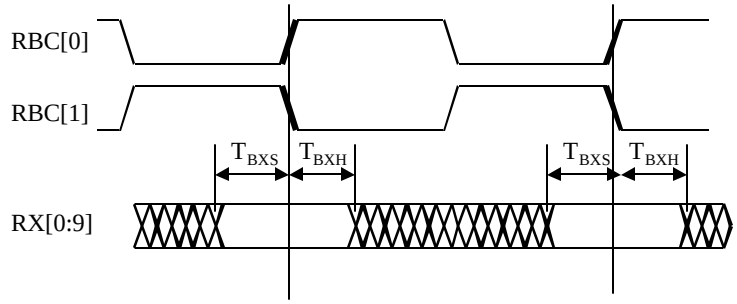


Figure 8. Mode B Timing Diagram (RX_RATE=0, RBC_SYNC=1)

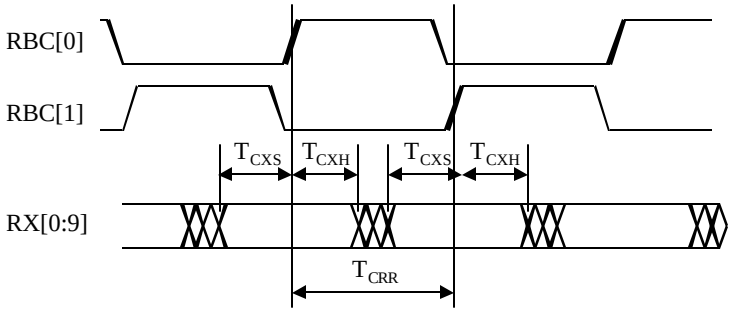


Figure 9. Mode C Timing Diagram (RX_RATE=1, RBC_SYNC=0)

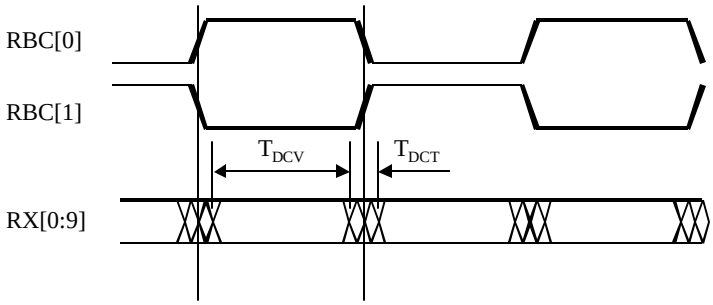


Figure 10. Mode D Timing Diagram (RX_RATE=1, RBC_SYNC=1)

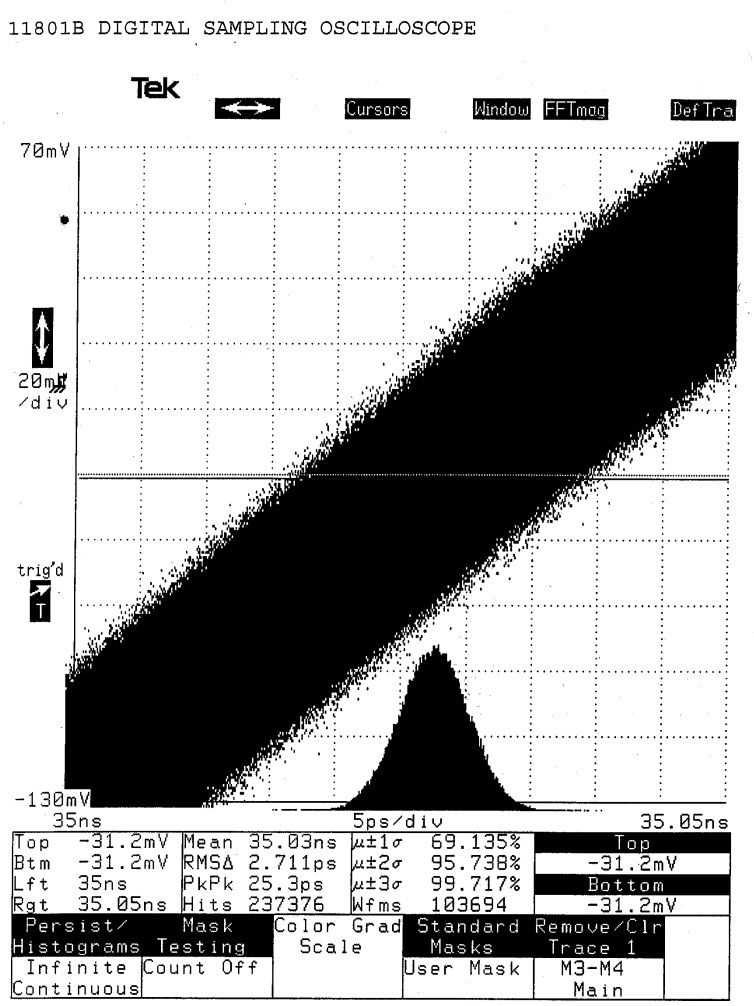
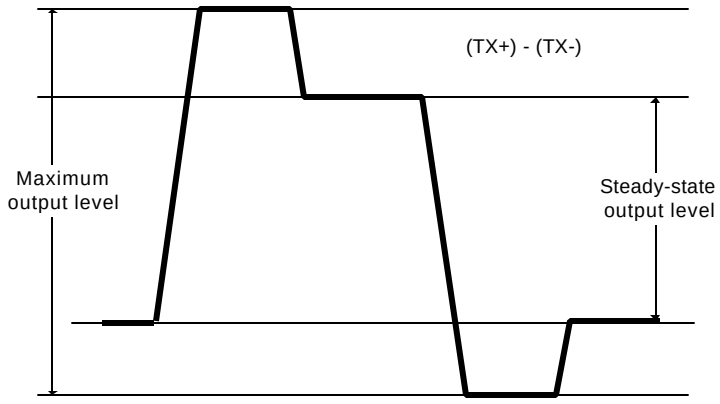


Figure 11. TX+/TX- Output Random Jitter with Equalization Disabled



TX+/- terminated by 50 ohms, V_{DD} = 2.5V, T_A = 25 °C
The maximum output level (EQ pin = 0V) = V_sout50 in the DC specifications.

Figure 12. Waveform for Pre-emphasis Values

Pins Descriptions

Functional Pins

Pin Name	Pin #	Type	Description
TX[0], TX[1], TX[2], TX[3], TX[4], TX[5], TX[6], TX[7], TX[8], TX[9]	2, 3, 4, 6, 7, 8, 9, 11, 12, 13	In - SSTL2	TX[0:9] : Input pins for the 10-bit encoded data character that is to be transmitted serially over the TX+,TX- differential outputs. The first serial bit transmitted will be TX[0].
RX[0], RX[1] RX[2], RX[3], RX[4], RX[5], RX[6], RX[7], RX[8], RX[9]	45, 44, 43, 41, 40, 39, 38, 36, 35, 34	Out - SSTL2	RX[0:9] : 10-bit received data.
TX+ TX-	62 61	Out Out	TX+, TX- : Serialized, high speed. When parallel loop-back is disabled (EWRAP=0) these pins are active. When EWRAP=1, these pins are driven to logic 1.
RX+ RX-	54 52	In In	RX+, RX- : Serialized, high speed, differential inputs. These pins are active when loop-back is disabled (EWRAP=0).
REFCLK[1], REFCLK[0]	22 23	In-LVPECL/LVTTL In-LVPECL/LVTTL	REFCLK[0:1] are differential reference clock inputs. This clock source is used by both transmit and receive sections of the device. When REF_RATE=1, these pins are used to input a 53.125 MHz clock signal. When REF_RATE=0, these pins input a 106.25 MHZ clock signal. These pins can be driven by a differential PECL clock source, or by a LVTTL single-ended clock on REFCLK[1] with REFCLK[0] connecting to GND via 0.1µF capacitor.
TBC	1	In - SSTL2	Transmit byte clock. This clock is used to capture the parallel input data (TX[0:9]). When TX_RATE = 0, the falling edge of TBC is used to capture the parallel data. When TX_RATE=1, data is captured between both the rising and falling edges of TBC resulting in a doubling of the data rate.
RBC[1] RBC[0]	30 31	Out - SSTL2	Recovered clock output. These clock outputs are used by external devices to capture the RX[0:9] parallel data. The two clocks are 180 degrees out of phase with each other. The relationship between these clocks and the parallel data depends on the settings of RX_RATE, RBC_SYNC (see output timing figures for details).
REF_RATE	29	In - LVTTL	Sets the rate of the input reference clock. REF_RATE=0, the reference clock frequency is 106.25 MHz. REF_RATE=1 the reference clock frequency is 53.125 MHz.
RX_RATE	55	In - LVTTL	Receiver rate. The setting of this signal determines the rate at which the receiver operates. RX_RATE=0, the incoming serial stream is sampled at 1.0625 Gbps and the parallel data is driven out on the rising edge of RBC[1]. RX_RATE=1, the incoming serial stream is sampled at 2.125 Gbps and the parallel data is driven out on the rising edge of RBC[1] and RBC[0].
TX_RATE	14	In - LVTTL	Transmitter rate. The setting of this signal determines the rate at which the transmitter operates. TX_RATE=0, the incoming parallel data stream is sampled on the falling edge of TBC. The data is then serialized and transmitted at a rate of 1.0625 Gbps. TX_RATE=1, the incoming serial stream is sampled between BOTH edges of TBC. The data is then serialized and transmitted at a rate of 2.125 Gbps.
NC	16	-	No connect
NC	17	-	No connect

Functional Pins (continued)

Pin Name	Pin #	Type	Description
RBC_SYNC	10	In - SSTL2	When RX_RATE = 0, Setting RBC_SYNC determines the frequency of RBC, RBC=53.125 MHz for RBC_SYNC = 0, and RBC= 106.25 MHz for RBC_SYNC= 1. When RX_RATE = 1, setting RBC_SYNC = 1 the receiver parallel output data and clocks transition simultaneously.
EQ	56	In- Analog	Equalization control. This pin is used to input a voltage reference that sets the amount of equalization on the TX+/- outputs. To disable equalization this pin must be connected to a voltage below 600mV. As the voltage input on the pin is raised above 600mV the strength of the equalization is increased, reaching a maximum when the voltage input on EQ equals VDD. The following list shows the typical amount of pre-emphasis obtained for three settings of the EQ voltage reference. See Figure 12 for reference. **Voltage input = 0V:** Maximum output level = 100% Steady-state output level = 95% **Voltage input = 1.25V:** Maximum output level = 125% Steady-state output level = 65% **Voltage input = 2.0V:** Maximum output level = 155% Steady-state output level = 30%
EWRAP	19	In - LVTTL	Enable parallel loop-back mode. When loop-back is enabled, parallel input data is looped to the parallel output data, the serializer/deserializer circuits are bypassed. EWRAP=0 loop-back mode is disabled. EWRAP=1, loop-back mode is enabled.
EN_CDET	24	In - LVTTL	Enable comma detection (activated with high).
COM_DET	27	Out - SSTL2	Comma detection signal. This signal is driven high when a comma character of positive disparity (0011111xxx) is detected on the high-speed serial input lines.
RX_LOS	26	Out - SSTL2	Indicates whether there is any valid signal on RX+/- pins. If RX+/- > 200mVp-p, RX_LOS = 0 If RX+/- < 200mVp-p and RX+/- > 75mV, RX_LOS = undefined If RX+/- < 75mVp-p, RX_LOS = 1, RX[0:9] = B'1111111111'
VREFT	5	In - Analog	Voltage reference input, set by external voltage divider to 1.25V for SSTL2 input.
VREFR	47	Out - Analog	Voltage reference output, externally outputs the voltage reference corresponding to 1.25V for SSTL2 output.
PLLBW	49	In - LVTTL	PLL bandwidth control. PLLBW = 0, PLL bandwidth is reduced for filtering input reference clock jitter PLLBW = 1, bandwidth is normal If this pin is left unconnected, it will be internally pulled high (normal bandwidth) by default.
RXZ_CNT	48	In - LVTTL	RX input impedance matching control RXZ_CNT = 0, RX differential inputs are terminated by 50 ohms RXZ_CNT = 1, RX differential inputs are terminated by 75 ohms If this pin is left unconnected, it will be internally pulled down (terminated by 50 ohms) by default.

Power & Ground Pins

Pin Name	Pin #	Type	Description
VDD	28, 57	Power	Power supply for digital logic circuits.
VDD_RX	53	Power	High Speed Receiver Supply. For the best performance, this supply should be as noise free as possible.
VDD_TX	59, 60, 63	Power	High Speed Transmiter Supply. For the best performance, this supply should be as noise free as possible.
GND	15, 21, 25, 32, 33, 46, 51, 58, 64	Ground	Power ground for digital logic circuits.
VDD_SSTL	37, 42, 50	Power	Power supply for I/O pads (2.5V).
VDDQ	20	Power	Power supply for internal PLL interface (2.5V). For the best performance, this supply should be as noise free as possible.
VDDP	18	Power	Power supply for PLL (2.5V). For the best performance, this supply should be as noise free as possible.

Package Dimensions

64-pin MQPF Package Dimensions

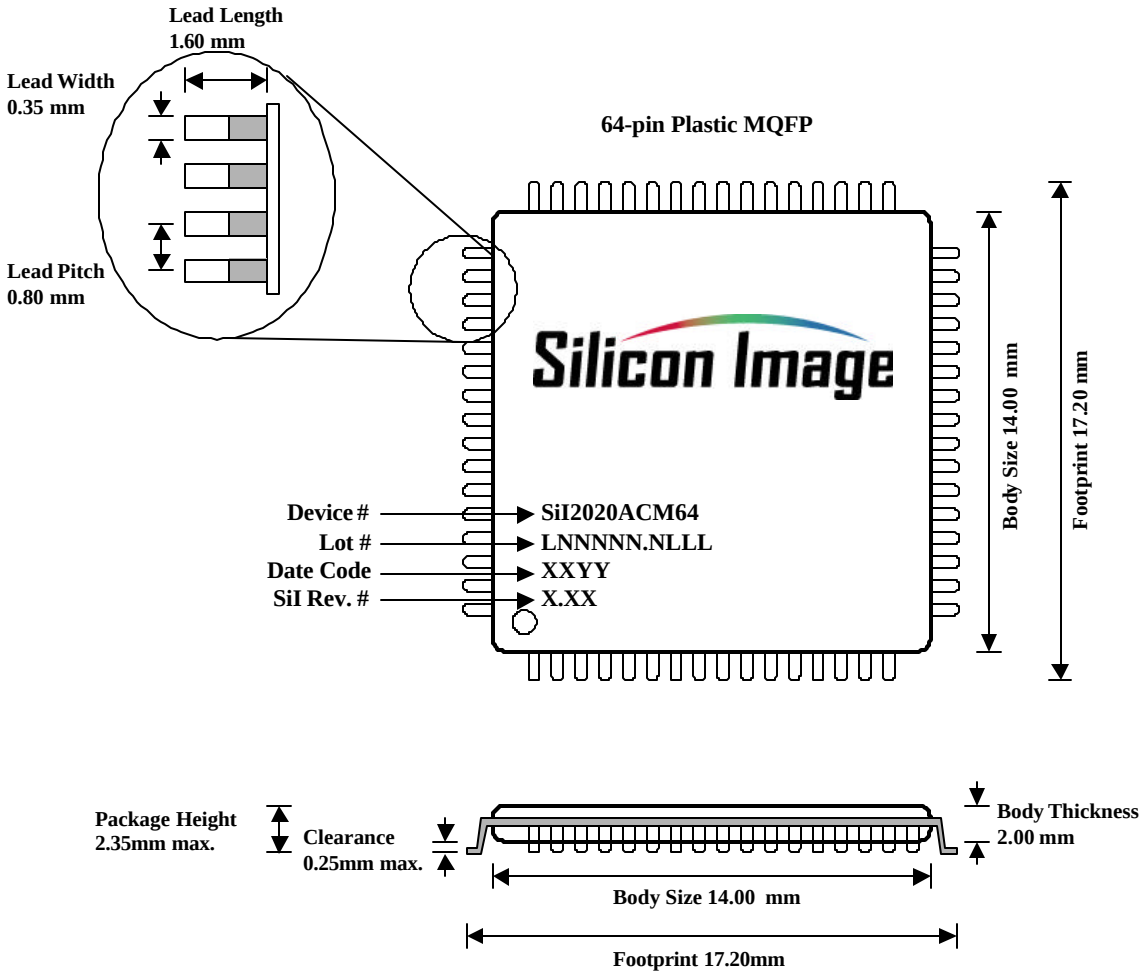
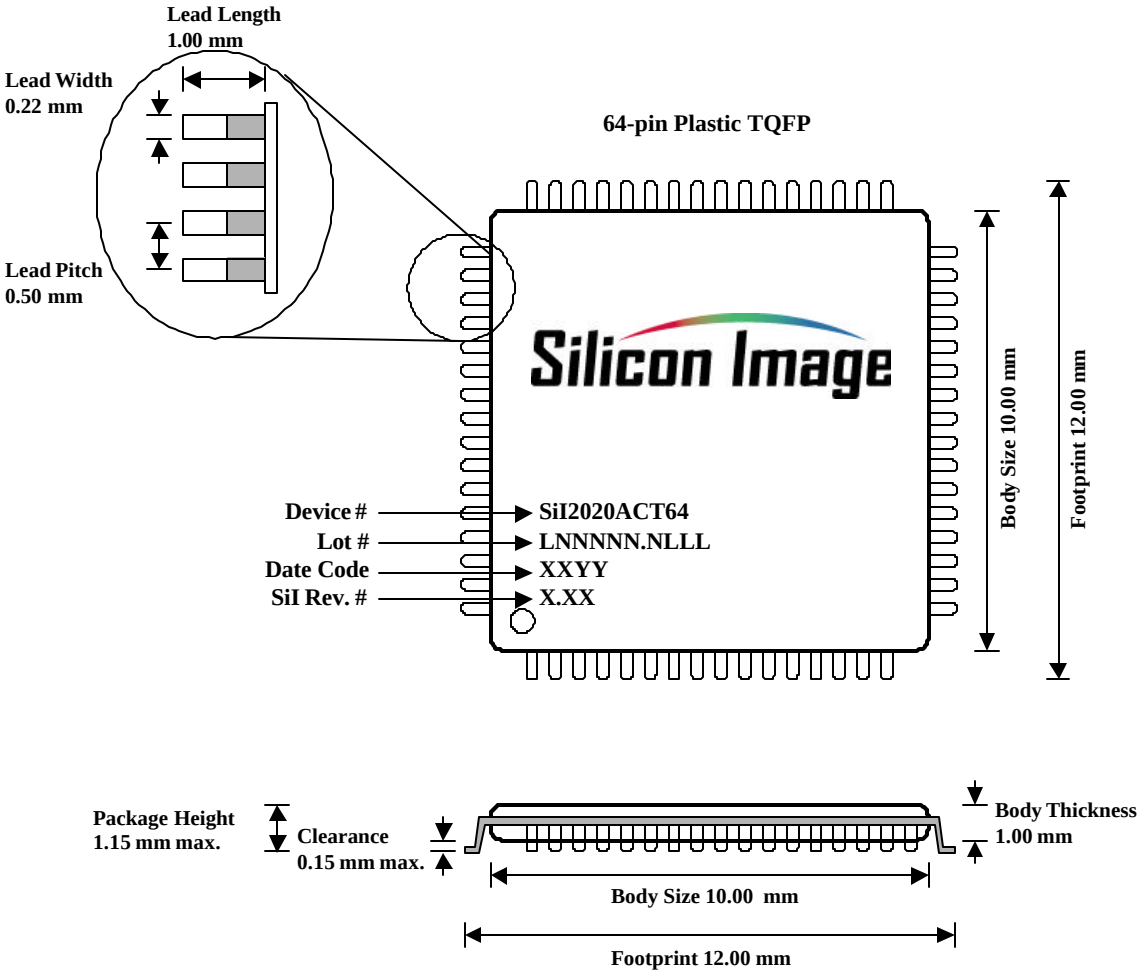


Figure 13. SiI2020ACM64 Package Diagram

Package Dimensions

64-pin TQPF Package Dimensions



JEDEC code MS-026 ACD

Figure 14. SiI2020ACT64 Package Diagram

Part Ordering Number:
SiI2020ACM64 (64 pin MQFP)
SiI2020ACT64 (64 pin TQFP)

Revision History:

Revision	Comment	Date
A	Final Data Sheet	03/08/02

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