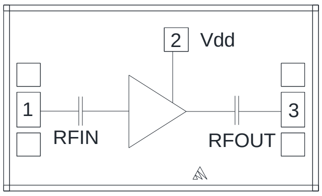
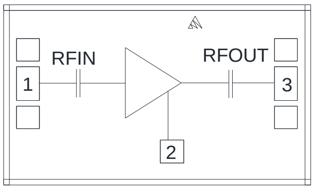
Feature

Frequency ： 10~18GHz
Noise： 1.1dB
Gain ： 24dB
Gain Flatness： ±1dB
P1dB Pout： 9dBm
Psat： 10dBm
Output IP3： 20dBm
Bias Condition： Single Power Supply:+5V@25mA
Input/Output Impedence： 50 Ω
Dimension： 1.34mm×0.8mm×0.07mm

Function Diagram





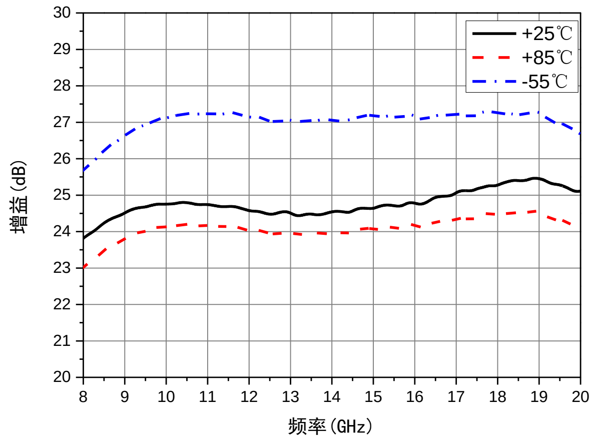
Electrical Specification(T_A = +25℃,50 Ω system, Vdd = +5V， Idd = 25mA)

Symbol	Parameter	Min	Typical	Max	Unit
Frequency	Frequency	10		18	GHz
Gain	Gain		24		dB
ΔG	Gain Flatness		±1		dB
NF	Noise		1.1		dB
IRL	Input Return Loss		12		dB
ORL	Output Return Loss		13		dB
P1dB	1dB Compression Pad Pout		+9		dBm
Psat	Psat		+10		dBm
Idd	Operation Current		25		mA

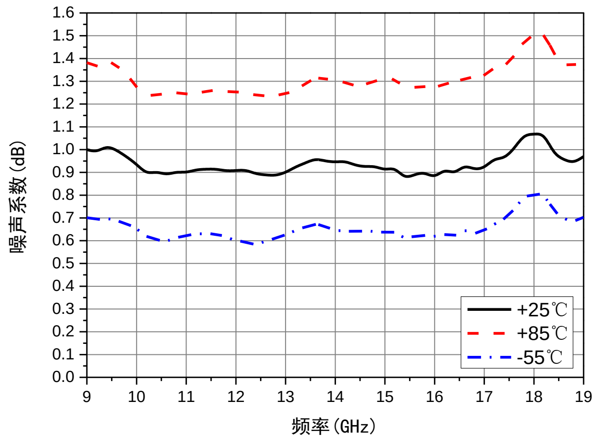
Note: The MMIC has been 100%DC and RF tested on chip.

Test Curves

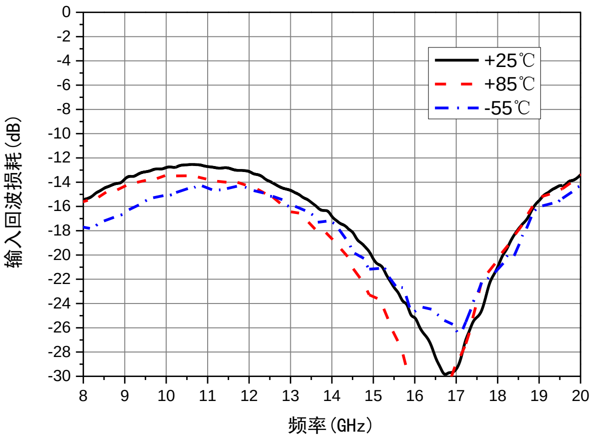
Small Signal Gain vs. Frequency vs. Temperature



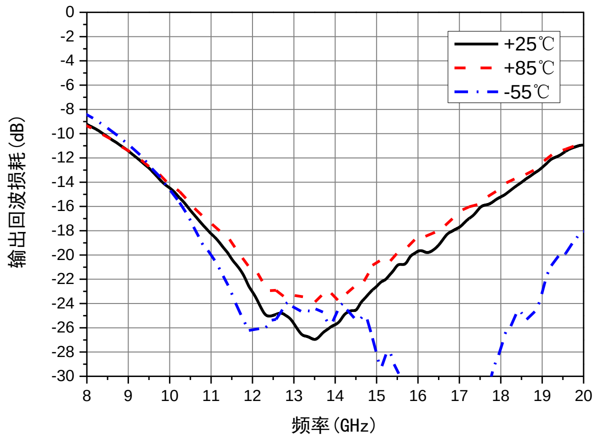
Noise vs. Frequency vs. Temperature



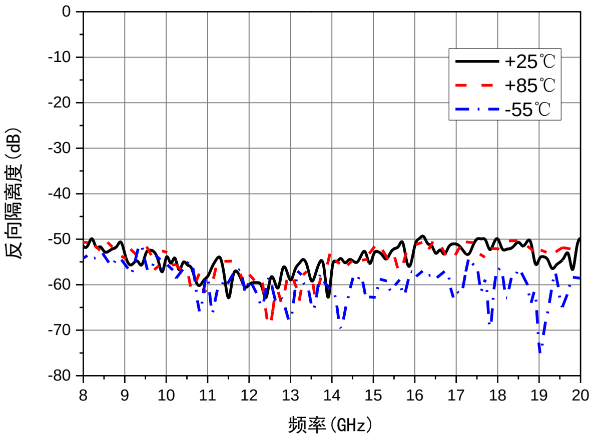
Input Return Loss vs. Frequency vs. Temperature



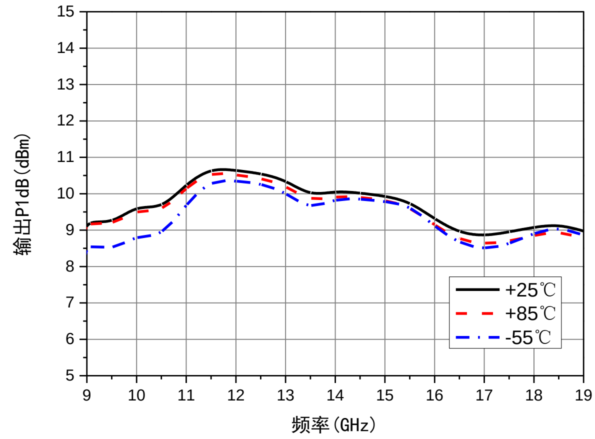
Output Return Loss vs. Frequency vs. Temperature



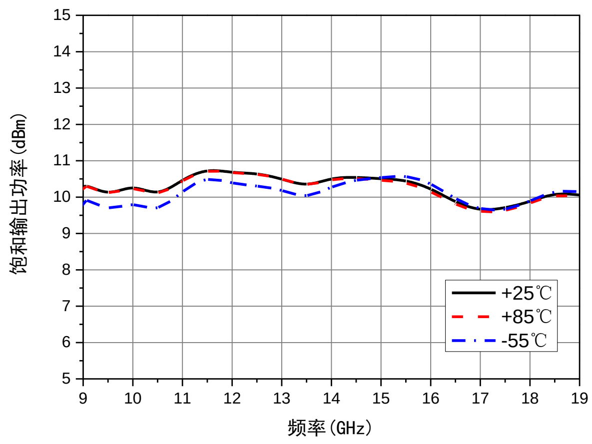
Reverse Isolation vs. Frequency vs. Temperature



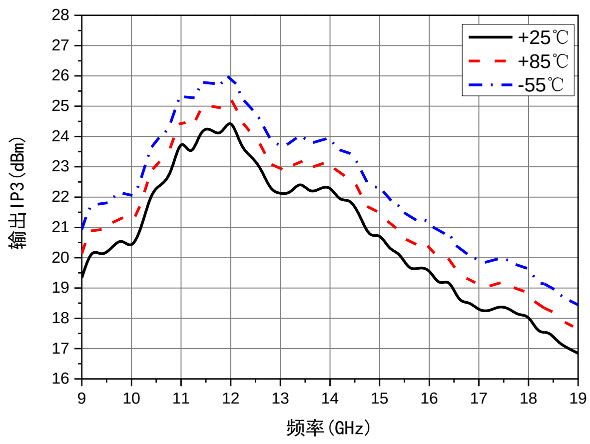
Output P1dB vs. Frequency vs. Temperature



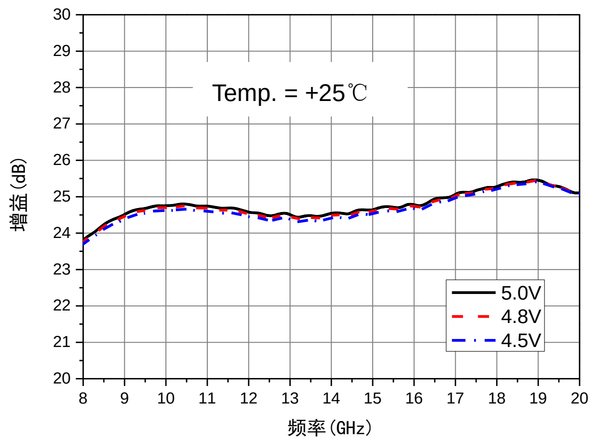
Psat vs. Frequency vs. Temperature



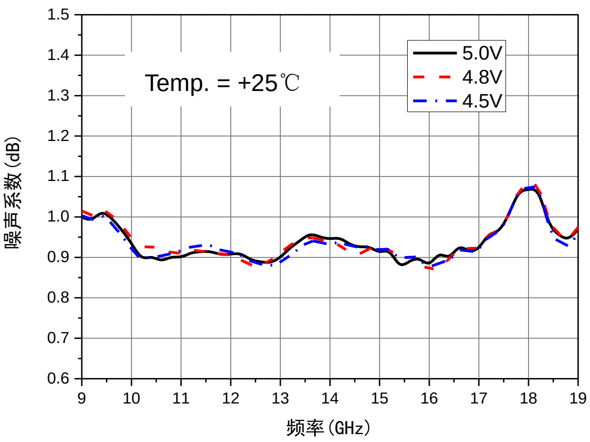
Output IP3 vs. Frequency vs. Temperature



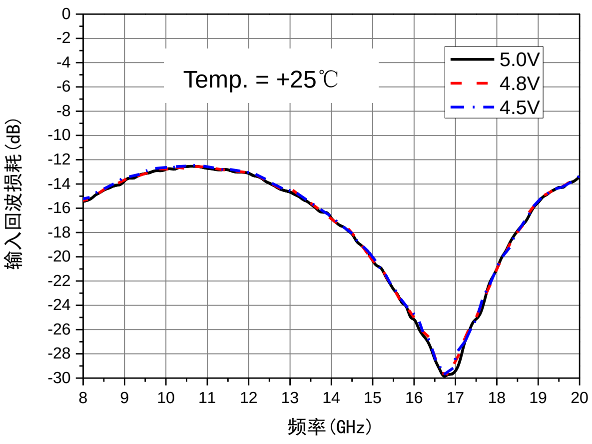
Small Signal Gain vs. Frequency vs. Vd



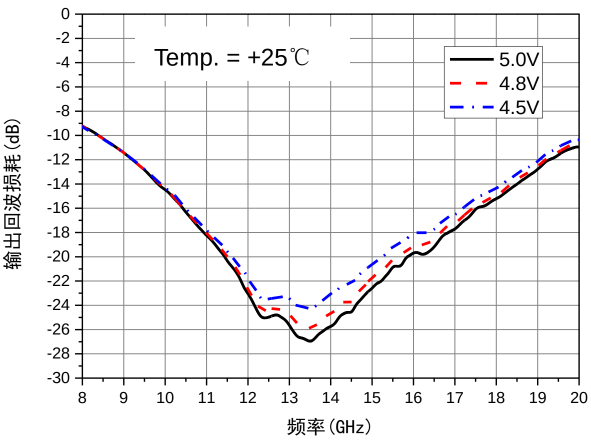
Noise vs. Frequency vs. Vd



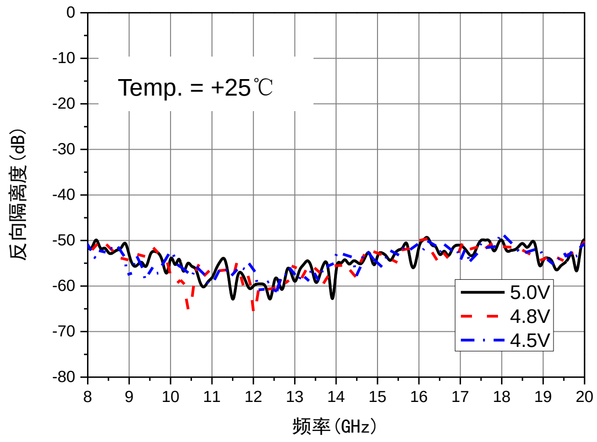
Input Return Loss vs. Frequency vs. Vd



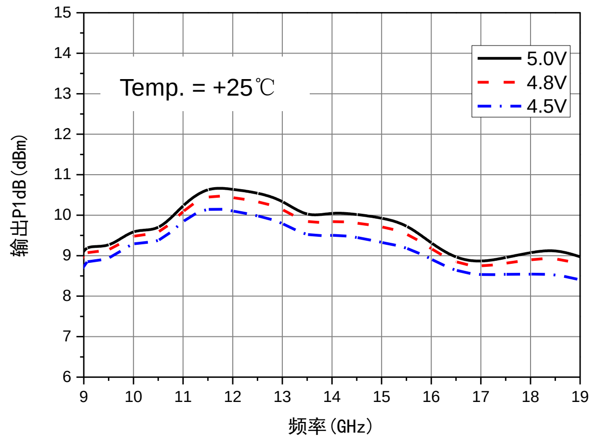
Output Return Loss vs. Frequency vs. Vd



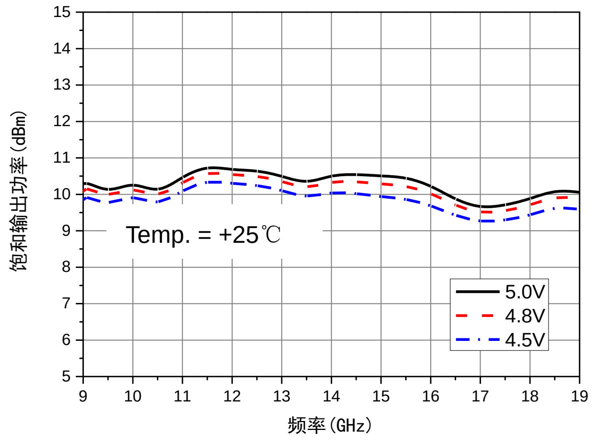
Reverse Isolation vs. Frequency vs. Vd



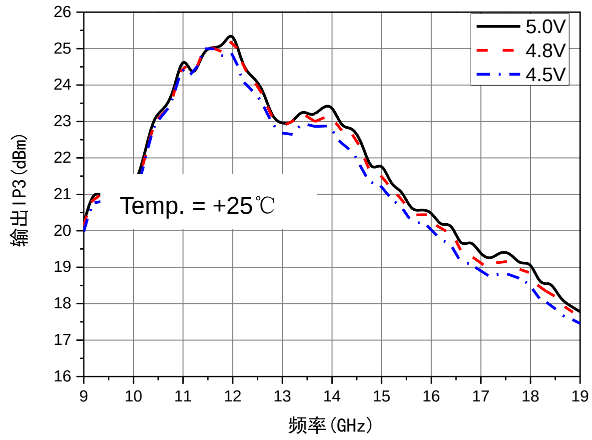
Output P1dB vs. Frequency vs. Vd



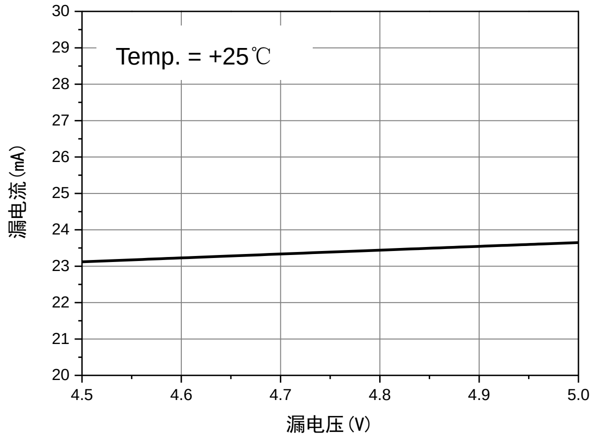
Psat vs. Frequency vs. Vd



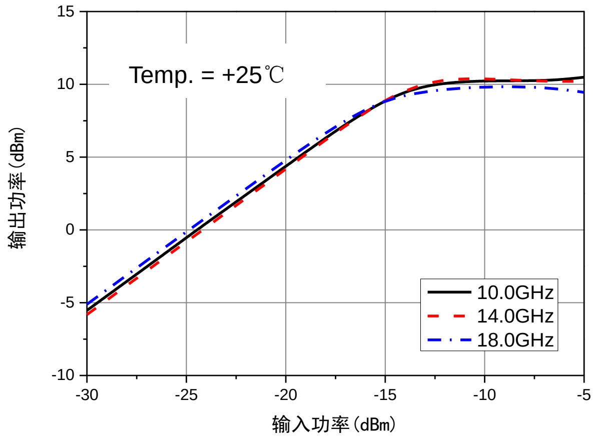
Output IP3 vs. Frequency vs. Vd



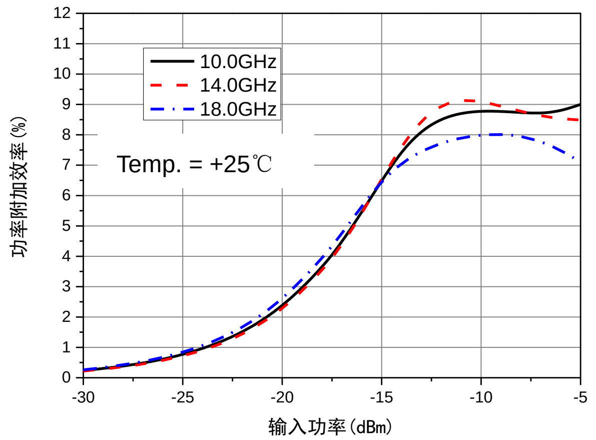
Id vs. Vd



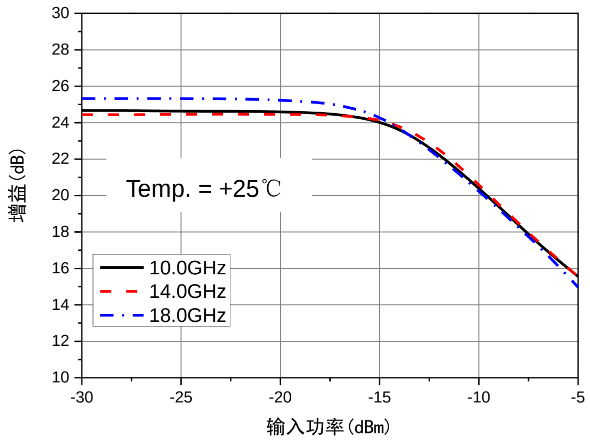
Pout vs. Pin vs. Frequency



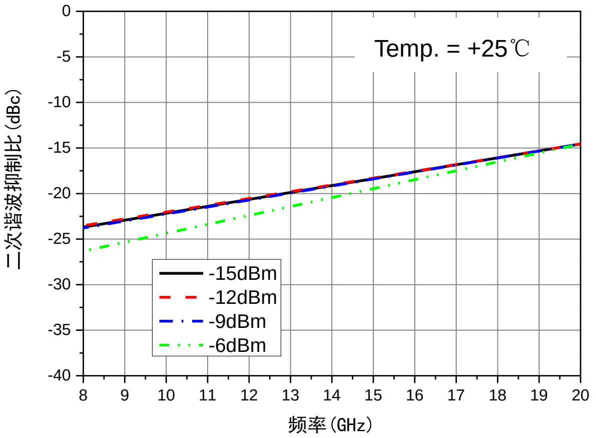
PAE vs. Pin vs. Frequency



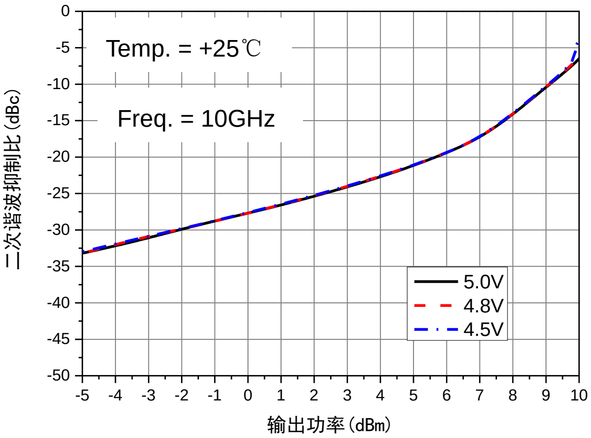
Gain vs. Pin vs. Frequency



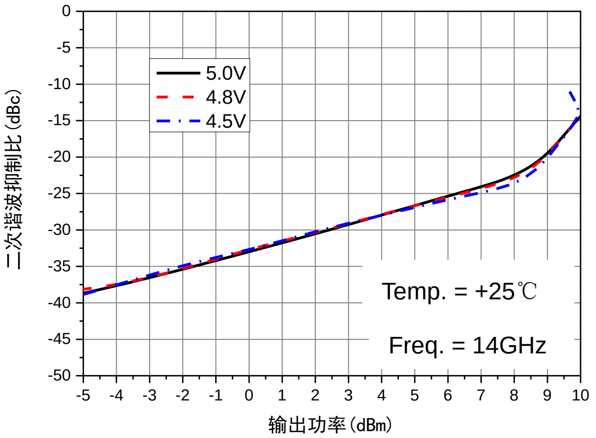
Second Harmonic suppression Ratio vs. Frequency vs. Pin



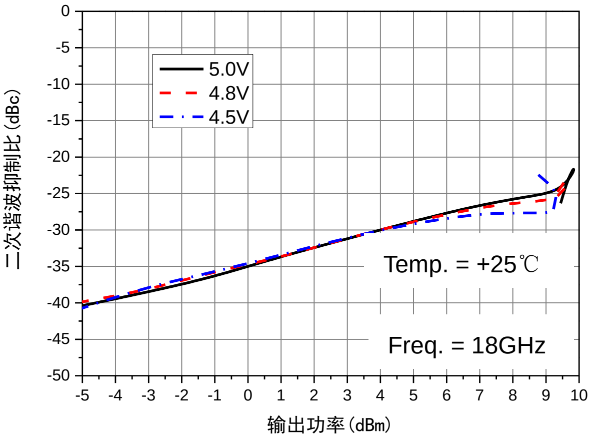
Second Harmonic suppression Ratio vs. Pout vs. Vd



Second Harmonic suppression Ratio vs. Pout vs. Vd



Second Harmonic suppression Ratio vs. Pout vs. Vd



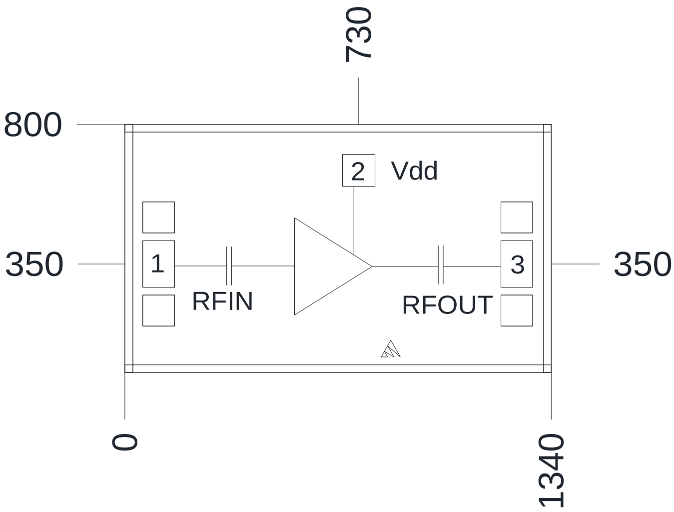
Max Limited Values

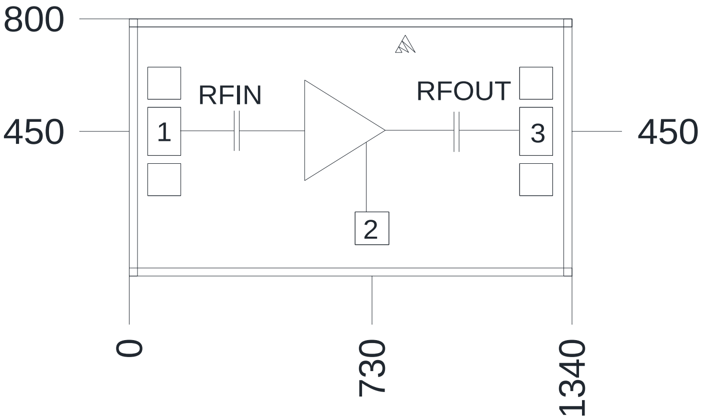
Parameter	Values
P_{IN}， 50Ω	+17dBm
Vdd	+6V
Rth	28.3℃/W
T_{CH}	175℃
Bonding Temperature （20seconds ， N_2 protection）	320℃
Storage Temperature	-55~+150℃
Operation Temperature	-55~+125℃

ELECTROSTATIC SENSITIVE E

OBSERVE HANDLING PRECAUTIONS

Outline and Dimension





Note：

1.unit：um

2.The back of the mmic should be golden.

3.The back of the mmic should be grounded.

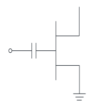
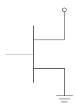
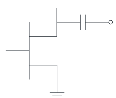
4.Bonding pad， 1、3 ： 100um×150um；

pad dimension： 2 ： 100um×100um；

5.The through-hole can not be bonded.

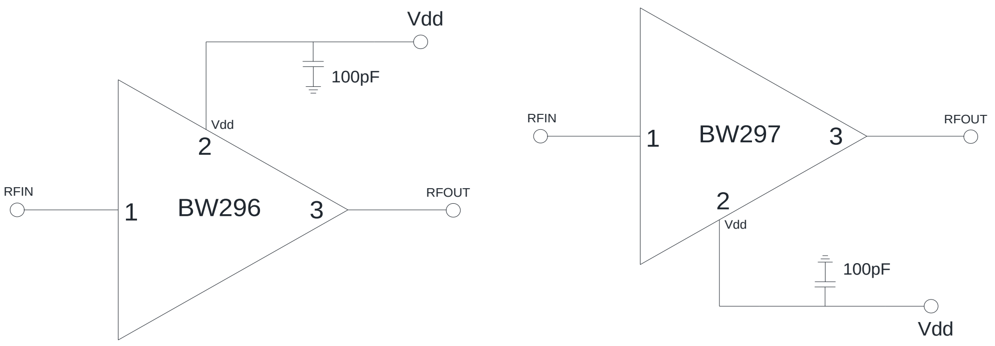
6.tolerance：±50um

Bonding pad definition

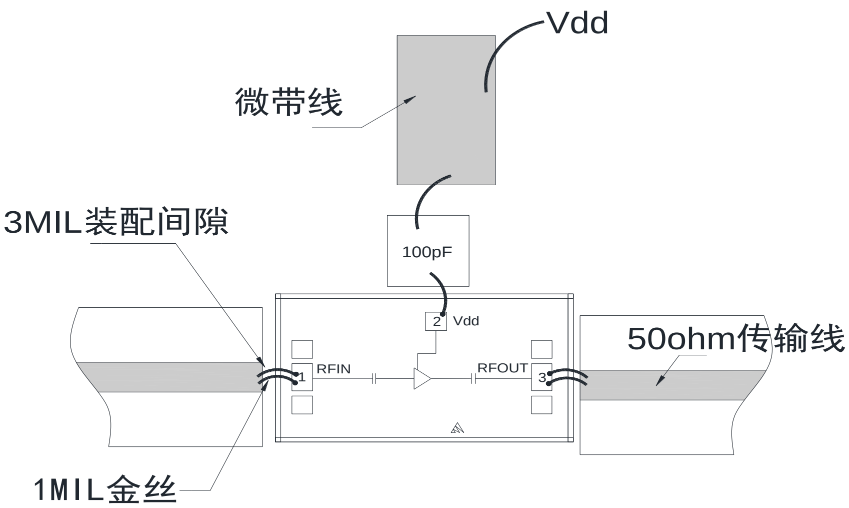
Pad Number	Symbol	Description	Equivalent Circuit
1	RFIN	RF signal input port, 50Ω system should be externally integrated, the block capacitor is not needed.	 RFIN
2	Vdd	Vdd，100pF bypass capacitor should be externally integrated.	 Vdd
3	RFOUT	RF signal output port, 50Ω system should be externally integrated, the block capacitor is not needed.	 RFOUT
Back of mmic	GND	The bottom of the mmic and RF and DC ground should be well connected.	 GND

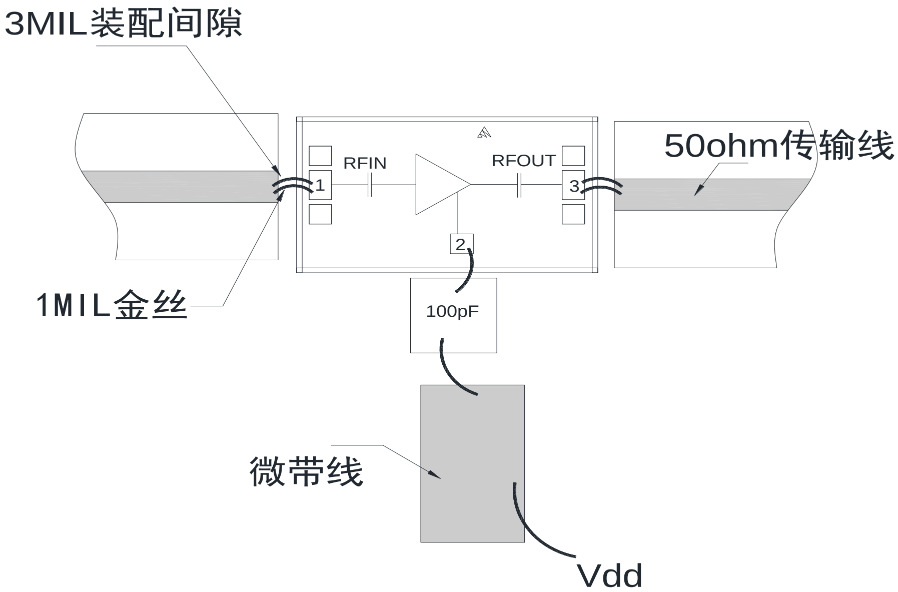
Application Information

1. Application Circuit

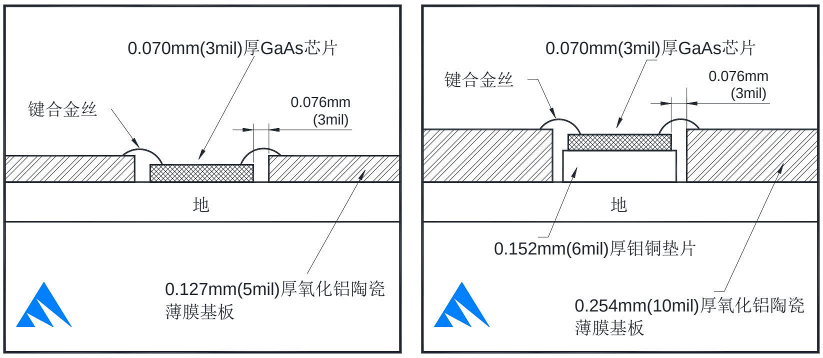


2.Assembly Diagram (The filter capacitor should be as close as possible to the pad to minimize the influence of the length of the bond wire)





3. Assembly Instruction



Note: The ceramic substrate should be as close to the chip as possible to shorten the size of the bonding alloy wire. The typical assembly gap is 0.076 to 0.152 mm (3 to 6 mils).

Attention

Storage: The chip must be placed in a container with electrostatic protection and stored in a nitrogen atmosphere.

Cleaning: The bare chip must be operated in a clean environment. Liquid cleaning agents are prohibited from cleaning the chip.

Electrostatic Protection: Please strictly abide by ESD protection requirements to avoid static damage to the device.

Regular operation: Use a vacuum chuck or precision pointed tweezers to pick up the chip. Avoid tools or fingers touching the surface of the chip during operation.

Mounting operation: Chip mounting can use AuSn solder eutectic sintering or conductive adhesive bonding process. The mounting surface must be clean and flat.

Sintering process: It is recommended to use an AuSn solder sheet with a gold/tin ratio of 80/20. The working surface temperature reached 255℃ and the tool (vacuum chuck) temperature reached 265℃. When the high-temperature gas mixture (nitrogen-hydrogen ratio is 90/10) is blown onto the chip, the temperature at the tip of the tool is raised to 290℃. Do not allow the chip to go above 320℃ for more than 20 seconds. Rubbing time should not exceed 3 seconds.

Adhesion process: The amount of conductive glue to be dispensed should be as small as possible. After the chip is placed in the installation position, the conductive adhesive can be seen around it. Curing conditions refer to information provided by the manufacturer of conductive adhesives.

Bonding operation: Φ0.025mm (1mil) gold wire is used for both spherical and wedge bonding. Thermosonic bonding temperature 150℃. Ball bond guillotine pressure 40~50gf, wedge bond guillotine pressure 18~22 gf. Use as little ultrasonic energy as possible. Bonding starts at the pressure point on the chip and ends at the package (or substrate).