ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H141
Four-Bit Universal Shift Register

PRELIMINARY INFORMATION

This document contains specifications and information which are subject to change.

Features/Benefits

- **Shift frequency, 250 MHz min**
- **Power dissipation, 425 mW typical**
- **Noise margin 150 mV**
- **Voltage compensated**
- **ECL 10K-compatible**

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H141	J,N,NL(20)	Com

Description

The MC10H141 is a four-bit universal shift register which performs shift-left, or shift-right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control

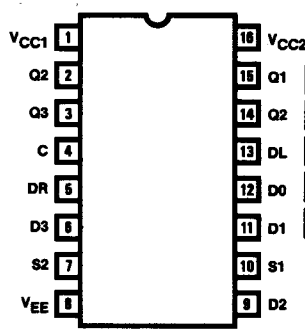
(See following page)

Function Table

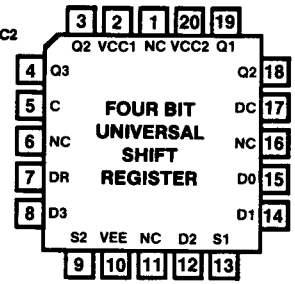
SELECT		OUTPUTS				OPERATING MODE
S1	S2	$Q0_{n-1}$	$Q1_{n-1}$	$Q2_{n-1}$	$Q3_{n-1}$	
L	L	D0	D1	D2	D3	Parallel entry
L	H	$Q1_n$	$Q2_n$	$Q3_n$	DR	Shift right*
H	L	DL	$Q0_n$	$Q1_n$	$Q2_n$	Shift left*
H	L	$Q0_n$	$Q1_n$	$Q2_n$	$Q3_n$	Stop shift

* Outputs as exist after pulse appears at "C" input with input conditions as shown (Pulse Positive transition of clock input).

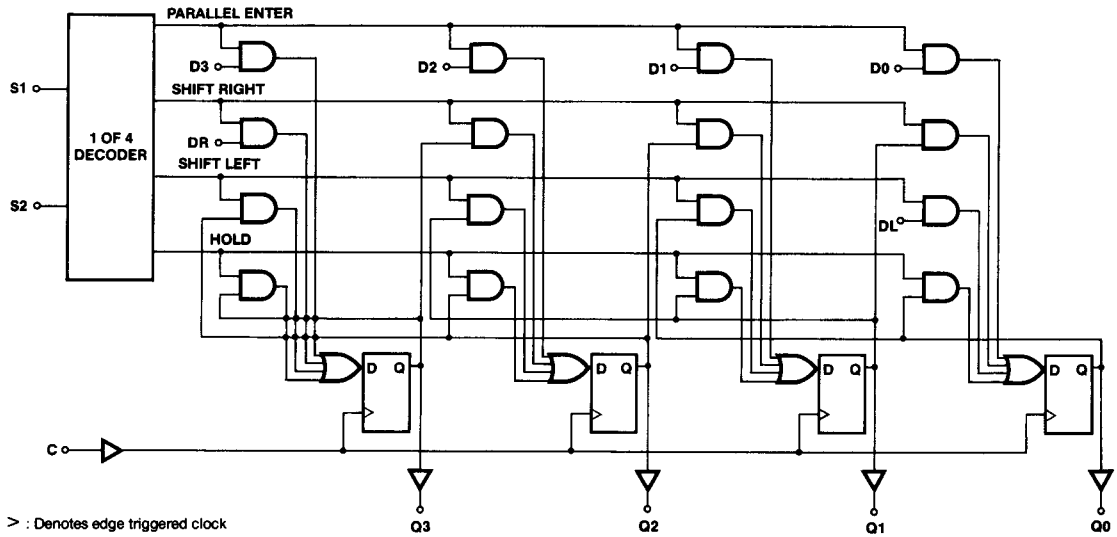
MC10H141
Four-Bit Universal Shift Register



MC10H141



Logic Diagram



> : Denotes edge triggered clock

Portions of this Data Sheet reproduced with the courtesy of Motorola Inc.

TWX: 910-338-2376
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
Monolithic Memories

Absolute Maximum Ratings

Supply voltage, V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 V_{dc}
Input voltage, V_I (V_{CC} = 0) ..... 0 V_{dc} to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating free-air temperature		0		75	°C
T_{STG}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	112	—	102	—	112	mA
I_{inH}	Input current HIGH	Pins 5, 6, 9, 11, 12, 13	—	405	—	255	—	255	µA
		Pins 7, 10	—	416	—	260	—	260	
		Pins 4,	—	510	—	320	—	320	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	µA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-0.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay		1.1	2.0	1.0	2.0	1.1	2.1	ns
t_{hold}	Hold time		1.0	—	1.0	—	1.0	—	ns
t_{set}	Setup time	Data	1.5	—	1.5	—	1.5	—	ns
		Select	3.0	—	3.0	—	3.0	—	
t_r, $t+$	Rise time		0.5	2.4	0.5	2.4	0.5	2.4	ns
t_f, $t-$	Fall time		0.5	2.4	0.5	2.4	0.5	2.4	ns
f_{shift}	Shift frequency		250	—	250	—	250	—	MHz

NOTE: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 V.

Description (Continued)

the four possible operations of the register without external gating of the clock. The flip-flops shift information on the positive edge of the clock. The four operations are stop shift, shift-left, shift-right, and parallel entry of data. The other six inputs are all data type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR). This device is a functional/pinout duplication of the standard ECL 10K part, with 100% improvement in propagation delay and operation frequency and no increase in power supply current.