

CLC520 Amplifier with Voltage Controlled Gain, AGC+Amp

General Description

The CLC520 is a wideband DC-coupled amplifier with voltage-controlled gain (AGC). The amplifier has a high-impedance, differential signal input, a high-bandwidth gain control input and a single-ended voltage output. Signal channel performance is outstanding with 160MHz small signal bandwidth, 0.5 degree linear phase deviation (to 60MHz) and 0.04% signal nonlinearity at 4V_{pp} output.

Gain-control is very flexible. Maximum gain may be set over a nominal range of 2 to 100 with one external resistor. In addition, the gain-control input provides more than 40dB of voltage-controlled gain adjustment from the maximum gain setting. For example, a CLC520 may be set for a maximum gain of 2 (or 6dB) for a voltage-controlled gain range from 6dB to less than -34dB. Alternatively, the CLC520 could be set for a maximum gain of 100 (40dB) for a voltage-controlled gain range from 40dB to less than 0dB.

Besides being flexible, the gain-control is easy to use. Gain-control bandwidth is superb, 100MHz, simplifying AGC/ALC loop stabilization. And since the gain is minimum with a zero volt input and maximum with a +2 volt input, driving the control input is simple.

Finally, differential inputs, and a ground-referenced voltage output take the trouble out of designing DC-coupled AGC circuits for display normalizers, etc. The CLC520 is available in several versions:

CLC520AJP	-40°C to +85°C	14-pin plastic DIP
CLC520AJE	-40°C to +85°C	14-pin plastic SOIC
CLC520ALC	-40°C to +85°C	dice
CLC520AMC	-55°C to +125°C	dice qualified to Method 5008, MIL-STD-883, Level B

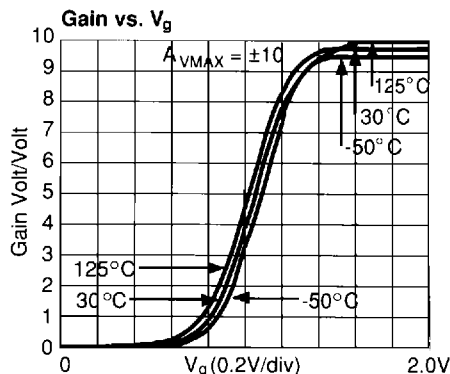
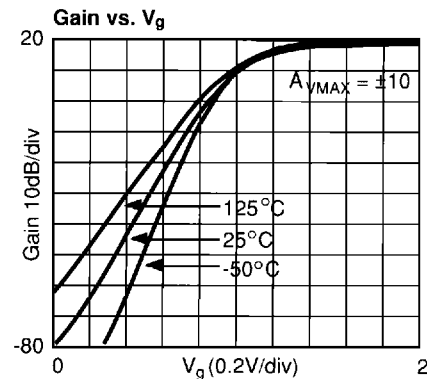
DESC SMD number: 5962-91694

Features

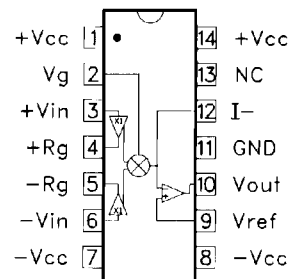
- 160MHz, -3dB bandwidth
- 2000V/μsec slew rate
- 0.04% signal nonlinearity at 4V_{pp} output
- -43dB feedthrough at 30MHz
- User adjustable gain range
- Differential voltage input and single-ended voltage output

Applications

- Wide-bandwidth AGC systems
- Automatic signal-leveling
- Video signal processing
- Voltage controlled filters
- Differential amplifier
- Amplitude modulation



Pinout DIP & SOIC



CLC520 Electrical Characteristics ($A_v = +10, V_{cc} = \pm 5V, R_L = 100\Omega, R_f = 1k\Omega, R_g = 182\Omega, V_g = +2V$)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS				UNITS	SYMBOL
			+25°C	-40°C	+25°C	+85°C		
Ambient Temperature	CLC520AJ	+25°C	-40°C	+25°C	+85°C			
FREQUENCY DOMAIN RESPONSE								
-3dB bandwidth	$V_{out} < 0.5V_{pp}$	160	>110	>120	>120	MHz	SSBW	
	$V_{out} < 0.5V_{pp}$ (AJE only)	140	>90	>100	>100	MHz	SSBW	
	$V_{out} < 4.0V_{pp}$	140	>85	>100	>100	MHz	LSBW	
-3dB bandwidth	$V_{out} < 0.5V_{pp}$							
gain control channel	$V_{in} = +0.2V, V_g = +1VDC$	100	>80	>80	>80	MHz	SBWC	
gain flatness	$V_{out} < 0.5V_{pp}$							
peaking	0.1MHz to 30MHz	0	<0.4	<0.3	<0.4	dB	GFPL	
peaking	0.1MHz to 20MHz	0	<0.7	<0.5	<0.7	dB	GFPH	
rolloff	0.1MHz to 30MHz	0.1	<0.4	<0.3	<0.4	dB	GFRL	
rolloff	0.1MHz to 60MHz	0.5	<1.3	<1	<1.3	dB	GFRH	
linear phase deviation	0.1MHz to 60MHz	0.5	<1.2	<1	<1.2	°	LPD	
feedthrough	$V_g = 0V, V_{in} = -22dBm$	-38	<-31	<-31	<-31	dB	FDTH	
rise and fall time	0.5V step	2.5	<3.7	<3	<3	ns	TRS	
	4.0V step	3.7	<5	<5	<5	ns	TRL	
settling time to $\pm 0.1\%$	2.0V step	12	<18	<18	<18	ns	TS	
overshoot	0.5V step	0	<15	<15	<15	%	OS	
slew rate	4V step	2000	>1450	>1450	>1450	V/ μ sec	SR	
2nd harmonic distortion	$2V_{pp}, 20MHz$	-47	<-40	<-40	<-35	dBc	HD2	
3rd harmonic distortion	$2V_{pp}, 20MHz$	-60	<-50	<-50	<-45	dBc	HD3	
equivalent output noise	(+10 for input noise) ¹							
noise floor	1MHz to 200MHz	-132	<-130	<-130	<-129	dBm/Hz	SNF	
integrated noise	1MHz to 200MHz	800	<1000	<1000	<1100	μ V	INV	
differential gain ²	at 3.58MHz	0.15				%	DG	
differential phase ²	at 3.58MHz	0.15				°	DP	
STATIC, DC PERFORMANCE								
integral signal nonlinearity	$V_{out} = 4V_{pp}$	0.04	<0.1	<0.1	<0.2	%	SGNL	
gain accuracy	$R_f = 1k\Omega, R_g = 182\Omega$							
for nominal max gain = 20dB		± 0	± 1.0	± 0.5	± 0.5	dB	GACCU	
*output offset voltage		40	<150	<120	<150	mV	VOS	
average temperature coefficient		100	<400	—	<300	μ V/°C	DVOS	
*input bias current		12	<61	<28	<28	μ A	IB	
average temperature coefficient		100	<415	—	<165	nA/°C	DIB	
input offset current		0.5	<4	<2	<2	μ A	IOS	
average temperature coefficient		5	<40	—	<20	nA/°C	DIOS	
power supply sensitivity	output referred DC	10	<28	<28	<28	MV/V	PSS	
common mode rejection ratio	input referred	70	>59	>59	>59	dB	CMRR	
*supply current	no load	28	<38	<38	<38	mA	ICC	
V_{in} signal input	resistance	200	>50	>100	>100	k Ω	RIN	
	capacitance	1	<2	<2	<2	pF	CIN	
V_{in} differential voltage range	for $R_g = 182\Omega$ only	± 280	$> \pm 250$	$> \pm 250$	$> \pm 210$	mV	DMIR	
V_{in} common mode voltage range		± 2.2	> 1.4	> 1.2	> 1.2	V	CMIR	
V_g control input	resistance	750	>535	>600	>600	Ω	RINC	
	capacitance	1	<2	<2	<2	pF	CINC	
V_g input voltage	for maximum gain	1.6	<2	<2	<2	k Ω	VGHI	
	for minimum gain	0.4	>0	>0	>0	V	VGLO	
output impedance	at DC	0.1	<0.3	<0.2	<0.2	Ω	RO	
output voltage range	no load	± 3.5	$> \pm 3$	$> \pm 3.2$	$> \pm 3.2$	V	VO	
output current		± 70	$> \pm 35$	$> \pm 50$	$> \pm 50$	mA	IO	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

V_{cc}	$\pm 7V$
I_{out}	output is short circuit protected to ground, however, maximum reliability is obtained if I_{out} does not exceed... 70mA
common mode input voltage	$\pm V_{cc}$
V_{in} differential input voltage	10V
V_g input voltage	$\pm V_{cc}$
V_{ref} input voltage	$\pm V_{cc}$
junction temperature	+175°C
operating temperature range	-40°C to +85°C
AJ/AI	-65°C to +150°C
storage temperature range	10 sec
lead solder duration (+300°C)	500V
ESD rating (human body model)	

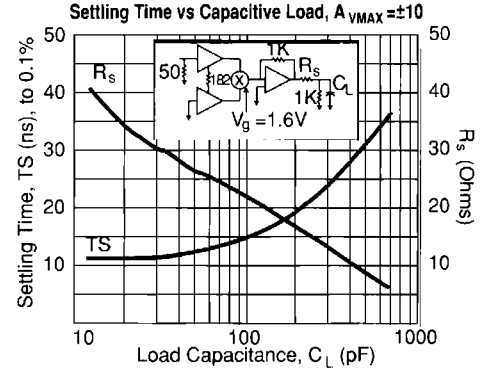
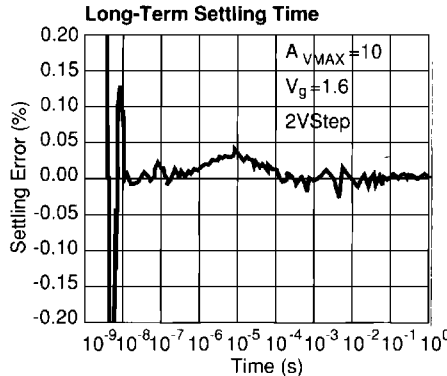
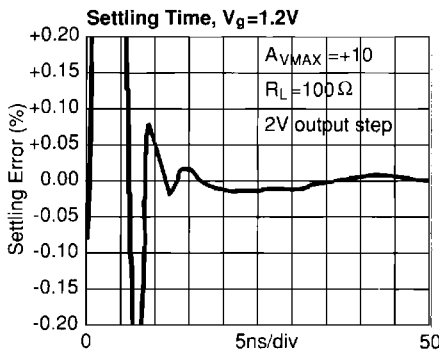
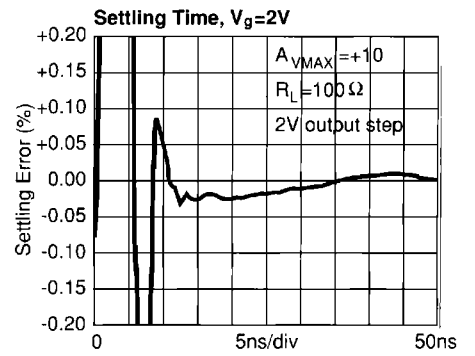
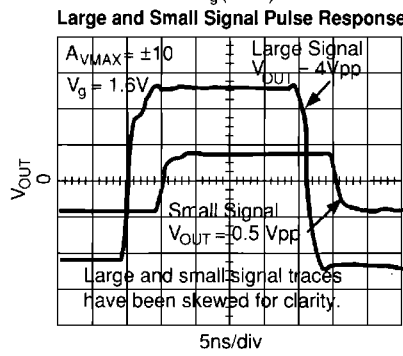
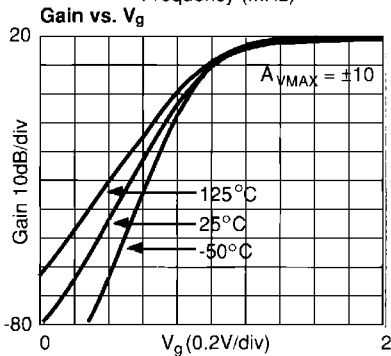
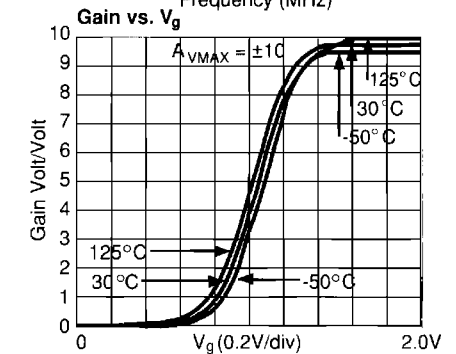
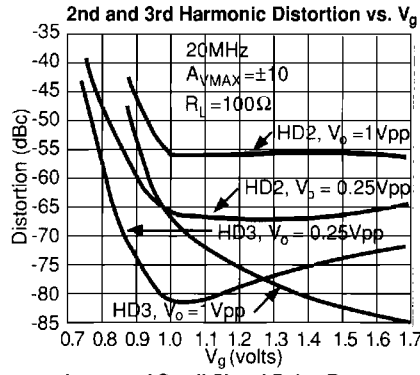
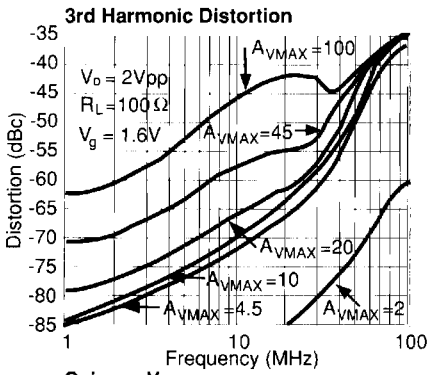
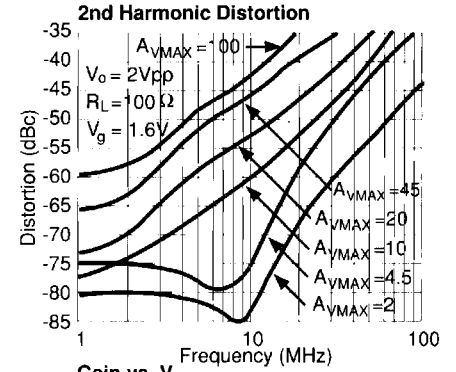
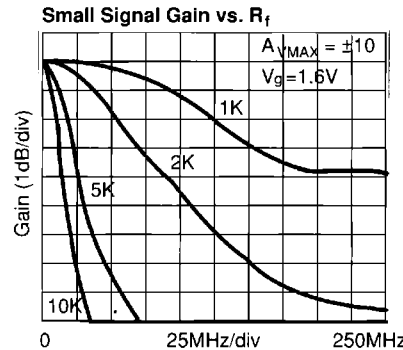
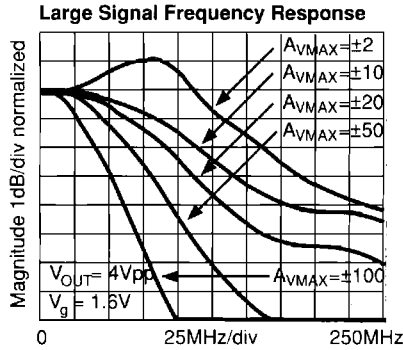
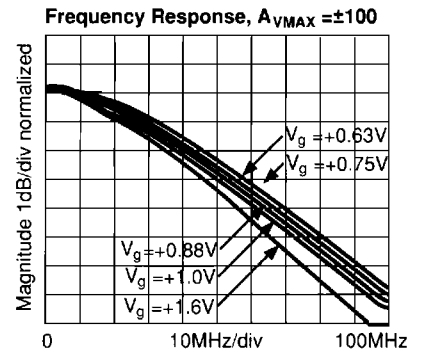
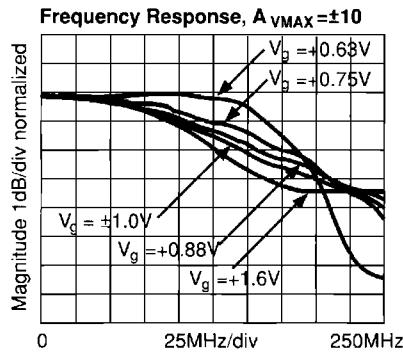
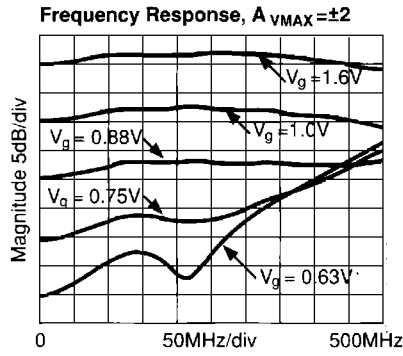
Miscellaneous Ratings

recommended gain range:	± 2 to ± 100
recommended V_{REF}	$\pm 150mV$
Notes:	AJ 100% tested at +25°C.
note 1:	Measured at $A_{vmax} = 10, V_g = +2V$
note 2:	Differential gain and phase are measured at: $A_v = +20, V_g = +2V, R_L = 150\Omega, R_f = 2k\Omega, R_g = 182\Omega,$ equivalent video signal of 0-100 IRE with 40 IRE _{pp} at 3.58 MHz.
Transistor Count	42

Package Thermal Resistance

Package	θ_{JC}	θ_{JA}
AJP	55°C/W	105°C/W
AJE	45°C/W	120°C/W

Typical Performance Characteristics ($T_A = 25^\circ$, $A_{VMAX} = \pm 10$, $V_{CC} = \pm 5V$, $R_L = 100\Omega$, $R_f = 1k\Omega$, $R_g = 182\Omega$, $V_g = +2V$)



Typical Performance Characteristics ($T_A = 25^\circ$, $A_V = +10$, $V_{CC} = \pm 5V$, $R_L = 100\Omega$, $R_f = 1k\Omega$, $R_g = 182\Omega$, $V_g = +2V$)

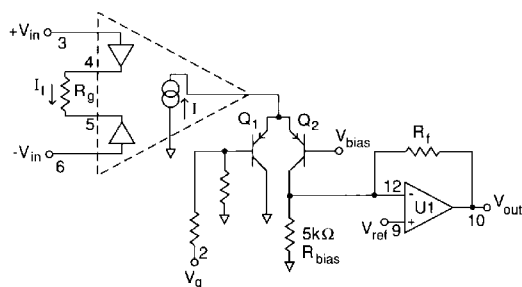
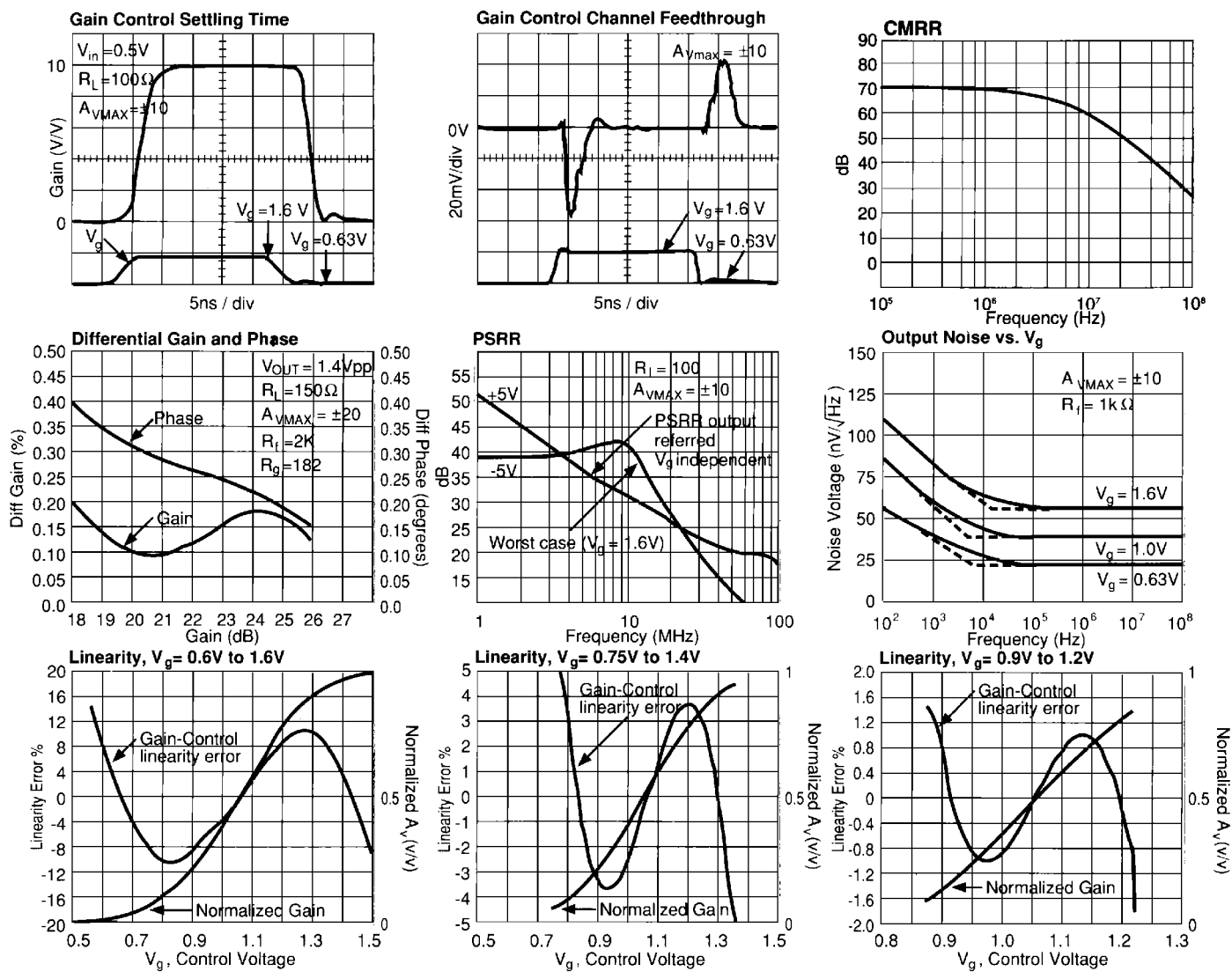


Figure 1: CLC520 Simplified Schematic

Simplified Circuit Description

A simplified schematic for the CLC520 is given in Figure 1. $+V_{in}$ and $-V_{in}$ are buffered with closed-loop voltage followers inducing a signal current in R_g proportional to $(+V_{in}) - (-V_{in})$, the differential input voltage. This current controls a current source which supplies two well-matched transistors, Q1 and Q2.

The current flowing through Q2 is converted to the final output voltage using R_f and output amplifier, U1. By changing the fraction of the signal current I which flows through Q2 the

gain is changed. This is done by changing the voltage applied differentially to the bases of Q1 and Q2. For example, with $V_g = 0$, Q1 conducts heavily and Q2 is off. With none of I flowing through R_f , the CLC520's input to output gain is strongly attenuated. With $V_g = 2V$, Q1 is off and all of the signal current flows through Q2 to R_f producing maximum gain. With V_g set to 1.1V, the bases of Q1 and Q2 are set to approximately the same voltage, Q1 and Q2 have the same collector currents – equal to one half of signal current I, thus the gain is approximately one half the maximum gain at $V_g = 1.1V$.

Typical application circuit

Figure 2 illustrates a voltage-controlled gain block offering broadband performance in a 50Ω system environment. The input signal is applied to pin 3 of the CLC520 and terminating resistor R2. Gain-control signals are applied to pin 2. The net gain-control port input impedance is 50Ω , set by the parallel combination of R_1 and the 750Ω input impedance of pin 2 of the CLC520.

R_f is set to the standard value, $1k\Omega$, and R_g sets the maximum voltage gain (with a high Z load connected to the output) to $10V/V$. Output impedance is set by R_o to 50Ω so with 50Ω source and load terminations, the gain is approximately 14dB.

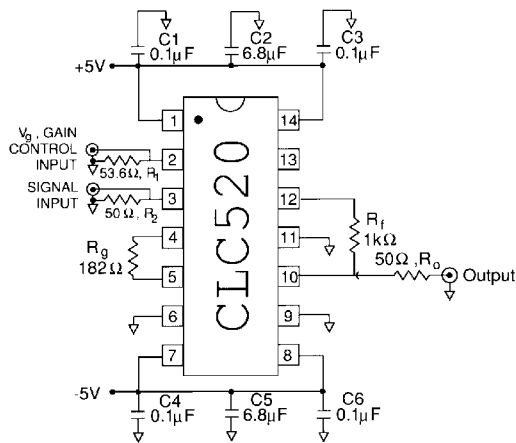


Figure 2: CLC520 Typical Application Circuit

Capacitors C1-C6 provide broadband power-supply bypassing. C2 and C5 should be tantalum capacitors. All other capacitors should be high-quality ceramic capacitors (CK-05 or equivalent).

Adjusting offset

Offset can be broken into two parts: an input-referred and an output-referred term. The input-referred offset shows up as a variation in output voltage as V_g is changed. This can be trimmed using the circuit in Figure 3 by placing a low frequency square wave ($V_l=0V$, $V_h=2V$) into V_g (with V_{in} set to zero volts) and adjusting R1 until the CLC520 output produces a steady DC value. After adjusting the input-referred offset, adjust R2 (with $V_{in}=0$, $V_g=0$) until V_{out} is zero. Finally, in inverting applications V_{in} may be applied to pin 6 and the offset adjustment to pin 3. This offset trim does not improve output offset temperature coefficient.

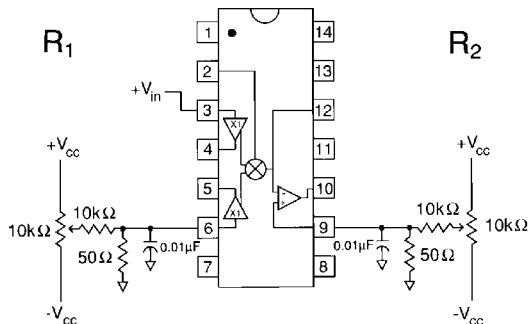


Figure 3: CLC520 Offset Adjustment Circuitry (other external elements not shown)

Selecting component values

Maximum input amplitude and maximum gain are the two key specifications that determine component values in a CLC520 application.

The output stage op amp is a current-feedback type amplifier optimized for $R_f=1k\Omega$. R_g can then be computed as:

$$R_g = \frac{R_f \cdot 1.85}{A_{vmax}} - 3.0\Omega \text{ with } R_f = 1k\Omega \quad (1)$$

To determine whether the maximum input amplitude will overdrive the CLC520, compute:

$$V_{dmax} = (R_g + 3.0\Omega) \cdot 0.00135 \quad (2)$$

the maximum differential input voltage for linear operation.

If the maximum input amplitude exceeds this limit, the CLC520 should either be moved to a location in the signal chain where amplitudes are reduced, A_{vmax} should be reduced or the values for R_g and R_f should be increased.

If the input amplitude is reduced, recompute the impact of the CLC520 on signal-to-noise ratio. If A_{vmax} is reduced,

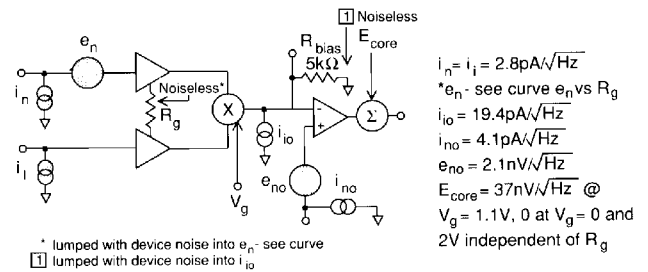


Figure 4: CLC520 Noise Model

“downstream” amplifier gain should be increased, or another gain stage added to make up for reduced A_{vmax} .

To increase R_g and R_f , compute the lowest acceptable value for R_g :

$$R_g > 740 \cdot V_{dmax} - 3\Omega \quad (3)$$

where $V_{dmax} = (+V_{in}) - (-V_{in})$, the largest expected peak differential input voltage. Operating with R_g larger than this value insures linear operation of the input buffers.

R_f may be computed from the selected R_g and A_{vmax} :

$$R_f = \frac{A_{vmax} \cdot (R_g + 3.0\Omega)}{1.85} \quad (4)$$

R_f should be $\geq 1k\Omega$. $R_f < 1k\Omega$ can be implemented using a loop gain reducing resistor to ground on the inverting summing node of the output amplifier (see application note OA-13).

Printed Circuit Layout

A good high-frequency PCB layout including ground plane construction and power supply bypassing close to the package are critical to achieving full performance. The amplifier is sensitive to stray capacitance to ground at the I- input (pin 12); keep trace area small. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

For best performance at low maximum gains ($A_{vmax} < 10$) R_{g+} and R_{g-} connections should be treated in a similar fashion. Capacitance to ground should be minimized by removing the ground plane from under the body of R_g .

Parasitic or load capacitance directly on the output (pin 10) degrades phase margin leading to frequency response peaking. A small series resistor before this capacitance, if present, effectively decouples this effect (see Settling Time vs. Capacitive Load).

Precision buffed resistors (PRP8351 series from Precision Resistive Products) must be used for R_f for rated performance. Precision buffed resistors are suggested for R_g for low gain settings ($A_{vmax} < 10$). Carbon composition resistors and RN55D metal-film resistors may be used with reduced performance.

Evaluation PC boards (part no. 730021) for the CLC520 are available from Comlinear at minimal cost.

Predicting the output noise

Seven noise sources (e_n , i_n , i_i , i_o , i_{no} , e_{no} , E_{core}) are used to model the CLC520 noise performance (Figure 4). e_n , i_n , and i_i model the equivalent input noise terms for the input buffer while i_o , i_{no} , and e_{no} model the noise terms for the output buffer. To simplify the model e_n includes the effect of resistor R_g (see Figure 5 for e_n vs R_g). To simplify the model further, R_{bias} is assumed noiseless and its noise contribution is included in i_{io} .

An additional term E_{core} mimics the active device noise contribution from the Gilbert multiplier core. Core noise is theoretically zero when the multiplier is set to maximum gain or zero gain ($V_g > 1.6V$ or $V_g < 0.63V$ respectively at room temperature) and reaches a maximum of $37nV/\sqrt{Hz}$ at $A_{vmax}/2$.

This page intentionally left blank.

Customer Design Applications Support

National Semiconductor is committed to design excellence. For sales, literature and technical support, call the National Semiconductor Customer Response Group at **1-800-272-9959** or fax **1-800-737-7018**.

Life Support Policy

National's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of National Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, a) are intended for surgical implant into the body, or b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation

1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe

Fax: (+49) 0-180-530 85 86
E-mail: europe.support.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Francais Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.

13th Floor, Straight Block
Ocean Centre, 5 Canton Road
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.

Tel: 81-043-299-2309
Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.