

# **NATEL**

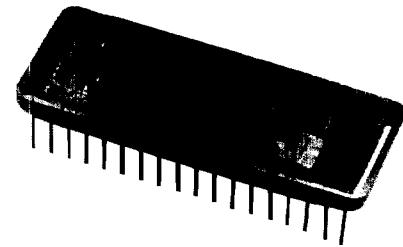
## **HSD/HRD1014**

# **Synchro (Resolver)-to-Digital Converter**

## **Microprocessor Compatible 14-bit Hybrid**

### **Features**

- **3-state latched output**  
(inhibit does not interrupt tracking)
- **8- and 16-bit microprocessor compatible**
- **2.6 arc-minute accuracy**
- **Very high tracking rate**  
(3600 degrees per second)
- **High common-mode rejection**  
(true differential inputs)
- **High input impedance**
- **Programmable Gain Control**
- **TTL and CMOS compatible**
- **Analog velocity and error voltages outputs**
- **Single 36-pin hybrid DDIP package**
- **MIL-STD-883 Processing is Available**



**ACTUAL SIZE**

**HSD/HRD1014**

### **Applications**

Avionics systems  
Antenna monitoring  
Servo systems  
Coordinate conversion  
Fire control systems  
Axis rotation  
Engine controllers  
Industrial control systems  
Simulation  
Robotics  
Machine tool control systems  
Solar panel control systems

### **Description**

The HSD1014 (HRD1014), a 14-bit Synchro (Resolver)-to-Digital Converter, packaged in a 36-pin DDIP hybrid, offers high accuracy, microprocessor compatibility and excellent dynamic performance. Requiring only a single +15 V-dc main power supply for its operation, the converter maintains both static and dynamic accuracy over a wide range of power supply variations. The digital output voltage levels can be controlled independently by a logic voltage input  $V_L$ . The logic supply voltage  $V_L$  can range from 4.5 V-dc to the main power supply voltage. At 5 V-dc logic supply the output is CMOS/TTL compatible and can drive one 54/74 gate load or four 54LS/74LS gate loads.

Using a high-accuracy differential signal conditioner for the resolver input and a resistive scott-tee for the synchro-input, the converter provides common mode rejection in excess of 70 dB. The input impedance remains constant and balanced independent of dc power to the converter. This feature prevents loading of the synchro and reference input lines when the converter is not powered. This technique also permits resistor programming for non-standard input voltages.

Transferring data from the 1014 is facilitated by the use of a transparent latch with 3-state outputs, configured as two independently enabled bytes. Not only does this allow data to be read without interrupting converter tracking, it also permits memory-mapped data interface and control with the most popular 8- and 16-bit microprocessors and single-board computers.

Three analog outputs: velocity, unfiltered dc error and filtered dc error near null are made available from the 1014. A gain-control pin (Ge) is provided to allow user to program the converter for non-standard input voltages without degrading the accuracy of the converter.

*Although pin-compatible Synchro (Resolver)-to-Digital converters are available, Natel's Model 1014 offers superior dynamic performance while maintaining its high accuracy. In addition, the Model 1014 uses established reliability (ER) components and is built in accordance with the requirements of MIL-STD-883B including 168 hours of active burn-in.*

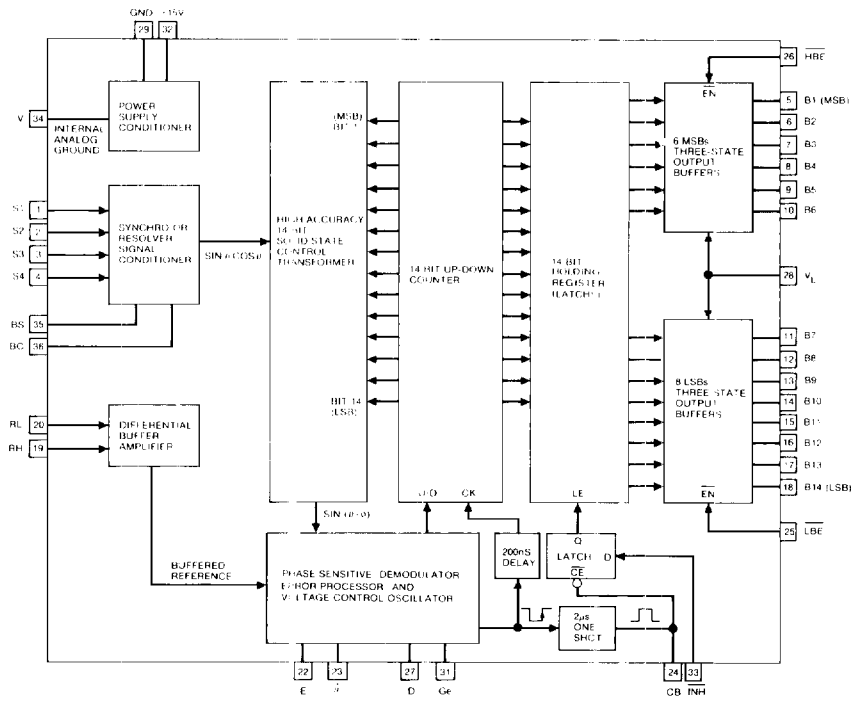


FIGURE 1 1014 Block Diagram

## Theory of Operation

The operation of the Model HSD1014 is illustrated in the functional block diagram of figure 1. The HSD1014 is a high gain Type II tracking converter exhibiting zero error for a constant velocity input. The basic conversion process consists of continuously comparing the digital output angle ( $\phi$ ) and the Synchro (or Resolver) input angle ( $\theta$ ). An up-down counter, containing the feed-back angle, is changed (increased or decreased) until the feed-back angle equals the input angle. Once synchronized, the output angle tracks the input angle continuously and the data is always fresh and always available (except during transitions). The input signal conditioner accepts either a Synchro or Resolver input and converts it into low level signals  $\sin \theta$  and  $\cos \theta$ . The feed-back loop consisting of an error processor, voltage-controlled oscillator and a 14-bit up-down counter produces a 14-bit digital angle ( $\phi$ ). The input and feed-back signals are combined in a solid state control transformer to obtain an error voltage, ( $e$ ) according to the following trigonometric identity:

$$"e" = \sin (\theta - \phi) = \sin \theta \cos \phi - \cos \theta \sin \phi$$

When the error voltage goes to null,  $\sin (\theta - \phi)$  is zero, which makes the angle  $\theta$  equal to the angle  $\phi$ . Thus, the digital output represents the input shaft angle. The error voltage ( $e$ ) is an ac signal proportional to the instantaneous error between the input angle and the feed-back angle. This error voltage is synchronously demodulated with the buffered reference signal. The demodulated output is a dc signal proportional to the tracking error ( $\theta - \phi$ ). The dc error is integrated to produce a voltage proportional to the converter's tracking velocity. The velocity signal (available at pin 23) is the control input to a voltage-controlled oscillator. The VCO output changes the up-down counter, which contains the feed back angle,  $\phi$ . The up-down counter functions as the second integrator in the tracking loop. The output of the counter is then supplied to a holding register and dual 3-state buffers for output interface.

## Output Interface

The output interface circuit consists of a 14-bit holding register (latches) and dual three-state buffers. This not only imparts a versatile interface capability (data multiplexing on 8- or 16-bit data bus) to the HSD1014, but also enables the  $\overline{INH}$  (inhibit) control to be used without opening the converter loop. This feature is important since synchro/resolver-to-digital converters typically disable the up-down counter during data transfer causing severe transients in the output data when the converter is re-enabled (inhibit removed) and the tracking loop is forced to re-synchronize.

When  $\overline{INH}$  is at logic "high" or open, each clock pulse from the VCO changes the up-down counter and output by 1 LSB. When  $\overline{INH}$  is at a logic low, the holding register is latched (within 3  $\mu$ sec maximum) and although the up-down counter is updated continuously, the output data is stable. A 2  $\mu$ sec pulse is generated at CB (pin 24) every time up-down counter changes by 1 LSB.

The outputs of the holding register are buffered with two three-state buffers with separate enable controls. When  $\overline{HBE}$  is at logic "low," the 6MSBs (B1 through B6) are enabled. When  $\overline{LBE}$  is at logic "low," the 8 LSBs (B7 through B14) are enabled. When  $\overline{HBE}$  and/or  $\overline{LBE}$  are at logic "high" the corresponding bits are in the high impedance state (disabled) and the data-bus sees an essentially open line.

Note that applying inhibit to the converter will latch the data in the 14-bit holding register (and will prevent it from being updated) . . . but will not interfere with the continuous operation of the conversion process.

Enable controls  $\overline{HBE}$  and  $\overline{LBE}$  operate only on three-state buffers and do not affect the converter loop.

## Synchro/Resolver Connections and Phasing

The connections for synchro and resolver inputs are shown in figure 2. The input signal conditioner of the Model 1014 converter is designed to accept either synchro or resolver inputs. In addition it uses differential amplifiers and matched precision resistors to provide a high common-mode rejection ratio. This eliminates the need for external transformers for most applications. The input signal conditioner performs two functions. For both synchro and resolver format inputs it serves as a precision attenuator reducing the amplitude of high level ac input signals to levels which can be processed by the converter. For a synchro input, this network transforms three wire synchro information into resolver format ( $\sin \theta$  and  $\cos \theta$ ).

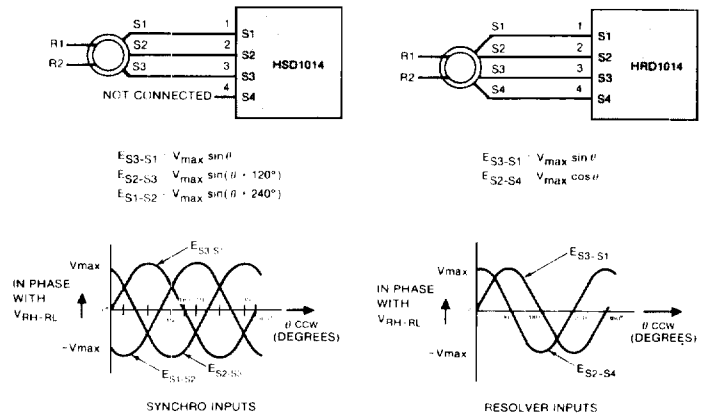


FIGURE 2 Synchro/Resolver Inputs

## Input Protection

Both signal and reference inputs are true differential inputs and use precision thin-film resistors for signal attenuation. If input voltages exceed the absolute maximum ratings, the thin-film resistors may be destroyed. To prevent this from happening, it is recommended that transient voltage suppressors be installed on both signal and reference lines. Synchros and resolvers are highly inductive and can generate or couple transients many times greater than their normal

signal voltages and can easily exceed the absolute maximum ratings. This situation is particularly likely to occur in cases where the excitation or source voltage for the synchro (resolver) is switched on or off. Transients can also occur by other equipment being turned on or off. Figures 3 and 4 show recommended methods of connecting synchro and resolver inputs. Transient voltage suppressor given in the tables (or equivalent) must be used to assure input protection.

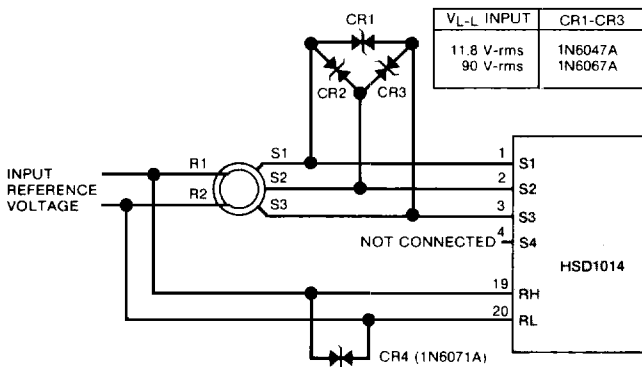


FIGURE 3 HSD1014 Input Protection

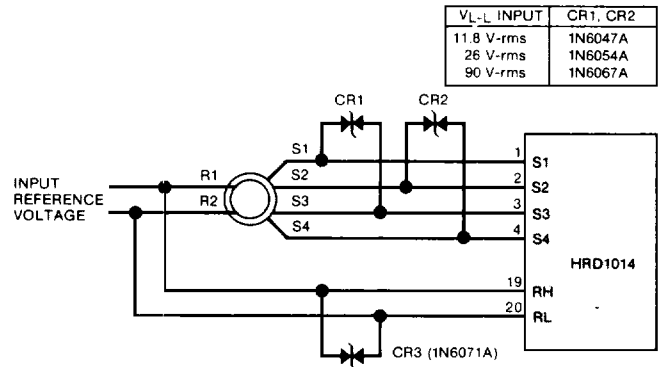


FIGURE 4 HRD 1014 Input Protection

## Resistor Programming for Non-standard Input Voltages

Non-standard input signal voltages are accommodated with the addition of an external resistor connected between Gain control,  $G_e$  (pin 31), and Bias Voltage,  $V$  (pin 34). The circuit configuration for resistor programming is shown in figure 5. The formula for determining the value of external resistor  $R_1$  and the converter model to be used are shown in the table. The resistor  $R_1$  increases the gain of Voltage Control Oscillator (VCO), thereby compensating for lower input voltages. For input voltages greater than 90 V-rms line-to-line, the method described in Natel HSRD1006 data sheet can be used. Contact factory if you require assistance.

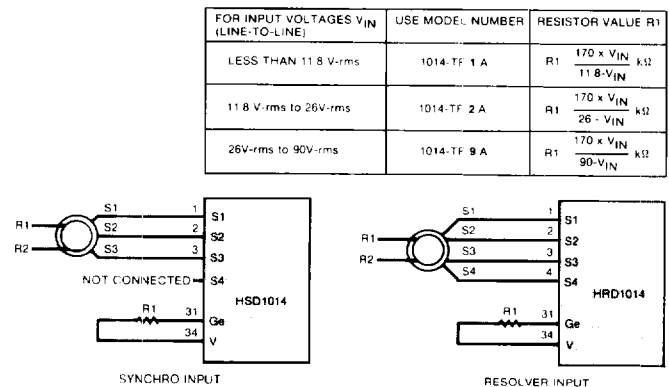


FIGURE 5 Resistor Programming for Non-standard Inputs

## Asynchronous Data Transfer

Asynchronous data transfer from the Model 1014 Converter is shown in figure 6. Control functions  $\overline{\text{HBE}}$  and  $\overline{\text{LBE}}$  have internal pull-down circuitry, permitting these pins to be left open. The data is continuously available at the output pins, but it may be changing at any specific time. In order not to transfer data during transition times, the inhibit function should be used. There are two methods available for transferring data. One method is to monitor the CB output and transfer data at the trailing edge of the CB pulse. The preferred method is on command signal. Set the  $\overline{\text{INH}}$  input to logic "low" for not less than  $3\ \mu\text{sec}$ . The 14-bits of output data may then be transferred.

Note that within  $4\ \mu\text{sec}$  after the inhibit is removed, updated accurate data is available for the next cycle of data transfer. This is made possible as the  $\overline{\text{INH}}$  does not interrupt the conversion process.

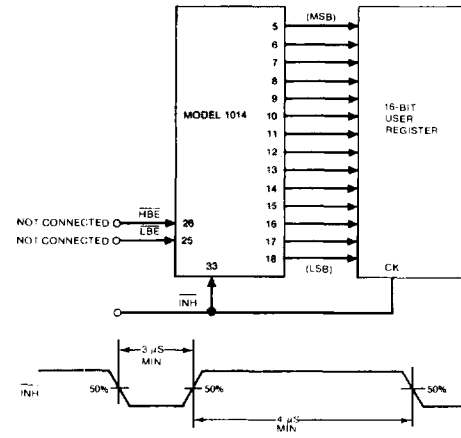


FIGURE 6 Circuit Configuration for Asynchronous Data Transfer

## Two-Byte Data Transfer On 8-Bit Data-Bus

The circuit configuration for transferring the 14-bit output of the Model 1014 to an 8-bit data-bus is shown in figure 7. Note that  $\overline{\text{INH}}$  signal, a logic "low," is applied for the entire data transfer cycle to prevent updating of internal holding register (latches). After  $\overline{\text{INH}}$  is applied, wait for  $3\ \mu\text{sec}$  before transferring any data. When  $\overline{\text{HBE}}$  is at logic "0," the 6 MSBs are transferred to the data-bus. When  $\overline{\text{LBE}}$  is at logic "0" the 8 LSBs are transferred to data-bus. Note that for the data transfer,  $\overline{\text{HBE}}$  and  $\overline{\text{LBE}}$  can be applied in any order.

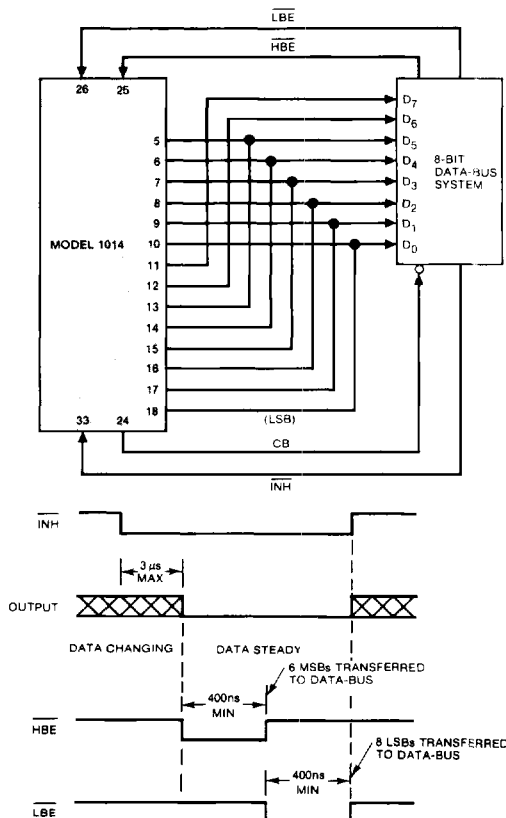


FIGURE 7 Digital Connections and Timing for Two-Byte Data Transfer

## Single-Byte Data Transfer

The circuit configuration for transferring the output of the Model 1014 to a 16-bit data-bus is shown in figure 8. Apply logic "low" to  $\overline{\text{INH}}$  input. Wait for  $3\ \mu\text{sec}$  and then apply a logic low to enable inputs ( $\overline{\text{HBE}}$  and  $\overline{\text{LBE}}$ ).

Note that within  $4\ \mu\text{sec}$  after the inhibit is removed, updated accurate data is available for the next cycle of data transfer. This is made possible as the  $\overline{\text{INH}}$  does not interrupt the conversion process. Only the holding register (latches) are prevented from updating during the time  $\overline{\text{INH}}$  is at logic "low."

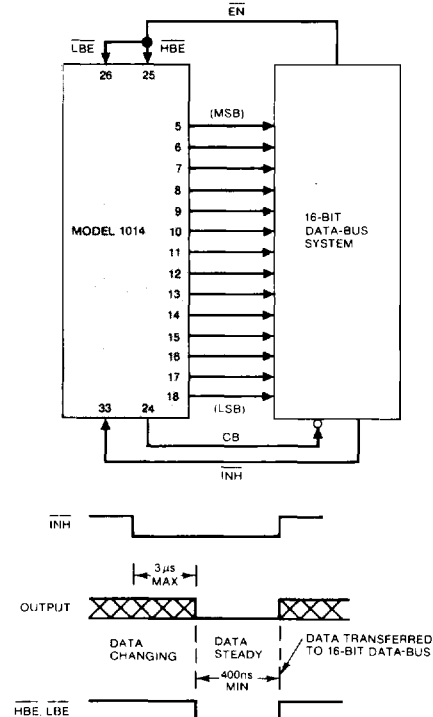


FIGURE 8 Digital Connections and Timing for Single-Byte Data Transfer

## Dynamic Performance

The 1014 design incorporates the proven Type II tracking design ( $KV = \infty$ ) and has been configured to provide superior dynamic performance independent of power supply voltage over the range of 11 V-dc to 17 V-dc.

The converter will track the input angles up to specified tracking rates (see specifications, pages 6 and 7) with no lag error. The acceleration constant ( $K_A$ ) for the converter is  $48,000^\circ/\text{sec}^2$ . Both small and large signal response for the Model 1014 are shown in figure 11.

The **Large Signal** transient response is dependent solely on the maximum velocity ( $\omega_{\text{max}}$ ) and the maximum acceleration ( $\alpha_{\text{max}}$ ) of which the converter is capable. The large signal parameters are defined in figure 9. The synchronizing time ( $t_{\text{SYNC}}$ ) for large signals can be partitioned into three distinct intervals. Acceleration time ( $t_{\text{ACC}}$ ) Slew time ( $t_{\text{SLEW}}$ ) and Overshoot time ( $t_{\text{OS}}$ ).

Acceleration time is the time interval from application of the step-input to the point at which the converter reaches its maximum velocity.

Slew time is the time interval from the point at which maximum velocity is obtained to the point at which the output angle is first equal to the input angle.

Overshoot time is the time interval from the point at which the converter output angle first equals the input angle (and applies constant acceleration in the opposite direction) to the point at which the output angle again reaches the input angle.

At the end of overshoot time, the small signal response becomes dominant and the converter will settle to the final value according to its small signal transient response function.

The **Small Signal** settling time ( $t_s$ ) is specified for step inputs of less than 1.4 degrees. For small signal steps, the settling time is a function of the transient response of the converter. The transfer functions for both 60 Hz and 400 Hz models are shown in figure 10.

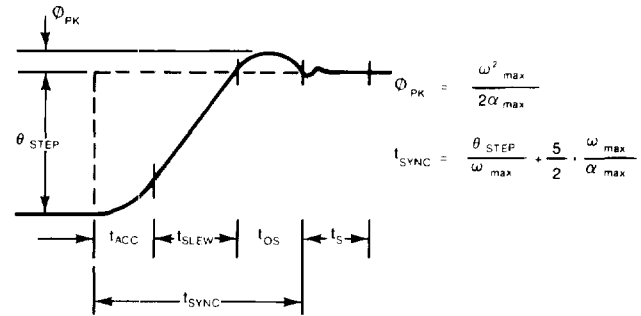
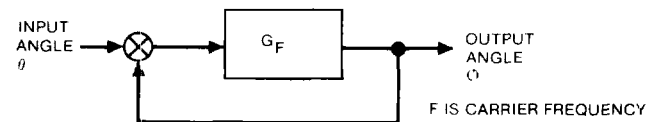


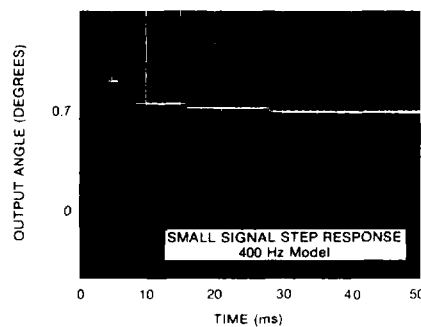
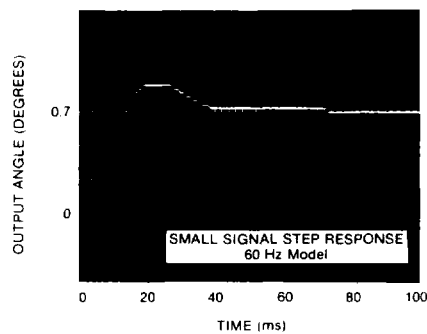
FIGURE 9 Large Signal ( $\geq 1.4^\circ$ ) Response Parameters



$$G_{60} = \frac{55^2 \left(1 + \frac{S}{25}\right)}{S^2 \left(1 + \frac{S}{250}\right)} \quad G_{400} = \frac{220^2 \left(1 + \frac{S}{100}\right)}{S^2 \left(1 + \frac{S}{1000}\right)}$$

FIGURE 10 Transfer Functions for 1014

### Small Signal Input Step = 0.7 Degrees



### Large Signal Input Step = 179 Degrees

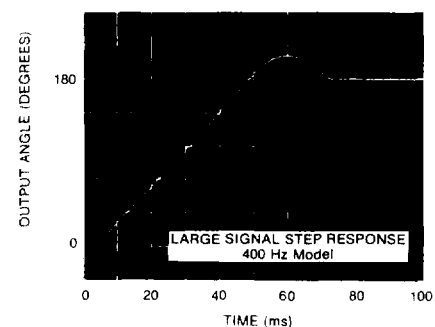
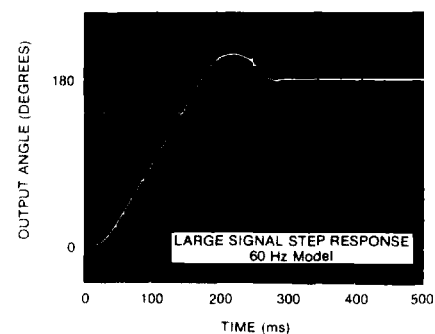


FIGURE 11 Dynamic Characteristics

## Specifications

PARAMETER	VALUE	REMARKS
<b>Digital Output Resolution</b>	14-bits (1.32 arc-minutes)	
Accuracy	$\pm 5.2$ arc-minutes (option S) $\pm 2.6$ arc-minutes (option H)	Accuracy applies over operating temperature range and includes hysteresis
<b>Reference Input</b>		
Voltage	4 to 130 V-rms	
Frequency	360 to 1000 Hz 47 to 1000 Hz	400 Hz Models 60 Hz Models
Input Impedance	200 k $\Omega$ Single Ended 400 k $\Omega$ Differential	
Common Mode Range	$\pm 250$ V peak maximum	dc plus recurrent ac peak
<b>Synchro/Resolver Inputs</b>		
Input Voltages (Line-to-Line)	11.8 V-rms 26 V-rms 90 V-rms	Accuracy of the converter is maintained with $\pm 10\%$ variation in signal voltages
Input Impedance	Differential	Line-to-GND
	60 k $\Omega$ 150 k $\Omega$ 500 k $\Omega$	30 k $\Omega$ 75 k $\Omega$ 250 k $\Omega$
Impedance Unbalance	0.1% maximum	For all models
Common Mode Range	$\pm 30$ V peak $\pm 60$ V peak $\pm 180$ V peak	11.8 V-rms models 26 V-rms models 90 V-rms models
Common Mode Rejection Ratio	70 dB minimum	dc to 1000 Hz
Harmonic Distortion	10% maximum	Without degradation in accuracy specification
<b>Digital Inputs</b>		CMOS transient protected
Voltage Levels Logic "0" Logic "1"	-0.3 V-dc to 0.8 V-dc 2.4 V-dc	For $V_L = 5$ V-dc
Logic "0" Logic "1"	-0.3 V-dc to 0.3 $V_L$ 0.7 $V_L$ to $V_L$	For $V_L = 15$ V-dc
Input Currents $\overline{INH}$	-15 $\mu$ A typical, "active" pull-up to power supply ( $V_L$ )	When not used, may be left unconnected
$\overline{HBE}$ , $\overline{LBE}$	15 $\mu$ A typical "active" pull-down to ground (GND)	When not used may be left unconnected
<b>Digital Input Controls</b>		
$\overline{INH}$	Logic "1" Logic "0"	Digital output follows analog input signals Output data latched in holding register. (Does not interrupt converter tracking-loop.)
$\overline{HBE}$	Logic "0" Logic "1"	6 MSBs are enabled 6 MSBs are in high impedance state of 3-state output
$\overline{LBE}$	Logic "0" Logic "1"	8 LSBs are enabled 8 LSBs are in high impedance state of 3-state output
<b>Digital Outputs</b>		
Logic Type	TTL/CMOS compatible	Depends on logic supply voltage ( $V_L$ )
<b>Drive Capability</b>		
Data Bits (B1-B14) CB	1 Standard TTL 1 Standard TTL	For 5 V-dc logic supply voltage ( $V_L$ )
Data Bits (B1-B14)	Natural Binary Angle	Positive Logic
CB	Logic "0" Logic "1" (2 $\mu$ sec pulse for every LSB change)	Output angle not changing Output angle changing (Leading edge initiates output change)

PARAMETER	VALUE	REMARKS
<b>Analog Outputs</b>		Typical Values unless otherwise specified
V (Bias Voltage)	$(+15 \text{ V}-0.7)/2$	+7.15 V-dc for +15 V-dc main power supply
-D (Unfiltered Error)	-16 mV-dc per +1 LSB	dc voltage referenced to V
-E (Filtered Error)	-1 V-dc per +1 LSB	dc voltage referenced to V
$\dot{\theta}$ (Velocity Output)	0.48 V-dc per rps 1.85 V-dc per rps	400 Hz models 60 Hz models
BS (Buffered Sin $\theta$ ) -BC (Buffered -Cos $\theta$ )	1 V-rms maximum Angular accuracy 1 arc minute	ac voltage referenced to V ( $\theta$ is input shaft angle)
Drive Capability	1 mA maximum	All analog outputs
<b>Analog Gain Control (Ge)</b>		Gain programming pin
Gain Control Range	4 to 1	Without degradation of accuracy specification
<b>Dynamic Characteristics</b>		Typical values unless otherwise specified
Maximum Tracking Rate	$\pm 10$ rps (3600° per sec) minimum $\pm 2$ rps (720° per sec) minimum	400 Hz models 60 Hz models
Maximum Acceleration	200,000°/sec <sup>2</sup> 15,000°/sec <sup>2</sup>	400 Hz models 60 Hz models
Acceleration for 1 LSB error	1,000°/sec <sup>2</sup> 65°/sec <sup>2</sup>	400 Hz models 60 Hz models
Settling Time to 1 LSB (for 179° step change)	150 msec 500 msec	400 Hz models 60 Hz models
Settling Time to 1 LSB (small signal step $\leq 1.4^\circ$ )	20 msec 100 msec	400 Hz models 60 Hz models
<b>Power Supplies</b>		
Main Power Supply (+15 V)		
Voltage	11 V-dc to 17 V-dc	Without degradation in accuracy specification
Current:	20 mA typical 30 mA maximum	For +15 V-dc power supply
Logic Voltage (V <sub>L</sub> )		
Voltage	4.5 V-dc to main power supply	5 V-dc $\pm 10\%$ for TTL compatible output
Current	1 mA maximum 3 mA maximum	For 5 V-dc logic supply For 15 V-dc logic supply
<b>Physical Characteristics</b>		
Type	36 PIN Double DIP	
Size	0.78 x 1.9 x 0.21 inch (20 x 48 x 5.3 mm)	3 standoffs are added to the package to insulate it from printed circuit board traces (standoffs included in 0.21 inch height dimension)
Weight	0.6 oz (17 g) max	

Model 1014 converter uses thin-film resistors (as compared to screened thick-film resistors), thereby allowing flexibility of design changes. Non-standard voltages, frequency, dynamic requirements, etc. can be accommodated with minor modifications, often, without any additional costs.

If your application requires non-standard input or output characteristics, contact a Natel Applications Engineer or sales department.

## Pin Designations

+15 V	Main Power Supply - 11 V-dc to 17 V-dc
V <sub>L</sub>	Logic Voltage - 5 V-dc (For TTL compatible output) 4.5 V-dc to +15 V supply (For CMOS compatible output)
GND	Power Supply Ground Digital Ground
B1 - B14	Parallel Output Data Bits - B1 is MSB = 180 degrees B14 is LSB = 0.022 degree
S1, S2, S3, S4	Input Analog Signals - Leave S4 unconnected for synchro-input
BS, -BC	Buffered Sin $\theta$ and -Cos $\theta$ outputs
RH, RL	Reference Voltage Input
TP1, TP2	Test points - (For future expansion to 16-bits) (For factory use only)
Ge	External Gain Control (see text for details)
-D	Unfiltered dc null error - Output is referenced to bias voltage (V) (see text for details)
-E	Amplified, filtered dc null voltage - Output is referenced to bias voltage (V) (see text for details)
$\dot{\theta}$	Velocity Output - dc analog voltage proportional to rotational speed of the input shaft angle. Output is referenced to bias voltage (V)
V	Bias Voltage - Internally regulated reference voltage serves as reference ground for all analog outputs.
$\overline{\text{INH}}$	Inhibit Function - A logic "low" freezes the digital angular output. Internal loop keeps tracking the analog input. All other outputs keep following the input. For continuous operation this pin may be left unconnected. Internal active pull-up will apply V <sub>L</sub> to the pin.

S1	1	36	-BC
S2	2	35	BS
S3	3	34	V
S4	4	33	$\overline{\text{INH}}$
B1	5	32	+15V
B2	6	31	Ge
B3	7	30	TP2
B4	8	29	GND
B5	9	28	V <sub>L</sub>
B6	10	27	-D
B7	11	26	$\overline{\text{HBE}}$
B8	12	25	$\overline{\text{LBE}}$
B9	13	24	CB
B10	14	23	$\dot{\theta}$
B11	15	22	-E
B12	16	21	TP1
B13	17	20	RL
B14	18	19	RH

FIGURE 12 HSD1014/HRD1014 Pin Assignment

CB	Converter Busy - A 2 $\mu$ s pulse which occurs during updating of the holding register. Output data can be transferred at the trailing edge of the CB pulse. When converter output is not changing CB is at logic "low."
$\overline{\text{HBE}}$	High Byte Enable - Data bits B1 through B6 are enabled (low- impedance state of 3-state output) when $\overline{\text{HBE}}$ is set to a logic "low." When $\overline{\text{HBE}}$ is set to a logic "high," the data bits B1 through B6 are disabled (high-impedance state of 3-state output).
$\overline{\text{LBE}}$	Low Byte Enable - Data bits B7 through B14 are enabled when $\overline{\text{LBE}}$ is set to a logic "low." When $\overline{\text{LBE}}$ is set to a logic "high," the data bits B7 through B14 are disabled.

Note: For continuous 14-bit parallel output  $\overline{\text{HBE}}$  and  $\overline{\text{LBE}}$  may be left open. Internal active pull-down to ground will apply logic "low" to these pins thus enabling all data bits B1 through B14.

## Absolute Maximum Ratings

Signal Inputs .....	Twice Normal Voltage
Reference Input .....	200 V-rms
Main Power Supply (+15 V) .....	+18 V-dc
Logic Voltage (V <sub>L</sub> ) .....	+4.5 V-dc to +15 V supply
Digital Inputs .....	-0.3 V-dc to V <sub>L</sub>
Storage Temperature .....	-65°C to +135°C

When installing on or removing the converter from printed circuit boards or sockets, it is recommended that the power supplies and input signals be turned off. Decoupling capacitors are recommended on the main power supply (+15 V) as well as logic voltage (V<sub>L</sub>). A 1  $\mu$ F tantalum capacitor in parallel with 0.01  $\mu$ F ceramic capacitor should be mounted as close to the supply pins (32 and 28) as possible.

## Dynamic Electrical Characteristics

$T_a = 25^\circ\text{C}$   $R_L = 200\text{ k}\Omega$  Input  $t_r, t_f = 20\text{ ns}$   $V_L = 5\text{ V-dc}$   $C_L = 50\text{ pF}$

CHARACTERISTIC	LIMITS			UNITS
	MIN	TYP	MAX	
INHIBIT PULSE WIDTH, $t_{PI}$	3	—	—	$\mu\text{s}$
BUSY PULSE WIDTH, $t_{PB}$	1	2	4	$\mu\text{s}$
ENABLE PULSE WIDTH, $t_{PE}$ (HBE OR LBE)	400	—	—	ns
HIGH Z TO LOGIC "1", $t_{PZH}$	—	150	220	ns
HIGH Z TO LOGIC "0", $t_{PZL}$	—	200	300	ns
LOGIC "1" TO HIGH Z, $t_{PHZ}$	—	150	220	ns
LOGIC "0" TO HIGH Z, $t_{PLZ}$	—	200	300	ns
TRANSITION TIMES				
LOW TO HIGH, $t_{TLH}$	—	250	375	ns
HIGH TO LOW, $t_{THL}$	—	50	75	ns
INPUT CAPACITANCE, $C_{IN}$ (ANY INPUT)	—	5	7.5	pF

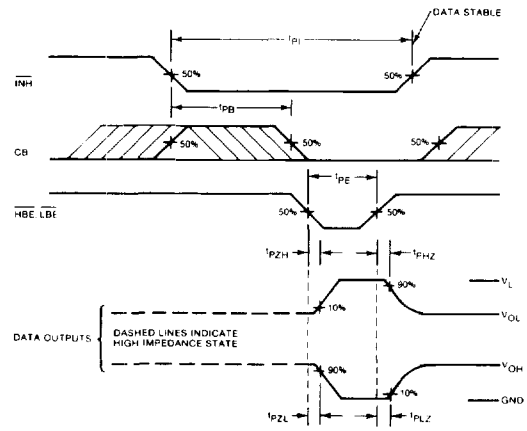


FIGURE 13 Interface Timing Diagram

## Analog Outputs

The outputs of the signal conditioner . . . resistive scott-tee for synchro-input and differential attenuator for resolver input . . . are the sine and cosine of the input shaft angle " $\theta$ ." In the converter the sine and cosine outputs of signal conditioner are processed to obtain digital output. These outputs are also brought out on pin 35 (BS) and pin 36 (-BC) as buffered sine and cosine outputs. Nominal voltage for sine maximum and cosine maximum is 1 V-rms referred to bias voltage V (pin 34) . . . the internal analog ground. The ratio accuracy of sine and cosine outputs is better than 1 arc-minute.

Other analog outputs available from the 1014 converters are

- D . . . . . unfiltered dc error (pin 27)
- E . . . . . filtered dc error (pin 22)
- $\theta$  . . . . . velocity output (pin 23)

and are referenced to bias voltage (V).

The bias voltage V is equal to  $\frac{1}{2}$  (+15 V-0.7). For main power supply voltage of +15 V-dc, the bias voltage is 7.15 V-dc.

- D is an unfiltered dc voltage proportional to error voltage  $\sin(\theta - \phi)$ , where  $\theta$  is input angle and  $\phi$  is the digital output angle. -16 mV-dc error voltage corresponds to an error of +1 LSB (0.022 degree).
- E is filtered dc voltage proportional to  $(\theta - \phi)$ . A -1 V-dc voltage corresponds to an error of +1 LSB (0.022 degree).

$\theta$  is a dc voltage proportional to the velocity of the input shaft angle (and output digital angle). The voltage goes positive for increasing digital angle and goes negative for decreasing digital angle. A +1 V-dc signal corresponds to +2.1 rps for 400 Hz models and +0.54 rps for 60 Hz models.

Scaling of all analog outputs is independent of main-power supply voltage between 11 V-dc and 17 V-dc. Also all analog outputs are operational amplifier outputs and have a drive capability of 1 mA.

The analog outputs -D, -E and  $\theta$  are by-products of the technique used in mechanizing the conversion process and are made available. They are not closely controlled or characterized functions.

If a bipolar signal is required for any analog output a difference circuit, as shown in figure 14, may be used. The output can be scaled to a desired value by selecting the gain of the circuit. Also if reverse polarity output is desirable, the bias and signal connections to the difference amplifier should be reversed.

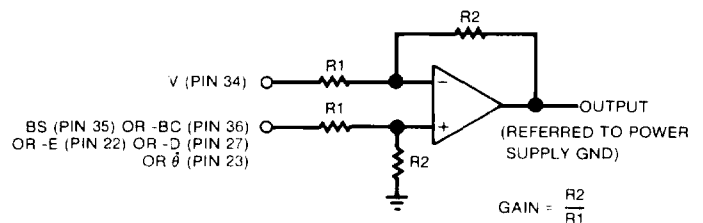


FIGURE 14 Difference Circuit for Bipolar Analog Outputs

## Other Synchro Conversion products available from NATEL

- Two-speed logic combiner with 20-bit, 3-state output, in a 1.3 x 2.6 x .35 inch size (TSL1x36)
- 14 and 16-bit Digital to Synchro/Resolver converters, with internal power amplifiers (5012, 5112, 5116)
- High power Synchro/Resolver Drivers
- 10 to 20-bit single-speed Synchro-to-Digital converters
- Hybrid synchro converters - see page 12
- Low profile Digital-to-Synchro/Resolver converters
- Two-speed Synchro (Resolver)-to-Digital converters with 16 and 20-bit resolutions in a single package. (Models 2SD402 and 2SD412).
- Solid State control transformers (SSCT) and differential transmitters (SCDX).
- Angle position indicators and synchro instrumentation for one-speed and multi-speed applications.

## Burn-in Circuit

As a standard practice all Natel hybrid synchro converters go through a power burn-in for 168 hours at maximum operating temperature. Although customer specifications in some cases, may not require it, we at Natel have found active power burn-in well worth the expense. Added initial costs save field failures and much higher system failure costs.

A burn-in circuit for Synchro (Resolver)-to-Digital Converter Model 1014 is shown in figure 15. An ac source provides the excitation voltage for the synchro (resolver) as well as a reference voltage for the 1014 converter. The frequency and voltage of the ac source are determined by the options of the unit under burn-in. A synchro (resolver) or a synchro (resolver) simulator e.g., a digital-to-synchro (resolver) converter may be used for signal input. To exercise a random digital pattern the synchro or synchro simulator may be rotated to apply a changing input shaft angle. Input S4 is left unconnected for synchro input models. The main power supply is set at +15 V-dc and the logic supply may be set at 5 V-dc or 15 V-dc. TP1, TP2 and Ge are left

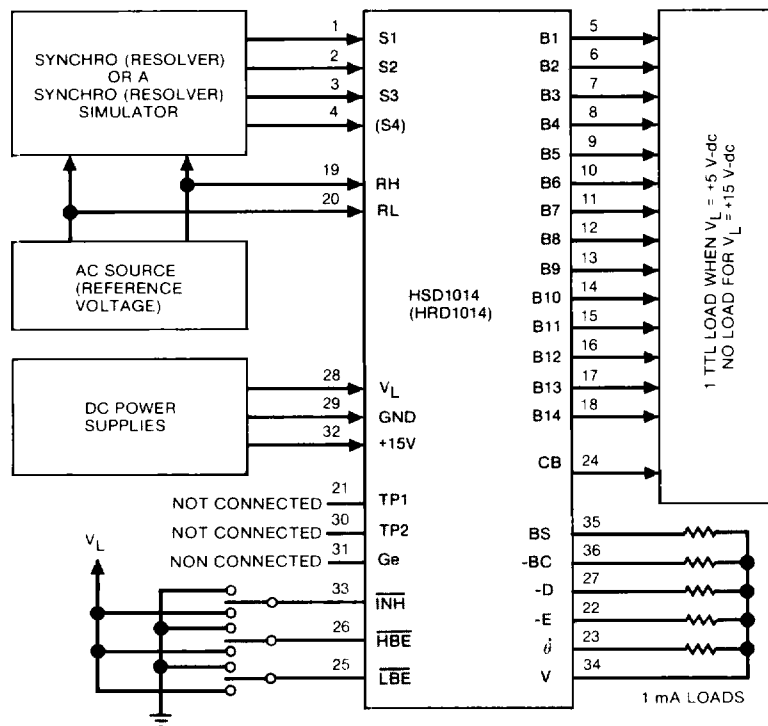


FIGURE 15 Burn-in Circuit

unconnected. Control functions INH, LBE and HBE are randomly connected to GND or  $V_L$ . Analog outputs are connected to a 1 mA

load. Data bits B1 - B14 and CB output are connected to 1 TTL load or left unconnected, depending on  $V_L$ .

## Testing Synchro (Resolver)-to-Digital Converters

All Model 1014 converters are guaranteed to meet the specifications described in the data sheet. All converters are 100% tested for their specifications (except for design parameters) at the factory. A copy of the data sheet with a record of the accuracy test is supplied with each unit.

Figure 16 shows a convenient test set-up for checking the static accuracy of the converter at incoming inspection. The synchro (resolver) input is set to "test angles." The output is monitored on a 6-digit numerical readout and compared with the standard angles for their accuracy.

Equipment described in figure 16 or equivalent may be used for testing. Synchro (Resolver) standard or simulator used must have an accuracy of at least 5 times (preferably 10 times) better than the unit under test. If the required equipment is not available arrangements may be made with Natel for source inspection at our facilities.

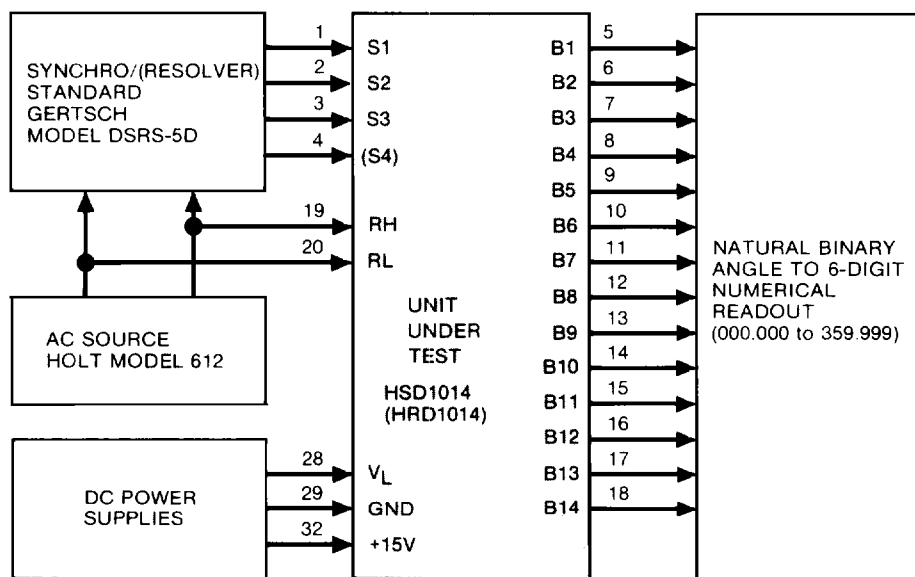
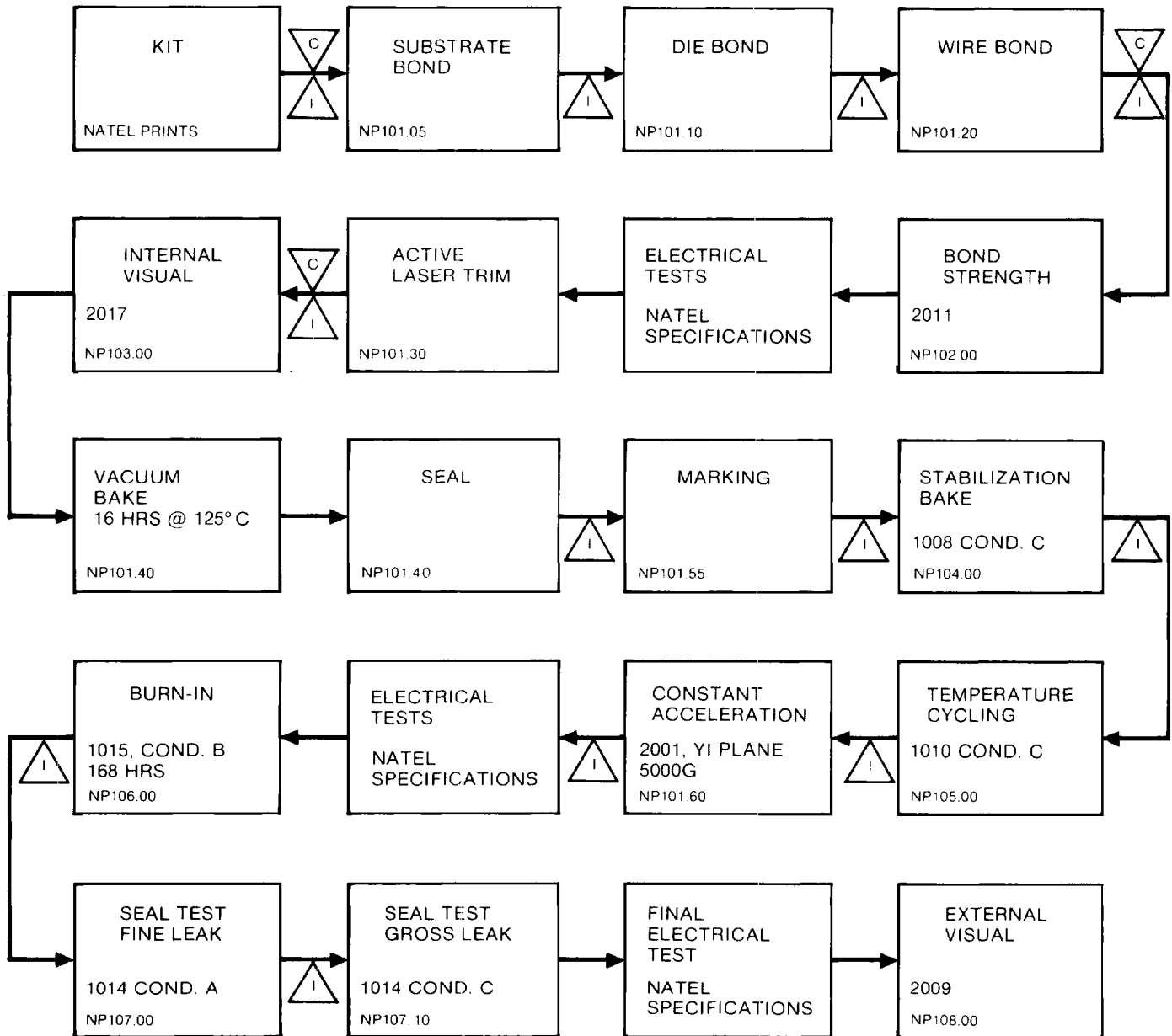


FIGURE 16 Static Accuracy Test Configuration

## Hybrid Converter Assembly and Testing

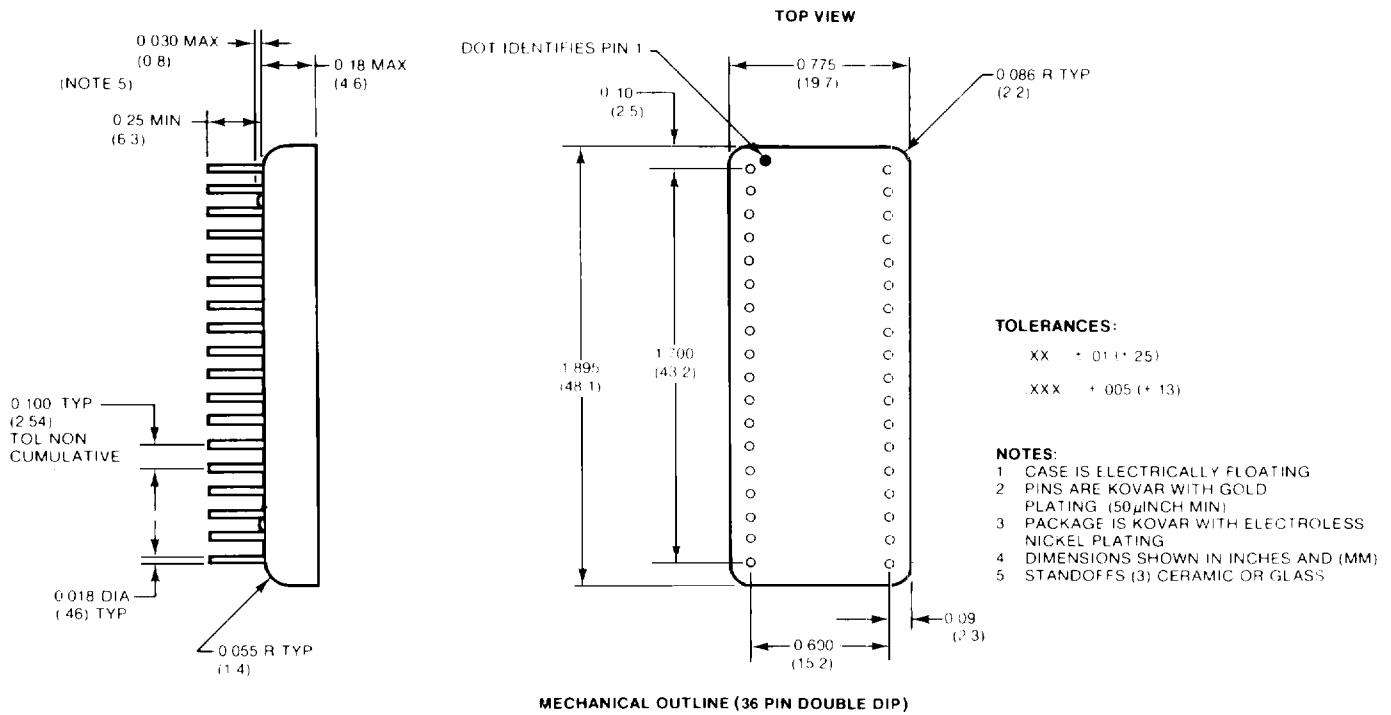
As a standard practice all Natel hybrid synchro converters are manufactured in accordance with the requirements of MIL-STD-883B method 5008. All active semiconductors and integrated circuit chips are 100% electrically probed at the vendor. All passive components used are established reliability (ER) type. Incoming inspection is per method 2010 of MIL-STD-883B. In addition, Natel may perform sample tests at incoming inspection to verify device performance. A hybrid assembly / test flow chart is shown in figure 17. Additional tests may be performed to assure long-term performance of converters.

All hybrid synchro converters have a traceability record to component level on a lot basis (lot consists of 20 or less converters). During manufacturing all work-in process and components are stored in controlled environment (dry boxes). All assembly and testing before sealing is performed in a class 100,000 clean-room. Each bonding machine/operator is evaluated at the start of every 4 hour shift by performing destructive pull-test on at least 10 wires consisting of chip to substrate bond, per paragraph 3.4.2 of method 5008. Final electrical tests are performed at room temperature as well as minimum and maximum operating temperatures.



△C = CLEAN IF REQUIRED    △I = INSPECTION

**FIGURE 17 Hybrid Assembly / Test Flow Chart**



### Ordering Information

<b>HSD1014 - T</b>	<b>F</b>	<b>A</b>
Temperature Range		Accuracy
1 0° C to + 70° C		S ± 5.2 arc. minutes
2 -25° C to + 85° C		H ± 2.6 arc. minutes
3 -55° C to +125° C		
Frequency Range		Input Signal
4 360 Hz to 1000 Hz		1 11.8 V-rms
6 47 Hz to 1000 Hz		2 26 V-rms
		9 90 V-rms
		0 Ext. Signal XFMRs
		5 Ext. Signal and Reference XFMRs

SPECIFY HRD1014 FOR RESOLVER INPUT

**MIL-STD-883 COMPLIANT HYBRIDS AVAILABLE**  
 Contact Natel Engineering for Delivery

### Other Hybrid products in 36 pin DDIP size:

- 16-bit microprocessor-compatible synchro/resolver-to-digital converter, with 3 state output, operating from a single +5-V power supply (HSRD1006)
- 16-bit microprocessor-compatible digital to synchro/resolver converter with double buffered inputs and 1 arc-minute accuracy (HDSR2006).
- 14-bit digital-to-synchro/resolver converter that is pin-compatible with existing designs with transformation and angular accuracy improvement of a factor of 2 to 4 (HDSR2504)
- 10-bit synchro (resolver)-to-digital converters that are pin compatible with existing designs (HSD/HRD1510)
- 14/16-bit synchro (resolver) control transformer with 1 arc minute accuracy (HSCT/HRCT3006)

A wide range of applications assistance is available from Natel. Application Notes can be requested when available . . . and Natel's applications engineers are at your disposal for specific problems.

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