Cortina Systems® IXF1010 10-Port 100/1000 Mbps Ethernet Media Access Controller

Datasheet

The Cortina Systems® IXF1010 10-Port 100/1000 Mbps Ethernet Media Access Controller (IXF1010 MAC) is a 10-port Ethernet Media Access Controller (MAC) that supports IEEE 802.3 100 and 1000 Mbps applications. The device supports a System Packet Interface Level 4 Phase 2 (SPI4-2) system interface to the network processor or ASIC.

The IXF1010 MAC implements the Reduced Gigabit Media Independent Interface (RGMII), as defined in Version 1.2a of the Hewlett-Packard* specification for PHY connectivity. The RGMII reduces the interface ball count from GMII to allow for higher port densities.

Applications

In general, the IXF1010 MAC is appropriate for high-end switching applications where MAC and PHY functions are not integrated into the system ASIC.

- High-End Ethernet Switches
- Multi-Service Ethernet Switches
- High-End Ethernet LAN/WAN Routers

Product Features

- RGMII interface with optical module connections/MDIO for Ethernet physical connectivity
- System Packet Interface Level 4 Phase 2 (SPI4-2)
- Capable of data transfers from 10.24 Gbps up to 12.8 Gbps
- Supports dynamic phase alignment
- Integrated termination
- Ten independent 100/1000 Mbps full-duplex Ethernet MAC ports
- 32-bit CPU interface
- Operating Temperature Range:
  - Min: 0 °C Max: +70 °C
- RMON statistics
- JTAG boundary scan
- Compliant with IEEE 802.3x Standard for flow control
- Jumbo frame support for 9.6 KB packets
- .18 µ CMOS process technology
- Internal 17.0 KB receive FIFO and 4.5 KB transmit FIFO per port
- Independent enable/disable of any port
- Detection of short or overly large packets
- Counters for dropped and errored packets
- CRC calculation and error detection
- Programmable options:
  - Filter packets with errors
  - Filter, broadcast, multicast, and unicast address packets
  - Automatically pad transmitted packets less than the minimum frame size
- 552-Ceramic BGA (RoHS-compliant)
- 1.8 V and 2.5 V operation
- Power consumption: 480 mW per-port typical

Contents

Figures

Tables

Revision History

Revision 10.0 Revision Date: 5 July 2007
First release of this document from Cortina Systems, Inc.
Clock Specification Changes: • Changed frequency range for CLK50 from 40 MHz—50 MHz to 42 MHz—50 MHz • Changed frequency range for RDCLK_x (8 x CLK50) from 320 MHz—400 MHz to 336 MHz—400 MHz **Clock Voltage Changes:** • Changed voltage for CLK125 from 2.5 V CMOS to 3.3 V LVTTL • Changed voltage for CLK50 from 2.5 V CMOS to 3.3 V LVTTL

Revision 009 Revision Date: 07 October 2005
Added Section n, *552-Ceramic BGA (RoHS-compliant)*
Table 7 “JTAG Interface Signal Descriptions” Changed Standard to 3.3 V LVTTL from 2.5 V CMOS
Modified Table 11 “Ball List in Alphanumeric Order by Signal Name” and Table 12 “Ball List in Alphanumeric Order by Ball Location”:
Figure 6 “Ethernet Frame Format” Changed Preamble byte count to 7 bytes
Figure 7 “PAUSE Frame Format” Changed Preamble byte count to 7 bytes
Table 39 “RGMII I/O Electrical Characteristics” Changed VOH, VOL, VIH, VIL minimum conditions, Input High Current, Input Low Current to V_{DD}, and changed VIN value to V_{DD} + 0.3
Table 41 “MDIO Timing Parameters” Changed MDC to MDIO Output delay max for t3 for 2.5 MHz from 200 to 300 and min to 42
Table 78 “PHY Control ($ Port_Index + 0x60)” Added “Need one-sentence descriptions of register” and register default value, changed bit 13:00 and bit 6:00 to “Reserved”
Table 79 “PHY Status ($ Port_Index + 0x61)” Added “Need one-sentence descriptions of register” and register default value
Table 80 “PHY ID 1 (Addr: Port_Index + 0x62)” Added “Need one-sentence descriptions of register” and register default value
Table 81 “PHY ID 2 ($ Port_Index + 0x63)” Added “Need one-sentence descriptions of register” and register default value
Table 82 “Auto-Negotiation Advertisement ($ Port_Index + 0x64)” Added “Need one-sentence descriptions of register” and register default value
Table 83 “Auto-Negotiation Base Page Ability ($ Port_Index + 0x65)” Added “Need one-sentence descriptions of register” and register default value
Table 84 “Auto-Negotiation Expansion ($ Port_Index + 0x66)” Added “Need one-sentence descriptions of register” and register default value
Table 85 “Auto-Negotiation Next Page Transmit ($ Port_Index + 0x67)” Added “Need one-sentence descriptions of register” and register default value
Figure 44 “Markings” New image (Added RoHS marking)
Modified Figure 47 “Ordering Information - Sample”

Revision 008 Revision Date: August 10, 2004
Globally replaced the following: “AVDD” to “AVDD1P8_1” and “AVDD2” to “AVDD2P5_1”.
Globally replaced the following: “AIDD” to “AIDD1P8_1” and “AIDD2” to “AIDD2P5_1”.
Corrected ball number for RDAT15_P from K1 to K12 in Table 3 “SPI4-2 Interface Signal Descriptions”.
Added Section 6.2, “Analog Power Filtering”.

Revision 007 Revision Date: May 5, 2004
Changed product ordering number to reflect B2 [HFIXF1010CC.B2: 860741].
Added note under Section 5.1.2.1, “Padding of Undersized Frames on Transmit”.
Modified Section 5.1.2.3.1, “Filter on Unicast Packet Match” [added text to end of paragraph].
Added Section 5.1.3, “Flow Control”.
Modified third and fourth paragraphs of Section 5.2.2.2, “CALENDAR_M”.
Added Section 6.3.1.3, “TX FIFO Drain (IXF1010 MAC Version)”.
Modified Section 6.3.1, “TX FIFO” [added note].
Added Table 48 “SPI4-2 LVDS Rise/Fall Times”.
Modified Table 72 “RX Packet Filter Control ($ Port_Index + 0x19)” (removed table note from the bit 4 description].
Modified Table 114 “SPI4-2 RX Calendar ($ 0x702)” [changed Register bits 3:0 to Reserved].
Modified Table 94 “JTAG ID Revision ($ 0x50C)” [added table note 2].
Added Table 105 “TX FIFO Drain ($0x620)”.
Modified Table 116 “IXF1010 MAC Product Information” [changed part number and mm number to reflect B2].

Revision 006 Revision Date: December 30, 2003
Changed Table 98: TX FIFO Port Reset Register (Addr: 0x620) to Reserved.

Revision 005 (Sheet 1 of 2) Revision Date: November 24, 2003
Added product ordering and operating temperature range information, and changed SFF-8053, Revision 5.5 Compatible to SFP MSA compatible.
Deleted old Figures 6, 7, and 8 (Revision 004) and replaced with Figure 6 “IXF1010 552-Ball CBGA Assignments (Top View)”
Added new Section 3.1, “IXF1010 Ball List Tables” including Table 1 “IXF1010 Ball List in Alphanumeric Order by Signal Name” and Table 2 “IXF1010 Ball List in Alphanumeric Order by Ball Location”.
Modified Figure 4 “IXF1010 Interface Diagram”.
Broke up old Table 3 into Table 3 “IXF1010 SPI4-2 Interface Signal Descriptions” through Table 12 “IXF1010 System Interface Signal Descriptions”.
Modified Table 5 “IXF1010 CPU Interface Signal Descriptions”.
Added note under Section 5.1.2.3.5, “Filter PAUSE Packets”.
Added note under Section 5.1.2.3.6, “Filter CRC Errored Packets”.
Modified Figure 6 “IXF1010 SPI4-2 Interfacing with the Network Processor or Forwarding Engine”.
Added Table 17 “IXF1010 SPI4-2 Interface Signal Summary”.
Added new Section 5.2.1.2, “EOP Abort”.
Added note under Section 5.3.4.2, “TXERR and RXERR Coding”.
Modified Section 5.3.5, “100 Mbps Operation”.
Added note to “UPX_RDY” under Section 5.8.2, “Functional Description”.
Added note under Section 6.2.1, “TX FIFO”.
Added note under Section 6.2.1.1, “MAC Transfer Threshold”.
Modified Table 33 “IXF1010 Operating Conditions”.
Modified Table 34 “IXF1010 2.5 V LVTTL and CMOS I/O Electrical Characteristics”.
Added Section 7.2, “Undershoot/Overshoot Specifications”.
Modified Table 38 “IXF1010 RGMII I/O Electrical Characteristics”

Revision 005 (Sheet 2 of 2) Revision Date: November 24, 2003
Modified Table 41 “IXF1010 CPU Timing Parameters”.
Added caution note under Section 8.0, “Register Definitions”.
Modified Table 52 “IXF1010 Global Status and Configuration Register Map”.
Modified Table 63 “IPG Transmit Time Register (Addr: Port_Index + 0x0C)”.
Modified Table 64 “Pause Threshold Register (Addr: Port_Index + 0x0E)”.
Modified Table 67 “FC Enable Register (Addr: Port_Index + 0x12)”.
Modified Table 68 “Short Runts Threshold Register (Addr: Port_Index + 0x14)”.
Modified Table 70 “Diverse Config Register (Addr: Port_Index + 0x18)”.
Modified Table 71 “RX Packet Filter Control Register (Addr: Port_Index + 0x19)” (removed note 2 from bit 4, modified bit 5 description).
Modified Table 74 “MAC RX Statistics Registers (Addr: Port_Index + 0x20 - Port_Index + 0x39)”.
Added Table 86 “Core Clock Soft Reset Register (Addr: 0x504)”.
Added Table 87 “MAC Soft Reset Register (Addr: 0x505)”.
Added Table 97 “RX FIFO Port Reset Register (Addr: 0x59E)”.
Added Section 104, “TX FIFO Port Reset Register (Addr: 0x620)”.
Modified Table 106 “TX FIFO Number of Frames Removed Ports 0-9 (Addr: 0x622 - 0x62B)”.
Modified Table 113 “SPI4-2 RX Calendar Register (Addr: 0x702)”.
Modified Table 114 “SPI4-2 TX Synchronization Register (Addr: 0x703) (B0 Silicon Revision)”.

1.0 Introduction

This Datasheet describes the functionality and operation of the Cortina Systems® IXF1010 10-Port 100/1000 Mbps Ethernet Media Access Controller (IXF1010 MAC).

1.1 What You Will Find in This Document

This document contains the following sections:

- Section 2.0, *General Description*, on page 15
  IXF1010 MAC block diagram system architecture.
- Section 3.0, *Ball Assignments and Ball List Tables*, on page 17
  IXF1010 MAC ball grid diagram with two ball list tables (by pin number and signal name)
- Section 4.0, *Ball Assignments and Signal Descriptions*, on page 18
  Signal naming methodology and signal descriptions.
- Section 5.0, *Functional Description*, on page 40
  Detailed information about the operation of the IXF1010 MAC including general features, and interface types and descriptions.
- Section 6.0, *Applications*, on page 86
  Discusses the following:
  - Section 6.1, *Power Supply Sequencing*
  - Section 6.3, *TX FIFO and RX FIFO Operation*
  - Section 6.4, *Reset and Initialization*
- Section 7.0, *Electrical Specifications*, on page 93
  Information on the product-operating parameters, electrical specifications, and timing parameters.
- Section 8.0, *Register Definitions*, on page 107
  Memory map/detailed descriptions and default values for the register set.
- Section 9.0, *Mechanical Specifications*, on page 165
  IXF1010 MAC packaging information.
- Section 10.0, *Product Ordering Information*, on page 169
  Provides a table with part-number information and diagram to order the IXF1010 MAC.

1.2 Related Documents

Title	Document Number
IXF1010 MAC Specification Update	249357
IXF1010 MAC Design and Layout Guide	250676
IXF1010 MAC Demo Board Development Kit Manual	250709
Cortina Systems® SPI4 Phase 2 Performance in Gigabit Ethernet Media Access Controllers Application Note	250643

Title	Document Number
Interfacing with the IXF1010 MAC and IXF1110 MAC 10-Port Gigabit Ethernet Media Access Controllers Application Note	250856
IXF1010 MAC Thermal Design Considerations Application Note	250288
Flow Control in theIXF1010 MAC and IXF1110 MAC 10-Port Gigabit Ethernet Media Access Controllers Application Note	250236

2.0 General Description

The IXF1010 MAC is a 10-port 100/1000 Mbps Ethernet Media Access Controller (MAC). The 10 Gigabit interface to the network processor is supported through a System Packet Interface Level 4 Phase 2 (SPI4-2), and the /PHY interface is a Reduced Gigabit Media Independent Interface (RGMII).

Figure 2 illustrates the IXF1010 MAC block diagram. Figure 2 represents the IXF1010 MAC system block diagram.

Figure 1 IXF1010 MAC Block Diagram

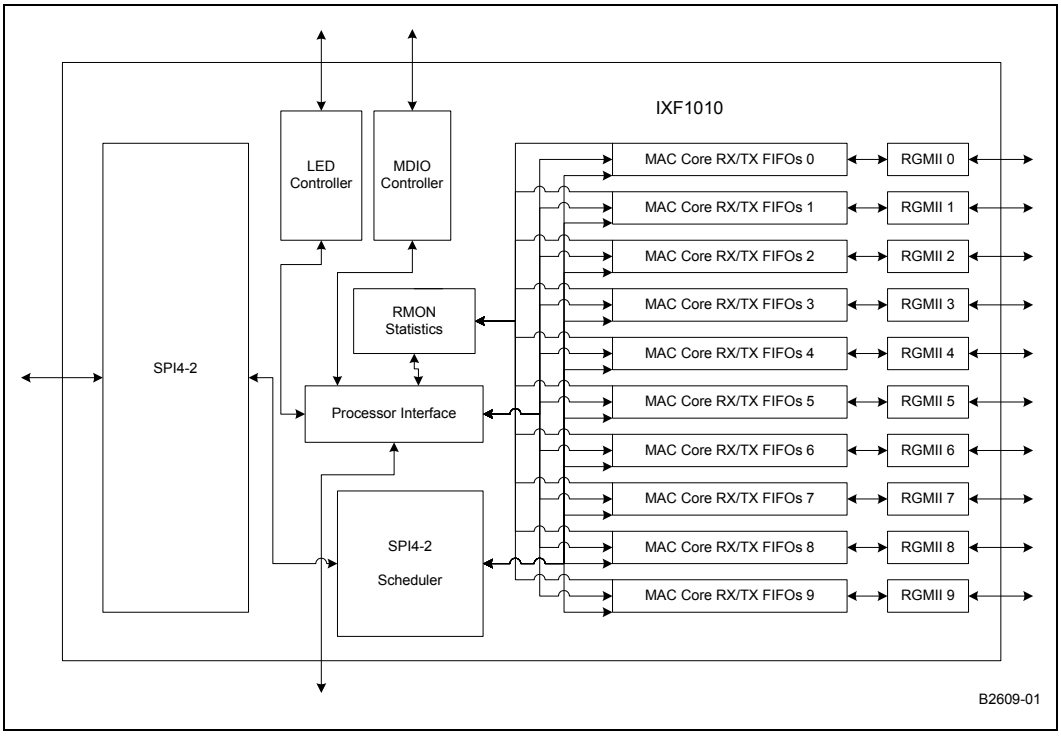
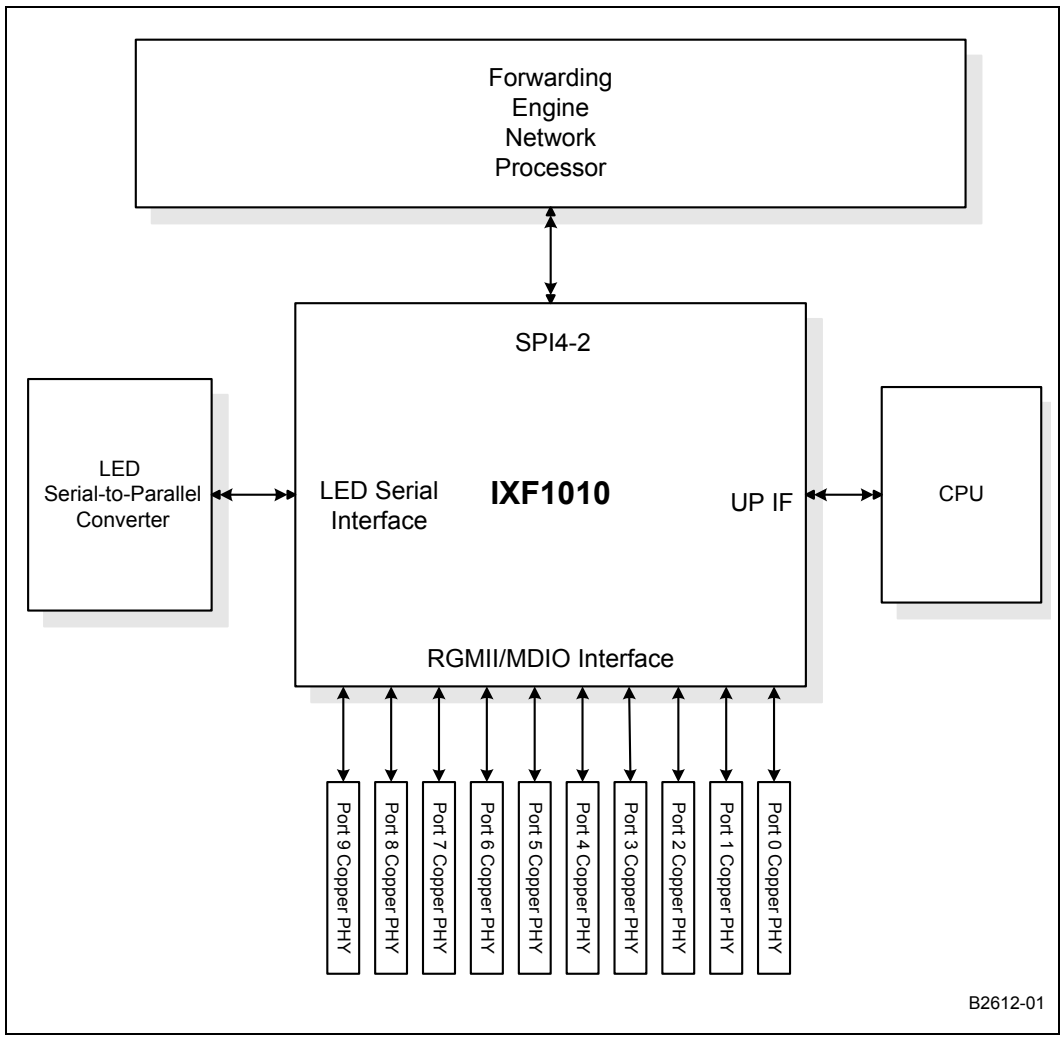


Figure 2 IXF1010 MAC System Block Diagram



3.0 Ball Assignments and Ball List Tables

Figure 3 illustrates the 552-Ball CBGA assignments. Table 11 and Table 12 provide ball list tables in alphanumeric order by signal name and ball location under Section 4.3, *Ball List Tables*, on page 29.

Figure 3 552-Ball CBGA Assignments (Top View)

	AD	AC	AB	AA	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
1	AD1	AC1	AB1	AA1	Y1	W1	V1	U1	T1	R1	L1	N1	M1	L1	K1	J1	H1	G1	F1	E1	D1	C1	B1	A1	1
2	AD2	AC2	AB2	AA2	Y2	W2	V2	U2	T2	R2	P2	N2	M2	L2	K2	J2	H2	G2	F2	E2	D2	C2	B2	A2	2
3	AD3	AC3	AB3	AA3	Y3	W3	V3	U3	T3	R3	P3	N3	M3	L3	K3	J3	H3	G3	F3	E3	D3	C3	B3	A3	3
4	AD4	AC4	AB4	AA4	Y4	W4	V4	U4	T4	R4	P4	N4	M4	L4	K4	J4	H4	G4	F4	E4	D4	C4	B4	A4	4
5	AD5	AC5	AB5	AA5	Y5	W5	V5	U5	T5	R5	P5	N5	M5	L5	K5	J5	H5	G5	F5	E5	D5	C5	B5	A5	5
6	AD6	AC6	AB6	AA6	Y6	W6	V6	U6	T6	R6	P6	N6	M6	L6	K6	J6	H6	G6	F6	E6	D6	C6	B6	A6	6
7	AD7	AC7	AB7	AA7	Y7	W7	V7	U7	T7	R7	P7	N7	M7	L7	K7	J7	H7	G7	F7	E7	D7	C7	B7	A7	7
8	AD8	AC8	AB8	AA8	Y8	W8	V8	U8	T8	R8	P8	N8	M8	L8	K8	J8	H8	G8	F8	E8	D8	C8	B8	A8	8
9	AD9	AC9	AB9	AA9	Y9	W9	V9	U9	T9	R9	P9	N9	M9	L9	K9	J9	H9	G9	F9	E9	D9	C9	B9	A9	9
10	AD10	AC10	AB10	AA10	Y10	W10	V10	U10	T10	R10	P10	N10	M10	L10	K10	J10	H10	G10	F10	E10	D10	C10	B10	A10	10
11	AD11	AC11	AB11	AA11	Y11	W11	V11	U11	T11	R11	P11	N11	M11	L11	K11	J11	H11	G11	F11	E11	D11	C11	B11	A11	11
12	AD12	AC12	AB12	AA12	Y12	W12	V12	U12	T12	R12	P12	N12	M12	L12	K12	J12	H12	G12	F12	E12	D12	C12	B12	A12	12
13	AD13	AC13	AB13	AA13	Y13	W13	V13	U13	T13	R13	P13	N13	M13	L13	K13	J13	H13	G13	F13	E13	D13	C13	B13	A13	13
14	AD14	AC14	AB14	AA14	Y14	W14	V14	U14	T14	R14	P14	N14	M14	L14	K14	J14	H14	G14	F14	E14	D14	C14	B14	A14	14
15	AD15	AC15	AB15	AA15	Y15	W15	V15	U15	T15	R15	P15	N15	M15	L15	K15	J15	H15	G15	F15	E15	D15	C15	B15	A15	15
16	AD16	AC16	AB16	AA16	Y16	W16	V16	U16	T16	R16	P16	N16	M16	L16	K16	J16	H16	G16	F16	E16	D16	C16	B16	A16	16
17	AD17	AC17	AB17	AA17	Y17	W17	V17	U17	T17	R17	P17	N17	M17	L17	K17	J17	H17	G17	F17	E17	D17	C17	B17	A17	17
18	AD18	AC18	AB18	AA18	Y18	W18	V18	U18	T18	R18	P18	N18	M18	L18	K18	J18	H18	G18	F18	E18	D18	C18	B18	A18	18
19	AD19	AC19	AB19	AA19	Y19	W19	V19	U19	T19	R19	P19	N19	M19	L19	K19	J19	H19	G19	F19	E19	D19	C19	B19	A19	19
20	AD20	AC20	AB20	AA20	Y20	W20	V20	U20	T20	R20	P20	N20	M20	L20	K20	J20	H20	G20	F20	E20	D20	C20	B20	A20	20
21	AD21	AC21	AB21	AA21	Y21	W21	V21	U21	T21	R21	P21	N21	M21	L21	K21	J21	H21	G21	F21	E21	D21	C21	B21	A21	21
22	AD22	AC22	AB22	AA22	Y22	W22	V22	U22	T22	R22	P22	N22	M22	L22	K22	J22	H22	G22	F22	E22	D22	C22	B22	A22	22
23	AD23	AC23	AB23	AA23	Y23	W23	V23	U23	T23	R23	P23	N23	M23	L23	K23	J23	H23	G23	F23	E23	D23	C23	B23	A23	23
24	AD24	AC24	AB24	AA24	Y24	W24	V24	U24	T24	R24	P24	N24	M24	L24	K24	J24	H24	G24	F24	E24	D24	C24	B24	A24	24
	AD	AC	AB	AA	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

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4.0 Ball Assignments and Signal Descriptions

4.1 Naming Conventions

4.1.1 Signal Name Conventions

Signal names begin with a Signal Mnemonic, and can also contain one or more of the following designations: a differential pair designation, a serial designation, a port designation (RGMII interface), and an active Low designation. Signal naming conventions are as follows:

Differential Pair + Port Designation. The positive and negative components of differential pairs tied to a specific port are designated by the Signal Mnemonic, immediately followed by an underscore and either P (positive component) or N (negative component), and an underscore followed by the port designation. For example, SerDes interface signals for port 0 are identified as TX_P_0 and TX_N_0.

Serial Designation. A set of signals that are not tied to any specific port are designated by the Signal Mnemonic, followed by a bracketed serial designation. For example, the set of 11 CPU Address Bus signals is identified as UPX_ADD[10:0].

Port Designation. Individual signals that apply to a particular port are designated by the Signal Mnemonic, immediately followed by an underscore and the Port Designation. For example, RGMII Transmit Control signals would be identified as TX_CTL_0, TX_CTL_1, TX_CTL_2, etc.

Port Bus Designation: A set of bus signals that apply to a particular port are designated by the Signal Mnemonic, immediately followed by a bracketed bus designation, followed by an underscore and the port designation. For example, RGMII transmit data bus signals would be identified as TD[3:0]_0, TD[3:0]_1, TD[3:0]_2, etc.

Active Low Designation. A control input or indicator output that is active Low is designated by a final suffix consisting of an underscore followed by an upper case “L”. For example, the CPU cycle complete identifier is shown as UPX_RDY_L.

4.1.2 Register Address Conventions

Registers located in on-chip memory are accessed using a register address, which is provided in Hex notation. A Register Address is indicated by the dollar sign ($), followed by the memory location in Hex.

4.2 Interface Signal Groups

This section describes the IXF1010 MAC signals in groups according to the associated interface or function. Figure 4 and Table 1, *SPI4-2 Interface Signal Descriptions* through Table 10, *Unused Balls/Reserved*, on page 28 describe the IXF1010 MAC signals.

Figure 4 Interface Diagram

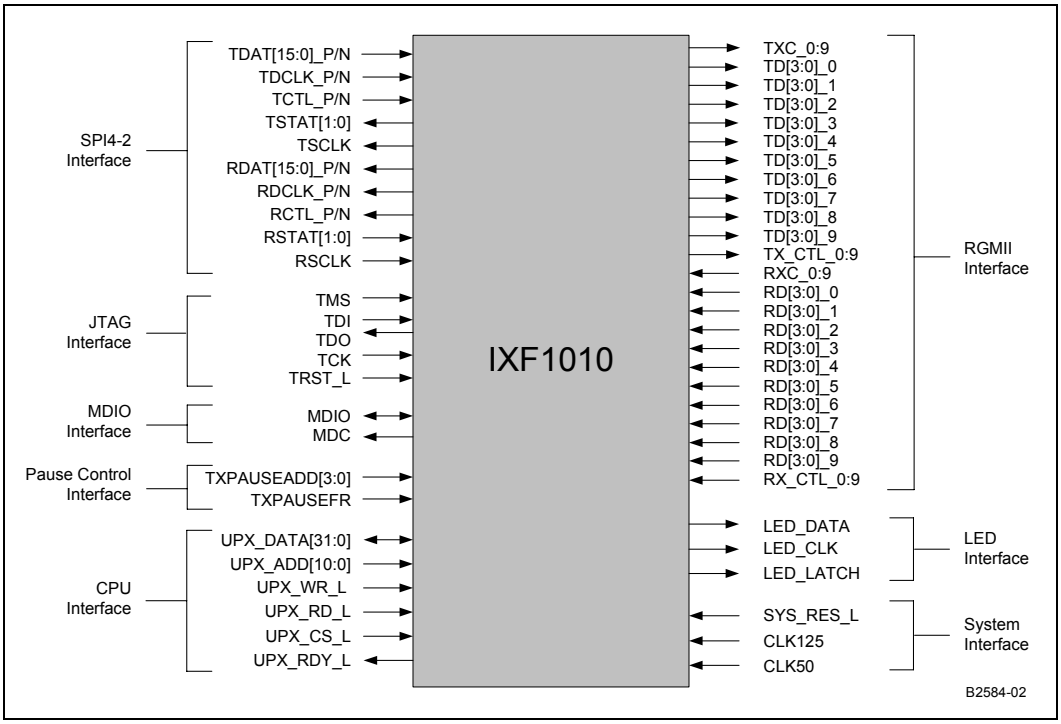


Table 1 SPI4-2 Interface Signal Descriptions (Sheet 1 of 2)

Signal Name	Ball Designator	Type	Standard	Signal Description
TDAT15_P, TDAT15_N TDAT14_P, TDAT14_N TDAT13_P, TDAT13_N TDAT12_P, TDAT12_N TDAT11_P, TDAT11_N TDAT10_P, TDAT10_N TDAT9_P, TDAT9_N TDAT8_P, TDAT8_N TDAT7_P, TDAT7_N TDAT6_P, TDAT6_N TDAT5_P, TDAT5_N TDAT4_P, TDAT4_N TDAT3_P, TDAT3_N TDAT2_P, TDAT2_N TDAT1_P, TDAT1_N TDAT0_P, TDAT0_N	G11 H11 C9 D9 J9 K10 H7 J8 E8 E7 E9 F9 B7 C8 L5 M5 C7 C6 L8 L7 G5 H5 F7 G6 G9 H9 B5 C5 H3 J3 J6 J5	Input	LVDS	**Transmit Data Bus:** Carries payload data and in-band control words to the IXF1010 MAC link-layer device. Internally terminated differentially with 100 Ω.
TDCLK_P TDCLK_N	D3 E4	Input	LVDS	**Transmit Data Clock:** Clock associated with TDAT[15:0] and TCTL. Data and control lines are driven off the rising and falling edges of the clock. Internally terminated differentially with 100 Ω. **NOTE:** If TDCLK is applied to the IXF1010 MAC after the device has come out of reset, the system designer must ensure the TDCLK is stable when applied. Failure to due so can result in the IXF1010 MAC training on a non-stable clock, causing DIP4 errors and data corruption.
TCTL_P TCTL_N	M10 N10	Input	LVDS	**Transmit Control:** TCTL is High when a control word is present on TDAT[15:0]. Otherwise, TCTL is Low. Internally terminated differentially with 100 Ω.
TSCLK	C11	Output	2.5 V LVTTL	**Transmit Status Clock:** Clock associated with TSTAT [1:0]. Frequency is equal to one-quarter TDCLK.
TSTAT1 TSTAT0	E6 E5	Output	2.5 V LVTTL	**Transmit FIFO Status:** Carries round-robin FIFO status information, along with associated error detection and framing.

Table 1 SPI4-2 Interface Signal Descriptions (Sheet 2 of 2)

Signal Name	Ball Designator	Type	Standard	Signal Description
RDAT15_P, RDAT15_N RDAT14_P, RDAT14_N RDAT13_P, RDAT13_N RDAT12_P, RDAT12_N RDAT11_P, RDAT11_N RDAT10_P, RDAT10_N RDAT9_P, RDAT9_N RDAT8_P, RDAT8_N RDAT7_P, RDAT7_N RDAT6_P, RDAT6_N RDAT5_P, RDAT5_N RDAT4_P, RDAT4_N RDAT3_P, RDAT3_N RDAT2_P, RDAT2_N- RDAT1_P, RDAT1_N RDAT0_P, RDAT0_N	K12 K13 F16 G16 E13 E14 A13 A14 J16 K15 G17 G18 D18 E18 C16 D16 M15 N15 E16 E17 L17 L18 J18 J19 G21 H20 F18 G19 B20 C20 E19 E20	Output	LVDS	**Receive Data:** Carries payload data and in-band control from the IXF1010 MAC link-layer device. Internally terminated differentially with 100 Ω.
RDCLK_P RDCLK_N	C18 C19	Output	LVDS	**Receive Data Clock:** Clock associated with RDAT[15:0] and RCTL. Data and control lines are driven off the rising and falling edges of the clock. The frequency range is 336-400 Mhz. Frequency is always a multiplied- by-8 Version of the CLK50 reference clock. Internally terminated differentially with 100 Ω.
RCTL_P RCTL_N	H16 H18	Output	LVDS	**Receive Control:** RCTL is High when a control word is present on RDAT[15:0]. Otherwise, RCTL is Low. Internally terminated differentially with 100 Ω.
RSCLK	J17	Input	2.5 V LVTTL	**Receive Status Clock:** The clock associated with RSTAT[1:0].
RSTAT1 RSTAT0	J20 L20	Input	2.5 V LVTTL	**Receive FIFO Status:** Carries round-robin FIFO status information, along with associated error detection and framing.

Table 2 RGMII Interface Signal Descriptions (Sheet 1 of 2)

Signal Name	Ball Designator				Type	Standard	Signal Description
TXC_0 TXC_1 TXC_2 TXC_3 TXC_4 TXC_5 TXC_6 TXC_7 TXC_8 TXC_9	R22 R20 AD20 AB19 W16 AA11 Y11 AD6 N5 N1				Output	2.5 V CMOS	**Transmit Reference Clock**: Operates at: 125 MHz for 1 Gigabit operation 25 MHz for 100 Mbps operation
TD[3:0]_0 TD[3:0]_1 TD[3:0]_2 TD[3:0]_3 TD[3:0]_4 TD[3:0]_5 TD[3:0]_6 TD[3:0]_7 TD[3:0]_8 TD[3:0]_9	L23 P17 AB18 AA22 W18 Y10 Y7 AD5 T6 P2	M24 V23 Y17 R15 W14 W11 W9 AC5 P8 M1	L21 N20 AD19 R13 AA20 V9 AB8, AD4 R5 L2	L22 V17 AD18 R12 AB15 V12 Y9 AC3 T2 P4	Output	2.5 V CMOS	**Transmit Data:** This bus contains bits 3:0 on the rising edge of the TXC and bits 7:4 on the falling edge of TXC.
TX_CTL_0 TX_CTL_1 TX_CTL_2 TX_CTL_3 TX_CTL_4 TX_CTL_5 TX_CTL_6 TX_CTL_7 TX_CTL_8 TX_CTL_9	N24 Y21 AA16 M20 AC14 U11 T4 AB2 R7 L1				Output	2.5 V CMOS	**Transmit Control:** This signal is TXEN on the rising edge of TXC and a logical derivative of TXEN and TXERR on the falling edge.

Table 2 RGMII Interface Signal Descriptions (Sheet 2 of 2)

Signal Name	Ball Designator				Type	Standard	Signal Description
RXC_9 RXC_8 RXC_7 RXC_6 RXC_5 RXC_4 RXC_3 RXC_2 RXC_1 RXC_0	R1 AB6 W7 R10 AB17 Y18 P21 AB23 T23 J21				Input	2.5 V CMOS	**Receiver reference clock:** 125 MHz for 1 Gigabit operation 25 MHz for 100 Mbps operation
RD[3:0]_0 RD[3:0]_1 RD[3:0]_2 RD[3:0]_3 RD[3:0]_4 RD[3:0]_5 RD[3:0]_6 RD[3:0]_7 RD[3:0]_8 RD[3:0]_9	M18 P23 AB21 U16 V13 Y12 V2 Y8 W5 R3	K20 T21 AC20 T17 V16 AB10 T9 AB7 U7 P1	K24 P24 AD21 T19 Y16 Y13 L6 AC7 T7 M3	K22 M22 AC22 U18 U14 AA18 U9 AA9 V7 L4	Input	2.5 V CMOS	**Receive Data:** This bus contains bits 3:0 on the rising edge of the clock and bits 7:4 on the falling edge.
RX_CTL_0 RX_CTL_1 RX_CTL_2 RX_CTL_3 RX_CTL_4 RX_CTL_5 RX_CTL_6 RX_CTL_7 RX_CTL_8 RX_CTL_9	L24 R24 W20 T18 AA14 AC11 T8 AA7 AA3 L3				Input	2.5 V CMOS	**Receive Control:** This signal is RXDV on the rising edge of RXC and a logical derivative of RXDV and RXERR on the falling edge.

Table 3 CPU Interface Signal Descriptions (Sheet 1 of 2)

Signal Name	Ball Designator	Type	Standard	Signal Description
UPX_ADD10 UPX_ADD9 UPX_ADD8 UPX_ADD7 UPX_ADD6 UPX_ADD5 UPX_ADD4 UPX_ADD3 UPX_ADD2 UPX_ADD1 UPX_ADD0	C2 F1 F5 C3 G1 E2 E3 H1 F3 G4 J1	Input	2.5 V CMOS	**Address bus:** 11-bit address bus
UPX_CS_L	F20	Input	2.5 V CMOS	**Chip Select Signal:** Active Low chip select
UPX_DATA31 UPX_DATA30 UPX_DATA29 UPX_DATA28 UPX_DATA27 UPX_DATA26 UPX_DATA25 UPX_DATA24 UPX_DATA23 UPX_DATA22 UPX_DATA21 UPX_DATA20 UPX_DATA19 UPX_DATA18 UPX_DATA17 UPX_DATA16 UPX_DATA15 UPX_DATA14 UPX_DATA13 UPX_DATA12 UPX_DATA11 UPX_DATA10 UPX_DATA9 UPX_DATA8 UPX_DATA7 UPX_DATA6 UPX_DATA5 UPX_DATA4 UPX_DATA3 UPX_DATA2 UPX_DATA1 UPX_DATA0	C23 B22 A21 B18 A17 C17 A16 G14 E15 B16 G13 A15 A12 F14 C14 D14 D7 F11 E10 G12 A11 E12 A9 A10 A8 C13 E11 C12 A7 B9 A4 B3	Input/ Output	2.5 V CMOS	**Bi-directional data bus:** 32-bit bi-directional data bus
1. This I/O meets the 2.5 V CMOS specification only during boundary scan mode.				

Table 3 CPU Interface Signal Descriptions (Sheet 2 of 2)

Signal Name	Ball Designator	Type	Standard	Signal Description
UPX_WR_L	A18	Input	2.5 V CMOS	**Write Strobe:** Active Low Write strobe
UPX_RD_L	H14	Input	2.5 V CMOS	**Read Strobe:** Active Low Read strobe
UPX_RDY_L	C22	Open Drain Output*	2.5 V CMOS[1]	**Cycle complete indicator:** Indicates that Read or Write is complete. ***Note:*** An external pull-up resistor is required for proper operation. ***Note:*** *Dual-mode I/O. Normal operation: Open drain output Boundary Scan Mode: Standard CMOS output
1. This I/O meets the 2.5 V CMOS specification only during boundary scan mode.				

Table 4 Pause Control Interface Signal Descriptions

Signal Name	Ball Designator	Type	Standard	Signal Description
TXPAUSEFR	J7	Input	2.5 V CMOS	**Pause Strobe:** Indicates when a Pause frame is to be sent
TXPAUSEADD3 TXPAUSEADD2 TXPAUSEADD1 TXPAUSEADD0	K1 J2 G2 G3	Input	2.5 V CMOS	**Pause Address Bus:** Selects the port for the Pause frames

Table 5 MDIO Interface Signal Descriptions

Signal Name	Ball Designator	Type	Standard	Signal Description
MDIO	J22	Input/ Output	2.5 V CMOS	**Management Data Input/Output:** Data signal for MDIO.
MDC	H22	Output	2.5 V CMOS	**Management Data Clock:** Clock to external devices.

Table 6 LED Interface Signal Descriptions

Signal Name	Ball Designator	Type	Standard	Signal Description
LED_CLK	A19	Output	2.5 V CMOS	**LED Clock:** Clock output for the LED block.
LED_DATA	A20	Output	2.5 V CMOS	**LED Data:** Data output for the LED block.
LED_LATCH	K18	Output	2.5 V CMOS	**LED Latch:** Latch enable for the LED block.

Table 7 JTAG Interface Signal Descriptions

Signal Name	Ball Designator	Type	Standard	Signal Description
TCK	AA24	Input	3.3 V LVTTL	**JTAG Test Clock:** Reference clock for JTAG.
TMS	T16	Input	3.3 V LVTTL	**JTAG Test Mode Select:** Selects test mode for JTAG.
TDI	AC18	Input	3.3 V LVTTL	**JTAG Test Data Input:** Test data sampled with respect to the rising edge of TCK.
TRST_L	N18	Input	3.3 V LVTTL	**JTAG Test Reset:** Reset input for JTAG test.
TDO	Y24	Output	3.3 V LVTTL	**JTAG Test Data Output:** Test data driven with respect to the falling edge of TCK.

Table 8 System Interface Signal Descriptions

Signal Name	Ball Designator	Type	Standard	Signal Description
CLK125	AA5	Input	3.3 V LVTTL	**125 MHz Reference Clock:** Input clock to PLL.
CLK50	C21	Input	3.3 V LVTTL	**SPI4-2 Reference Clock:** Input clock to SPI4-2 RX PLL. Input range is 42 MHz to 50 MHz. This clock multiplied by eight must equal the required RX SPI4-2 data clock frequency.
SYS_RES_L	Y4	Input	2.5 V CMOS	**System Reset:** System hard reset (active Low).

Table 9 Power Supply Signal Descriptions (Sheet 1 of 2)

Signal Name	Ball Designator	Type	Standard	Signal Description
AVDD1P8_1	D1 E24 ,	–	–	**1.8 V Analog Power Supply**
AVDD2P5_1	Y1	–	–	**2.5 V Analog Power Supply**

Table 9 Power Supply Signal Descriptions (Sheet 2 of 2)

Signal Name	Ball Designator	Type	Standard	Signal Description
VDD	D6 D10 D11 D15 D19 D20 E21 F4 F21 H10 H15 J4 J11 J14 K3 K4 K5 K8 K17 K21 L9 L11 L14 L16 P9 P11 P14 P16 R4 R8 R17 R21 T11 T14 U10 U15 W4 W21 AA6 AA10 AA15 AA19 AB4	–	–	**1.8 V Digital Power Supply:** 1.8 V core supply
VDD2	B4 B8 B12 B13 B17 B21 D2 D23 F8 F12 F13 F17 G10 H2 H6 H19 H23 J12 J13 M2 M6 M9 M12 M13 M16 M23 N2 M19 N9 N12 N13 N6 N19 N23 T12 N16 U2 U6 U19 T13 W8 W12 W13 U23 AA2 AA23 AC4 W17 AC12 AC13 AC17 AC8 AC21	–	–	**2.5 V Digital Power Supply:** 2.5 V I/O supply
GND	B6 B10 B15 B19 C4 D4 D5 D8 D12 D13 D17 D21 D22 D24 E1 F2 F6 F10 F15 F19 F23 H4 H8 H12 H13 H17 H21 J10 J15 J23 K2 K6 K9 K11 K14 K16 K19 K23 L10 L12 L13 L15 M4 M8 M11 M14 M17 M21 N4 N8 N11 N14 N17 N21 P10 P12 P13 P15 R2 R6 R9 R11 R14 R16 R19 R23 T10 T15 T20 T22 T24 U13 U4 U8 U12 U17 U20 U21 U22 U24 V3 V4 V5 V24 W2 W3 W6 W10 W1 W19 W23 W24 Y2 Y3 Y5 Y6 Y15 AA1 AA4 AA8 AA12 AA13 AA17 AA21 AB13 AB14 AB16 AC6 AC10 AC15 AC16 AD15 AC19 AD13 AD14 AD16	–	–	**Ground:** Ground return for all signals.

Table 10 Unused Balls/Reserved

Signal Name	Ball Designator	Type	Standard	Signal Description
NC	A5 A6 B11 B14 C10 C15 E22 E23 F22 F24 G7 G8 G15 G20 G22 G23 G24 H24 J24 K7 L19 M7 N3 N7 N22 P3 P5 P6 P7 P18 P19 P20 P22 R18 T1 T3 T5 U1 U3 U5 V1 V6 V8 V10 V11 V14 V15 V18 V19 V20 V21 V22 W1 W22 Y14 Y19 Y20 Y22 Y23 AB3 AB5 AB9 AB11 AB12 AB20 AB22 AC9 AD7 AD8 AD9 AD10 AD11 AD12 AD17	–	–	No connection.
No Ball	A2 A3 A22 A23 A24 B1 B2 B23 B24 C1 C24 AB1 AB24 AC1 AC2 AC23 AC24 AD1 AD2 AD3 AD22 AD23 AD24	–	–	Balls removed from substrate.
No Pad	A1	–	–	Pad removed from substrate. Use this ball location as a key for device placement onto the PCB.

4.3 Ball List Tables

Ball list tables are provided in alphanumeric order by signal name (Table 11) and by ball location order (Table 12).

Note: Cortina recommends that all unconnected balls be tied to their inactive states through external pull-ups or pull-downs.

4.3.1 Balls Listed in Alphanumeric Order by Signal Name

Table 11 shows the ball locations and signal names arranged in alphanumeric order by signal name.

Table 11 Ball List in Alphanumeric Order by Signal Name

Signal	Ball	Signal	Ball	Signal	Ball
AVDD1P8_1	D1	GND	H12	GND	N14
AVDD1P8_1	E24	GND	H13	GND	N17
AVDD2P5_1	Y1	GND	H17	GND	N21
CLK125	AA5	GND	H21	GND	P10
CLK50	C21	GND	J10	GND	P12
GND	B6	GND	J15	GND	P13
GND	B10	GND	J23	GND	P15
GND	B15	GND	K2	GND	R2
GND	B19	GND	K6	GND	R6
GND	C4	GND	K9	GND	R9
GND	D4	GND	K11	GND	R11
GND	D5	GND	K14	GND	R14
GND	D8	GND	K16	GND	R16
GND	D12	GND	K19	GND	R19
GND	D13	GND	K23	GND	R23
GND	D17	GND	L10	GND	T10
GND	D21	GND	L12	GND	T15
GND	D22	GND	L13	GND	U4
GND	D24	GND	L15	GND	U8
GND	E1	GND	M4	GND	U12
GND	F2	GND	M8	GND	U13
GND	F6	GND	M11	GND	U17
GND	F10	GND	M14	GND	U21
GND	F15	GND	M17	GND	V3
GND	F19	GND	M21	GND	W2
GND	F23	GND	N4	GND	W3
GND	H4	GND	N8	GND	W6
GND	H8	GND	N11	GND	W10

Signal	Ball
GND	W15
GND	W19
GND	W23
GND	Y2
GND	Y3
GND	Y15
GND	AA1
GND	AA4
GND	AA8
GND	AA12
GND	AA13
GND	AA17
GND	AA21
GND	AC6
GND	AC10
GND	AC15
GND	AC19
GND	U22
GND	U20
GND	T24
GND	V24
GND	AB14
GND	AD14
GND	AC16
GND	AD15
GND	V4
GND	Y5
GND	T22
GND	T20
GND	U24
GND	W24
GND	AB13
GND	AD13
GND	AB16
GND	AD16
GND	V5
GND	Y6
LED_CLK	A19
LED_DATA	A20

Signal	Ball
LED_LATCH	K18
MDC	H22
MDIO	J22
NC	P7
NC	P18
NC	V6
NC	V11
NC	V14
NC	V18
NC	N3
NC	N22
NC	P3
NC	P22
NC	V10
NC	V15
NC	L19
NC	G22
NC	G23
NC	J24
NC	F22
NC	E23
NC	H24
NC	G20
NC	E22
NC	G24
NC	F24
NC	G15
NC	A5
NC	A6
NC	C10
NC	C15
NC	G7
NC	G8
NC	K7
NC	M7
NC	N7
NC	P5
NC	P6
NC	P19

Signal	Ball
NC	P20
NC	R18
NC	T1
NC	U1
NC	V1
NC	V8
NC	V19
NC	W1
NC	Y14
NC	AB3
NC	AB5
NC	AB20
NC	AB22
NC	AD7
NC	AD8
NC	AD17
NC	B14
NC	B11
NC	V21
NC	Y20
NC	W22
NC	Y22
NC	AB11
NC	AD11
NC	AC9
NC	AD10
NC	U3
NC	U5
NC	V20
NC	Y19
NC	V22
NC	Y23
NC	AB12
NC	AD12
NC	AB9
NC	AD9
NC	T3
NC	T5
No Ball	A2

Signal	Ball
No Ball	A3
No Ball	A22
No Ball	A23
No Ball	A24
No Ball	B1
No Ball	B2
No Ball	B23
No Ball	B24
No Ball	C1
No Ball	C24
No Ball	AB1
No Ball	AB24
No Ball	AC1
No Ball	AC2
No Ball	AC23
No Ball	AC24
No Ball	AD1
No Ball	AD2
No Ball	AD3
No Ball	AD22
No Ball	AD23
No Ball	AD24
No Pad	A1
RCTL_N	H18
RCTL_P	H16
RD0_0	K22
RD0_1	M22
RD0_2	AC22
RD0_3	U18
RD0_4	U14
RD0_5	AA18
RD0_6	U9
RD0_7	AA9
RD0_8	V7
RD0_9	L4
RD1_0	K24
RD1_1	P24
RD1_2	AD21
RD1_3	T19

Signal	Ball
RD1_4	Y16
RD1_5	Y13
RD1_6	L6
RD1_7	AC7
RD1_8	U7
RD1_9	M3
RD2_0	K20
RD2_1	T21
RD2_2	AC20
RD2_3	T17
RD2_4	V16
RD2_5	AB10
RD2_6	T9
RD2_7	AB7
RD2_8	T7
RD2_9	P1
RD3_0	M18
RD3_1	P23
RD3_2	AB21
RD3_3	U16
RD3_4	V13
RD3_5	Y12
RD3_6	V2
RD3_7	Y8
RD3_8	W5
RD3_9	R3
RDAT0_N	E20
RDAT0_P	E19
RDAT1_N	C20
RDAT1_P	B20
RDAT2_N	G19
RDAT2_P	F18
RDAT3_N	H20
RDAT3_P	G21
RDAT4_N	J19
RDAT4_P	J18
RDAT5_N	L18
RDAT5_P	L17
RDAT6_N	E17

Signal	Ball
RDAT6_P	E16
RDAT7_N	N15
RDAT7_P	M15
RDAT8_N	D16
RDAT8_P	C16
RDAT9_N	E18
RDAT9_P	D18
RDAT10_N	G18
RDAT10_P	G17
RDAT11_N	K15
RDAT11_P	J16
RDAT12_N	A14
RDAT12_P	A13
RDAT13_N	E14
RDAT13_P	E13
RDAT14_N	G16
RDAT14_P	F16
RDAT15_N	K13
RDAT15_P	K12
RDCLK_N	C19
RDCLK_P	C18
RSCLK	J17
RSTAT0	L20
RSTAT1	J20
RX_CTL_0	L24
RX_CTL_1	R24
RX_CTL_2	W20
RX_CTL_3	T18
RX_CTL_4	AA14
RX_CTL_5	AC11
RX_CTL_6	T8
RX_CTL_7	AA7
RX_CTL_8	AA3
RX_CTL_9	L3
RXC_0	J21
RXC_1	T23
RXC_2	AB23
RXC_3	P21
RXC_4	Y18

Signal	Ball
RXC_5	AB17
RXC_6	R10
RXC_7	W7
RXC_8	AB6
RXC_9	R1
SYS_RES_L	Y4
TCK	AA24
TCTL_N	N10
TCTL_P	M10
TD0_0	L23
TD0_1	P17
TD0_2	AB18
TD0_3	AA22
TD0_4	W18
TD0_5	Y10
TD0_6	Y7
TD0_7	AD5
TD0_8	T6
TD0_9	P4
TD1_0	M24
TD1_1	V23
TD1_2	Y17
TD1_3	R15
TD1_4	W14
TD1_5	W11
TD1_6	W9
TD1_7	AC5
TD1_8	P8
TD1_9	L2
TD2_0	L21
TD2_1	N20
TD2_2	AD19
TD2_3	R13
TD2_4	AA20
TD2_5	V9
TD2_6	AB8
TD2_7	AD4
TD2_8	R5
TD2_9	M1

Signal	Ball
TD3_0	L22
TD3_1	V17
TD3_2	AD18
TD3_3	R12
TD3_4	AB15
TD3_5	V12
TD3_6	Y9
TD3_7	AC3
TD3_8	T2
TD3_9	P2
TDAT0_N	J5
TDAT0_P	J6
TDAT1_N	J3
TDAT1_P	H3
TDAT2_P	B5
TDAT3_N	H9
TDAT3_P	G9
TDAT4_N	G6
TDAT4_P	F7
TDAT5_N	H5
TDAT5_P	G5
TDAT6_N	L7
TDAT6_P	L8
TDAT7_N	C6
TDAT7_P	C7
TDAT8_N	M5
TDAT8_P	L5
TDAT9_N	C8
TDAT9_P	B7
TDAT10_N	F9
TDAT10_P	E9
TDAT11_N	E7
TDAT11_P	E8
TDAT12_N	J8
TDAT12_P	H7
TDAT13_N	K10
TDAT13_P	J9
TDAT14_N	D9
TDAT14_P	C9

Signal	Ball
TDAT15_N	H11
TDAT15_P	G11
TDAT2_N	C5
TDCLK-	E4
TDCLK_P	D3
TDI	AC18
TDO	Y24
TMS	T16
TRST_L	N18
TSCLK	C11
TSTAT0	E5
TSTAT1	E6
TX_CTL_0	N24
TX_CTL_1	Y21
TX_CTL_2	AA16
TX_CTL_3	M20
TX_CTL_4	AC14
TX_CTL_5	U11
TX_CTL_6	T4
TX_CTL_7	AB2
TX_CTL_8	R7
TX_CTL_9	L1
TXC_0	R22
TXC_1	R20
TXC_2	AD20
TXC_3	AB19
TXC_4	W16
TXC_5	AA11
TXC_6	Y11
TXC_7	AD6
TXC_8	N5
TXC_9	N1
TXPAUSEADD0	G3
TXPAUSEADD1	G2
TXPAUSEADD2	J2
TXPAUSEADD3	K1
TXPAUSEFR	J7
UPX_ADD0	J1
UPX_ADD2	F3

Signal	Ball
UPX_ADD3	H1
UPX_ADD4	E3
UPX_ADD5	E2
UPX_ADD6	G1
UPX_ADD7	C3
UPX_ADD8	F5
UPX_ADD9	F1
UPX_ADD1	G4
UPX_ADD10	C2
UPX_CS_L	F20
UPX_DATA0	B3
UPX_DATA1	A4
UPX_DATA2	B9
UPX_DATA3	A7
UPX_DATA4	C12
UPX_DATA5	E11
UPX_DATA6	C13
UPX_DATA7	A8
UPX_DATA8	A10
UPX_DATA9	A9
UPX_DATA10	E12
UPX_DATA11	A11
UPX_DATA12	G12
UPX_DATA13	E10
UPX_DATA14	F11
UPX_DATA15	D7
UPX_DATA16	D14
UPX_DATA17	C14
UPX_DATA18	F14
UPX_DATA19	A12
UPX_DATA20	A15
UPX_DATA21	G13
UPX_DATA22	B16
UPX_DATA23	E15
UPX_DATA24	G14
UPX_DATA25	A16
UPX_DATA26	C17
UPX_DATA27	A17
UPX_DATA28	B18

Signal	Ball
UPX_DATA29	A21
UPX_DATA30	B22
UPX_DATA31	C23
UPX_RD_L	H14
UPX_RDY_L	C22
UPX_WR_L	A18
VDD	D6
VDD	D10
VDD	D11
VDD	D15
VDD	D19
VDD	D20
VDD	E21
VDD	F4
VDD	F21
VDD	H10
VDD	H15
VDD	J4
VDD	J11
VDD	J14
VDD	K3
VDD	K4
VDD	K5
VDD	K8
VDD	K17
VDD	K21
VDD	L9
VDD	L11
VDD	L14
VDD	L16
VDD	P9
VDD	P11
VDD	P14
VDD	P16
VDD	R4
VDD	R8
VDD	R17
VDD	R21
VDD	T11

Signal	Ball
VDD	T14
VDD	U10
VDD	U15
VDD	W4
VDD	W21
VDD	AA6
VDD	AA10
VDD	AA15
VDD	AA19
VDD	AB4
VDD2	G10
VDD2	B4
VDD2	B8
VDD2	B12
VDD2	B13
VDD2	B17
VDD2	B21
VDD2	D2
VDD2	D23
VDD2	F8
VDD2	F12
VDD2	F13
VDD2	F17
VDD2	H2
VDD2	H6
VDD2	H19
VDD2	H23
VDD2	J12
VDD2	J13
VDD2	M2
VDD2	M6
VDD2	M9
VDD2	M12
VDD2	M13
VDD2	M16
VDD2	M19
VDD2	M23
VDD2	N2
VDD2	N6

Signal	Ball
VDD2	N9
VDD2	N12
VDD2	N13
VDD2	N16
VDD2	N19
VDD2	N23
VDD2	T12
VDD2	T13
VDD2	U2
VDD2	U6
VDD2	U19
VDD2	U23
VDD2	W8
VDD2	W12
VDD2	W13
VDD2	W17
VDD2	AA2
VDD2	AA23
VDD2	AC4
VDD2	AC8
VDD2	AC12
VDD2	AC13
VDD2	AC17
VDD2	AC21

4.3.2 Balls Listed in Alphanumeric Order by Ball Location

Table 12 shows the ball locations and signal names arranged in alphanumeric order by ball location.

Note: Cortina recommends that all unconnected balls be tied to their inactive states through external pull-ups or pull-downs.

Table 12 Ball List in Alphanumeric Order by Ball Location

Ball	Signal
A1	No Pad
A2	No Ball
A3	No Ball
A4	UPX_DATA1
A5	NC
A6	NC

Ball	Signal
A7	UPX_DATA3
A8	UPX_DATA7
A9	UPX_DATA9
A10	UPX_DATA8
A11	UPX_DATA11
A12	UPX_DATA19

Ball	Signal
A13	RDAT12_P
A14	RDAT12_N
A15	UPX_DATA20
A16	UPX_DATA25
A17	UPX_DATA27
A18	UPX_WR_L

Ball	Signal
A19	LED_CLK
A20	LED_DATA
A21	UPX_DATA29
A22	No Ball
A23	No Ball
A24	No Ball
B1	No Ball
B2	No Ball
B3	UPX_DATA0
B4	VDD2
B5	TDAT2_P
B6	GND
B7	TDAT9_P
B8	VDD2
B9	UPX_DATA2
B10	GND
B11	NC
B12	VDD2
B13	VDD2
B14	NC
B15	GND
B16	UPX_DATA22
B17	VDD2
B18	UPX_DATA28
B19	GND
B20	RDAT1_P
B21	VDD2
B22	UPX_DATA30
B23	No Ball
B24	No Ball
C1	No Ball
C2	UPX_ADD10
C3	UPX_ADD7
C4	GND
C5	TDAT2_N
C6	TDAT7_N
C7	TDAT7_P
C8	TDAT9_N
C9	TDAT14_P

Ball	Signal
C10	NC
C11	TSCLK
C12	UPX_DATA4
C13	UPX_DATA6
C14	UPX_DATA17
C15	NC
C16	RDAT8_P
C17	UPX_DATA26
C18	RDCLK_P
C19	RDCLK_N
C20	RDAT1_N
C21	CLK50
C22	UPX_RDY_L
C23	UPX_DATA31
C24	No Ball
D1	AVDD1P8_1
D2	VDD2
D3	TDCLK_P
D4	GND
D5	GND
D6	VDD
D7	UPX_DATA15
D8	GND
D9	TDAT14_N
D10	VDD
D11	VDD
D12	GND
D13	GND
D14	UPX_DATA16
D15	VDD
D16	RDAT8_N
D17	GND
D18	RDAT9_P
D19	VDD
D20	VDD
D21	GND
D22	GND
D23	VDD2
D24	GND

Ball	Signal
E1	GND
E2	UPX_ADD5
E3	UPX_ADD4
E4	TDCLK-
E5	TSTAT0
E6	TSTAT1
E7	TDAT11_N
E8	TDAT11_P
E9	TDAT10_P
E10	UPX_DATA13
E11	UPX_DATA5
E12	UPX_DATA10
E13	RDAT13_P
E14	RDAT13_N
E15	UPX_DATA23
E16	RDAT6_P
E17	RDAT6_N
E18	RDAT9_N
E19	RDAT0_P
E20	RDAT0_N
E21	VDD
E22	NC
E23	NC
E24	AVDD1P8_1
F1	UPX_ADD9
F2	GND
F3	UPX_ADD2
F4	VDD
F5	UPX_ADD8
F6	GND
F7	TDAT4_P
F8	VDD2
F9	TDAT10_N
F10	GND
F11	UPX_DATA14
F12	VDD2
F13	VDD2
F14	UPX_DATA18
F15	GND

Ball	Signal
F16	RDAT14_P
F17	VDD2
F18	RDAT2_P
F19	GND
F20	UPX_CS_L
F21	VDD
F22	NC
F23	GND
F24	NC
G1	UPX_ADD6
G2	TXPAUSEADD1
G3	TXPAUSEADD0
G4	UPX_ADD1
G5	TDAT5_P
G6	TDAT4_N
G7	NC
G8	NC
G9	TDAT3_P
G10	VDD2
G11	TDAT15_P
G12	UPX_DATA12
G13	UPX_DATA21
G14	UPX_DATA24
G15	NC
G16	RDAT14_N
G17	RDAT10_P
G18	RDAT10_N
G19	RDAT2_N
G20	NC
G21	RDAT3_P
G22	NC
G23	NC
G24	NC
H1	UPX_ADD3
H2	VDD2
H3	TDAT1_P
H4	GND
H5	TDAT5_N
H6	VDD2

Ball	Signal
H7	TDAT12_P
H8	GND
H9	TDAT3_N
H10	VDD
H11	TDAT15_N
H12	GND
H13	GND
H14	UPX_RD_L
H15	VDD
H16	RCTL_P
H17	GND
H18	RCTL_N
H19	VDD2
H20	RDAT3_N
H21	GND
H22	MDC
H23	VDD2
H24	NC
J1	UPX_ADD0
J2	TXPAUSEADD2
J3	TDAT1_N
J4	VDD
J5	TDAT0_N
J6	TDAT0_P
J7	TXPAUSEFR
J8	TDAT12_N
J9	TDAT13_P
J10	GND
J11	VDD
J12	VDD2
J13	VDD2
J14	VDD
J15	GND
J16	RDAT11_P
J17	RSCLK
J18	RDAT4_P
J19	RDAT4_N
J20	RSTAT1
J21	RXC_0

Ball	Signal
J22	MDIO
J23	GND
J24	NC
K1	TXPAUSEADD3
K2	GND
K3	VDD
K4	VDD
K5	VDD
K6	GND
K7	NC
K8	VDD
K9	GND
K10	TDAT13_N
K11	GND
K12	RDAT15_P
K13	RDAT15_N
K14	GND
K15	RDAT11_N
K16	GND
K17	VDD
K18	LED_LATCH
K19	GND
K20	RD2_0
K21	VDD
K22	RD0_0
K23	GND
K24	RD1_0
L1	TX_CTL_9
L2	TD1_9
L3	RX_CTL_9
L4	RD0_9
L5	TDAT8_P
L6	RD1_6
L7	TDAT6_N
L8	TDAT6_P
L9	VDD
L10	GND
L11	VDD
L12	GND

Ball	Signal
L13	GND
L14	VDD
L15	GND
L16	VDD
L17	RDAT5_P
L18	RDAT5_N
L19	NC
L20	RSTAT0
L21	TD2_0
L22	TD3_0
L23	TD0_0
L24	RX_CTL_0
M1	TD2_9
M2	VDD2
M3	RD1_9
M4	GND
M5	TDAT8_N
M6	VDD2
M7	NC
M8	GND
M9	VDD2
M10	TCTL_P
M11	GND
M12	VDD2
M13	VDD2
M14	GND
M15	RDAT7_P
M16	VDD2
M17	GND
M18	RD3_0
M19	VDD2
M20	TX_CTL_3
M21	GND
M22	RD0_1
M23	VDD2
M24	TD1_0
N1	TXC_9
N2	VDD2
N3	NC

Ball	Signal
N4	GND
N5	TXC_8
N6	VDD2
N7	NC
N8	GND
N9	VDD2
N10	TCTL_N
N11	GND
N12	VDD2
N13	VDD2
N14	GND
N15	RDAT7_N
N16	VDD2
N17	GND
N18	TRST_L
N19	VDD2
N20	TD2_1
N21	GND
N22	NC
N23	VDD2
N24	TX_CTL_0
P1	RD2_9
P2	TD3_9
P3	NC
P4	TD0_9
P5	NC
P6	NC
P7	NC
P8	TD1_8
P9	VDD
P10	GND
P11	VDD
P12	GND
P13	GND
P14	VDD
P15	GND
P16	VDD
P17	TD0_1
P18	NC

Ball	Signal
P19	NC
P20	NC
P21	RXC_3
P22	NC
P23	RD3_1
P24	RD1_1
R1	RXC_9
R2	GND
R3	RD3_9
R4	VDD
R5	TD2_8
R6	GND
R7	TX_CTL_8
R8	VDD
R9	GND
R10	RXC_6
R11	GND
R12	TD3_3
R13	TD2_3
R14	GND
R15	TD1_3
R16	GND
R17	VDD
R18	NC
R19	GND
R20	TXC_1
R21	VDD
R22	TXC_0
R23	GND
R24	RX_CTL_1
T1	NC
T2	TD3_8
T3	NC
T4	TX_CTL_6
T5	NC
T6	TD0_8
T7	RD2_8
T8	RX_CTL_6
T9	RD2_6

Ball	Signal
T10	GND
T11	VDD
T12	VDD2
T13	VDD2
T14	VDD
T15	GND
T16	TMS
T17	RD2_3
T18	RX_CTL_3
T19	RD1_3
T20	GND
T21	RD2_1
T22	GND
T23	RXC_1
T24	GND
U1	NC
U2	VDD2
U3	NC
U4	GND
U5	NC
U6	VDD2
U7	RD1_8
U8	GND
U9	RD0_6
U10	VDD
U11	TX_CTL_5
U12	GND
U13	GND
U14	RD0_4
U15	VDD
U16	RD3_3
U17	GND
U18	RD0_3
U19	VDD2
U20	GND
U21	GND
U22	GND
U23	VDD2
U24	GND

Ball	Signal
V1	NC
V2	RD3_6
V3	GND
V4	GND
V5	GND
V6	NC
V7	RD0_8
V8	NC
V9	TD2_5
V10	NC
V11	NC
V12	TD3_5
V13	RD3_4
V14	NC
V15	NC
V16	RD2_4
V17	TD3_1
V18	NC
V19	NC
V20	NC
V21	NC
V22	NC
V23	TD1_1
V24	GND
W1	NC
W2	GND
W3	GND
W4	VDD
W5	RD3_8
W6	GND
W7	RXC_7
W8	VDD2
W9	TD1_6
W10	GND
W11	TD1_5
W12	VDD2
W13	VDD2
W14	TD1_4
W15	GND

Ball	Signal
W16	TXC_4
W17	VDD2
W18	TD0_4
W19	GND
W20	RX_CTL_2
W21	VDD
W22	NC
W23	GND
W24	GND
Y1	AVDD2P5_1
Y2	GND
Y3	GND
Y4	SYS_RES_L
Y5	GND
Y6	GND
Y7	TD0_6
Y8	RD3_7
Y9	TD3_6
Y10	TD0_5
Y11	TXC_6
Y12	RD3_5
Y13	RD1_5
Y14	NC
Y15	GND
Y16	RD1_4
Y17	TD1_2
Y18	RXC_4
Y19	NC
Y20	NC
Y21	T X_CTL_1
Y22	NC
Y23	NC
Y24	TDO
AA1	GND
AA2	VDD2
AA3	RX_CTL_8
AA4	GND
AA5	CLK125
AA6	VDD

Ball	Signal
AA7	RX_CTL_7
AA8	GND
AA9	RD0_7
AA10	VDD
AA11	TXC_5
AA12	GND
AA13	GND
AA14	RX_CTL_4
AA15	VDD
AA16	T X_CTL_2
AA17	GND
AA18	RD0_5
AA19	VDD
AA20	TD2_4
AA21	GND
AA22	TD0_3
AA23	VDD2
AA24	TCK
AB1	No Ball
AB2	TX_CTL_7
AB3	NC
AB4	VDD
AB5	NC
AB6	RXC_8
AB7	RD2_7
AB8	TD2_6
AB9	NC
AB10	RD2_5
AB11	NC
AB12	NC
AB13	GND
AB14	GND
AB15	TD3_4
AB16	GND
AB17	RXC_5
AB18	TD0_2
AB19	TXC_3
AB20	NC
AB21	RD3_2

Ball	Signal
AB22	NC
AB23	RXC_2
AB24	No Ball
AC1	No Ball
AC2	No Ball
AC3	TD3_7
AC4	VDD2
AC5	TD1_7
AC6	GND
AC7	RD1_7
AC8	VDD2
AC9	NC
AC10	GND
AC11	RX_CTL_5
AC12	VDD2
AC13	VDD2
AC14	TX_CTL_4
AC15	GND
AC16	GND
AC17	VDD2
AC18	TDI
AC19	GND
AC20	RD2_2
AC21	VDD2
AC22	RD0_2
AC23	No Ball
AC24	No Ball
AD1	No Ball
AD2	No Ball
AD3	No Ball
AD4	TD2_7
AD5	TD0_7
AD6	TXC_7
AD7	NC
AD8	NC
AD9	NC
AD10	NC
AD11	NC
AD12	NC

Ball	Signal
AD13	GND
AD14	GND
AD15	GND
AD16	GND
AD17	NC
AD18	TD3_2
AD19	TD2_2
AD20	TXC_2
AD21	RD1_2
AD22	No Ball
AD23	No Ball
AD24	No Ball

5.0 Functional Description

5.1 Media Access Controller

5.1.1 General Description

The IXF1010 MAC main functional block consists of a 100/1000 Mbps Ethernet Media Access Controller (MAC), supporting the following features:

- 100/1000 Mbps full-duplex operation
- Independent enable/disable of any port
- Detection of length error, runt, or overly large packets
- RMON statistics and error counters
- Cyclic Redundancy Check (CRC) calculation and error detection
- Programmable options:
  - Filter packets with errors
  - Filter, broadcast, multicast, and unicast address packets
  - Automatically pad transmitted packets less than the minimum frame size
- Compliance with IEEE 802.3x Standard for Flow Control (symmetric pause capability)
- Full compliance with the HP version 1.2a Reduced Gigabit Media Independent Interface (RGMII)

The MAC is fully integrated, designed for use with Ethernet 802.3 Frame types, and is compliant with all of the required IEEE 802.3 MAC requirements.

The MAC adds preamble and Start-of-Frame Delimiter (SFD) to all frames sent to it (transmit path) and removes preamble and SFD on all frames received by it (receive path). A CRC check is also applied to all transmit and receive packets. Packets with a bad CRC are marked, counted in the statistics block, and may be optionally dropped or sent to the SPI4-2 interface.

Note: The MAC operates in full-duplex mode only. The PHYs attached to the IXF1010 MAC must advertise full-duplex mode during any auto-negotiation process.

5.1.2 MAC Functions

Section 5.1.2.1, *Padding of Undersized Frames on Transmit*, on page 40 through Section 5.1.2.3, *Filtering of Receive Packets*, on page 41 cover the MAC functions.

5.1.2.1 Padding of Undersized Frames on Transmit

The padding feature allows Ethernet frames smaller than 64 bytes to be transferred across the SPI4-2 interface and automatically padded up to 64 bytes by the MAC. This feature is enabled by setting bit 7 of the *Diverse Config ($ Port_Index + 0x18)*, on page 120.

Note: If frames under 64 bytes are sent to the MAC, the padding feature must be enabled for proper operation. A 9-byte packet is the minimum size packet that can be padded up to 64 bytes. Packets under 9 bytes are not padded and are automatically dropped.

5.1.2.2 Automatic CRC Generation

The Automatic CRC Generation is used in conjunction with the padding feature to generate and append a correct CRC to any incoming frame from the SPI4-2 interface. This feature is enabled by setting bit 6 of the *Diverse Config ($ Port_Index + 0x18)*, on page 120.

Note: When padding of undersized frames on transmit is enabled, the automatic CRC generation must be enabled for proper operation of the IXF1010 MAC.

5.1.2.3 Filtering of Receive Packets

This feature allows the MAC to filter receive packets under various conditions and drop the packets via an interaction with the Receive FIFO control.

Note: Jumbo frames (1519 - 9600 bytes) matching the filter conditions, which would cause the frame to be dropped by the RX FIFO, are not dropped. Instead, jumbo frames that are expected to be dropped by the RX FIFO, based on the filter settings in the *RX Packet Filter Control ($ Port_Index + 0x19)*, on page 121, are sent across the SPI4-2 interface as an EOP abort frame. Jumbo frames matching the filter conditions are not counted in the RX FIFO Number of Frames Removed Register because they are not removed by the RX FIFO. Only standard packet sizes (64 - 1518 bytes) meeting the filter conditions set in the *RX Packet Filter Control ($ Port_Index + 0x19)*, on page 121 are actually dropped by the RX FIFO and counted in the RX FIFO Number of Frames Removed.

5.1.2.3.1 Filter on Unicast Packet Match

This feature is enabled when bit 0 of the RX Packet Filter Control Register = 1. Any frame received in this mode containing a Unicast Destination Address that does not match the Station Address is marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable Register = 1. Otherwise, all unicast frames are sent to the SPI4-2 interface, but with an EOP Abort code to the switch or Network Processor.

Note: The VLAN filter overrides the unicast filter. Thus, a VLAN frame cannot be filtered based on the unicast address.

5.1.2.3.2 Filter on Multicast Packet Match

This feature is enabled when bit 1 of the RX Packet Filter Control Register = 1. Any frame received in this mode containing a Multicast Destination Address which does not match the Port Multicast Address is marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable register = 1. Otherwise, all multicast frames are sent to the SPI4-2 interface, but with an EOP Abort code to the switch or Network Processor.

5.1.2.3.3 Filter Broadcast Packets

This feature is enabled when bit 2 of the *RX Packet Filter Control ($ Port_Index + 0x19)* = 1. Any broadcast frame received in this mode is marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable Register = 1. Otherwise, all broadcast frames are sent to the SPI4-2 interface, but with an EOP Abort code to the switch or Network Processor.

5.1.2.3.4 Filter VLAN Packets

This feature is enabled when bit 3 of the *RX Packet Filter Control ($ Port_Index + 0x19)* = 1. VLAN frames received in this mode are marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable Register = 1. Otherwise, all VLAN frames are sent to the SPI4-2 interface, but with an EOP Abort code to the switch or Network Processor.

5.1.2.3.5 Filter PAUSE Packets

This feature is enabled when bit 4 of the *RX Packet Filter Control ($ Port_Index + 0x19)* = 0. PAUSE frames received in this mode are marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the *RX FIFO Errored Frame Drop Enable ($ 0x59F)* = 1. Otherwise, all PAUSE frames are sent to the SPI4-2 interface.

Table 13 Pause Packets Drop Enable Behavior

Pause Frame Pass	Frame Drop En	Actions
1	0	Packets are passed to the SPI4-2 interface. They are not marked as bad and are sent to the switch or Network Processor.
0	0	Packets are marked as bad but not dropped in the RX FIFO. These packets are sent to the SPI4-2 interface, but with an EOP Abort code to the switch or Network Processor.
1	1	Packets are not marked as bad and sent to the switch or Network Processor, regardless of the Frame Drop En setting.
0	1	PAUSE Packets are marked as bad, are dropped in the RX FIFO, and never appear at the SPI4-2 interface.

5.1.2.3.6 Filter CRC Errored Packets

This feature is enabled when bit 5 of the *RX Packet Filter Control ($ Port_Index + 0x19)* = 0. Frames received with an errored CRC are marked as bad frames and may optionally be dropped in the RX FIFO. Otherwise, the frames are sent to the SPI4-2 interface and may be dropped by the switch or system controller (see *CRC Errored Packets Drop Enable Behavior*, on page 42).

Note: When the CRC Error Pass Filter bit = 0 (*RX Packet Filter Control ($ Port_Index + 0x19)*, on page 121), it takes precedence over the other filter bits. Any packet (Pause, Unicast, Multicast or Broadcast packet) with a CRC error will be marked as a bad frame when the CRC Error Pass Filter bit = 0.

Table 14 CRC Errored Packets Drop Enable Behavior (Sheet 1 of 2)

CRC Errored PASS	Frame Drop En	Actions
1	0	Packets are passed to the SPI4-2 interface. They are not marked as bad and are sent to the switch or Network Processor.

Table 14 CRC Errored Packets Drop Enable Behavior (Sheet 2 of 2)

CRC Errored PASS	Frame Drop En	Actions
0	0	Packets are marked as bad but not dropped in the RX FIFO. These packets are sent to the SPI4-2 interface, but with an EOP Abort code to the switch or Network Processor.
1	1	Packets are not marked as bad and are sent to the switch or Network Processor regardless of the Frame Drop En setting.
0	1	CRC errored packets are marked as bad, dropped in the RX FIFO, and never appear at the SPI4-2 interface.

5.1.3 Flow Control

Flow Control is an IEEE 802.3x-defined mechanism for one network node to request that its link partner take a temporary “Pause” in packet transmission. This allows the requesting network node to prevent FIFO overruns and dropped packets, by managing incoming traffic to fit its available memory. The temporary pause allows the device to process packets already received or in transit, thus freeing up the FIFO space allocated to those packets.

The IXF1010 MAC implements the IEEE 802.3x standard RX FIFO threshold-based Flow Control. When appropriately programmed, the MAC can both generate and respond to IEEE standard pause frames. The IXF1010 MAC also supports externally triggered flow control through the Transmit Pause Control interface.

5.1.3.1 802.3x Flow Control (Full-Duplex Operation)

The IEEE 802.3x standard identifies four options related to system flow control:

- No Pause
- Symmetric Pause (both directions)
- Asymmetric Pause (Receive direction only)
- Asymmetric Pause (Transmit direction only)

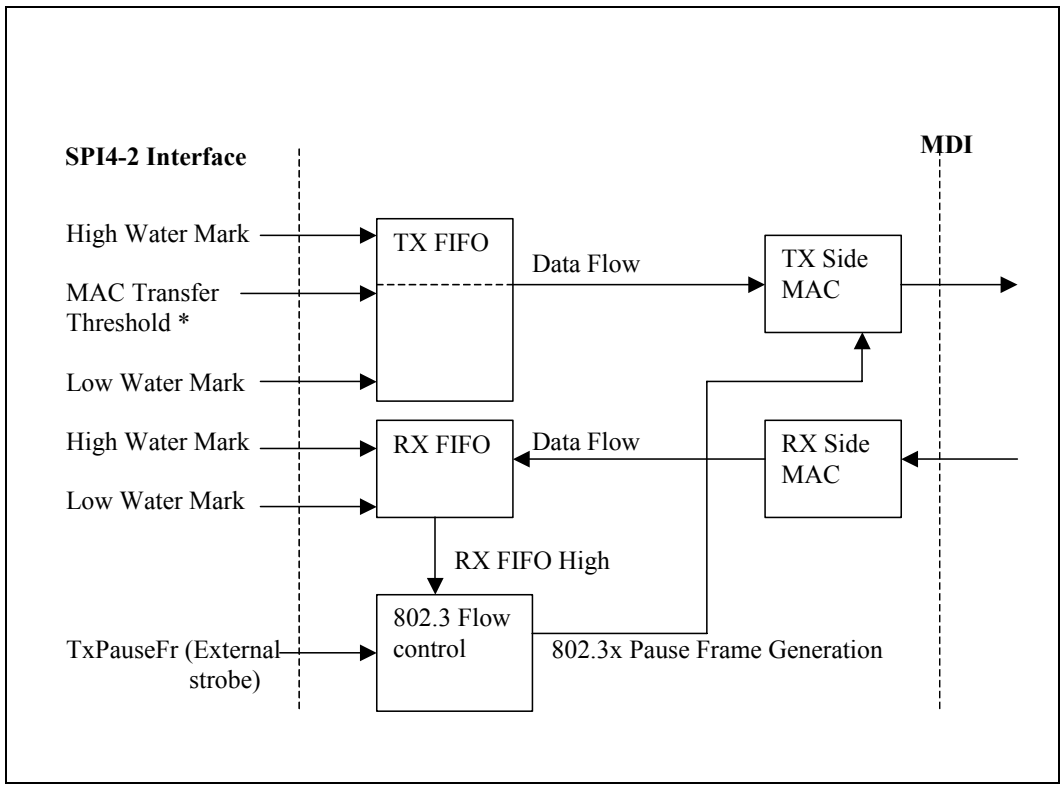
The IXF1010 MAC supports all four options on a per-port basis. Bits 1:0 of the *FC Enable ($ Port_Index + 0x12)*, on page 119 provide programmable control for enabling or disabling flow control in each direction independently.

The IEEE 802.3x flow control mechanism is accomplished within the MAC sublayer, and is based on RX FIFO thresholds called watermarks. The RX FIFO level rises and falls as packets are received and processed. When the RX FIFO reaches a watermark (either exceeding a High or dropping below a Low after exceeding a High), the IXF1010 MAC control sublayer signals an internal state machine to transmit a PAUSE frame. The FIFOs automatically generate PAUSE frames (also called control frames) to initiate the following:

- Halt the link partner when the High watermark is reached.
- Restart the link partner when the data stored in the FIFO falls below the Low watermark.

Figure 5 illustrates the IEEE 802.3 FIFO flow control functions.

Figure 5 Packet Buffering FIFO



5.1.3.1.1 Pause Frame Format

PAUSE frames are MAC control frames that are padded to the minimum size (64 bytes). Figure 6 and Figure 6 illustrate the frame format and contents.

Figure 6 Ethernet Frame Format

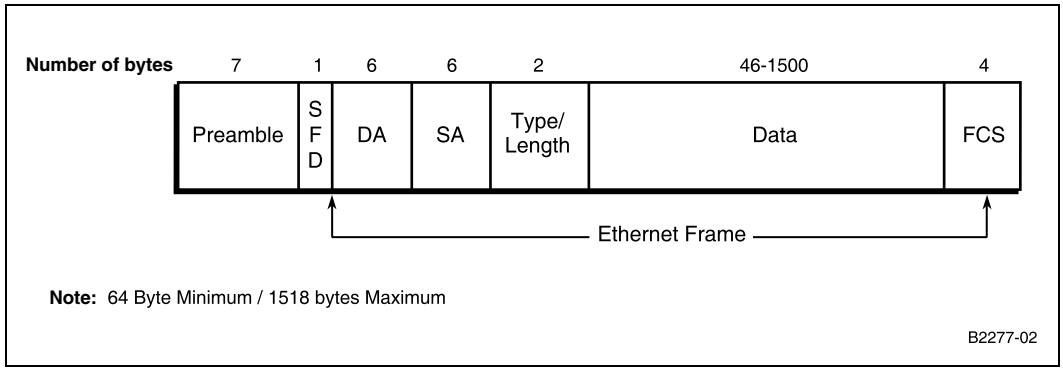
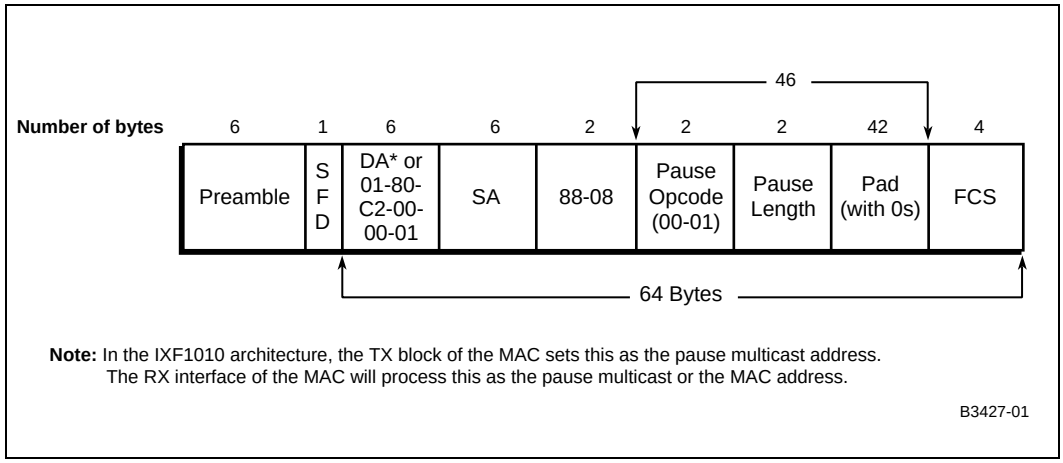


Figure 7 PAUSE Frame Format



An IEEE 802.3 MAC PAUSE frame is identified by detecting all of the following:

- OpCode of 00-01
- Length/Type field of 88-08
- DA matching the unique multicast address (01-80-C2-00-00-01)

XOFF. A PAUSE frame informs the link partner to halt transmission for a specified length of time. The PauseLength octets specify the duration of the no-transmit period. If this time is greater than zero, the link partner must stop sending any further packets until this time has elapsed. This is referred to as XOFF.

XON. The MAC continues to transmit PAUSE frames with the specified Pause Length as long as the FIFO level exceeds the threshold. If the FIFO level falls below the threshold before the Pause Length time expires, the MAC sends another PAUSE frame with the Pause Length time specified as zero. This is referred to as XON and informs the link partner to resume normal transmission of packets.

5.1.3.1.2 Pause Settings

The MAC must send PAUSE frames repeatedly to maintain the link partner in a Pause state. The following two inter-related variables control this process:

- Pause Length is the amount of time, measured in multiples of 512 bit times, that the MAC requests the link partner to halt transmission for.
- Pause Threshold is the amount of time, measured in multiples of 512 bit times, prior to the expiration of the Pause Length that the MAC transmits another Pause frame to maintain the link partner in the pause state.

The transmitted Pause Length in the IXF1010 MAC is set by the *FC TX Timer Value ($ Port_Index + 0x07)*, on page 117.

The IXF1010 MAC PAUSE frame transmission interval is set by the *Pause Threshold ($ Port_Index + 0x0E)*, on page 118.

5.1.3.1.3 Response to Received PAUSE Command Frames

When Flow Control is enabled in the receive direction (bit 0 in the *FC Enable ($ Port_Index + 0x12)*, on page 119), the IXF1010 MAC responds to PAUSE Command frames received from the link partner as follows:

1. The IXF1010 MAC checks the entire frame to verify that it is a valid PAUSE control frame addressed to the Multicast Address 01-80-C2-00-00-01 (as specified in IEEE 802.3, Annex 31B) or has a Destinations Address matching the address programmed in the *Station Address Low ($ Port_Index + 0x00)*, on page 116 through *Station Address High ($ Port_Index + 0x01)*, on page 116.
2. If the PAUSE frame is valid, the transmit side of the IXF1010 MAC pauses for the required number of PAUSE Quanta, as specified in IEEE 802.3, Clause 31.
3. PAUSE does not begin until completion of the frame currently being transmitted.

The IXF1010 MAC response to valid received PAUSE frames is independent of the PAUSE frame filter settings. Refer to Section 5.1.2.3.5, *Filter PAUSE Packets*, on page 42 for additional details.

5.1.3.1.4 Transmit Pause Control Interface

The Transmit Pause Control interface allows an external device to trigger the generation of pause frames. The Transmit Pause Control interface is completely asynchronous. It consists of four address signals (TXPAUSEADD[3:0]) and a strobe signal (TXPAUSEFR). The required address for this interface operation is placed on the TXPAUSEADD[3:0] signals and the TXPAUSEFR is pulsed High and returned Low. Refer to Figure 8, *Transmit Pause Control Interface*, on page 47 and *Transmit Pause Control Interface Parameters*, on page 102. Table 15, *Valid Decodes for TXPAUSEADD[3:0]*, on page 46 shows the valid decodes for the TXPAUSEADD[3:0] signals. Figure 8, *Transmit Pause Control Interface*, on page 47 illustrates the transmit pause control interface.

Note: Flow control must be enabled in the *FC Enable ($ Port_Index + 0x12)*, on page 119 for Transmit Pause Control interface operation.

Note: There are two additional decodes provided that allow the user to generate either an XOFF frame or XON frame from all ports simultaneously.

The default pause quanta for each port is held by the *FC TX Timer Value ($ Port_Index + 0x07)*, on page 117). The default value of this register is 0x05E after reset is applied.

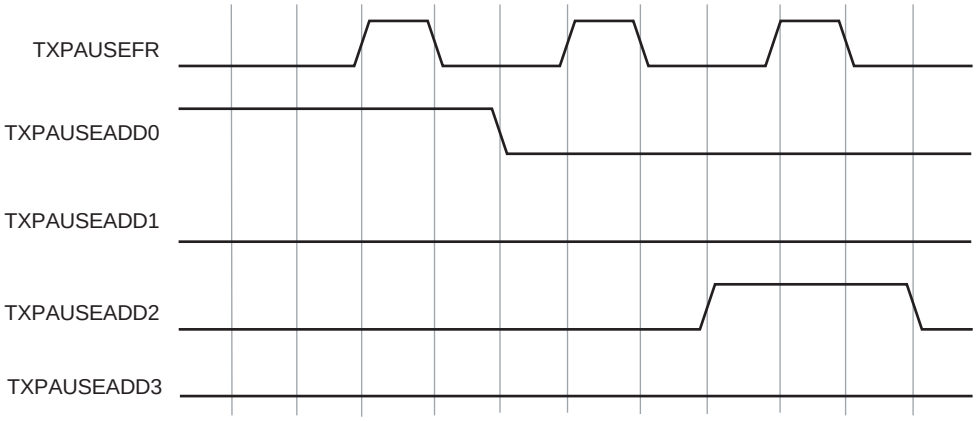
Table 15 Valid Decodes for TXPAUSEADD[3:0] (Sheet 1 of 2)

TXPAUSEADD[3:0]	TX Pause Control Interface Operation
0x0	Transmits a PAUSE frame on every port with a pause_time = ZERO (XON) (Cancels all previous pause commands).
0x1	Transmits a PAUSE frame on port 0 with pause_time equal to the value programmed in the port 0 *FC TX Timer Value ($ Port_Index + 0x07)* (XOFF).
0x2	Transmits a PAUSE frame on port 1 with pause_time equal to the value programmed in the port 1 *FC TX Timer Value ($ Port_Index + 0x07)* (XOFF).
0x3	Transmits a PAUSE frame on port 2 with pause_time equal to the value programmed in the port 2 *FC TX Timer Value ($ Port_Index + 0x07)* (XOFF).
0x4	Transmits a PAUSE frame on port 3 with pause_time equal to the value programmed in the port 3 *FC TX Timer Value ($ Port_Index + 0x07)* (XOFF).
0x5	Transmits a PAUSE frame on port 4 with pause_time equal to the value programmed in the port 4 *FC TX Timer Value ($ Port_Index + 0x07)* (XOFF).
0x6	Transmits a PAUSE frame on port 5 with pause_time equal to the value programmed in the port 5 *FC TX Timer Value ($ Port_Index + 0x07)* (XOFF).
0x7	Transmits a PAUSE frame on port 6 with pause_time equal to the value programmed in the port 6 *FC TX Timer Value ($ Port_Index + 0x07)* (XOFF).

Table 15 Valid Decodes for TXPAUSEADD[3:0] (Sheet 2 of 2)

TXPAUSEADD[3:0]	TX Pause Control Interface Operation
0x8	Transmits a PAUSE frame on port 7 with pause_time equal to the value programmed in the port 7 *FC TX Timer Value ($ Port_Index + 0x07)* (XOFF).
0x9	Transmits a PAUSE frame on port 8 with pause_time equal to the value programmed in the port 8 *FC TX Timer Value ($ Port_Index + 0x07)* (XOFF).
0xA	Transmits a PAUSE frame on port 9 with pause_time equal to the value programmed in the port 9 *FC TX Timer Value ($ Port_Index + 0x07)* (XOFF).
0xB - 0XE	Reserved
0xF	Transmits a PAUSE frame on every port with pause_time equal to the value programmed in the *FC TX Timer Value ($ Port_Index + 0x07)* for each port (XOFF).

Figure 8 Transmit Pause Control Interface



This example shows the following conditions:

Strobe 1:
- Port 0: Transmit Pause Packet (XOFF)

Strobe 2:
- All Ports: Transmit Pause Packet with pause_time = 0 (XON)

Strobe 3:
- Port 3: Transmit Pause Packet (XOFF)

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5.1.4 Auto-Negotiation

Auto-negotiation is carried out by the PHY connected to the RGMII interface. The PHY registers should be configured to select the desired advertisements based upon the MAC supported abilities and enable auto-negotiation.

The MDIO interface block contains the logic through which the registers in the connected PHYs can be accessed. For more information on the MDIO interface of the IXF1010 MAC, refer to Section 5.4, *MDIO Control and Interface*, on page 69.

The following IXF1010 MAC capabilities should be advertised during auto-negotiation in the connected PHY Auto-Negotiation Advertisement Register.

- Speed

— TheIXF1010 MAC supports both 100 and 1000 Mbps operation. All required speed adjustments, clocks, etc., are supplied by theIXF1010 MAC. The operating speed of the MAC is programmable via the RGMII Speed Register (*RGMII Speed ($ Port_Index + 0x10)*, on page 119).

- Duplex
  - — The IXF1010 MAC supports full-duplex only, and this must be the only mode advertised by the connected PHY during auto-negotiation. If the IXF1010 MAC is connected to a link partner that does not support auto-negotiation and the PHY reverts to parallel detection, the duplex setting between the IXF1010 MAC and the local and remote PHYs become out of step, leading to a link collision.
- Flow Control
  - — The connected PHY should advertise that IXF1010 MAC supports the ability to send and receive flow control frames (symmetric).

The user must poll the PHY by using the IXF1010 MAC MDIO interface to determine when auto-negotiation is complete. After completion of auto-negotiation by the PHY, the user programs the IXF1010 MAC to read the PHY Auto-Negotiation Link Partner Base Page Ability Register. From the settings in this register, the following IXF1010 MAC registers must be programmed to match the connected PHY configuration:

- **Speed:** TheIXF1010 MAC Speed should be set to either 100 or 1000 Mbps in the *RGMII Speed ($ Port_Index + 0x10)*, on page 119.
- **Link:** While link is established, the user must write Link LED Enable Register (Addr: 0x502) (link to register). Note: This register controls link LED (refer to Section 5.5, *LED Interface*, on page 73). The link LED does not update automatically. The Link LED Register should be updated anytime there is a change in link status in order to have the link LED Green show expected behavior.
- **Flow Control:** If the link partner does not support flow control, the *FC Enable ($ Port_Index + 0x12)*, on page 119).

Note: If any changes in the speed, duplex, or flow control capabilities of the link partner are detected, the system software must once again update the IXF1010 MAC registers.

5.1.5 Jumbo Packet Support

The IXF1010 MAC supports the concept of jumbo frames. The jumbo frame length is dependent on the application, and the IXF1010 MAC design has been optimized for 9.6 KB jumbo frame length. Lengths larger than this can be programmed, but will limit system performance.

The value programmed into the Max Frame Size Register (Addr: Port_Index + 0x0F) determines the maximum length frame size the MAC can receive or transmit without activating any error counters, and without truncation.

The Max Frame Size Register (Addr: Port_Index + 0x0F) bits 13:0 set the frame length. The default value programmed into this register is 0x05EE (1518). The value is internally adjusted by +4 if the frame has a VLAN tag. The overall programmable maximum is 0x3FFF or 16383 bytes. The register should be programmed to 0x2667 for the 9.6 KB length jumbo frame for which the IXF1010 MAC is optimized.

The RMON counters are also affected for jumbo frame support as follows:

RX Statistics:

- RXOctetsTotalOK (Addr: Port_Index + 0x20)

- RXPkts1519toMaxOctets (Addr: Port_Index + 0x2B)
- RXFCSErrors (Addr: Port_Index + 0x2C)
- RXDataError (Addr: Port_Index + 0x02E)
- RXAlignErrors (Addr: Port_Index + 0x2F)
- RXLongErrors (Addr: Port_Index + 0x30)
- RXJabberErrors (Addr: Port_Index + 0x31)
- RXVeryLongErrors (Addr: Port_Index + 0x34)

TX Statistics:

- TXOctetsTotalOK (Addr: Port_Index + 0x40)
- TxPkts1519toMaxOctets (Addr: Port_Index + 0x4B)
- TxExcessiveLengthDrop (Addr: Port_Index + 0x53)
- TXCRCError (Addr: Port_Index + 0x56)

The IXF1010 MAC checks the CRC for all legal length jumbo frames (frames between 1519 and the Max Frame Size). On transmission, the MAC can be programmed to append the CRC to the frame or check the CRC and increment the appropriate counter. On reception, the MAC transmits these frames across the SPI4-2 interface (jumbo frames with a bad CRC cannot be dropped and are sent across the SPI4-2 interface). If the receive frame has a bad CRC, the appropriate counter is incremented and the EOP Abort code is set in the SPI4-2 control word.

Jumbo frames also impact flow control. The maximum frame size needs to be taken into account when determining the FIFO watermarks. The current transmission must be completed before a Pause frame can be transmitted (needed when the receiver FIFO high watermark has been exceeded). If the current transmission is a jumbo frame, the delay may be significant and increase data loss due to insufficient available FIFO space.

5.1.6 RMON Statistics Support

5.1.6.1 RMON Statistics

The IXF1010 MAC supplies RMON statistics via the CPU interface. These statistics are available in the form of counter values that can be accessed at specific addresses in the IXF1010 MAC memory map. Once read, these counters automatically reset and begin counting from zero. A separate set of RMON statistics is available for each MAC device in the IXF1010 MAC.

Implementation of the RMON Statistics block is similar to the functionality provided by existing Cortina switch and router products. This implementation allows the IXF1010 MAC to provide all of the RMON Statistics group as defined by RFC2819.

The IXF1010 MAC supports the RMON RFC2819 Group 1 statistics counters. Table 16 notes the differences and additional statistics registers supported by the IXF1010 MAC that are outside the scope of the RMON RFC2819 document.

Table 16 RMON Additional Statistics Registers (Sheet 1 of 2)

RMON Ethernet Statistics Group 1 Statistics	Type	IXF1010 MAC Equivalent Statistics	Type	Definition of RMON Versus IXF1010 MAC Documentation
etherStatsIndex	Integer32	N/A	N/A	N/A
etherStatsDataSource	Object Identifier	N/A	N/A	N/A
etherStatsDropEvents	Counter32	RX/TX FIFO Number of Frames Removed	Counter32	See Table note 1.
etherStatsOctets	Counter32	RXOctetsTotalOK RXOctetsBad TXOctetsTotalOK TXOctetsBad	Counter32	**Note:** The IXF1010 MAC has two counters for RX and TX that use different naming conventions for total Octets and Octets bad. These counters need to be combined to meet the RMON spec.
etherStatsPkts	Counter32	RX/TXUCPkts RX/TXBCPkts RX/TXMCPkts	Counter32	**Note:** The IXF1010 MAC has three counters for etherStatsPkts that need to be combined to give the total packets as defined by the RMON spec.
etherStatsBroadcastPkts	Counter32	RX/TXBCPkts	Counter32	OK
etherStatsMulticastPkts	Counter32	RX/TXMCPkts	Counter32	See table note 2.
etherStatsCRCAlignErrors	Counter32	RXAlignErrors RXFCSErrors TXCRCError	Counter32	**Note:** The IXF1010 MAC has two counters for alignment and CRC errors for the RX side only. The IXF1010 MAC has CRCError for the TX side.
etherStatsUndersizePkts	Counter32	RXRuntErrors RXShortErrors RX Statistic ONLY	Counter32	**Note:** The IXF1010 MAC has two counters for RuntErrors and ShortErrors for the RX side only.
etherStatsOversizePkts	Counter32	RXLongErrors TXExcessiveLengthDrop	Counter32	OK
etherStatsFragments	Counter32	RXRuntErrors	Counter32	OK
etherStatsJabbers	Counter32	RXJabberErrors	Counter32	OK
etherStatsCollisions	Counter32	TXSingleCollisions TXMultipleCollisions TXLateCollisions TXTotalCollisions	Counter32	OK **Note:** Registers exist on the TX side but should not increment since the IXF1010 MAC only supports full-duplex.
etherStatsPkts64Octets	Counter32	RX/TXPkts64Octets	Counter32	OK
etherStatsPkts65to127Octets	Counter32	RX/TXPkts65to127Octets	Counter32	OK
etherStatsPkts128to255Octets	Counter32	RX/TXPkts128to255Octets	Counter32	OK
etherStatsPkts256to511Octets	Counter32	RX/TXPkts256to511Octets	Counter32	OK

1. The RMON spec requires that this is, “The total number of events where packets were dropped by the probe due to a lack of resources. Note that this number is not necessarily the number of packets dropped; it is the number of times this condition has been detected.” The RX/TX FIFO Number of Frames Removed Register in the IXF1010 MAC supports this and will increment when either an RX or TX FIFO has over flowed. If any IXF1010 MAC programmable packet filtering is enabled, the RX/TX Number of Frames Removed Register increments with every frame removed in addition to the existing frames counted due to FIFO overflow.
2. TheIXF1010 MAC has an extra counter RX/TXUCPkts that can be used.
3. The IXF1010 MAC has an extra counter RX/TXPktstoMaxOctets that can be used in addition to the RMON stats. This is required to accommodate the Jumbo packet frames requirement.

Table 16 RMON Additional Statistics Registers (Sheet 2 of 2)

RMON Ethernet Statistics Group 1 Statistics	Type	IXF1010 MAC Equivalent Statistics	Type	Definition of RMON Versus IXF1010 MAC Documentation
etherStatsPkts512to1023Octets	Counter32	RX/TXPkts512to1023Octets	Counter32	OK
etherStatsPkts1024to1518Octets	Counter32	RX/ TXPkts1024to1518Octets	Counter32	See table note 3.
etherStatsOwner	Owner String	N/A	N/A	N/A
etherStatsStatus	Entry Status	N/A	N/A	N/A

1. The RMON spec requires that this is, “The total number of events where packets were dropped by the probe due to a lack of resources. Note that this number is not necessarily the number of packets dropped; it is the number of times this condition has been detected.” The RX/TX FIFO Number of Frames Removed Register in the IXF1010 MAC supports this and will increment when either an RX or TX FIFO has over flowed. If any IXF1010 MAC programmable packet filtering is enabled, the RX/TX Number of Frames Removed Register increments with every frame removed in addition to the existing frames counted due to FIFO overflow.
2. TheIXF1010 MAC has an extra counter RX/TXUCPkts that can be used.
3. The IXF1010 MAC has an extra counter RX/TXPktstoMaxOctets that can be used in addition to the RMON stats. This is required to accommodate the Jumbo packet frames requirement.

5.1.6.2 Conventions

The following conventions are used throughout the RMON MIB and its companion documents.

- **Good Packets**: Error-free packets that have a valid frame length. For example, on Ethernet, good packets are error-free packets that are between 64 octets long and 1518 octets long. They follow the form defined in IEEE 802.3, Section 3.2.
- **Bad Packets**: Packets that have proper framing and are therefore recognized as packets, but contain errors within the packet or have an invalid length. For example, on Ethernet, bad packets have a valid preamble and SFD, but have a bad CRC, or are either shorter than 64 octets or longer than 1518 octets.

5.1.6.3 Additional Statistics

The following additional IXF1010 MAC registers support features not documented in RMON:

- MAC (flow) control frames
- VLAN tagged frames
- Sequence errors
- Symbol errors
- CRC errors

These additional counters allow for additional differentiation over and above standard RMON probes.

5.2 System Packet Interface Level 4 Phase 2

The System Packet Interface Level 4 Phase 2 (SPI4-2) provides a high-speed connection to a network processor or an ASIC. The interface implemented on the IXF1010 MAC operates at data rates up to 12.8 Gbps and supports up to ten 1 Gbps MAC ports. The data path is 16 lanes wide in each direction, with each lane operating from 640 Mbps up to

800 Mbps. Port addressing, start/end packet control, and error control codes are all transferred “in-band” on the data bus. In-band addressing supports up to 10 ports. Separate transmit and receive FIFO status lines are used for flow control. By keeping the FIFO status information out-of-band, the transmit and receive interfaces may be de-coupled to operate independently. Figure 9 and Table 17 provide an overview of the IXF1010 MAC SPI4-2 interface.

Figure 9 SPI4-2 Interfacing with the Network Processor or Forwarding Engine

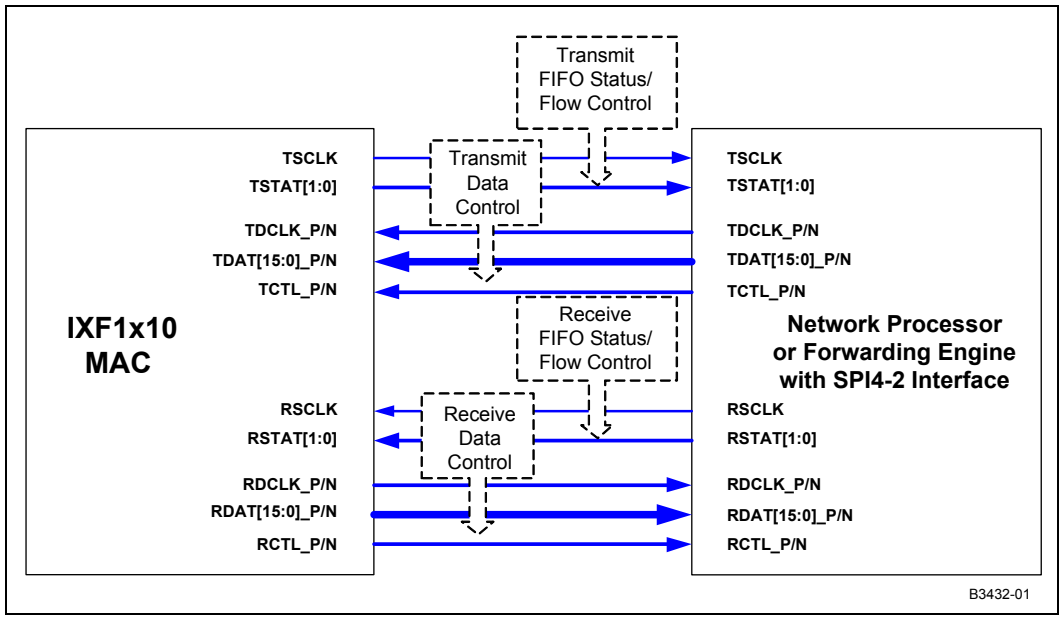


Table 17 SPI4-2 Interface Signal Summary (Sheet 1 of 2)

Signal Name	Signal Description
Transmit	
TDAT[15:0]_P/N	**Transmit Data Bus:** Differential LVDS lines used to carry payload data and in-band control words. Internally terminated differentially with 100 Ω.
TDCLK_P/N	**Transmit Data Clock:** Differential LVDS clock associated with TDAT[15:0] and TCTL. Data and control lines are driven off the rising and falling edges of the clock. Internally terminated differentially with 100 Ω. **NOTE:** If TDCLK is applied to the IXF1010 MAC after the device has come out of reset, the system designer must ensure the TDCLK is stable when applied. Failure to due so can result in the IXF1010 MAC training on a non-stable clock, causing DIP4 errors and data corruption.
TCTL_P/N	**Transmit Control:** Differential LVDS lines used to indicate when a control word is being transmitted. A High level indicates a control word present on TDAT[15:0]. Internally terminated differentially with 100 Ω.
TSCLK	**Transmit Status Clock:** LVTTL clock associated with TSTAT [1:0]. Frequency is equal to one-quarter TDCLK.
TSTAT1, TSTAT0	**Transmit FIFO Status:** LVTTL lines used to carry round-robin FIFO status information, along with associated error detection and framing.

Table 17 SPI4-2 Interface Signal Summary (Sheet 2 of 2)

Signal Name	Signal Description
Receive	
RDAT[15:0]_P/N	**Receive Data:** Carries payload data and in-band control from the IXF1010 MAC link-layer device. Internally terminated differentially with 100 Ω
RDCLK_P/N	**Receive Data Clock:** Differential LVDS clock associated with RDAT[15:0] and RCTL. Data and control lines are driven off the rising and falling edges of the clock. Internally terminated differentially with 100 Ω
RCTL_P/N	**Receive Control:** RCTL is High when a control word is present on RDAT[15:0]. Otherwise, RCTL is Low. Internally terminated differentially with 100 Ω
RSCLK	**Receive Status Clock:** LVTTL clock associated with RSTAT[1:0].
RSTAT1, RSTAT0	**Receive FIFO Status:** LVTTL lines used to carry round-robin FIFO status information, along with associated error detection and framing.

5.2.1 Data Path

Transfer of complete packets or shorter bursts is controlled by the programmed MaxBurst1 or MaxBurst2 in conjunction with the FIFO status bus. The maximum configured payload data transfer size must be a multiple of 16 bytes. Control words are inserted between burst transfers only. Once a transfer begins, data words are sent uninterrupted until an end-of-packet, or until a multiple of 16 bytes is reached as programmed in MaxBurst1 and MaxBurst2. The interval between the end of a given transfer and the next payload control word (marking the start of another transfer) consists of zero or more idle control words and/or training patterns.

Note: The system designer should be aware that the MAC Transfer Threshold Register must be set to a value which exceeds the MaxBurst1 setting of the network processor or ASIC. Otherwise, a TX FIFO under-run may result.

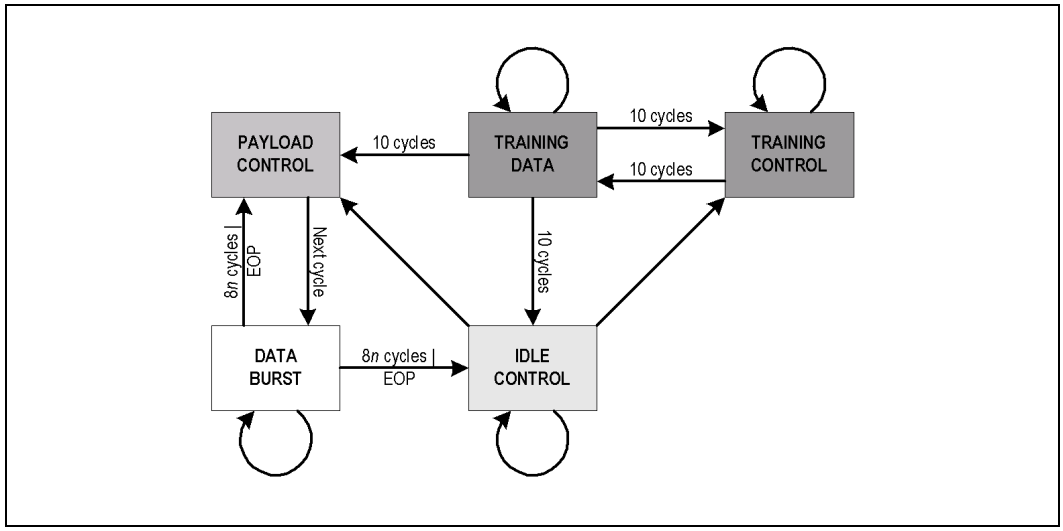
The minimum and maximum supported packet lengths are determined by the application. Because the IXF1010 MAC is targeted at the Ethernet environment, the minimum frame size is 64 bytes and the maximum frame size is 1522 bytes for VLAN packets (1518 bytes for non-VLAN packets). For larger frames, adjust the value of *Max Frame Size ($ Port_Index + 0x0F)*, on page 118. For ease of implementation, successive start-of-packets must occur not less than eight cycles apart, where a cycle is one control or data word. The gap between shorter packets is filled with idle control words.

Note: Data packets with frame lengths less than 64 bytes should not be transferred to the IXF1010 MAC unless packet padding is enabled. If this rule is disregarded, unwanted fragments may be generated on the network at the RGMII interface.

Figure 10 on page 54 shows cycle-by-cycle behavior of the data path for valid state transitions. The states correspond to the type of words transferred on the data path. Transitions from the “Data Burst” state (to “Payload Control” or “Idle Control”) are possible only on the integer multiples of eight cycles (corresponding to multiples of 16-byte segmentations) or upon end-of-packet. A data burst must immediately follow a payload control word on the next cycle. Arcs not annotated correspond to single cycles.

In the IXF1010 MAC, the RX FIFO Status channel operates in a “pessimistic mode.” It is termed as pessimistic because it has the longest latency and largest impact on usable bandwidth. However, as a DIP-2 check error is a rare event, there will be no ‘real world’ effect on bandwidth utilization and no possibility of data loss. For example, if there is a DIP-2 check error found, all previously granted credits are cancelled and the internal status for each port is set to SATISFIED. Any current data burst in transmission is completed. No new credits are granted until a complete FIFO status cycle has been received and validated by a correct DIP-2 check. This is the only method of operation that can eliminate the possibility of an overrun in the link partner device.

Figure 10 Data Path State



5.2.1.1 Control Words

A common control word format is used in both the transmit and receive interfaces. Table 18 describes the fields in the control word. When inserted in the data path, the control word is aligned such that its MSB is sent on the MSB of the transmit or receive data lines. A payload control word that separates two adjacent burst transfers contains status information pertaining to the previous transfer and the following transfer. Table 19 provides a list of control-word definitions.

Table 18 Control Word Format

Bit Position	Label	Description
15	Type	**Control Word Type.** Set to either of the following values: 0 = Idle or training control word 1 = Payload control word (payload transfer will immediately follow the control word)
14:13	EOPS	**End-of-Packet (EOP) Status.** Set to the following values according to the status of the immediately preceding payload transfer: 00 = Not an EOP. 01 = EOP Abort (application-specific error condition 10 = EOP Normal termination, 2 bytes valid 11 = EOP Normal termination, 1 byte valid EOPS is valid in the first control word following a burst transfer. It is ignored and set to “00” otherwise.
12	SOP	**Start-of-Packet.** Set to 1 if the payload transfer immediately following the control word corresponds to the start of a packet. Set to 0 otherwise. Set to 0 in all idle and training control words
11:4	ADR	**Port Address.** 8-bit port address of the payload data transfer immediately following the control word. None of the addresses are reserved (all are available for payload transfer). Set to all zeroes in all idle control words Set to all ones in all training control words
3:0	DIP-4	**4-bit Diagonal Interleaved Parity.** 4-bit odd parity computed over the current control word and the immediately preceding data words (if any) following the last control word

Table 19 Control Word Definitions (Sheet 1 of 2)

	Bit [15:12]	Next Word Status	Prior Word Status	Meaning
0	0000	Idle	Continued	Idle, not EOP, training control word
1	0001	Reserved	Reserved	Reserved
2	0010	Idle	EOP w/abort	Idle, Abort last packet
3	0011	Reserved	Reserved	Reserved
4	0100	Idle	EOP w/ 2 bytes	Idle, EOP with 2 bytes valid
5	0101	Reserved	Reserved	Reserved
6	0110	Idle	EOP w/ 1 byte	Idle, EOP with 1byte valid
7	0111	Reserved	Reserved	Reserved
8	1000	Valid	None	Valid, no SOP, no EOP
9	1001	Valid/SOP	None	Valid, SOP, no EOP
A	1010	Valid	EOP w/abort	Valid, no SOP, abort
B	1011	Valid/SOP	EOP w/abort	Valid, SOP, abort

Table 19 Control Word Definitions (Sheet 2 of 2)

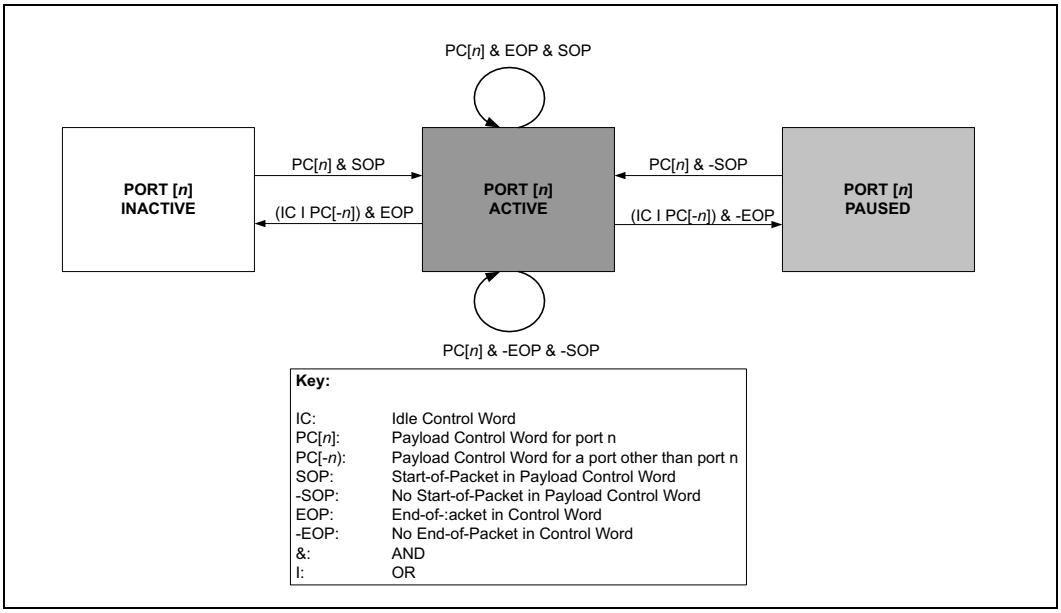
	Bit [15:12]	Next Word Status	Prior Word Status	Meaning
C	1100	Valid	EOP w/ 2 bytes	Valid, no SOP, EOP with 2 bytes valid
D	1101	Valid	EOP w/ 2 bytes	Valid, SOP, EOP with 2 bytes valid
E	1110	Valid	EOP w/ 1 byte	Valid, no SOP, EOP with 1byte valid
F	1111	Valid	EOP w/ 1 byte	Valid, SOP, EOP with 1byte valid

The SPI4-2 specification details all available Payload Control Words and should be used to reference the specific meaning of each. The IXF1010 MAC supports all required functions per this specification. However, there are various specifics in the way certain Control Words affect the balance of the IXF1010 MAC operation, such as how the device deals with EOP Aborts.

The SPI4-2 specification allows the EOP Abort Payload Control word, which signals that the data associated with a particular frame is errored and should be dropped, or errored and dropped by the far-end link partner. In the IXF1010 MAC, all TX SPI4-2 transfers that end with an EOP Abort code have the TX RGMII CRC corrupted. This is true regardless of the MAC configuration.

Figure 11 shows per-port state transitions at control-word boundaries. At any given time, a port may be active (sending data), paused (not sending data but pending the completion of an outstanding packet), or inactive (not sending data, no outstanding packet).

Figure 11 Per-Port State Diagram with Transitions at Control Words



5.2.1.2 EOP Abort

EOP Aborts is an End-of-Packet (EOP) termination that is sent out of the IXF1010 MAC SPI4-2 to tell the upstream SPI4-2 device that a packet is bad. EOP Abort packets are sent by the IXF1010 MAC under the following conditions:

- Standard size (64-1518 byte) packets that are filtered (*RX Packet Filter Control ($ Port_Index + 0x19)*, on page 121) but not dropped due to the setting in *RX FIFO Errored Frame Drop Enable ($ 0x59F)*, on page 147 (see Section 5.1.2.3, *Filtering of Receive Packets*, on page 41).
- Standard size (64-1518 byte) packets that are greater in size than the setting in *Max Frame Size ($ Port_Index + 0x0F)*, on page 118 and are not dropped due to the setting in *RX FIFO Errored Frame Drop Enable ($ 0x59F)*, on page 147.
- Jumbo frames that meet the filter conditions set in *RX Packet Filter Control ($ Port_Index + 0x19)*, on page 121 or are above *Max Frame Size ($ Port_Index + 0x0F)*, on page 118.
- RX FIFO overflows.
- Runt Packets (under 64 bytes) received that are not dropped due to the setting in *RX FIFO Errored Frame Drop Enable ($ 0x59F)*, on page 147.

Note: EOP Abort packets sent out on the RX SPI4-2 may have the packet size modified. When an EOP abort packet is received on the TX SPI4-2, the IXF1010 MAC sends the packet out to the RGMII interface with an invalid CRC and is recorded in the TX statistics as a CRC error.

5.2.1.3 DIP4

Figure 12 shows the range over which the Diagonal Interleaved Parity (DIP-4) parity bits are computed. A functional description of calculating the DIP-4 code is given as follows. Assume that the stream of 16-bit data words are arranged as shown in Figure 13 (MSB at the left most column, time moving downward). (The first word received is at the top of the figure; the last word is at the bottom of the figure.) The parity bits are generated by summing diagonally (in the control word, the space occupied by the DIP-4 code (bits a, b, c, d) is set to all 1s during encoding). The first 16-bit result is split into two bytes, which are added to each other modulo-2 to produce an 8-bit result. The 8-bit result is then divided into two 4-bit nibbles, which are added to each other modulo-2 to produce the final DIP-4 code. The procedure described applies to either parity generation on the Rx path or to check parity on the Tx path.

Figure 12 DIP-4 Calculation Boundaries

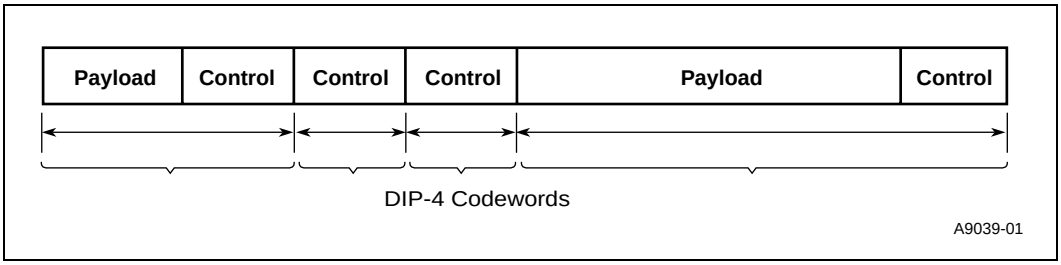
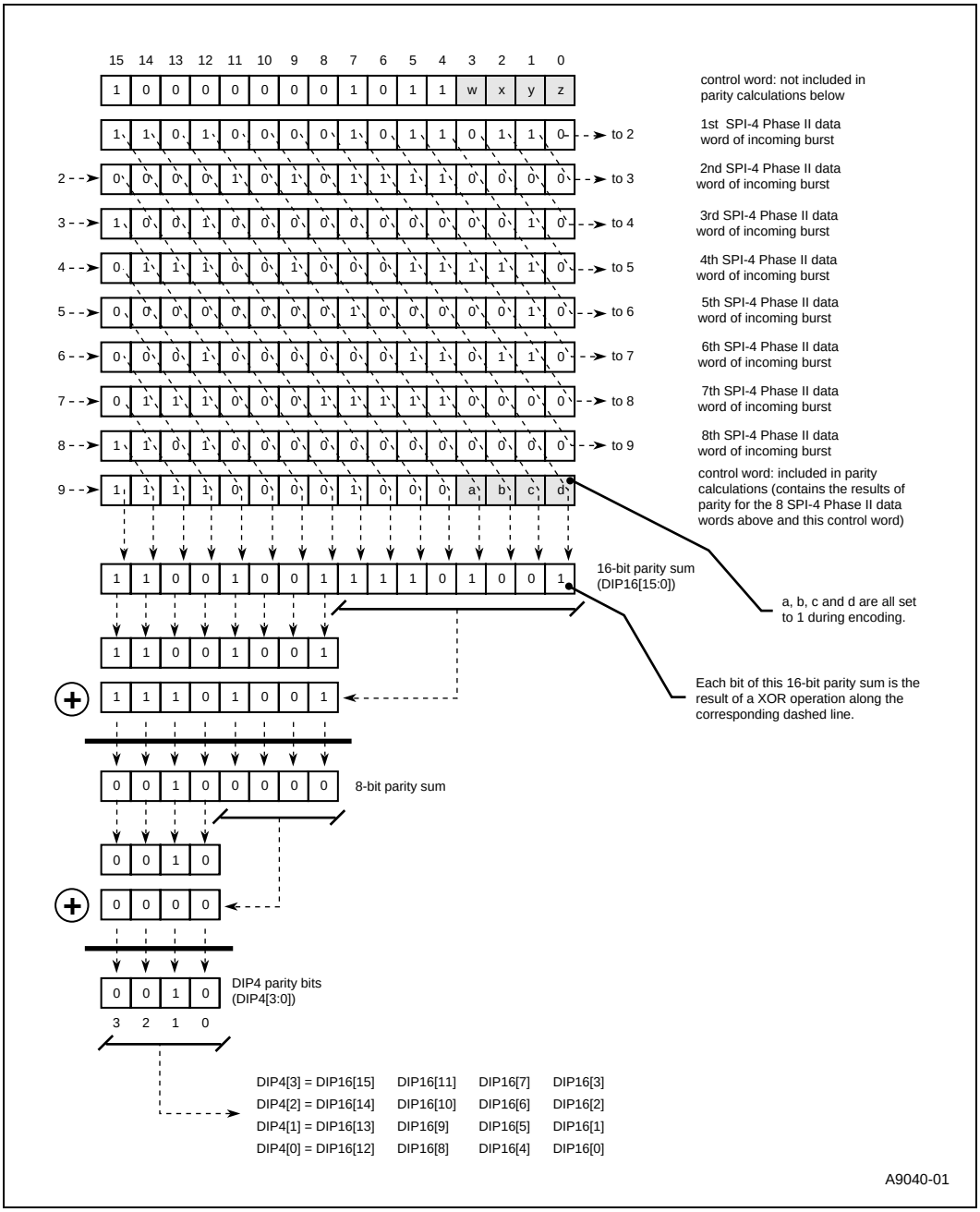


Figure 13 DIP-4 Calculation Algorithm



5.2.2 Start-Up Parameters

5.2.2.1 CALENDAR_LEN

CALENDAR_LEN specifies the length of each calendar sequence. As the IXF1010 MAC is a 10-port device, CALENDAR_LEN is fixed at 10 for both TX and RX data paths.

5.2.2.2 CALENDAR_M

CALENDAR_M specifies the number of times the calendar port status sequence is repeated between the framing and DIP2 cycle of the calendar sequence.

In the IXF1010 MAC, the TX path CALENDAR_M is fixed at 1; thus, the port status for ports 0 - 9 will be transmitted only once between the framing and DIP2 cycle of the calendar sequence.

In the IXF1010 MAC, the RX path CALENDAR_M is also fixed at 1. Thus, the status for port 0-9 must only be sent once between framing and DIP2.

Therefore, the value of both Tx and RX CALENDAR_M parameters is always fixed a 1.

5.2.2.3 DIP2_Thr

DIP2_Thr is a parameter specifying the number of consecutive correct DIP2s required by the RX SPI4-2 to validate a calendar sequence and therefore terminate sending training sequences. In *SPI4-2 RX Calendar ($ 0x702)*, on page 163, bits 19 to 16 specify this parameter. The default value for DIP2_Thr is 1.

5.2.2.4 Loss_Of_Sync

Loss_of_Sync is a parameter specifying the number of consecutive framing calendar cycles required to indicate a loss of synchronization and therefore restart training sequences. In *SPI4-2 RX Calendar ($ 0x702)*, on page 163, bits 11 to 8 specify this parameter. The default value for Loss_Of_Sync is three.

5.2.2.5 DATA_MAX_T

DATA_MAX_T is an RX SPI4-2 parameter specifying the interval between transmission of periodic training sequences. In *SPI4-2 RX Training ($ 0x701)*, on page 163, bits 15 to 0 specify this parameter. The default value for DATA_MAX_T is 0x0000, which disables periodic training sequence transmission.

5.2.2.6 REP_T

REP_T is an RX SPI4-2 parameter specifying the number of repetitions of the training sequence to be scheduled every DATA_MAX_T interval. In *SPI4-2 RX Training ($ 0x701)*, on page 163, bits 23 to 16 specify this parameter. The default value for REP_T is 0x00.

5.2.2.7 DIP4_UnLock

DIP4_UnLock is a TX SPI4-2 parameter specifying the number of consecutive incorrect DIP4 fields to be detected in order to declare loss of synchronization and drive TSTAT[1:0] bus with framing. In *SPI4-2 TX Synchronization ($ 0x703)*, on page 164, bits 15 to 8 specify this parameter. The default value for DIP4_UnLock is 0x4.

5.2.2.8 DIP4_Lock

DIP4_Lock is a TX SPI4-2 parameter specifying the number of consecutive correct DIP4 fields to be detected in order to declare synchronization achieved and enable the calendar sequence. In *SPI4-2 TX Synchronization ($ 0x703)*, on page 164, bits 7 to 0 specify this parameter. The default value for DIP4_Lock is 0x20.

5.2.2.9 MaxBurst1

MaxBurst1 is an RX SPI4-2 parameter specifying the maximum number of 16 byte blocks that may be transmitted when the associated FIFO status indicates “starving”. Bits 24 to 16 of the SPI4-2 RX Burst Size Register specify this parameter. The default value for MaxBurst1 is 0x006, indicating a MaxBurst1 of 96 bytes [see *SPI4-2 RX Burst Size ($ 0x700)*, on page 162].

5.2.2.10 MaxBurst2

MaxBurst2 is an RX SPI4-2 parameter specifying the maximum number of 16 byte blocks that may be transmitted when the associated FIFO status indicates “hungry”. Bits 8 to 0 of the SPI4-2 RX Burst Size Register specify this parameter. The default value for MaxBurst2 is 0x002, indicating a MaxBurst2 of 32 bytes (see *SPI4-2 RX Burst Size ($ 0x700)*, on page 162).

5.2.3 Dynamic Phase Alignment Training Sequence (Data Path De-skew)

5.2.3.1 Training at Start-up

The SPI4-2 Specification states that on power-up or after a reset, the training sequence (as defined in the SPI4-2 Specification) is sent indefinitely by the source side until it receives valid FIFO status on the FIFO bus. The specification also states that it is possible for the bus de-skew to be completed after one training sequence takes place. It is unlikely that the bus can be de-skewed in a single training sequence because of the presence of both random and deterministic jitter. The only way to account for the random element is to determine an average over repeated training sequences. Since the required number of repeats is dependent on several characteristics of the system in which the IXF1010 MAC is being used, power on training (or training following loss of synchronization) will continue until synchronization is achieved and the calendar is provisioned. The length of power on training will not be a fixed number of repeats.

The number of training sequence repeats could be fairly large (16, 32, or 64). If this is necessary every time training is required, a significant use of interface bandwidth is needed just to train and de-skew the data path. This is only done at power-up or reset for an optimal starting point interface. After this, periodic training provides a better adjustment and a substantially lower bandwidth overhead.

5.2.3.2 Periodic Training

A scheduled training sequence is sent at least once every pre-configured bounded interval (DATA_MAX_T) on both the transmit and receive paths. These training sequences are used by the receiving end of each interface for de-skewing bit arrival times on the data and control lines. The sequence allows the receiving end to correct for relative skew difference of up to +/- 1 bit time. The training sequence consists of one (1) idle control word followed by one or more repetitions of a 20- word training pattern consisting of 10 (repeated) training-control words followed by 10 (repeated) training-data words.

The initial idle control word removes dependencies of the DIP-4 in the training control words from preceding data words. Assuming a maximum of +/- bit time alignment jitter on each line, and a maximum of +/- bit time relative skew between lines, there are at least eight bit times when a receiver can detect a training control word prior to de-skew. The training data word is chosen to be orthogonal to the training control word. In the absence of bit errors in the training pattern, a receiver should be able successfully to de-skew the

data and control lines with one training pattern. The sending side of the data path on both the transmit and receive interfaces must schedule the training sequence at least once every DATA_MAX_T cycles.

Note: DATA_MAX_T may be set to zero, disabling periodic training on the interface (see *SPI4-2 RX Training ($ 0x701)*, on page 163). This is done when a system shows very little drift during normal operation, and no fine-grain correction on an on-going basis is needed. This allows the maximum possible bandwidth for data transfer. The transmit and receive interface training sequences are scheduled independently.

5.2.3.3 Training in a Practical Implementation

The OIF Standard states that it should be possible to train and de-skew the data input in a single training cycle. However, from the research carried out and the variances in jitter and skew due to board layout and clock tolerance issues, some sort of averaging over several repeated training patterns is required to reliably determine the optimal point at which to capture the incoming data. This is true for both static alignment and dynamic phase alignment. Therefore, several training patterns are required for an average. The more training patterns, the more accurate the average.

The de-skew circuit in the IXF1010 MAC uses dynamic phase alignment with a typical averaging requirement of 32 training patterns required to deliver a reliable result. During power-on training, an unlimited number of training cycles is sent by the data sourcing device. (The standard states that training must be sourced until a calendar has been provisioned.) In the IXF1010 MAC, the de-skew circuit waits until completion of its programmed average over the training patterns, ensuring that the required number of good DIP-4s is seen. Only then is a calendar provisioned.

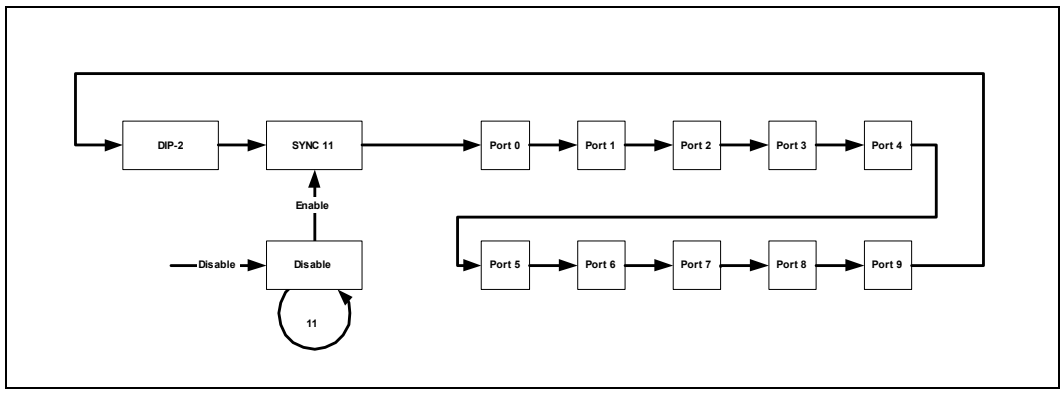
During periodic training, it is important to ensure that the training result is no less accurate than that already used for the initial decision during power-on training. Thus, a similar number of training cycles must be averaged over (32). This could make the overhead associated with periodic training large if it is required to be carried out too often. We therefore recommend that periodic training be scheduled infrequently (DATA_MAX_T = a large number) and that the number of repetitions of training be = 32(α).

5.2.4 FIFO Status Channel

FIFO status information is sent periodically over the TSTAT link from the IXF1010 MAC to the upper layer processor device, and over the RSTAT link from the upper layer processor to the IXF1010 MAC. The status channels operate independently.

Figure 14 shows the operation of the FIFO status channel. The sending side of the FIFO status channel is initially in the DISABLE state and sends the “1 1” pattern repeatedly. When FIFO status transmission is enabled, there is a transition to the SYNC state and the “1 1” framing pattern is sent. FIFO status words are then sent according to the calendar sequence, repeating the sequence CALENDAR_M times, followed by the DIP-2 code.

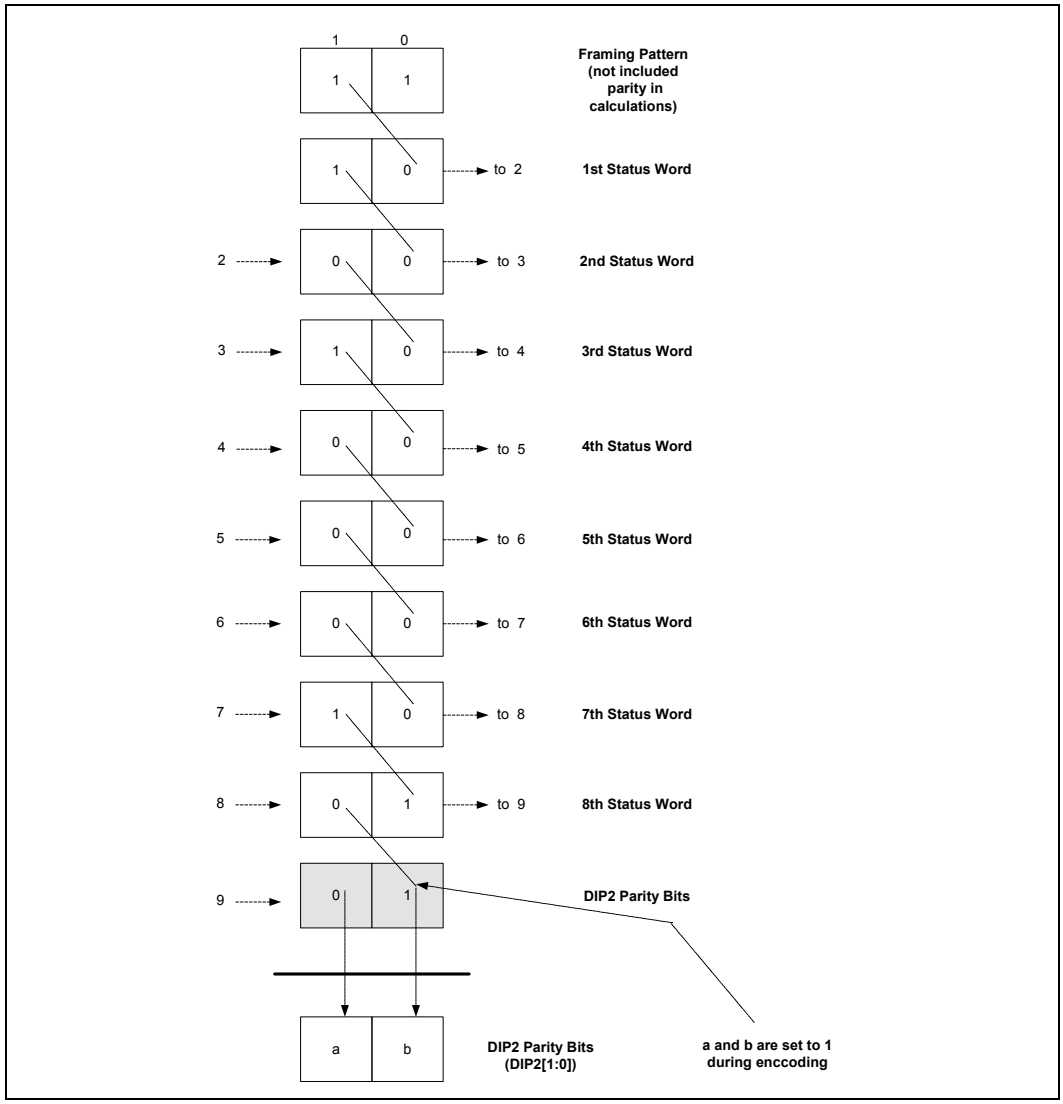
Figure 14 FIFO Status State Diagram



The FIFO status of each port is encoded in a 2-bit data structure, which is defined in *FIFO Status Format*, on page 64. The most significant bit of each port status is sent over TSTAT[1]/RSTAT[1] and the least significant bit is sent over TSTAT[0]/RSTAT[0]. The “1 1” pattern is reserved for In-band framing, which must be sent once prior to the start of the FIFO status sequence.

Immediately before the “1 1” framing pattern, a DIP-2 odd parity checksum is sent at the end of each complete sequence. The DIP-2 code is computed diagonally over TSTAT[1]/RSTAT[1] and TSTAT[0]/RSTAT[0] for all preceding FIFO status indications sent after the last “1 1” framing pattern, as shown in Figure 15, *Example of DIP-2 Encoding*, on page 63. The first word is at the top of the figure and the last word is at the bottom. The parity bits are computed by summing diagonally. Bits a and b in line 9 correspond to the space occupied by the DIP-2 parity bits and are set to 1 during encoding. The “1 1” framing pattern is not included in the parity calculation. The procedure described applies to either parity generation on the egress path or to check parity on the ingress path.

Figure 15 Example of DIP-2 Encoding



When the parity bits mimic the “1 1” pattern, the receiving end still frames successfully by syncing onto the last cycle in a repeated “1 1” pattern, and by making use of the configured sequence length when searching for the framing pattern.

To permit more efficient FIFO utilization, the MaxBurst1 and MaxBurst2 credits are granted and consumed in increments of 16-byte blocks. For any given port, these credits correspond to the most recently received FIFO status. They are not cumulative and supersede previously granted credits for the given port. A burst transfer shorter than 16 bytes (for example, an end-of-packet fragment) consumes an entire 16-byte credit.

A continuous stream of repeated “1 1” framing patterns indicates a disabled status link. For example, it may be sent to indicate that the data path de-skew is not yet completed or confirmed. When a repeated “1 1” pattern is detected, all outstanding credits are cancelled and set to zero.

Table 20 FIFO Status Format

MSB	LSB	Description
1	1	Reserved for framing or to indicate a disabled status link.
1	0	SATISFIED: Indicates that the corresponding port's FIFO is almost full. When SATISFIED is received, only transfers using the remaining previously granted 16-byte blocks (if any) may be sent to the corresponding port until the next status update. No additional transfers to that port are permitted while SATISFIED is indicated.
0	1	HUNGRY: When HUNGRY is received, transfers for up to MaxBurst2 16-byte blocks, or the remainder of what was previously granted (whatever is greater), may be sent to the corresponding port until the next status update.
0	0	STARVING: Indicates that buffer underflow is imminent in the corresponding PHY port. When STARVING is received, transfers for up to MaxBurst1 16-byte blocks may be sent to the corresponding port until the next status update

The indicated FIFO status is based on the latest available information. A STARVING indication provides additional feedback information, so that transfers are scheduled accordingly. Applications that do not distinguish between HUNGRY and STARVING may only examine the most significant FIFO status bit.

Note: If a port is disabled on the IXF1010 MAC, FIFO status for the port is set to SATISFIED to avoid the possibility of any data being sent to it by the controlling device. This applies to the IXF1010 MAC transmit path.

Upon reset, the FIFOs in the data path receiver are emptied, and any outstanding credits are cleared in the data path transmitter. After reset, and before active traffic is generated, the data transmitter sends continuous training patterns. Transmission of the training patterns continues until valid information is received on the FIFO Status channel. The receiver ignores all incoming data until it has observed the training pattern and acquired synchronization with the data. Synchronization may be declared after a provisional number of consecutive correct DIP-4 code words is seen. Loss of synchronization may be reported after a provisional number of consecutive DIP-4 code words is detected. [For details, see *SPI4-2 TX Synchronization ($ 0x703)*, on page 164.]

The DIP-4 thresholds are programmable. However, there is a potential issue with the possibility of a given link showing DIP-4 errors that may never lose synchronization and re-train to fix the issue. This would mean an on-going and potentially significant loss of data on the link affecting all ports transferring data at that time.

This issue may be seen in the following two instances:

- During training (most likely periodic training)
- During data transfers where each of the data transfers (MaxBurst1 or MaxBurst2) are separated by more than one idle control word

The mechanism for both issues is the same because data will not change during a repeated period of the same control word being transmitted on the link. If there have been some consecutive DIP-4 errors, they will be incremented towards the Loss-of-Sync threshold. This is most likely to occur from a path requiring de-skew. If either a stream of idles or training control words follow the burst and the DIP-4 associated with each of the words is checked, only the first one and the last one will be seen as invalid. Any other control words in the middle will be seen as having a valid DIP-4 and will reset the Loss-of-Sync threshold counter back to zero.

In order to avoid this, the IXF1010 MAC has altered the way in which the check is done for idle control words and training control words. We now only validate the first occurrence of the DIP-4 in both training control words and idle control words for correctness. We do still check each of the words but only use the first occurrence to clear the DIP-4 error counter. Any DIP-4 error in any of these words is still counted towards the Loss-of-Sync threshold counter. It is now impossible to mask the DIP-4 error on our interface.

5.2.5 DC Parameters

For DC parameters on the SPI4-2 interface, please refer to *2.5 V LVTTL and CMOS I/O Electrical Characteristics*, on page 94 and *LVDS I/O Electrical Characteristics*, on page 95.

5.3 Reduced Gigabit Media Independent Interface (RGMII)

The IXF1010 MAC supports Reduced Gigabit Media Independent Interface (RGMII) standards as defined in the Hewlett-Packard* RGMII Version 1.2a specification and only supports full-duplex and 100/1000 Mbps. The RGMII is an alternative to the IEEE 802.3u MII, the IEEE 802.3z GMII, and the Ten-Bit Interface (TBI). Section 5.3 discusses the IXF1010 MAC RGMII interface.

5.3.1 Purpose

The RGMII reduces the number of pins required to interconnect the MAC and the PHY, from a maximum of 28 pins (TBI) to 12 pins, in a cost-effective and technology-independent manner. The data paths and all associated control signals are reduced, control signals are multiplexed together, and both edges of the clock are used. For Gigabit operation, the clocks operate at 125 MHz, and for 100 Mbps operation, the clocks operate at 25 MHz. For 100 Mbps operation, the RGMII interface data path reverts to standard MII operational mode, as defined in IEEE 802.3, Clause 22. The multiplexed control signals operate as defined in RGMII Specification 1.2a.

5.3.2 Configuring the IXF1010 MAC for RGMII Operation

TheIXF1010 MAC automatically operates in RGMII mode. However, the user must read and write the MAC capabilities to the attached PHY via the MDIO interface. Please see Section 5.4, *MDIO Control and Interface*, on page 69 for more details.

5.3.3 MAC/PHY Interface, Signaling, and Operation

5.3.3.1 MAC/PHY Interface

Figure 16 illustrates the RGMII interface between the IXF1010 MAC and the PHY. The signal descriptions in Table 21 provide a functional description of each signal that uses positive logic. The RGMII Specification defines a signal as logic High when it is at a voltage level greater than V_{OH}-MIN, and logic Low when it is at a voltage level less than V_{OL}-MAX.

Figure 16 System Diagram (RGMII Signals)

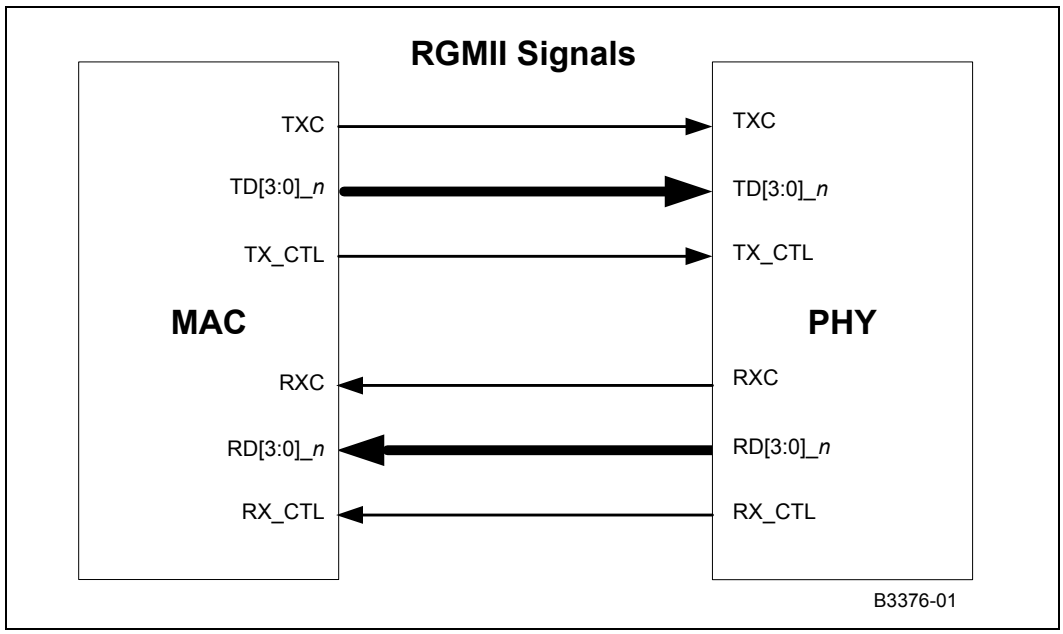


Table 21 RGMII Signal Descriptions

IXF1010 MAC Symbol	RGMII Standard Symbol	Source	Description
TXC_0:9	TXC	MAC	Depending on speed, the transmit reference clock is 125 MHz or 25 MHz +/- 100 ppm
TD[3:0]_0:9	TD<3:0>	MAC	Contains Register bits 3:0 on the rising edge of TXC and may contain Register bits 7:4 on the falling edge of TXC, depending on speed
TX_CTL_0:9	TX_CTL	MAC	TXEN on the rising edge of TXC TXEN xor TXERR on the falling edge of TXC
RXC_0:9	RXC	PHY	Continuous reference clock is 125 MHz or 25 MHz +/- 100 ppm
RD[3:0]_0:9	RD<3:0>	PHY	Contains Register bits 3:0 on the rising edge of RXC and may contain Register bits 7:4 on the falling edge of RXC, depending on speed
RX_CTL_0:9	RX_CTL	PHY	RX_CTL is on the rising edge of RXC RX_CTL xor RXERR is the falling edge of RXC

5.3.4 1000 Mbps Operation

5.3.4.1 Multiplexing of Data and Control

In RGMII, multiplexing of data and control information is achieved by utilizing both edges of the reference clocks and sending the lower four data bits on the rising edge and the upper four data bits on the falling edge. The GMII TXEN and GMII TXER signals are multiplexed and encoded to form one transmit control signal (TX_CTL). The same is true

of the receive side. The GMII RX_DV and GMII RXER signals are multiplexed and encoded to form one receive control signal (RX_CTL). The RGMII control signals are encoded to reduce power. The coding scheme for the transmit control signal is as follows:

- On the leading edge of the transmit clock (TXC), TX_CTL displays the GMII TXEN signal state (logic High represents the “true” state).
- On the falling edge of the transmit clock, TX_CTL displays the XOR combination of the GMII TXEN and TXER signals.
- The receive side operates in the same manner. This coding scheme reduces transitions because, during normal data flow, the appropriate control signal remains High, and during idle periods, the control signal remains Low.

An RGMII PHY can optionally communicate its link status, speed, and duplex mode via the RD_[3:0] signals. The IXF1010 MAC will not use this data to configure any status, speed, or duplex in the MAC. This must be set via the local CPU.

5.3.4.2 TXERR and RXERR Coding

To reduce interface power, the transmit error condition (TXERR) and the receive error condition (RXERR) are encoded on the RGMII interface to minimize transitions during normal network operation (refer to Table 22 for the encoding method). Table 19 provides signal definitions for RGMII. Figure 17 shows the transitions for frames with and without errors.

Note: The value of RGMII_TXER and RGMII_TXEN are valid at the rising edge of the clock while TXERR is presented on the falling edge of the clock. RXERR coding behaves in the same way.

TXERR <= RGMII_TXER (XOR) RGMII_TXEN

RXERR <= RGMII_RXER (XOR) RGMII_RXDV

Note: The following occurs if an RXERR is asserted (RXCTL is Low on the falling edge of RXC) or RX_DV is de-asserted (RXCTL is Low on the rising edge of RXC) during the first 17 bytes of the received packet after the SFD:

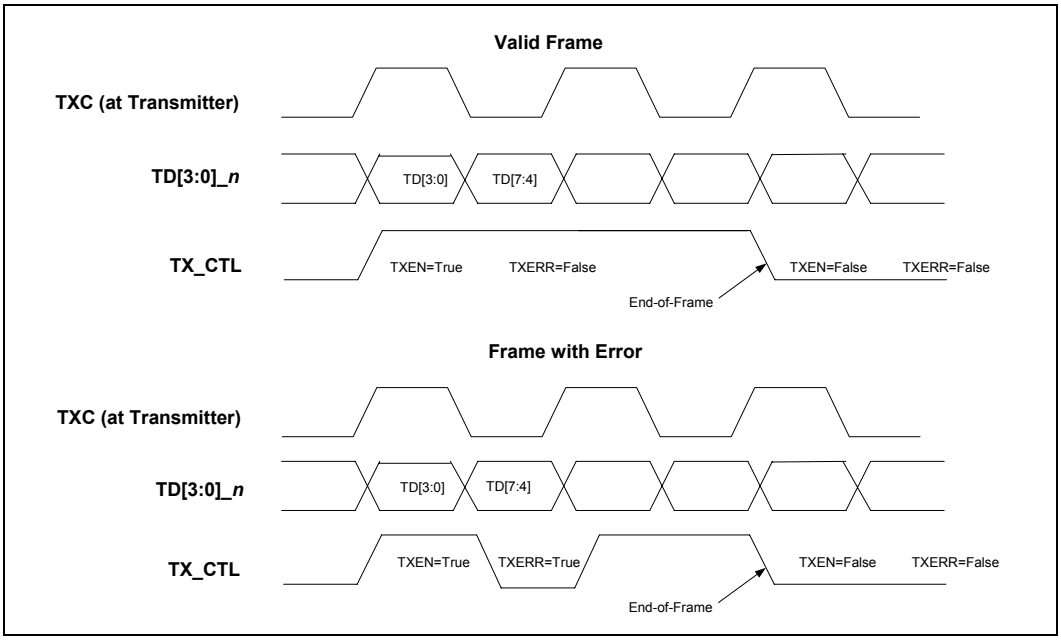
- The received packet is always dropped regardless of the setting the *RX FIFO Errored Frame Drop Enable ($ 0x59F)*, on page 147.
- The received packet is not recorded in the *RX FIFO Number of Frames Removed Ports 0 to 9 ($ 0x594 - 0x59D)*, on page 144.

The rest of the RX statistics will increment as defined.

Table 22 TXERR and RXERR Coding Example

Condition	Description	
Receiving valid frame, no errors	RX_CTL = true Logic High on rising edge of RXC	RXERR = false Logic High on the falling edge of RXC
Receiving valid frame, with errors	RX_CTL = true Logic High on rising edge of RXC	RXERR = true Logic Low on the falling edge of RXC
Receiving invalid frame (or no frame)	RX_CTL = false Logic Low on rising edge of RXC	RXERR = false Logic Low on the falling edge of RXC
Note: Refer to Figure 17 for TX_CTL Behavior.		

Figure 17 TX_CTL Behavior



5.3.5 100 Mbps Operation

The control signals are multiplexed, as in 1000 Mbps operation, by using both edges of the clock. The data signals do not need to be multiplexed and are driven off the rising edge of the clock. The clock rate is reduced to 25 MHz for 100 Mbps operation. The MAC generates the Transmit Reference Clock (TXC), and the Receive Reference Clock (RXC) is generated by the PHY. During packet reception, the RXC is stretched on either the positive or negative pulse to accommodate transition from the free-running clock to a data-synchronous clock domain (see Figure 31, *RGMII 100 Mbps Multiplexing and Timing*, on page 97). When the speed of the PHY changes, a similar stretching of the positive or negative pulses is allowed. No glitching of the clocks is allowed during speed transitions.

5.3.6 Timing Specifics

The IXF1010 MAC generates data, control, and clock signals simultaneously for transmission to the PHY. The PHY needs to operate in a similar manner when transmitting to the IXF1010 MAC. This approach is necessary to provide tight skew control among the different signals. The RGMII Specification requires that an additional delay from 1.5 to 2.8 ns be added to the clock (transmit and receive) with additional board trace.

Refer to Table 38, *RGMII 1000 Mbps Timing Specifics*, on page 96 for 1000 Mbps timing specifics.

Refer to Table 40, *RGMII 100 Mbps Timing Specifics*, on page 98 for 100 Mbps timing specifics.

5.3.7 Electrical Characteristics

The RGMII and RTBI signals (including MDIO/MDC) are based on 2.5 V CMOS interface voltages, as defined by JEDEC EIA/JESD8-5 (see Table 43, *JTAG Timing Parameters*, on page 102).

5.4 MDIO Control and Interface

5.4.1 MDIO Interface

The IXF1010 MAC supports the IEEE 802.3 MII Management Interface (also known as the Management Data Input/Output (MDIO) Interface). This interface allows the IXF1010 MAC to monitor and control each of the PHY devices that are connected to the device's 10 ports.

5.4.2 General Description

The MDIO Master Interface block is implemented once in the IXF1010 MAC. The MDIO Interface block contains the logic through which the user accesses the registers in PHY devices connected to the MDIO/MDC interface, controlled by each port. In auto-negotiation mode, the PHY completes auto-negotiation for the link. The IXF1010 MAC must communicate the supported abilities to the PHY and the results of the link partner auto-negotiation. This is done via the MDIO interface.

The MDIO Master Interface block supports the management frame format, specified by IEEE 802.3, Clause 22, Section 2.4.5. This block also supports single MDI access via the CPU interface and an autoscan mode. Autoscan allows the MDIO master to read all 32 registers of the per-port PHYs and store the contents in the IXF1010 MAC. This ability provides an external CPU-ready access to the PHY register contents via a single CPU Read without the latency of waiting on the low-speed serial MDIO data bus for each register access.

5.4.3 Single MDI Command Operation

The Management Data interface is accessed through the MDI Single Command and Address Register and the MDI Single Read and Write Data Register. A single management frame is sent by setting bit 20 to Logic 1 in the MDI Single Command and Address Register, and is automatically cleared when the frame is completed.

Write data is first set up in MDI Single Read and Write Data Register bits 15:0 for Write operation. The MDI Single Command and Address Register is initialized with the appropriate control information (start, op code, etc.) and MDI Single Command and Address Register bit 20 is set to Logic 1. Bit 20 is reset to Logic 0 when the frame is complete.

Read operation steps are identical, except in MDI Single Read and Write Data Register bits 15:0 where the data is ignored. Data received from the MDIO is read by the CPU interface from bits 31:16.

5.4.4 Clear When Done

The MDI Command Register bit, in the MDI Single Command and Address Register, clears upon command completion and is set by the user to start the requested single MDIO Read or Write operation. This bit is cleared automatically upon operation completion.

5.4.5 MDC Generation

The MDC clock is used for the MDIO/MDC interface. The frequency of the MDC clock is selectable by setting the MDC speed bit in the MDI Control Register (see Table 112, *MDI Control ($ 0x683)*, on page 161).

5.4.5.1 MDC High-Frequency Operation

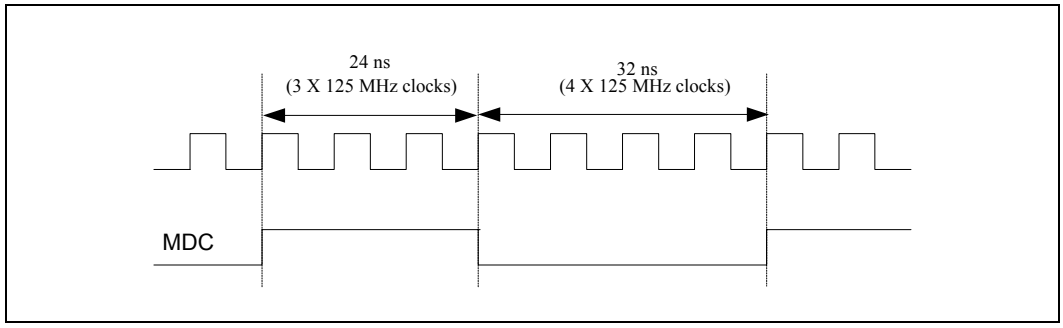
The high-frequency MDC is 18 MHz, derived from the 125 MHz system clock by dividing the frequency by 7.

The clock duty cycle is as follows:

- MDC High duration: 3 x (1/125 MHz) = 3 X 8 ns = 24 ns
- MDC Low duration: 4 x (1/125 MHz) = 4 X 8 ns = 32 ns
- MDC runs continuously after reset

5.4.5.2 MDC Low-Frequency Operation

Figure 18 High-Frequency MDC Timing

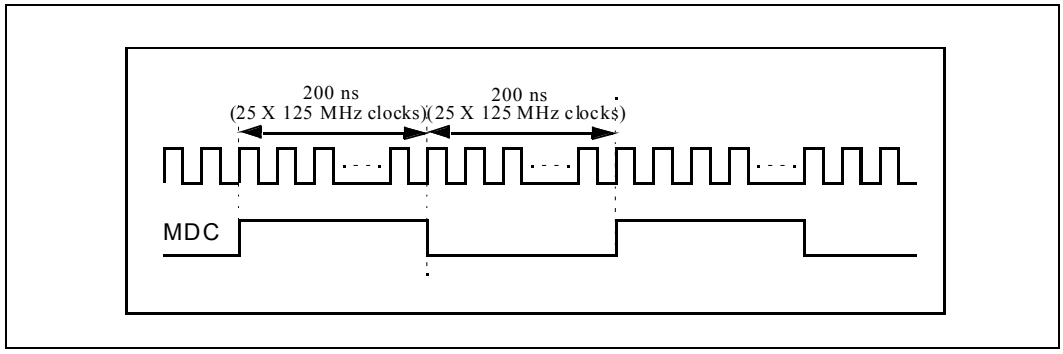


The low-frequency MDC is 2.5 MHz, which is derived from the 125 MHz system clock by dividing the frequency by 50.

The duty cycle is as follows:

- MDC High duration: 25 x (1/125 MHz) = 25 x 8 ns = 200 ns
- MDC Low duration: 25 x (1/125 MHz) = 25 x 8 ns = 200 ns
- MDC runs continuously after reset

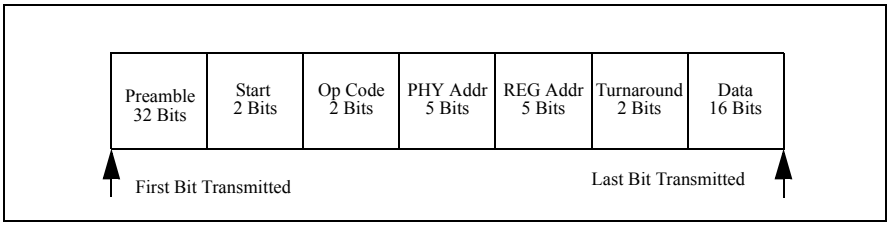
Figure 19 Low-Frequency MDC Timing



5.4.6 MDIO Management Frames

The MDIO Management interface serializes the external register access information into the format specified by IEEE 802.3, Clause 22, Section 2.4.5.

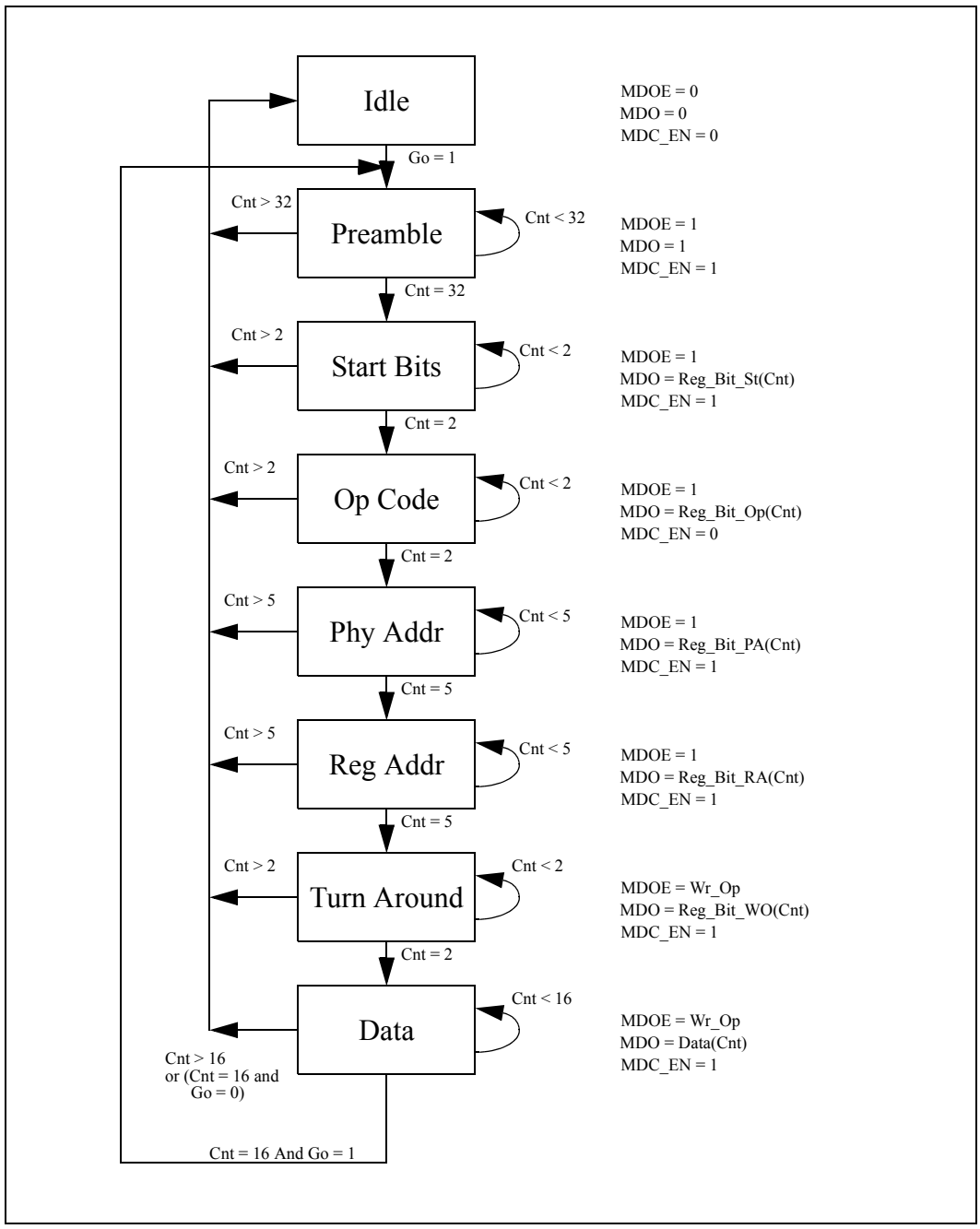
Figure 20 MDIO Management Frame Structure



5.4.7 MDI State Machine

The MDI State Machine sequences the information sent to it by the MDIO control registers and keeps track of the current sequence bit count, enabling or disabling the MDIO driver output (see Figure 21, *MDI State Diagram*, on page 72).

Figure 21 MDI State Diagram



5.4.8 Autoscan Operation

The Autoscan PHY Address Enable Register (*Autoscan PHY Address Enable ($ 0x682)*, on page 161) is used to determine which PHY addresses are used for each of the ten IXF1010 MAC ports. The Autoscan PHY Address Enable Register is 32 bits wide, which allows for PHY addresses 0 - 31 to be used. The bits set in this register correspond to

consecutive MAC ports. The Least Significant Bit (LSB) set in the Address Enable Register is port 0 for the IXF1010 MAC; the next significant bit set is assumed to be port 1, and this continues on to port 9. If more than 10 bits are set, the bits beyond the tenth bit are ignored. If less than 10 bits are set, the round-robin process reads only the PHY registers for the reduced MAC port count.

The autoscan function stores the 32 registers in each external PHY (up to 10) internally in the IXF1010 MAC. Autoscan is enabled by setting bit 1 of the MDI Control Register (*MDI Control ($ 0x683)*, on page 161). When enabled, autoscan runs continuously, reading each PHY register. When a PHY register access is instigated through the MDIO interface, the current autoscan register Read is completed before the MDIO register access starts. Upon completion of the MDIO access, the autoscan functionality restarts from the last autoscan register access prior to the MDIO register access.

For example, the IXF1010 MAC is connected to PHYs addressed 20-29, with the IXF1010 MAC port 0 connected to PHY address 20, and Port 1 connected to PHY address 21. This is continued to port 9, which is connected to PHY address 29. To enable autoscan for all 10 ports on the IXF1010 MAC, bits 29:20 in the Autoscan PHY Address Enable Register must be set to 1 and all other bits set to a 0. This enables the autoscan to read PHY addresses 20-29, which allows all 32 registers of each PHY to be stored in the connected IXF1010 MAC ports (refer to *PHY Autoscan Register Map*, on page 112).

5.4.9 MDIO Register Descriptions

MDIO Block Register Map, on page 116 provides an overview of the MDIO Register Set and *MDI Single Command ($ 0x680)*, on page 160 through *MDI Control ($ 0x683)*, on page 161 provide a register-by-register bit definition of the MDIO register set.

5.5 LED Interface

5.5.1 Introduction

The IXF1010 MAC uses a serial interface consisting of three signals to provide LED data to a serial-to-parallel logic external driver. The three signals are as follows:

- LED CLK: This clock is provided by the IXF1010 MAC to clock the external parallel-to-serial shift registers.
- LED DATA: This serial data is provided by the IXF1010 MAC to the external parallel-to-serial shift registers.
- LED LATCH: This latch is provided by the IXF1010 MAC to latch the data on the parallel-to-serial shift registers.

The LED_DATA stream provides data for 30 separate direct drive LEDs and allows three LEDs per MAC port. The three LED pins outlined above are detailed in *LED Signal Descriptions*, on page 74.

There are two modes of operation, each with its own separate LED decode mapping. Modes of operation and LEDs are detailed in Section 5.5.2, *Modes of Operation*.

5.5.2 Modes of Operation

Mode selection is accomplished by using bit 0 of the *LED Control ($ 0x509)*, on page 139. This bit is globally selected and controls the mode of operation of all ports Section 5.5.2.1 and Section 5.5.2.2 provide the two modes of operation.

5.5.2.1 Mode 0

This mode selects operations compatible with the SGS Thompson M5450 Led Display Driver Device. This device converts the serial data stream, output by the IXF1010 MAC, into 30 direct-drive LED outputs. In this mode, the latch signal is not required. This mode is selected by setting bit 0 of the *LED Control ($ 0x509)* to 0 (default).

5.5.2.2 Mode 1

This mode selects operations compatible with TTL (74LS595) or HCMOS (74HC595) octal shift registers. This device converts the serial data stream, output by the IXF1010 MAC, into 30 direct-drive LED outputs. In this mode the LED DATA, LED CLK and LED LATCH signals are used. This mode is selected by setting bit 0 of the *LED Control ($ 0x509)* to 1.

5.5.3 LED Interface Signal Description

The IXF1010 MAC LED interface consists of three output signal pins that are 2.5 V CMOS level pads. Table 23 provides LED signal names, pin numbers, and descriptions.

Table 23 LED Signal Descriptions

Signal Name	Ball Designator	Signal Description
LED_CLK	A20	**LED_CLK:** This signal is an output that provides a continuous clock synchronous to the serial data stream output on the LED_DATA pin. This clock has a maximum speed of 720 hz. The behavior of this signal remains constant in all modes of operation.
LED_DATA	A19	**LED_DATA:** This signal provides the data, in various formats, as a serial bit stream. The data must be valid on the rising edge of the LED_CLK signal. In Mode 0, the data presented on this pin is TRUE (Logic 1 = High). In Mode 1, the data presented on this pin is INVERTED (Logic 1 = Low).
LED_LATCH	K18	**LED_LATCH:** This is an output pin and the signal is used only in Mode 1 as the Latch enable for the shift register chain. This signal is not used in Mode 0, and should be left unconnected.

5.5.4 Mode 0: Detailed Operation

Note: Please refer to the SGS Thompson M5450 datasheet for device-operation information.

The operation of the LED Interface in Mode 0 is based on a 36-bit counter loop. The data for each LED is placed in turn on the serial data line and clocked out by the LED_CLK. Figure 22 shows the basic timing relationship and relative positioning in the data stream of each bit.

Figure 22 shows the 36 clocks that are output on the LED_CLK pin. The data changes on the falling edge of the clock and is valid for almost the entire clock cycle. This ensures that the data is valid during the rising edge of the LED_CLK, which is used to clock the data into the M5450 device.The actual data shown in Figure 22 consists of a chain of 36 bits only, 30 of which are valid LED DATA. The 36-bit data chain is built up as follows:

Figure 22 Mode 0 Timing

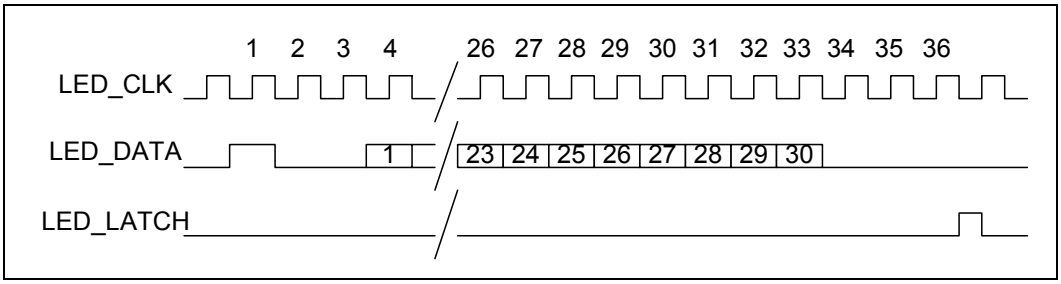


Table 24 Mode 0 Clock Cycle to Data Bit Relationship

LED_CLK CYCLE	LED_DATA NAME	LED_DATA DESCRIPTION
1	START BIT	This bit is used to synchronize the M5450 device to expect 35 bits of data to follow.
2:3	PAD BITS	These bits are used only as fillers in the data stream to extend the length from the actual 30 bit LED DATA to the required 36-bit frame length. These bits should always be a Logic 0.
4:33	LED DATA 1-30	These bits are the actual data transmitted to the M5450 device. The decode for each individual bit in each mode is defined in *LED Signal Descriptions*, on page 74. The data is TRUE. Logic 1(LED ON) = High
34:36	PAD BITS	These bits are used as fillers in the data stream to extend the length from the actual 30-bit LED DATA to the required 36-bit frame length. These bits should always be a Logic 0.

When implemented on a board with the M5450 device, the LED DATA bit 1 appears on output bit 3 of the M5450 and the LED DATA bit 2 appears on output bit 4, etc. This means that output bits 1, 2, 3, 34, and 35 will never have valid data and should not be used.

5.5.5 Mode 1: Detailed Operation

Note: Please refer to manufacturers' 74LS/HC595 datasheet for information on device operation.

The operation of the LED Interface in Mode 1 is again based on a 36-bit counter loop. The data for each LED is placed in turn on the serial data line and clocked out by the LED_CLK.

Figure 23 on page 76 shows the basic timing relationship and relative positioning in the data stream of each bit. Figure 23 shows the 36 clocks that are output on the LED_CLK pin. The data changes on the falling edge of the clock and is valid for almost the entire clock cycle. This ensures that the data is valid during the rising edge of the LED_CLK, which is used to clock the data into the Shift Register chain devices.

The LED_LATCH signal is required in Mode 1, and is used to latch the data shifted into the shift register chain into the output latches of the 74HC595 device. As seen in Figure 23, the LED_LATCH signal is active High during the Low period on the 36th LED_CLK cycle. This avoids any possibility of trying to latch data as it is shifting through the register.

When this operation mode is implemented on a board with a shift register chain containing three 74HC595 devices, the LED DATA bit 1 is output on Shift Register bit 1, and so on up the chain. Only Shift Register bits 31 and 32 do not contain valid data. The actual data shown in Figure 23 consists of a 36-bit chain, of which 30 bits are valid LED DATA. The 36-bit data chain is built up as follows:

Note: The LED_DATA signal is now inverted from the state in Mode 0.

Figure 23 Mode 1 Timing

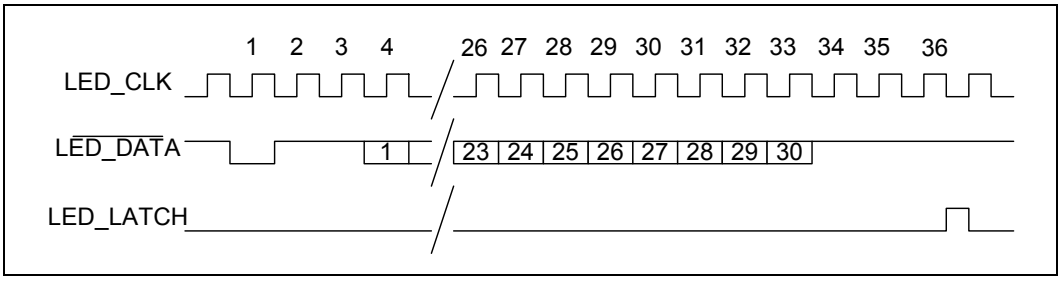


Table 25 Mode 1 Clock Cycle to Data Bit Relationship

LED_CLK CYCLE	LED_DATA NAME	LED_DATA DESCRIPTION
1	START BIT	This bit has no meaning in Mode 1 operation and is shifted out of the 32-stage shift register chain before the LED_LATCH signal is asserted.
2:3	PAD BITS	These bits have no meaning in Mode 1 operation and are shifted out of the 32-stage shift register chain before the LED_LATCH signal is asserted.
4:33	LED DATA 1-30	These bits are the actual data to be transmitted to the 32-stage shift register chain. The decode for each bit in each mode is defined in *Mode 1 Clock Cycle to Data Bit Relationship*, on page 76. The data is INVERTED. Logic 1 (LED ON) = Low.
34:36	PAD BITS	These bits have no meaning in Mode 1 operation and are latched into positions 31 and 32 in the shift register chain. These bits are not considered as valid data and should be ignored. They should always be a Logic 0 = High.

5.5.6 Power-On, Reset, and Initialization

The LED interface is disabled at power-on or reset. The system software controller must enable the LED interface. The internal state machines and output pins are held in reset until the full IXF1010 MAC configuration is completed.

5.5.6.1 Enabling the LED Interface

LED Control ($ 0x509), on page 139**:** This register must be set to globally enable LED interface. This is done by setting the LED_ENABLE bit to a logic 1. The power-on default for this bit is Logic 0.

Port Enable ($ 0x500), on page 136**:** This register enables and disables ports on a per port basis. A port must be enabled for the LEDs to operate for that port. If the port is not enabled, the LEDs will be off for that port. The power-on default for this register is 0x3FF, which means all ports are enabled.

Link LED Enable ($ 0x502), on page 137**:** This register must be set on a per port basis when link is detected by the system software. This enables the per-port link LEDs for the IXF1010 MAC. Link LEDs do not automatically update. For more details on which LEDs are affected by this register, refer to section Section 5.5.7.1, *LED Signaling Behavior*, on page 78.

5.5.7 LED Data Decodes

Table 26 shows the data decode of the data for theIXF1010 MAC.

Table 26 LED DATA Decodes

LED_DATA#	MACPORT#	IXF1010 MAC Designation
1	0	Link LED - Amber
2		Link LED - Green
3		Activity LED - Green
4	1	Link LED - Amber
5		Link LED - Green
6		Activity LED - Green
7	2	Link LED - Amber
8		Link LED - Green
9		Activity LED - Green
10	3	Link LED - Amber
11		Link LED - Green
12		Activity LED - Green
13	4	Link LED - Amber
14		Link LED - Green
15		Activity LED - Green
16	5	Link LED - Amber
17		Link LED - Green
18		Activity LED - Green
19	6	Link LED - Amber
20		Link LED - Green
21		Activity LED - Green
22	7	Link LED - Amber
23		Link LED - Green
24		Activity LED - Green
25	8	Link LED - Amber
26		Link LED - Green
27		Activity LED - Green
28	9	Link LED - Amber
29		Link LED - Green
30		Activity LED - Green

5.5.7.1 LED Signaling Behavior

The operation in each mode for the decoded LED data in Table 26 is detailed in Table 27.

Table 27 LED Behavior

Type	Status	Description
Link LED	Off	Port does not have a Remote Fault and *Link LED Enable ($ 0x502)*, on page 137 bit is not set.
	Amber On	Port has an RGMII RXERR condition detected and *Link LED Enable ($ 0x502)*, on page 137 bit is set
	Amber Blinking	Port has a remote fault and *LED Fault Disable ($ 0x50B)*, on page 140 is not set.
	Green On	*Link LED Enable ($ 0x502)*, on page 137 bit is set and port does not have RGMII RXERR error or Remote Fault condition present.
Activity LED - Green	Off	Port is not transmitting and receiving data.
	Blinking	*Link LED Enable ($ 0x502)*, on page 137 set: Port is transmitting and/or receiving. *Link LED Enable ($ 0x502)*, on page 137 not set: Port is receiving data.
Note: The LED behavior table assumes the port is enabled in the *Port Enable ($ 0x500)*, on page 136 and the LEDs are enabled in the *LED Control ($ 0x509)*, on page 139. If a port is not enabled, all the LEDs for that port will be off. If the LEDs are not enabled, all of the LEDs will be off.		

5.6 CPU Interface

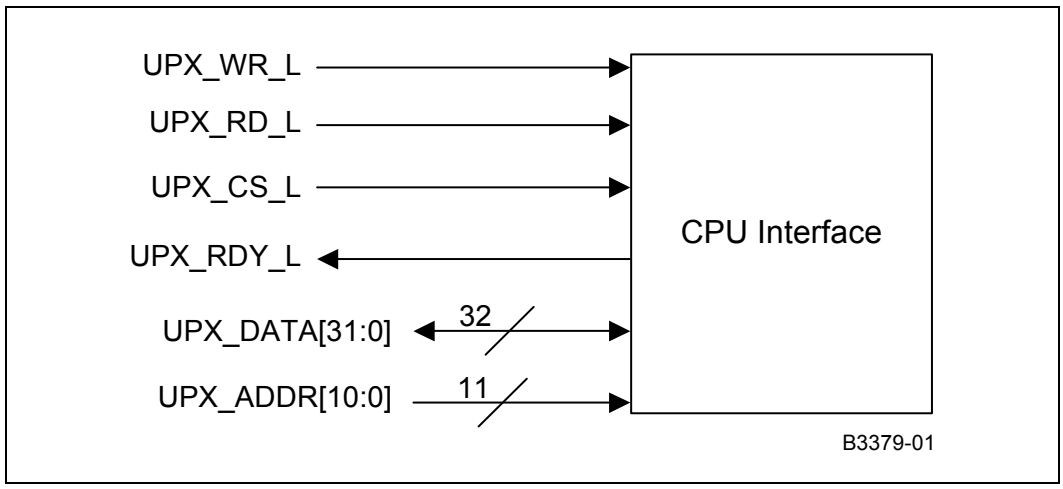
5.6.1 General Description

The CPU Interface block provides access to registers and statistics in the IXF1010 MAC. The interface is asynchronous externally and operates within the 125 MHz clock domain internally. The interface provides access to the following registers:

- MAC Control
- MAC RX Statistics
- MAC TX Statistics
- PHY Auto Scan
- Global Status and Configuration
- RX Block
- TX Block
- MDIO Block
- SPI4-2 Block

Figure 24 illustrates the I/O for the CPU interface on the IXF1010 MAC.

Figure 24 CPU Interface Inputs/Outputs



5.6.2 Functional Description

The CPU interface is designed for a generic 32-bit asynchronous CPU bus. The bus is a 32-bit data bus only and has an 11-bit address bus.

The IXF1010 MAC external CPU interface is asynchronous and has no clock. This allows flexibility for CPU selection.The interface to all IXF1010 MAC registers is synchronous to 125 MHz internally.

In some applications, synchronous-to-asynchronous glue logic is required between the IXF1010 MAC and the system CPU. This glue logic must be designed so that the IXF1010 MAC Read and Write access times are not violated. It may be possible to interface without glue logic if the CPU can meet the timing seen in Figure 25, *Read Timing – Asynchronous Interface*, on page 81, Figure 26, *Write Timing – Asynchronous Interface*, on page 81, and Table 42, *CPU Timing Parameters*, on page 100

Table 28 CPU Interface Signals

Name	Direction	Standard	Description
UPX_ADD[10:0]	Input	CMOS 2.5 V	Address bus
UPX_CS_L	Input	CMOS 2.5 V	Chip Select Signal
UPX_DATA[31:0]	Bi_Dir	CMOS 2.5 V	Bi-directional data bus
UPX_WR_L	Input	CMOS 2.5 V	Write Strobe
UPX_RD_L	Input	CMOS 2.5 V	Read Strobe
UPX_RDY_L	Output	CMOS 2.5 V	Cycle complete indicator

5.6.2.0.1 UPX_ADD[10:0]

Internal IXF1010 MAC registers and counters are selected using the 11-bit address bus input provided at the CPU interface. This address must be stable for the entire cycle.

5.6.2.0.2 UPX_CS_L

The chip select input when active Low selects IXF1010 MAC for the current cycle. No CPU cycle is recognized without this signal being active. At the end of the cycle, the chip select can be driven High to deselect the device or it can be left active if the next access is to the same device (as long as both Read and Write control signals are inactive between cycles).

The CPU usually supports multiple chip selects, and glue logic is required to drive separate chip selects if more than one IXF1010 MAC is being controlled by one CPU.

5.6.2.0.3 UPX_DATA[31:0]

These pins comprise the 32-bit data bus pins containing data to and from the CPU interface. This data is asynchronous on the IXF1010 MAC. The Write data provided by the CPU must be stable during the entire CPU cycle to prevent erroneous Write operations to a register.

5.6.2.0.4 UPX_WR_L

This pin indicates there is data on the CPU data bus to be written to the IXF1010 MAC. A Low-to-High transition latches the data and a High-to-Low transition latches the address. This Write operation is active Low.

5.6.2.0.5 UPX_RD_L

This pin indicates there is data on the CPU data bus to be read from the IXF1010 MAC. A High-to-Low transition latches the address. This Read operation is active Low.

5.6.2.0.6 UPX_RDY_L

This pin indicates the Read or Write cycle is complete for the IXF1010 MAC. This operation is active Low.

Note: External pull-up resistor required for proper operation.

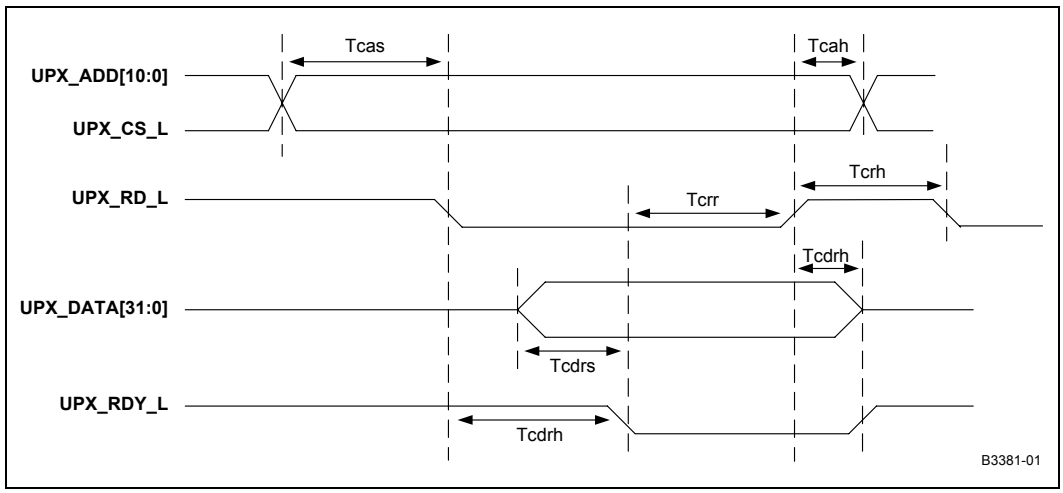
5.6.2.1 Read Access

The IXF1010 MAC read access cycle operation is done in the following order:

1. Chip Select (UPX_CS_L) is asserted at all times for the duration of the operation. The address to be read should be on the IXF1010 MAC address bus (UPX_ADD[10:0]).
2. UPX_RD_L should be asserted. The IXF1010 MAC latches the address.
3. IXF1010 MAC drives valid data onto the processor bus (UPX_DATA[31:0]).
4. IXF1010 MAC asserts asynchronous-ready (UPX_RDY_L). This indicates to the CPU that the Read cycle is complete.

Figure 25 provides the timing of the asynchronous interface for Read access.

Figure 25 Read Timing – Asynchronous Interface



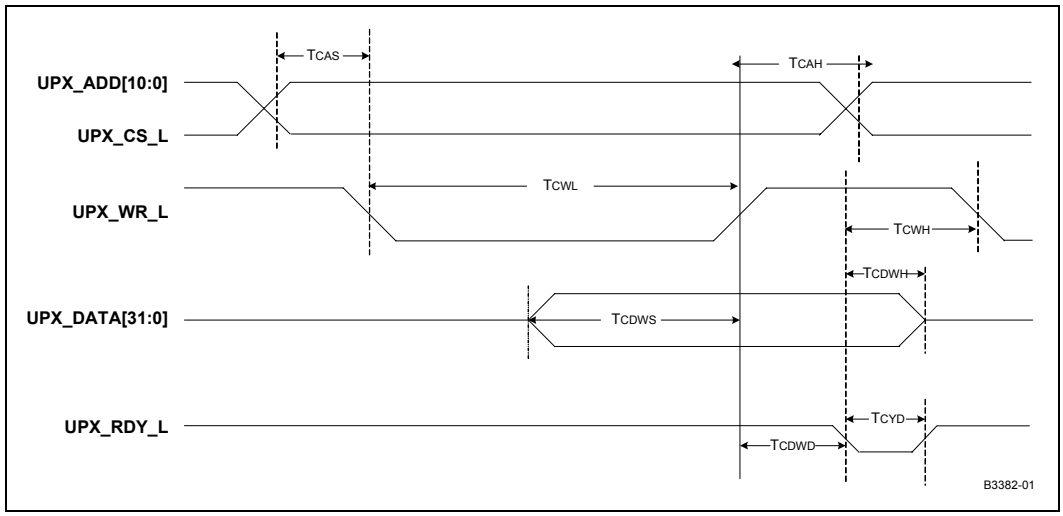
5.6.2.2 Write Access

The IXF1010 MAC Write access cycle operation is done in the following order:

1. Chip Select (UPX_CS_L) is asserted at all times for the duration of the operation. The address to be read should be on the IXF1010 MAC address bus (UPX_ADD[10:0]).
2. UPX_WR_L should be asserted. The IXF1010 MAC latches the address.
3. The CPU drives valid data onto the processor bus (UPX_DATA[31:0]).
4. The CPU de-asserts the asynchronous Write signal (UPX_WR_L) of the IXF1010 MAC. The IXF1010 MAC latches the data.
5. The IXF1010 MAC asserts asynchronous-ready (UPX_RDY_L). The glue logic indicates to the CPU that the Write cycle is complete.

Figure 26 provides the timing of the asynchronous interface for Write access.

Figure 26 Write Timing – Asynchronous Interface



5.6.2.3 Timing parameters

Timing parameters for the CPU interface are seen in Table 42, *CPU Timing Parameters*, on page 100.

5.6.3 Endian

The Endian of the CPU interface may be changed to allow connection of various CPUs to the IXF1010 MAC. The Endian selection is determined by setting the Endian bit in the *CPU Interface ($ 0x508)*, on page 139.

5.7 JTAG (Boundary Scan)

The IXF1010 MAC includes an IEEE 1149.1 boundary scan test port for board level testing. All inputs are accessible. The BSDL file for this device is available by accessing the Cortina website.

5.7.1 TAP Interface (JTAG)

The IXF1010 MAC includes an IEEE 1149.1 compliant Test Access Port (TAP) interface used during boundary scan testing. The interface consists of the following five pins:

- TDI – Serial data input
- TMS – Test mode select
- TCLK – TAP clock
- TRST_L – Active low asynchronous reset for the TAP
- TDO – Serial data output

TDI and TMS require external pull-up resistors to float the pins High per the IEEE 1149.1 specification. Pull-ups are recommended on TCK and TDO. For normal operation, TRST_L can be pulled Low, permanently disabling the JTAG interface. If the JTAG interface is used, the TAP controller must be reset as described in Section 5.7.2, *TAP State Machine*, on page 83 and returned to a logic High.

Note: The JTAG pins must be terminated correctly for proper device operation.

Table 29 Recommended JTAG Termination

Signal	Description
TRST_L[1]	Pull-down through 10 K Ω resistor
TDO	Pull-up through 10 K Ω resistor
TDI	Pull-up through 10 K Ω resistor
TMS	Pull-up through 10 K Ω resistor
TCK	Pull-up through 10 K Ω resistor

1. TRST_L must be pulled Low to ensure proper IXF1010 MAC operation. When TRST_L is Low, the JTAG interface is disabled. If the boundary scan logic is used, TRST_L must be pulsed Low after power-up to ensure reset of the TAP controller. For more information, refer to Section 5.7.2, *TAP State Machine*, on page 83 or the IEEE 1149.1 Boundary Scan Specification.

5.7.2 TAP State Machine

The TAP pins drive a TAP controller, which implements the 16-state machine specified by the IEEE 1149.1 specification. Following power up, the TAP controller must be reset by one of following two mechanisms:

- Asynchronous reset – achieved by pulsing or holding TRST_L low
- Synchronous reset – achieved by clocking TCK with five clock pulses while TMS is held or floats High.

This ensures that the boundary scan cells do not block the pin to core connections in the IXF1010 MAC.

5.7.3 Instruction Register and Supported Instructions

The instruction register is a 4-bit register that enacts the boundary scan instructions. After the state machine resets, the default instruction is IDCODE. The decode logic in the TAP controller selects the appropriate data register and configures the boundary scan cells for the current instruction. The table below shows the supported boundary scan instructions.

Table 30 Supported Boundary Scan Instructions

Instruction	Code	Description	Data Register
EXTEST	0000	External Test	Boundary Scan
SAMPLE	0001	Sample Boundary	Boundary Scan
HIGHZ	0101	Float Boundary	Bypass
IDCODE	0110	ID Code Inspection	ID
CLAMP	0111	Clamp Boundary	Bypass
BYPASS	1111	1-bit Bypass	Bypass

5.7.4 ID Register

The ID register is a 32-bit register. The IDCODE instruction connects this register between TDI and TDO. Refer to Table 95, *JTAG ID Revision ($ 0x50C)*, on page 141 for register bit descriptions.

Note: The four bit version field is stepping dependent. The seven bit Manufacturers ID is the manufacturer JEDEC ID less the parity bit per the IEEE 1149.1 specification.

5.7.5 Boundary Scan Register

The boundary scan register is a shift register made up of all the boundary scan cells associated with the device pins. The number, type, and order of the boundary scan cells are specified in the IXF1010 MAC BSDL file. The EXTEST and SAMPLE instructions connect this register between TDI and TDO.

5.7.6 Bypass Register

The bypass register is a one bit register that is used so the IXF1010 MAC can be bypassed to reduce the length of the JTAG chain when trying to access other devices on the chain besides the IXF1010 MAC. The BYPASS, HIGHZ, and CLAMP instructions connect this register between TDI and TDO.

5.8 Clocks

The IXF1010 MAC has system interface reference clocks, SPI4-2 data path input and output clocks, RGMII input and output clocks, MDIO output clock, a JTAG input clock, and an LED output clock. Section 5.8 details the unique clock source requirements.

5.8.1 System Interface Reference Clocks

There are two system interface clocks required by the IXF1010 MAC:

5.8.1.1 CLK125

The system interface clock, which supplies the clock to the majority of the internal circuitry, is the 125 MHz clock. The source of this clock must meet the following specifications:

- 3.3 V LVTTL drive
- +/- 50 ppm
- Maximum duty cycle distortion 40/60

5.8.1.2 CLK50

The other system interface clock supplies the clock source to the SPI4-2 receive circuitry. The source of this clock must meet the following specifications:

- 3.3 V LVTTL drive
- 1/8 frequency of the SPI4-2 data path clock (RDCLK_P/N)
- Maximum duty cycle distortion 45/55
- Maximum peak-to-peak jitter (low and high frequency) of 125 pS
- Range = 42 Mhz to 50 MHz

5.8.2 SPI4-2 Receive and Transmit Data Path Clocks

The SPI4-2 data path clocks are compliant with the OIF 2000.88.4 Specification.

The IXF1010 MAC has the following requirements on the transmit data path:

- 2.5 V LVDS drive
- Maximum duty cycle distortion 45/55
- Maximum peak-to-peak jitter (low and high frequency) of 125 pS
- Stable (frequency and level) when reset is removed or when sourced, whichever happens last
- TSCLK frequency is one-quarter TDCLK frequency

The IXF1010 MAC meets the following specifications on the receive data path:

- 2.5 V LVDS drive
- Maximum duty cycle distortion 45/55
- Maximum peak-to-peak jitter (low and high frequency) of 125 pS
- Stable when sourced

5.8.3 RGMII Clocks

The RGMII interface is governed by the HP 1.2a specification. The IXF1010 MAC is fully specification compliant as follows:

- 2.5 V CMOS drive
- Maximum duty cycle distortion 40/60
- +/- 100 ppm
- 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps

5.8.4 MDC Clock

The IXF1010 MAC device supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input/Output (MDIO) Interface. The IXF1010 MAC meets the following specification for this clock:

- 2.5 V CMOS drive
- 2.5/18 MHz operation (selectable by the MDC speed bit in the MDI Control Register)
- 50/50 duty cycle for 2.5 MHz operation
- 43/57 duty cycle for 18 MHz operation

5.8.5 JTAG Clock

The IXF1010 MAC supports JTAG. The source of this clock must meet the following specifications:

- 2.5 V CMOS drive
- Maximum clock frequency 11 MHz
- Maximum duty cycle distortion 40/60

5.8.6 LED Clock

The IXF1010 MAC supports a serial LED data stream. This interface implements a 2.5 V CMOS output clock with a maximum frequency of 720 Hz.

The IXF1010 MAC supports a serial LED data stream. The IXF1010 MAC meets the following specifications for this clock:

- 2.5 V CMOS drive
- Maximum frequency of 720 Hz
- Maximum duty cycle distortion: 50/50

6.0 Applications

6.1 Power Supply Sequencing

Follow the power-up and power-down sequence described in this section to ensure correct IXF1010 MAC operation. The sequence covers all IXF1010 MAC digital and analog supplies.

Caution: Failure to follow the power-up and power-down sequences will damage the IXF1010 MAC.

6.1.1 Power-Up Sequence

Ensure that the 1.8 V supplies (VDD/AVDD1P8_1) are applied and stable prior to the application of the 2.5 V supplies (VDD2/AVDD2P5_1).

Caution: If the 2.5 V supplies (VDD2/AVDD2P5_1) exceed the 1.8 V (VDD/AVDD1P8_1) supplies by more than 2.0 V during power-up, the ESD structures within the analog I/Os can be damaged.

6.1.2 Power-Down Sequence

The power-down sequence is the reverse of the power-up sequence. Remove the 2.5 V supplies prior to removing the 1.8 V supplies.

Figure 27 and Table 31 provide information on power sequencing.

Note: If the 2.5 V supplies (VDD2/AVDD2P5_1) exceed the 1.8 V (VDD/AVDD1P8_1) supplies by more than 2.0 V during power-down, damage can occur to the ESD structures within the analog I/Os.

Figure 27 Power Sequencing

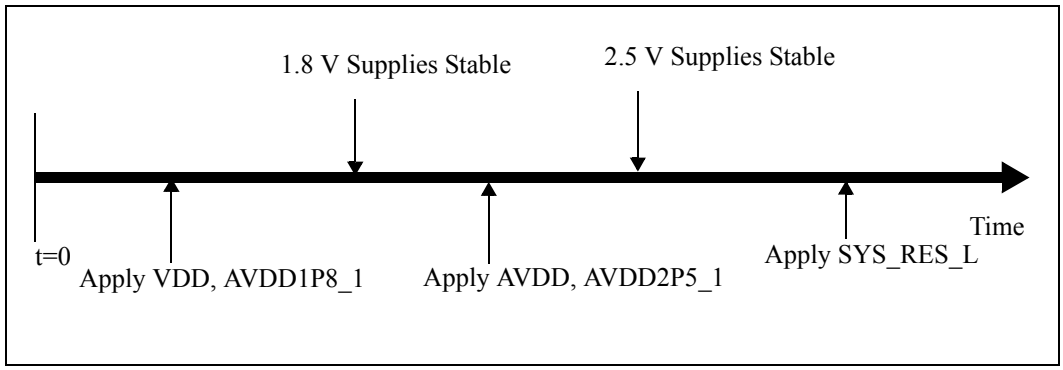


Table 31 Power Sequencing

Power Supply	Power-Up Order	Time Delta to Next Supply[1]	Description
VDD, AVDD1P8_1	First	0	1.8 V supplies
VDD2, AVDD2P5_1	Second	10 µs	2.5 V supplies

1. The value of 10 µs given is a nominal value only. The exact time difference between the application of the 2.5 V analog supply will be determined by a number of factors dependent on the power management method used.

6.2 Analog Power Filtering

Figure 28 illustrates an analog power supply filter network and Table 32 lists the analog power balls.

Figure 28 Analog Power Supply Filter Network

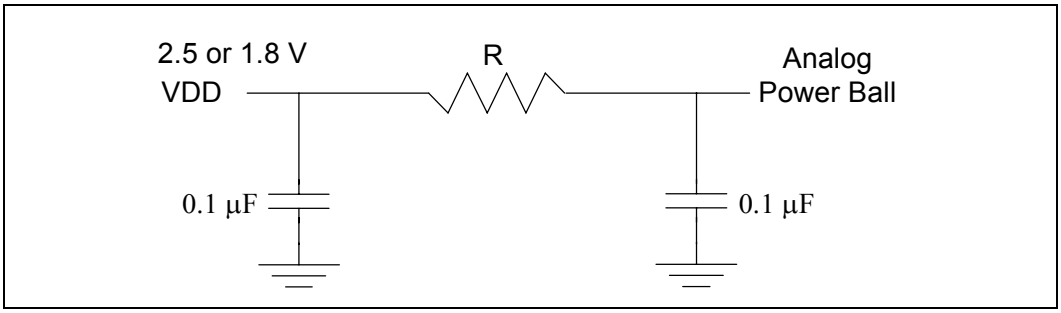


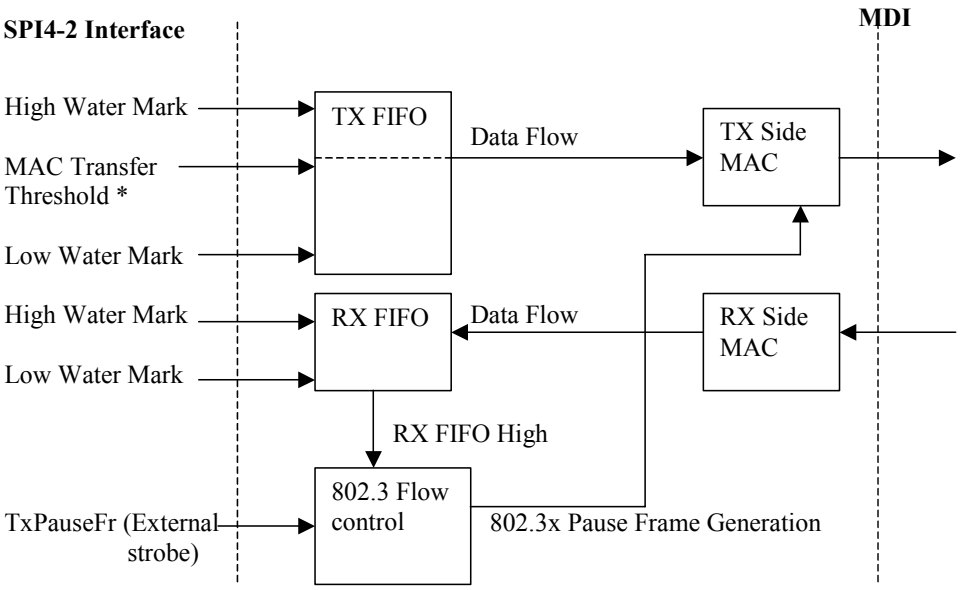
Table 32 Analog Power Balls

Signal Name	Ball Designator	Comments
AVDD1P8_1	D1 E24	Need to provide a filter (see Figure 28). **R:** AVDD1P8_1 and AVDD2P5_1 = 5.6 Ω resistor.
AVDD2P5_1	Y1	

6.3 TX FIFO and RX FIFO Operation

The IXF1010 MAC packet buffering is comprised of individual port FIFOs and system-interface FIFOs. Figure 29 illustrates the interaction of these FIFOs.

Figure 29 Packet Buffering FIFO



Note: The MAC Transfer Threshold determines when the transmit data is transferred from the TX FIFO to the TX side of the MAC. Once the data has been sent from the TX FIFO to the MAC, it will be transmitted to the PHY and cannot be flow controlled from the link partner.

6.3.1 TX FIFO

The IXF1010 MAC TX FIFOs are implemented with 4.5 KB for each port. This provides enough space for at least one maximum size packet per-port storage and ensures that no under-run conditions occur, assuming that the sending device can supply data at the required data rate.

Note: The TX FIFO High and Low Watermark must be programmed correctly to ensure that the TX FIFO does not overflow.

6.3.1.1 MAC Transfer Threshold

The *TX FIFO MAC Transfer Threshold Ports 0 to 9 ($ 0x614 - 0x61D)*, on page 154 parameter, which is user programmable, determines when data is transmitted out of the TX FIFO to the MAC. This parameter is configurable for specific block sizes and the user must ensure that an under-run does not occur. The threshold must be set to a value that exceeds the programmed MaxBurst1 parameter from the Network Processor (NPU) or SPI4-2 ASIC. This method of operation eliminates the possibility of under-run, except when the controlling NPU device fails.

The MAC transfer threshold operates on a per packet basis. Once the number of bytes of a packet received in the TX FIFO exceeds the MAC transfer threshold, it will start to be transmitted to the MAC. If the MAC transfer is greater than the packet size, the packet is sent to the MAC once an EOP is received.

The MAC transfer threshold should be set below the *TX FIFO High Watermark Ports 0 to 9 ($ 0x600 - 0x609)*, on page 150. If the MAC transfer threshold is set above the TX FIFO high watermark, the TX FIFO high watermark will act as the MAC transfer threshold. Data is transmitted out of the TX FIFO to the MAC when the TX FIFO high watermark is reached.

6.3.1.2 TX FIFO Relation to the SPI4-2 Transmit FIFO Status (TSTAT)

The amount of data in the TX FIFO dictates the FIFO status sent to the NPU on the TSTAT bus. The following lists how the FIFO status is determined from the TX FIFO High and Low Watermarks.

SATISFIED: The status given for a port when the amount of data in the per port TX FIFO is greater than the programmed *TX FIFO High Watermark Ports 0 to 9 ($ 0x600 - 0x609)*, on page 150.

HUNGRY: The status given for a port when the amount of data in the per port TX FIFO is between the programmed *TX FIFO High Watermark Ports 0 to 9 ($ 0x600 - 0x609)*, on page 150 and the *TX FIFO Low Watermark Ports 0 to 9 ($ 0x60A - 0x613)*, on page 152.

STARVING: The status given for a port when the amount of data in the per port TX FIFO is below the programmed value in *TX FIFO Low Watermark Ports 0 to 9 ($ 0x60A - 0x613)*, on page 152.

Note: The user must ensure the TX FIFO High and Low Watermarks are programmed correctly to ensure no underrrun or overflow occur. Failure to do this may result in packet loss.

6.3.1.3 TX FIFO Drain

The IXF1010 MAC can allow the SPI4-2 NPU or ASIC to dump data to the IXF1010 MAC while the link is down. This allows the NPU or ASIC to empty its FIFOs, if necessary.

The IXF1010 MAC operates in the following manner under normal operating conditions:

The TX FIFO status bus for a given port reports the status based on the amount of data in the TX FIFO.

The IXF1010 MAC operates in the following the manner when the TX FIFO drain is enabled:

The SPI4-2 FIFO status bus indicates STARVING for the given port. This tells the NPU or ASIC that it can pass data to the IXF1010 MAC for that port, regardless of the link status, and all data sent to that port will be discarded.

Note: The TX FIFO drain is enabled using the *TX FIFO Drain ($0x620)*, on page 157.

6.3.1.3.1 Enabling the TX FIFO Drain

The TX FIFO drain is enabled using the *TX FIFO Drain ($0x620)*, on page 157. The following occurs when the TX FIFO drain is enabled for a given port:

- The TX FIFO is held in reset

- The FIFO status for that port indicates SATISFIED
- All data sent to that port is discarded

6.3.1.3.2 Putting the TX FIFO in Drain Mode

Use the TX FIFO drain when the link is down. The following is a step-by-step sequence to put a port(s) into the TX FIFO drain mode:

1. The system detects that link is down for a given port using information from the PHY. The SPI4-2 TX FIFO status reports the actual FIFO status.
2. Set the appropriate bit to 1 for the given port in the TX FIFO Drain Register ($0x620) once link is down. This incurs the following:
   a. Enables the drain mode
   b. Causes the TX FIFO for the selected port to enter a reset state
   c. Causes the TX FIFO SPI4-2 FIFO status for that port to change to STARVING.
3. Set the MAC Soft Reset Register bit to 1 for the port(s) that has entered the TX FIFO drain mode.
4. De-assert the MAC Soft Reset Register. Redo the MAC configurations.
5. The connected SPI4-2 NPU or ASIC can now dump data to the port(s) that has entered the drain mode. All data sent to the port(s) selected is discarded and not recorded in any IXF1010 MAC register.
6. Monitor the attached PHY to reestablish link with the link partner. Once the system software detects link establishment, the TX FIFO drain mode must be exited. The TX FIFO status bus reports the actual TX FIFO status once the TX FIFO drain mode is exited.

6.3.1.3.3 Exiting the TX FIFO Drain Mode

To exit the TX FIFO drain mode.

1. Set the TX FIFO Drain Register bits back to 0. This exits the TX FIFO drain mode and the TX FIFO status bus now indicates the actual TX FIFO status.
2. The IXF1010 MAC is ready to resume normal data transmission.

6.3.2 RX FIFO

The IXF1010 MAC RX FIFOs are provisioned so that each port has its own 17.0 KB memory space. This is enough memory to ensure against an over-run on any port while transferring normal Ethernet frame-size data.

The RX FIFOs are configured by default to automatically generate Pause control frames to initiate the following:

- Halt the link partner when the RX FIFO High Watermark is reached
- Restart the link partner when the data stored in the RXFIFO falls below the Low Watermark.

Pause control frame generation is enabled by default in the *FC Enable ($ Port_Index + 0x12)*, on page 119. *Global RX Block Register Overview*, on page 141 documents the registers needed to set the RX FIFO watermarks.

Note: Users should ensure that flow control is enabled to prevent RX FIFO overflows. If an RX FIFO overflow occurs, data is sent out on the SPI4-2 interface regardless of the *RX FIFO*

Errored Frame Drop Enable ($ 0x59F), on page 147 settings. The data is marked with an EOP abort code to inform the upstream device that this data is corrupted.

6.4 Reset and Initialization

When powering up the IXF1010 MAC, the hardware reset signal (SYS_RES_L) should be held active Low for a minimum of 100 ns after all of the power rails have fully stabilized to their nominal values and the input clocks have reached their nominal frequency (TDCLK = 400 MHz, CLK125 = 125 MHz, and CLK50 = 50 MHz).

Note: In systems where the SYS_RES_L pin is driven from a single board-wide reset signal, the switch or network processor only comes out of reset at the same time as the IXF1010 MAC, or possibly later. This means the TDCLK may not be applied to the IXF1010 MAC when the SYS_RES_L pin is released. However, the system designer must ensure that the switch or network processor does not output TDCLK until it is stable and has reached its nominal operating frequency. Failure to apply a stable TDCLK to the IXF1010 MAC can result in the IXF1010 MAC training on a non-stable clock thus causing DIP4 errors and data corruption. This will require a re-training once the TDCLK is stable.

When the TDCLK is applied after the reset pin is released, a built-in feature in the IXF1010 MAC reactivates the internal reset once TDCLK is applied. The IXF1010 MAC extends this hardware reset internally to ensure synchronization of all internal blocks within the system. The internal reset is extended for a minimum of 4.11 ms after all clocks are stable.

The device is correctly initialized at this point and ready for use. Clocks start to appear at the relevant device ports and the SPI4-2 interface begins to source a training pattern on the receive side while waiting for a training pattern on the transmit side. The SPI4-2 interface synchronizes with the connected switch or network processor per the SPI4-2 Specification.

The CPU accesses can begin to configure the device for any existing user preferences desired.By default, all ports on the IXF1010 MAC are enabled after power-up. The device is ready for use at this time if the default settings are to be used. Otherwise, access the required registers via the CPU interface and configure the control registers to the required settings.

6.4.1 SPI4-2 Initialization

6.4.1.1 RX SPI4-2

After reset or Power-up the RX SPI4-2 interface will start to source training patterns on the data bus to the upstream SPI4-2 device. The IXF1010 MAC will continue to send the training patterns until a valid calendar is sent on RSTAT[1:0] from the upstream device to the IXF1010 MAC. At this point, synchronization with the upstream device is complete and the IXF1010 MAC will start to send data once data is available and a credit has been granted from the RSTAT[1:0] bus.

When synchronization is completed, bit 13 of the *SPI4-2 RX Calendar ($ 0x702)*, on page 163 is “1”. Before completion, bit 13 is “0”, indicating the IXF1010 MAC is sending out training patterns on the RX SPI4-2 data bus.

6.4.1.2 TX SPI4-2

After reset or power-up, the TX SPI4-2 interface outputs a constant framing pattern on TSTAT until it receives the proper SPI4-2 training pattern from the upstream SPI4-2 device. For more information on the required training pattern, see Section 5.2.3, *Dynamic Phase Alignment Training Sequence (Data Path De-skew)*, on page 60.

Note: If TDCLK is applied to the IXF1010 MAC after the device has come out of reset, the system designer must ensure the TDCLK is stable when applied. Failure to due so can result in the IXF1010 MAC training on a non-stable clock, causing DIP4 errors and data corruption.

Once the valid training pattern is received and the IXF1010 MAC outputs a 10-port calendar on TSAT, bit 12 of the *SPI4-2 RX Calendar ($ 0x702)*, on page 163 will be set. This indicates that synchronization on the TX SPI4-2 is complete.

Ports will show a SATISFIED status on the SPI4-2 TSTAT bus until a valid link is established for that port.

6.4.1.3 RGMII

The RGMII interface is ready for operation after power-up or reset. The user must ensure the RGMII clock is delayed 1.5 to 2.8 ns relative to the data with additional board trace per the RGMII specification. (Refer to Section 5.3, *Reduced Gigabit Media Independent Interface (RGMII)*, on page 65 for more information.)

6.4.1.4 CPU

The CPU interface is ready for operation after power-up or reset. Through this interface, the user can configure the device for any desired setting from the defaults. (Refer to Section 5.6, *CPU Interface*, on page 78 for more information.)

6.5 IXF1010 MAC Unused Ports

Cortina recommends the following be used to disable an unused port. The SPI4-2 TSTAT status bus will always reflect status for ten ports regardless of the number of IXF1010 MAC unused ports. Any port which is disabled will have a constant status of SATISFIED. RSTAT must also be input to reflect the status of all ten ports regardless of how many are disabled.

1. Disable the ports not being used in the *Port Enable ($ 0x500)*, on page 136.
2. Leave TXC, TD[3:0], and TX_CTL unconnected for unused ports.
3. For the inputs, tie RXC, RD[3:0], and RX_CTL to ground.

7.0 Electrical Specifications

Table 33 through Table 48 on page 106 and Figure 34 on page 100 through Figure 41 on page 105 represent the target specifications of the following IXF1010 MAC interfaces:

- Section 7.3, *RGMII Timing Specifications*
- Section 7.4, *MDIO Timing Specifications*
- Section 7.5, *CPU Timing Specification*
- Section 7.6, *JTAG Timing Specification*
- Section 7.7, *Transmit Pause Control Timing Specifications*
- Section 7.8, *System Timing Specifications*
- Section 7.9, *LED Timing Specifications*
- Section 7.10, *SPI4-2 Timing Specifications*

Note: These specifications are not guaranteed and are subject to change without notice. Minimum and maximum values listed in Table 35 through Table 48 on page 106 apply over the recommended operating conditions specified in Table 33.

Table 33 Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
Supply Voltage		VDD	-0.3	2.4	Volts
		AVDD1P8_1	-0.3	2.4	Volts
		VDD2	-0.3	3.0	Volts
		AVDD2P5_1	-0.3	3.0	Volts
Operating Temperature	Ambient	TOPA	-15	+85	°C
	Case	TOPC	–	+130	°C
Storage Temperature		TST	-65	+125	°C
Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.					

Table 34 Operating Conditions (Sheet 1 of 2)

Parameter	Symbol	Min	Typ[1]	Max	Units
Recommended Supply Voltage	VDD, AVDD1P8_1	1.71	1.80	1.89	Volts
	VDD2, AVDD2P5_1	2.375	2.50	2.625	Volts
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing. 2. Refer to the Cortina Systems® IXF1010 MAC Thermal Design Guidelines (document number 250288).					

Table 34 Operating Conditions (Sheet 2 of 2)

Parameter		Symbol	Min	Typ[1]	Max	Units
Operating Current	1000BASE-T	IDD, AIDD1P8_1	–	2.062	2.59	Amps
		IDD2, AIDD2P5_1	–	0.432	0.64	Amps
Recommended Operating Temperature[2]	Ambient	TOPA	0	–	70	°C
	Case with Heat Sink	TOPC-HS	0	–	118	°C
	Case without Heat Sink	TOPC-NHS	0	–	119	°C
Recommended Storage Temperature		TOST	-65	–	40	°C
Power Consumption	1000BASE-T full-duplex all ports enabled and passing data	P	–	4.8	6.6	Watts

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Refer to the Cortina Systems® IXF1010 MAC Thermal Design Guidelines (document number 250288).

7.1 DC Specifications

Table 35 2.5 V LVTTL and CMOS I/O Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low Voltage	V_{IL}	–	–	0.70	V	VCC = MIN
Input High Voltage[2]	V_{IH}	1.7	–	3.6	V	VCC = MIN
Output Low Voltage RGMII	VOLRG	–	–	0.40	V	VCC=MIN, IOL=6.9mA
Output Low Voltage All Others	V_{OL}	–	–	0.40	V	VCC = MIN, IOL = 3.9 mA
Output High Voltage RGMII	VOHRG	2.0	–	–	V	VCC=MIN, IOH=-5.2mA
Output High Voltage All Others	V_{OH}	2.0	–	–	V	VCC = MIN, IOH = -2.9 mA
Output Leakage Current	I_{OZ}	–	–	10	µA	VCC = MAX

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. 3.3 V CMOS tolerant.

Table 36 LVDS I/O Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Voltage Range	VI	-0.20	–	VddMax+ 0.20	V	–
Differential Input Voltage	|VID|	100	–	–	mV	@ 400 MHz
Input Common-Mode Current	ICM	–	–	–	µA	LVDS Input VOS = 1.2 V
Threshold Hysteresis	TH	25	–	–	mV	–
Differential Input Impedance	RIN	85	100	115	Ω	Typical 100 Ω
Output Low Voltage	VOL	0.95	–	–	V	–
Output High Voltage	VOH	–	–	1.51	V	–
Differential Output Voltage	|VOD|	330	–	446	mV	–
Delta Differential Output Voltage (Complementary States)	Δ|VOD|	–	–	25	mV	–
Offset (Common-Mode) Voltage	VOS	1.12	–	1.30	V	–
Output Leakage Current	IOZ	–	–	10	µA	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

7.2 Undershoot/Overshoot Specifications

The overshoot figures given in this section represent the maximum voltage that can be applied without affecting the reliability of the device (see Table 37).

Caution: Exceeding these values will damage the device.

Table 37 Undershoot/Overshoot Limits

Ball Type	Undershoot	Overshoot
2.5 V CMOS	-0.60 V	3.9 V
2.5 V LVTTL	-0.60 V	3.9 V

7.3 RGMII Timing Specifications

Figure 30 RGMII 1000 Mbps Multiplexing and Timing

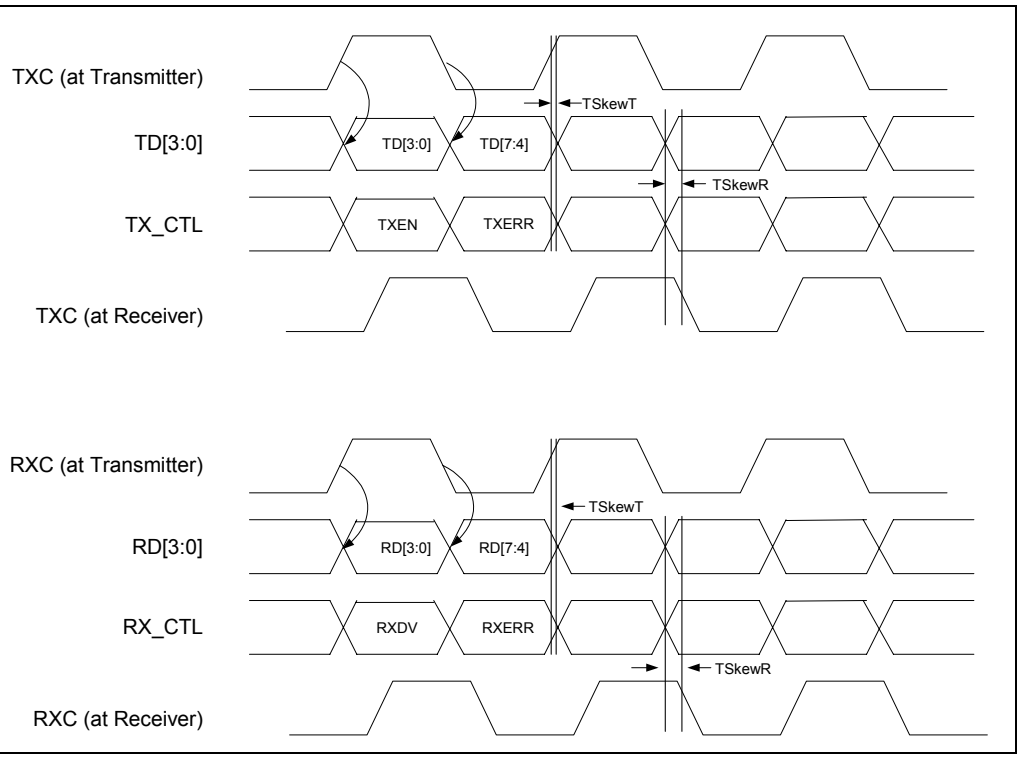


Table 38 RGMII 1000 Mbps Timing Specifics

Parameter	Symbol	Min	Typ[4]	Max	Units	Test Conditions
Data-to-Clock Output Skew (at Transmitter)	TskewT	-500	0	500	ps	–
Data-to-Clock Input Skew (at Receiver)[1]	TskewR	1	1.5	2.8	ns	–
Clock Cycle Duration[2]	Tcyc	7.2	8	8.8	ns	–
Duty Cycle for Gigabit[3]	Duty_T	45	50	55	%	–
Rise/Fall Time (20-80%)	Tr/Tf	–	–	0.75	ns	–

1. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
2. For 100 Mbps, Tcyc scales to 40 ns +/- 4 ns.
3. Duty cycle may be stretched/shrunk during speed changes or while transtioning to a received packet's clock domain, as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.
4. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 39 RGMII I/O Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Output High Voltage	V_{OH}	2.0	–	V_{DD} +.3	V	I_{OH} = -1.0 mA; V_{DD} = Min
Output Low Voltage	V_{OL}	GND -.3	–	0.40	V	I_{OL} = 1.0 mA; V_{DD} = Min
Input High Voltage	V_{IH}	1.7	–	V_{DD} +.3	V	V_{IH} > V_{IH_Min}; V_{DD} = Min
Input Low Voltage	V_{IL}	–	–	.70	V	V_{IH} > V_{IL_Max}; V_{DD} = Min
Input High Current	I_{IH}	–	–	15	µA	V_{DD} = Max; V_{IN} = 2.5V
Input Low Current	I_{IL}	-15	–	–	µA	V_{DD} = Max; V_{IN} = 0.4V

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 31 RGMII 100 Mbps Multiplexing and Timing

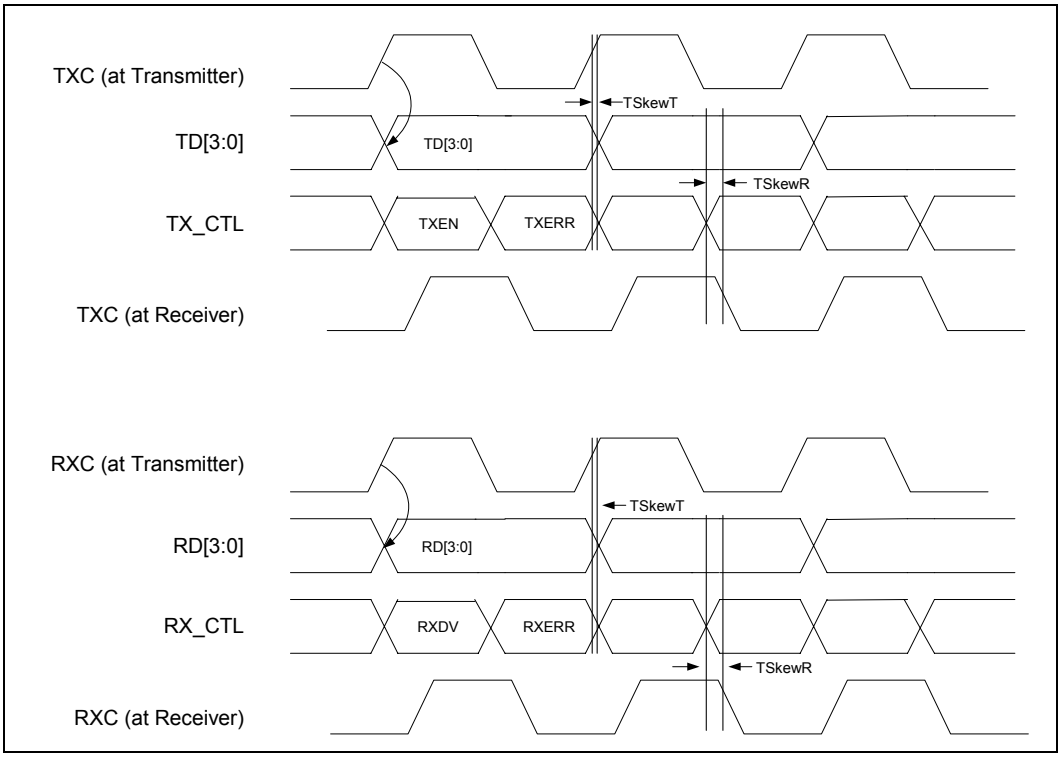


Table 40 RGMII 100 Mbps Timing Specifics

Parameter	Symbol	Min	Typ[4]	Max	Units	Test Conditions
Data-to-Clock Output Skew (at Transmitter)	TskewT	-500	0	500	ps	–
Data-to-Clock Input Skew (at Receiver)[1]	TskewR	1	1.5	2.8	ns	–
Clock Cycle Duration[2]	Tcyc	36	40	44	ns	–
Duty Cycle for 100T[3]	Duty_G	40	50	60	%	–
Rise/Fall Time (20-80%)	Tr/Tf	–	–	.75	ns	–

1. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
2. For 100 Mbps, Tcyc scales to 40 ns +/- 4 ns.
3. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain, as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.
4. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

7.4 MDIO Timing Specifications

Figure 32 MDIO Write Timing

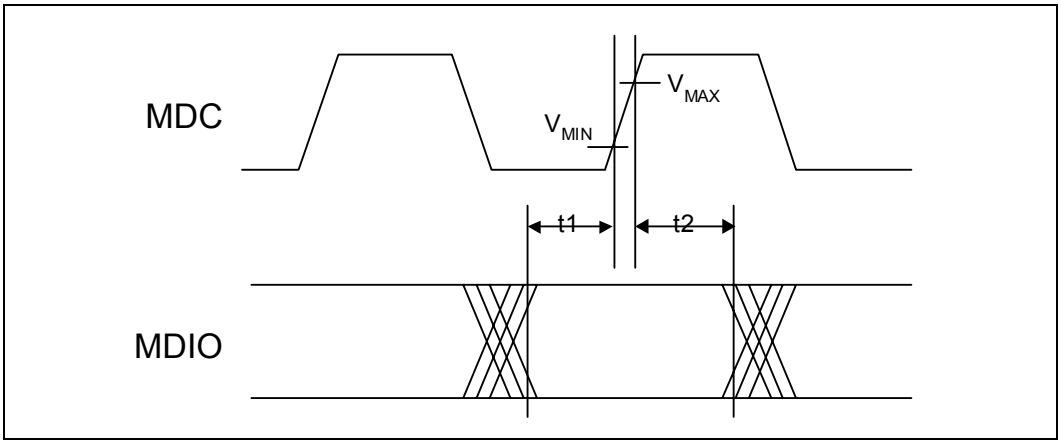


Figure 33 MDIO Read Timing

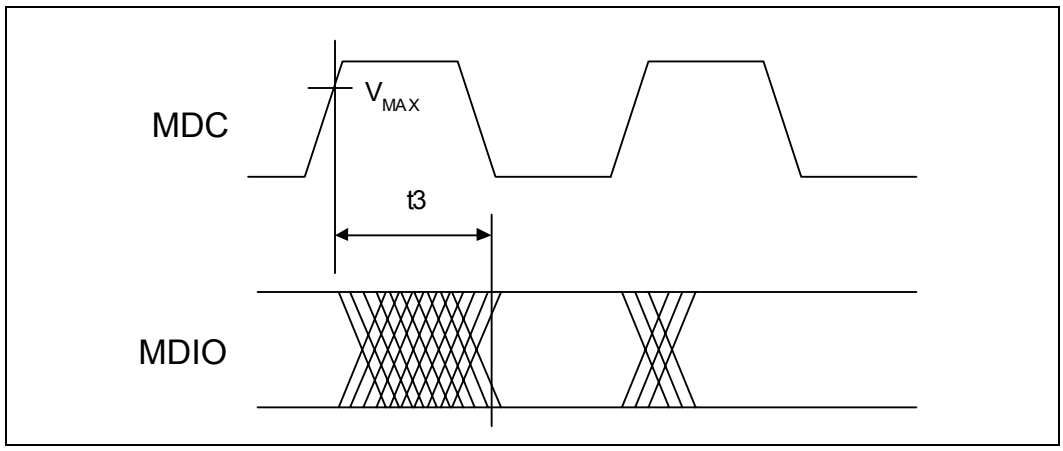


Table 41 MDIO Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
MDIO Setup before MDC.	t1	10	–	–	ns	MDC = 17.8 MHz
		10	–	–	ns	MDC = 2.5 MHz
MDIO Hold after MDC.	t2	10	–	–	ns	MDC = 17.8 MHz
		10	–	–	ns	MDC = 2.5 MHz
MDC to MDIO Output delay	t3	0	–	42	ns	MDC = 17.8 MHz
		0	–	300	ns	MDC = 2.5 MHz

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

7.5 CPU Timing Specification

Figure 34 CPU Port Read Timing

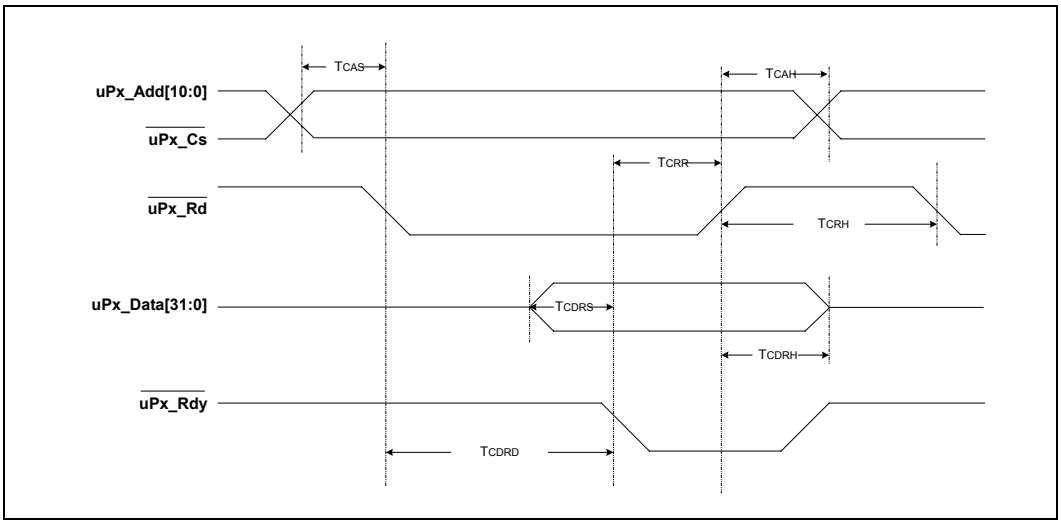


Figure 35 CPU Port Write Timing

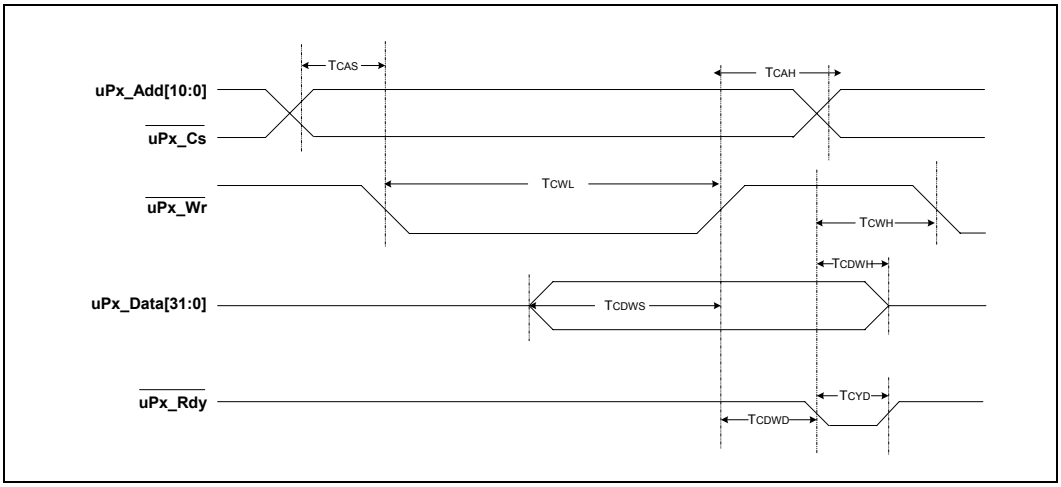


Table 42 CPU Timing Parameters (Sheet 1 of 2)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
UPX_ADD[12:0], UPX_CS_L Setup Time	TCAS	10	–	–	ns	–
UPX_ADD[12:0], UPX_CS_L Hold Time	TCAH	10	–	–	ns	–
UPX_RDY_L Assertion to UPX_RD_L De-assertion	TCRR	10	–	–	ns	–
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Table 42 CPU Timing Parameters (Sheet 2 of 2)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
UPX_RD_L High Width	TCRH	24 (3x cycle)	–	–	ns	–
UPX_DATA[31:0] to UPX_RDY_L Setup Time	TCDRS	10	–	–	ns	–
UPX_DATA[31:0] to UPX_RD_L Hold Time	TCDRH	8	–	32	ns	–
Read UPX_DATA[31:0] Driving Delay	TCDRD	24	–	355	ns	–
UPX_WR_L Width	TCWL	40	–	–	ns	–
UPX_RDY_L to UPX_WR_L Hold Time	TCWH	16	–	–	ns	–
UPX_DATA[31:0] to UPX_WR_L Setup Time	TCDWS	10	–	–	ns	–
UPX_RDY_L to UPX_DATA[31:0] Hold Time	TCDWH	10	–	–	ns	–
UPX_DATA[31:0] Latching Delay	TCDWD	8	–	40	ns	–
UPX_RDY_L Width in Write Cycle	TCYD	24	–	40	ns	–
Read UPX_RDY_L de-assertion to UPX_WR_L Assertion	TRTW	32	–	–	ns	–
Write UPX_RDY_L de-assertion to UPX_RD_L Assertion	TWTR	32	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

7.6 JTAG Timing Specification

Figure 36 JTAG Timing

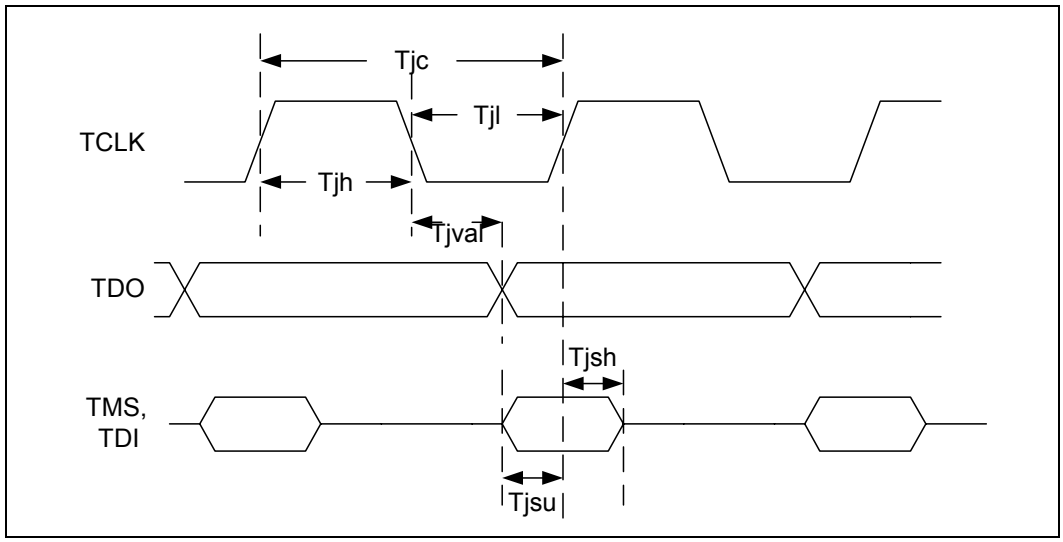


Table 43 JTAG Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
TCLK Cycle Time	TJC	90	–	–	ns	–
TCLK High Time	TJH	0.4 x TJC	–	0.6 x TJC	ns	–
TCLK Low Time	TJL	0.4 x TJC	–	0.6 x TJC	ns	–
TCLK Falling Edge to TDO Valid	TJVAL	–	–	25	ns	–
TMS/TDI Setup to TCLK	TJSU	20	–	–	ns	–
TMS/TDI Hold from TCLK	TJSH	5	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

7.7 Transmit Pause Control Timing Specifications

Figure 37 Transmit Pause Control Interface

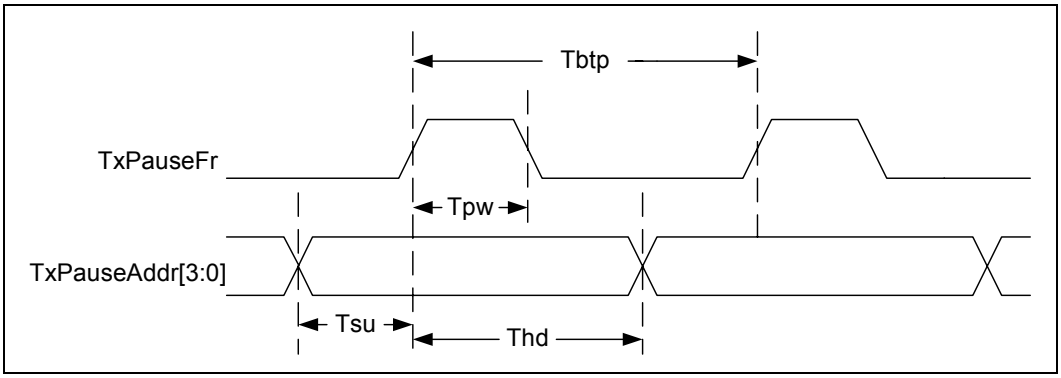


Table 44 Transmit Pause Control Interface Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
TXPAUSEFR Width	TPW	16	–	–	ns	–
TXPAUSEADDR[3:0] Setup to TXPAUSEFR	TSU	16	–	–	ns	–
TXPAUSEADDR[3:0] Hold from TXPAUSEFR	THD	32	–	–	ns	–
TXPAUSEFR Pulse to Pulse	TBTP	48	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

7.8 System Timing Specifications

Figure 38 Hardware Reset Timing

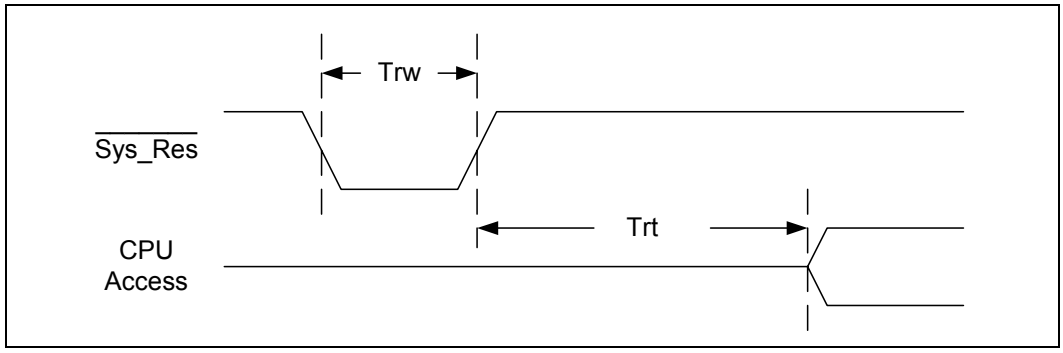


Table 45 Hardware Reset Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Reset Pulse Width	TRW	100	–	–	ns	–
Reset Recovery Time	TRT	4.11	–	–	ms	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

7.9 LED Timing Specifications

Figure 39 LED Timing

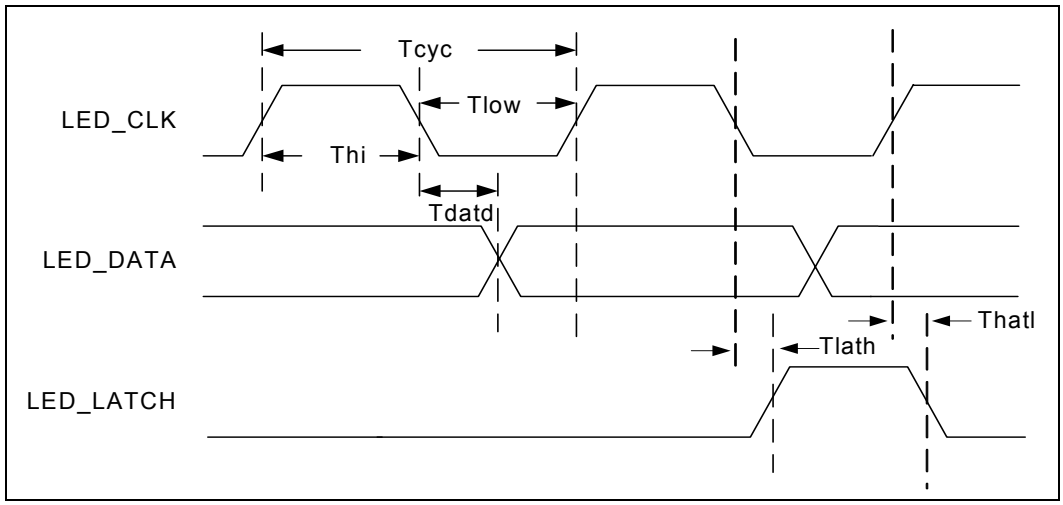


Table 46 LED Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions[2]
LED_CLK Cycle Time	TCYC	1.36	–	1.40	ms	–
LED_CLK High Time	THI	680	–	700	µs	50% duty cycle
LED_CLK Low Time	TLOW	680	–	700	µs	50% duty cycle
LED_CLK Falling Edge to LED_DATA Valid	TDATD	2	–	5	ns	–
LED_CLK Rising Edge to LED_LATCH Falling Edge	THATL	690	–	700	µs	–
LED_CLK Falling Edge to LED_LATCH Rising Edge	TLATH	690	–	700	µs	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Flash Rate = 100 ms, LED Mode 1.

7.10 SPI4-2 Timing Specifications

Figure 40 SPI4-2 Transmit FIFO Status Bus Timing

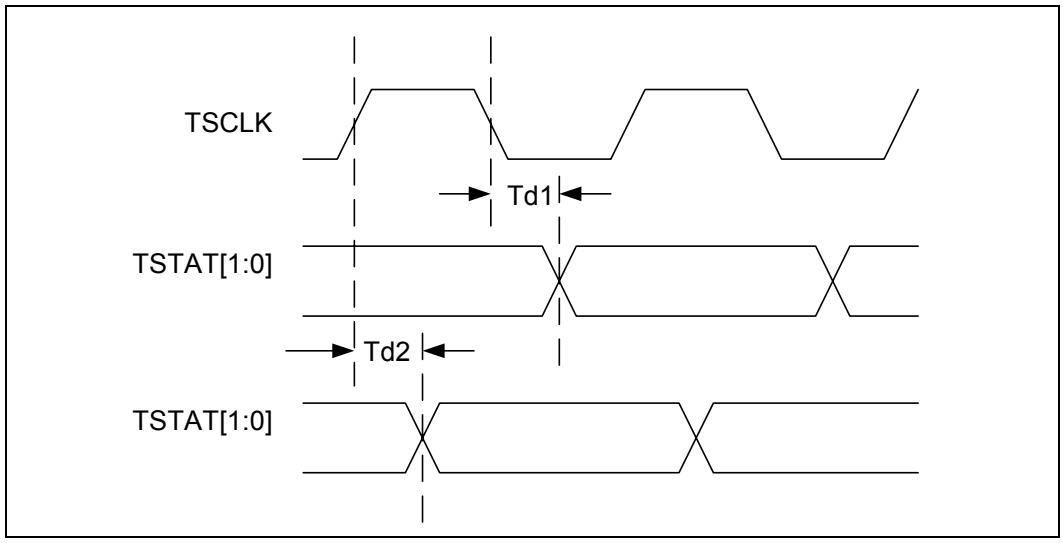


Table 47 SPI4-2 Transmit FIFO Status Bus Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
TSCLK Falling Edge to TSTAT[1:0] Valid (Active edge flipped to falling)	TD1	–	–	280	pS	–
TSCLK Rising Edge to TSTAT[1:0] Valid (Default operation)	TD2	–	–	280	pS	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 41 SPI4-2 Receive FIFO Status Bus Timing

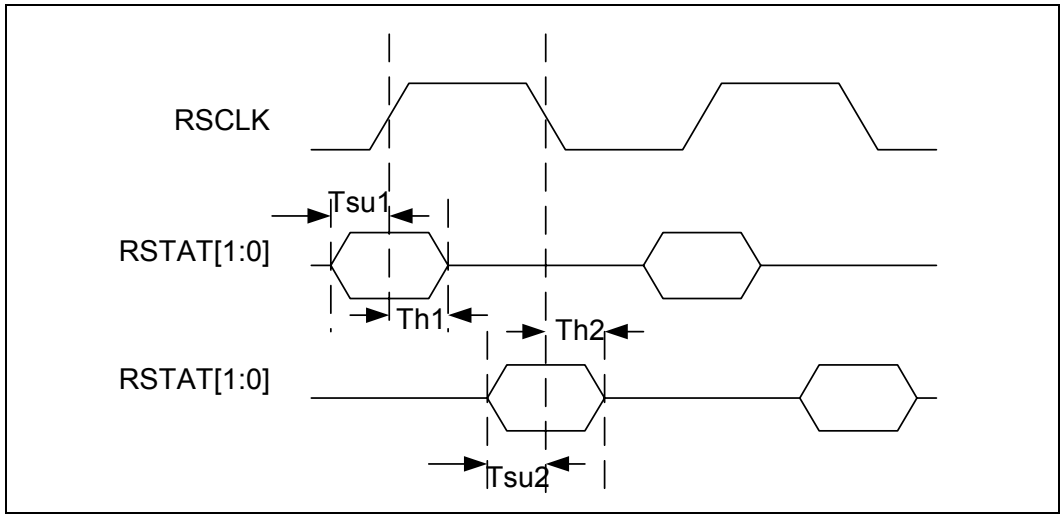


Table 48 SPI4-2 Receive FIFO Status Bus Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
RSTAT[1:0] Setup to RSCLK Rising Edge (Default operation)	TSU1	2	–	–	ns	–
RSTAT[1:0] Hold From RSCLK Rising Edge (Default operation)	TH1	0.5	–	–	ns	–
RSTAT[1:0] Setup to RSCLK Falling Edge (When active edge flipped to falling)	TSU2	2	–	–	ns	–
RSTAT[1:0] Hold From RSCLK Falling Edge (When active edge flipped to falling)	TH2	0.5	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 49 SPI4-2 LVDS Rise/Fall Times

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Rise/Fall at source	RTsrc	–	–	0.2	ns	400 Mhz operation – measured using conditions set forth in ANSI/TIA/EIA-644-A-2001
Rise/Fall at sink	RTsnk	–	–	0.4	ns	400 Mhz operation – measured using conditions set forth in ANSI/TIA/EIA-644-A-2001

8.0 Register Definitions

8.1 Introduction

This section provides information on the location and functionality of the IXF1010 MAC Control and Status Registers.

8.2 Document Structure

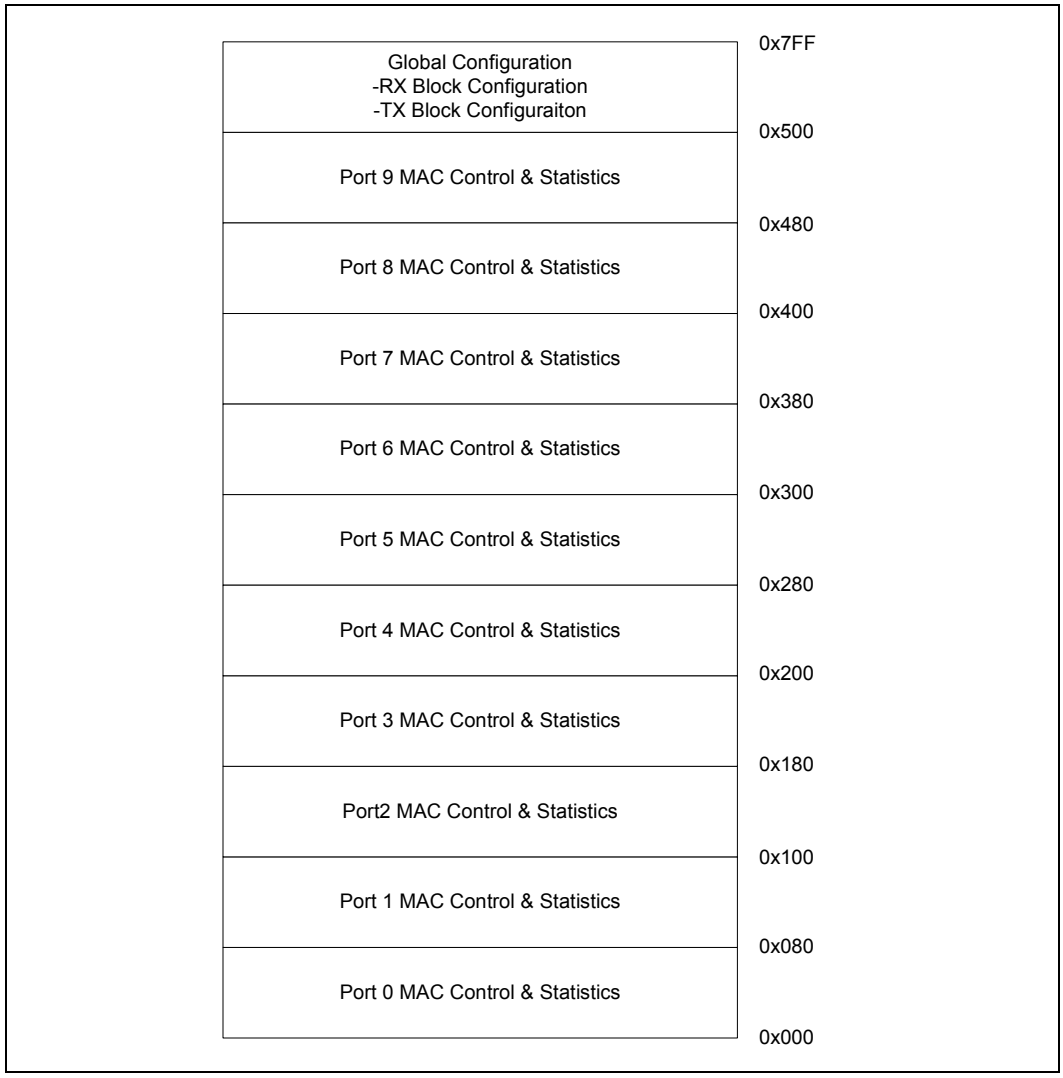
This document is structured to give a general overview of the register map and an in-depth description of each bit of a register in later sections.

8.3 Graphical Representation

Figure 42 represents an overview of the IXF1010 MAC Global Control Status Registers that are used to configure or report on all ports.

Caution: Do not write to any reserved register unless specified. Writing to a reserved register address may cause improper device operation.

Figure 42 Memory Overview

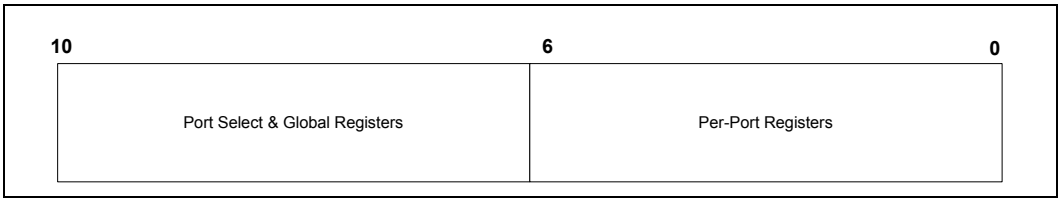


8.4 Per Port Registers

The following section covers all of the registers that are replicated in each of the 10 ports in the IXF1010 MAC. These registers perform an identical function in each port.

The address vector for the IXF1010 MAC is 11 bits wide. This allows for 7 bits of port-specific access and a 4-bit vector to address each port and all global registers. The address format is shown in Figure 43.

Figure 43 Register Overview



8.5 Memory Map

Table 50 through Table 58 on page 116 provide theIXF1010 MAC memory maps. A number of global control and status registers are used to configure or report on all ports, and some registers are replicated on a per-port basis.

Note: All registers in the IXF1010 MAC are 32 bits.

Table 50 MAC Control Register Map (Sheet 1 of 2)

Register	Bit Size	Mode[1]	Ref Page	Offset
MAC Control Registers (Port Index + Offset)				
Station Address Low ($ Port_Index + 0x00)	32	R/W	page 116	0x00
Station Address High ($ Port_Index + 0x01)	32	R/W	page 116	0x01
Reserved	32	RO	–	0x02
FDFC Type ($ Port_Index + 0x03)	32	R/W	page 117	0x03
Reserved	32	R	–	0x04
Reserved	32	RO	–	0x05
Reserved	32	RO	–	0X06
FC TX Timer Value ($ Port_Index + 0x07)	32	R/W	page 117	0x07
FDFC Address Low ($ Port_Index + 0x08)	32	R/W	page 117	0x08
FDFC Address High ($ Port_Index + 0x09)	32	R/W	page 117	0x09
Reserved	32	R	–	0x0A
Reserved	32	R	–	Ox0B
IPG Transmit Time ($ Port_Index + 0x0C)	32	R/W	page 118	0x0C
Reserved	32	R/W	--	0x0D
Pause Threshold ($ Port_Index + 0x0E)	32	R/W	page 118	0x0E
Max Frame Size ($ Port_Index + 0x0F)	32	R/W	page 118	0x0F
RGMII Speed	32	R/W	page 119	0x10
Reserved	32	RO	–	0x11
FC Enable ($ Port_Index + 0x12)	32	R/W	page 119	0x12
Reserved	32	RO	–	0x13
Short Runts Threshold ($ Port_Index + 0x14)	32	R/W	page 119	0x14

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 50 MAC Control Register Map (Sheet 2 of 2)

Register	Bit Size	Mode[1]	Ref Page	Offset
MAC Control Registers (Port Index + Offset)				
Discard Unknown Control Frame ($ Port_Index + 0x15)	32	R/W	page 120	0x15
Reserved	32	RO	–	0x16
Reserved	32	RO	–	0x17
Diverse Config ($ Port_Index + 0x18)	32	R/W	page 120	0x18
RX Packet Filter Control ($ Port_Index + 0x19)	32	R/W	page 121	0x19
Port Multicast Address Low ($ Port_Index + 0x1A)	32	R/W	page 122	0x1A
Port Multicast Address High ($ Port_Index + 0x1B)	32	R/W	page 122	0x1B
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 51 MAC RX Statistics Register Map (Sheet 1 of 2)

Register	Bit Size	Mode[1]	Ref Page	Offset
MAC RX Statistics Registers (Port Index + Offset)				
RXOctetsTotalOK	32	CoR	page 123	0x20
RXOctetsBAD	32	CoR	page 123	0x21
RXUCPckts	32	CoR	page 123	0x22
RXMCPkts	32	CoR	page 123	0x23
RXBCPkts	32	CoR	page 123	0x24
RXPkts64Octets	32	CoR	page 123	0x25
RXPkts65to127Octets	32	CoR	page 123	0x26
RXPkts128to255Octets	32	CoR	page 123	0x27
RXPkts256to511Octets	32	CoR	page 123	0x28
RXPkts512to1023Octets	32	CoR	page 123	0x29
RXPkts1024to1518Octets	32	CoR	page 123	0x2A
RXPkts1519toMaxOctets	32	CoR	page 123	0x2B
RXFCSErrors	32	CoR	page 123	0x2C
RXTagged	32	CoR	page 123	0x2D
RXDataError	32	CoR	page 123	0x2E
RXAlignErrors	32	CoR	page 123	0x2F
RXLongErrors	32	CoR	page 123	0x30
RXJabberErrors	32	CoR	page 123	0x31
RXPauseMacControlCounter	32	CoR	page 123	0x32
RXUnknownMacControlFrameCounter	32	CoR	page 123	0x33
RXVeryLongErrors	32	CoR	page 123	0x34
RXRuntErrors	32	CoR	page 123	0x35
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 51 MAC RX Statistics Register Map (Sheet 2 of 2)

Register	Bit Size	Mode[1]	Ref Page	Offset
MAC RX Statistics Registers (Port Index + Offset)				
RXShortErrors	32	CoR	page 123	0x36
RXCarrierExtendError	32	CoR	page 123	0x37
RXSequenceErrors	32	CoR	page 123	0x38
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 52 MAC TX Statistics Register Map

Register	Bit Size	Mode[1]	Ref Page	Offset
MAC TX Statistics Registers (Port Index + Offset)				
TXOctetsTotalOK	32	CoR	page 126	0x40
TXOctetsBad	32	CoR	page 126	0x41
TXUCPkts	32	CoR	page 126	0x42
TXMCPkts	32	CoR	page 126	0x43
TXBCPkts	32	CoR	page 126	0x44
TXPkts64Octets	32	CoR	page 126	0x45
TXPkts65to127Octets	32	CoR	page 126	0x46
TXPkts128to255Octets	32	CoR	page 126	0x47
TXPkts256to511Octets	32	CoR	page 126	0x48
TXPkts512to1023Octets	32	CoR	page 126	0x49
TXPkts1024to1518Octets	32	CoR	page 126	0x4A
TXPkts1519toMaxOctets	32	CoR	page 126	0x4B
TXDeferred	32	CoR	page 126	0x4C
TXTotalCollisions	32	CoR	page 126	0x4D
TXSingleCollisions	32	CoR	page 126	0x4E
TXMultipleCollisions	32	CoR	page 126	0x4F
TXLateCollisions	32	CoR	page 126	0x50
TXExcessiveCollisionErrors	32	CoR	page 126	0x51
TXExcessiveDeferralErrors	32	CoR	page 126	0x52
TXExcessiveLengthDrop	32	CoR	page 126	0x53
TXUnderrun	32	CoR	page 126	0x54
TXTagged	32	CoR	page 126	0x55
TXCRCError	32	CoR	page 126	0x56
TXPauseFrames	32	CoR	page 126	0x57
TXFlowControlCollisionsSend	32	CoR	page 126	0x58
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 53 PHY Autoscan Register Map

Register	Bit Size	Mode[1]	Ref Page	Offset
PHY Autoscan Registers (Port Index + Offset)				
PHY Control	32	R	page 129	0x60
PHY Status	32	R	page 130	0x61
PHY ID 1	32	R	page 131	0x62
PHY ID 2	32	R	page 132	0x63
Auto-Negotiation Advertisement	32	R	page 132	0x64
Auto-Negotiation Link Partner Base Page Ability	32	R	page 133	0x65
Auto-Negotiation Expansion	32	R	page 134	0x66
Auto-Negotiation Next Page Transmit	32	R	page 135	0x67
Reserved	32	R	--	0x68
Reserved	32	R	--	0x69
Reserved	32	R	--	0x6A
Reserved	32	R	--	0x6B
Reserved	32	R	--	0x6C
Reserved	32	R	--	0x6D
Reserved	32	R	--	0x6E
Reserved	32	R	--	0x6F
Vendor Specific	32	R	--	0x70
Vendor Specific	32	R	--	0x71
Vendor Specific	32	R	--	0x72
Vendor Specific	32	R	--	0x73
Vendor Specific	32	R	--	0x74
Vendor Specific	32	R	--	0x75
Vendor Specific	32	R	--	0x76
Vendor Specific	32	R	--	0x77
Vendor Specific	32	R	--	0x78
Vendor Specific	32	R	--	0x79
Vendor Specific	32	R	--	0x7A
Vendor Specific	32	R	--	0x7B
Vendor Specific	32	R	--	0x7C
Vendor Specific	32	R	--	0x7D
Vendor Specific	32	R	--	0x7E
Vendor Specific	32	R	--	0x7F

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 54 Global Status and Configuration Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
Global Status and Configuration Registers				
Port Enable ($ 0x500)	32	R/W	page 136	0x500
Reserved	32	R	–	0x501
Link LED Enable ($ 0x502)	32	R/W	page 137	0x502
Reserved	32	RO	–	0x503
Core Clock Soft Reset ($ 0x504)	32	R/W	page 138	0x504
MAC Soft Reset ($ 0x505)	32	R/W	page 138	0x505
MDIO Soft Reset	32	R/W	page 139	0x506
Reserved	32	R	–	0x507
CPU Interface ($ 0x508)	32	R/W	page 139	0x508
LED Control ($ 0x509)	32	R/W	page 139	0x509
LED Flash Rate ($ 0x50A)	32	R/W	page 140	0x50A
LED Fault Disable ($ 0x50B)	32	R/W	page 140	0x50B
JTAG ID Revision ($ 0x50C)	32	R/W	page 141	0x50C
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 55 RX Block Register Map (Sheet 1 of 2)

Register	Bit Size	Mode[1]	Ref Page	Address
RX Block Registers				
RX FIFO High Watermark Port 0	32	R/W	page 142	0x580
RX FIFO High Watermark Port 1	32	R/W	page 142	0x581
RX FIFO High Watermark Port 2	32	R/W	page 142	0x582
RX FIFO High Watermark Port 3	32	R/W	page 142	0x583
RX FIFO High Watermark Port 4	32	R/W	page 142	0x584
RX FIFO High Watermark Port 5	32	R/W	page 142	0x585
RX FIFO High Watermark Port 6	32	R/W	page 142	0x586
RX FIFO High Watermark Port 7	32	R/W	page 142	0x587
RX FIFO High Watermark Port 8	32	R/W	page 142	0x588
RX FIFO High Watermark Port 9	32	R/W	page 142	0x589
RX FIFO Low Watermark Port 0	32	R/W	page 143	0x58A
RX FIFO Low Watermark Port 1	32	R/W	page 143	0x58B
RX FIFO Low Watermark Port 2	32	R/W	page 143	0x58C
RX FIFO Low Watermark Port 3	32	R/W	page 143	0x58D
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 55 RX Block Register Map (Sheet 2 of 2)

Register	Bit Size	Mode[1]	Ref Page	Address
RX Block Registers				
RX FIFO Low Watermark Port 4	32	R/W	page 143	0x58E
RX FIFO Low Watermark Port 5	32	R/W	page 143	0x58F
RX FIFO Low Watermark Port 6	32	R/W	page 143	0x590
RX FIFO Low Watermark Port 7	32	R/W	page 143	0x591
RX FIFO Low Watermark Port 8	32	R/W	page 143	0x592
RX FIFO Low Watermark Port 9	32	R/W	page 143	0x593
RX FIFO Number of Frames Removed on Port 0	32	CoR	page 144	0x594
RX FIFO Number of Frames Removed on Port 1	32	CoR	page 144	0x595
RX FIFO Number of Frames Removed on Port 2	32	CoR	page 144	0x596
RX FIFO Number of Frames Removed on Port 3	32	CoR	page 144	0x597
RX FIFO Number of Frames Removed on Port 4	32	CoR	page 144	0x598
RX FIFO Number of Frames Removed on Port 5	32	CoR	page 144	0x599
RX FIFO Number of Frames Removed on Port 6	32	CoR	page 144	0x59A
RXFIFO Number of Frames Removed on Port 7	32	CoR	page 144	0x59B
RX FIFO Number of Frames Removed on Port 8	32	CoR	page 144	0x59C
RX FIFO Number of Frames Removed on Port 9	32	CoR	page 144	0x59D
RX FIFO Port Reset ($ 0x59E)	32	R/W	page 146	0x59E
RX FIFO Errored Frame Drop Enable ($ 0x59F)	32	R/W	page 147	0x59F
RX FIFO Overflow Event ($ 0x5A0)	32	CoR	page 149	0x5A0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 56 TX Block Register Map (Sheet 1 of 2)

Register	Bit Size	Mode[1]	Ref Page	Address
TX FIFO High Watermark Port 0	32	R/W	page 150	0x600
TX FIFO High Watermark Port 1	32	R/W	page 150	0x601
TX FIFO High Watermark Port 2	32	R/W	page 150	0x602
TX FIFO High Watermark Port 3	32	R/W	page 150	0x603
TX FIFO High Watermark Port 4	32	R/W	page 150	0x604
TX FIFO High Watermark Port 5	32	R/W	page 150	0x605
TX FIFO High Watermark Port 6	32	R/W	page 150	0x606
TX FIFO High Watermark Port 7	32	R/W	page 150	0x607
TX FIFO High Watermark Port 8	32	R/W	page 150	0x608
TX FIFO High Watermark Port 9	32	R/W	page 150	0x609
TX FIFO Low Watermark Port 0	32	R/W	page 150	0x60A

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 56 TX Block Register Map (Sheet 2 of 2)

Register	Bit Size	Mode[1]	Ref Page	Address
TX FIFO Low Watermark Port 1	32	R/W	page 152	0x60B
TX FIFO Low Watermark Port 2	32	R/W	page 152	0x60C
TX FIFO Low Watermark Port 3	32	R/W	page 152	0x60D
TX FIFO Low Watermark Port 4	32	R/W	page 152	0x60E
TX FIFO Low Watermark Port 5	32	R/W	page 152	0x60F
TX FIFO Low Watermark Port 6	32	R/W	page 152	0x610
TX FIFO Low Watermark Port 7	32	R/W	page 152	0x611
TX FIFO Low Watermark Port 8	32	R/W	page 152	0x612
TX FIFO Low Watermark Port 9	32	R/W	page 152	0x613
TX FIFO MAC Transfer Threshold Port 0	32	R/W	page 154	0x614
TX FIFO MAC Transfer Threshold Port 1	32	R/W	page 154	0x615
TX FIFO MAC Transfer Threshold Port 2	32	R/W	page 154	0x616
TX FIFO MAC Transfer Threshold Port 3	32	R/W	page 154	0x617
TX FIFO MAC Transfer Threshold Port 4	32	R/W	page 154	0x618
TX FIFO MAC Transfer Threshold Port 5	32	R/W	page 154	0x619
TX FIFO MAC Transfer Threshold Port 6	32	R/W	page 154	0x61A
TX FIFO MAC Transfer Threshold Port 7	32	R/W	page 154	0x61B
TX FIFO MAC Transfer Threshold Port 8	32	R/W	page 154	0x61C
TX FIFO MAC Transfer Threshold Port 9	32	R/W	page 154	0x61D
TX FIFO Overflow Event ($ 0x61E)	32	CoR	page 156	0x61E
Reserved	32	R	–	0x61F
TX FIFO Drain ($0x620)	32	R/W	page 157	0x620
TX FIFO Info Out-of-Sequence ($ 0x621)	32	CoR	page 158	0x621
TX FIFO Number of Frames Removed on Port 0	32	CoR	page 159	0x622
TX FIFO Number of Frames Removed on Port 1	32	CoR	page 159	0x623
TX FIFO Number of Frames Removed on Port 2	32	CoR	page 159	0x624
TX FIFO Number of Frames Removed on Port 3	32	CoR	page 159	0x625
TX FIFO Number of Frames Removed on Port 4	32	CoR	page 159	0x626
TX FIFO Number of Frames Removed on Port 5	32	CoR	page 159	0x627
TX FIFO Number of Frames Removed on Port 6	32	CoR	page 159	0x628
TX FIFO Number of Frames Removed on Port 7	32	CoR	page 159	0x629
TX FIFO Number of Frames Removed on Port 8	32	CoR	page 159	0x62A
TX FIFO Number of Frames Removed on Port 9	32	CoR	page 159	0x62B

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 57 MDIO Block Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
MDI Single Command	32	R/W	page 160	0x680
MDI Single Read and Write Data	32	R/W	page 161	0x681
Autoscan PHY Address Enable	32	R/W	page 161	0x682
MDI Control	32	R/W	page 161	0x683
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 58 SPI4-2 Block Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
SPI4-2 RX Burst Size ($ 0x700)	32	R/W	page 162	0x700
SPI4-2 RX Training ($ 0x701)	32	R/W	page 163	0x701
SPI4-2 RX Calendar ($ 0x702)	32	R/W	page 163	0x702
SPI4-2 TX Synchronization ($ 0x703)	32	R/W	page 164	0x703
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

8.5.1 MAC Control Registers

Table 59 through Table 75 on page 122 provide details on the control and status registers associated with each MAC port. The register address is '**Port_index + 0x****', where the port index is set at any value from 0x000 through 0x500. All registers are 32 bits.

Table 59 Station Address Low ($ Port_Index + 0x00)

Bit	Name	Description	Type[1]	Default
31:0	Station Address Low	Source MAC address bits 31-0. This address is inserted in the source address field when transmitting Pause frames, and is also used to compare against unicast Pause frames at the receiving side.	R/W	0x00000000
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 60 Station Address High ($ Port_Index + 0x01)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	R	0x0000
15:0	Station Address High	Source MAC address bits 47-32. This address is inserted in the source address field when transmitting Pause frames, and is also used to compare against unicast Pause frames at the receiving side.	R/W	0x0000
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 61 FDFC Type ($ Port_Index + 0x03)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	R	0x0000
15:0	FDFC Type	Contains the value of the type field transmitted in an internally generated flow control (pause) frame. Internally generated flow control frames are generated via the external pause interface or when the RX FIFO exceeds its high watermark.	R/W	0x8808
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 62 FC TX Timer Value ($ Port_Index + 0x07)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	R	0x0000
15:0	FC TX Timer Value	The pause length sent to the receiving station in 512 bit times	R/W	0x005E
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 63 FDFC Address Low ($ Port_Index + 0x08)

Bit	Name	Description	Type[1]	Default
31:0	FDFC Address Low	Contains the value of the lowest 32 bits of the destination address field transmitted in an internally generated flow control (pause) frame. Internally generated flow control frames are generated via the external pause interface or when the RX FIFO exceeds it high watermark.	R/W	0xC2000001
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 64 FDFC Address High ($ Port_Index + 0x09)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	R	0x0000
15:0	FDFC Address High	Contains the value of the highest 16 bits of the destination address filed transmitted in an internally generated flow control (pause) frame. Internally generated flow control frames are generated via the external pause interface or when the RX FIFO exceeds it high watermark.	R/W	0x0180
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 65 IPG Transmit Time ($ Port_Index + 0x0C)

Bit	Name	Description	Type[1]	Default
31:10	Reserved	Reserved	R	0x0000
9:0	IPG Transmit Time	IPG time for back-to-back transmissions (specified in multiples of 8 bit times). The value specified in this register is calculated as follows: (register value + 4) *8 = IPG length in terms of bit times. Therefore, the default value of 8 gives: (8+4) *8 = 96 bit times. 96 bit times is the minimum IPG. If a value of 8 or less is written to this register, the IPG remains 96 bit times.	R/W	0x0008
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 66 Pause Threshold ($ Port_Index + 0x0E)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	R	0x0000
15:0	Pause Threshold	When a pause frame is sent, an internal timer checks when a new pause frame must be scheduled for transmission to keep the link partner in pause mode. The pause threshold value is the minimum time to send before the earlier pause frame is aged out (specified in multiples of 512 bit times). **Note:** The value in this register is subtracted from the value in the *FC TX Timer Value ($ Port_Index + 0x07)* to set the internal pause threshold. This value determines how often a Pause frame is sent out to keep the link partner in pause mode.	R/W	0x002F
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 67 Max Frame Size ($ Port_Index + 0x0F)

Bit	Name	Description	Type[1]	Default
31:14	Reserved	Reserved	R	0x0000
13:0	Max Frame Size	The maximum frame size the MAC can receive or transmit without activating any error counters, and without truncation. The maximum frame size is internally adjusted by +4 if VLAN is tagged.	R/W	0x05EE
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 68 RGMII Speed ($ Port_Index + 0x10)

Bit	Name	Description	Type[1]	Default
31:2	Reserved	Reserved	R	0x00000000
1:0	RGMII Speed	These bits are used to define the speed of the IXF1010 MAC operation. 00 = Reserved 01 = 100 Mbps - RGMII TX_CLK is 25 MHz 1x = 1 Gbps - RGMII TX_CLK is 125 MHz	R/W	11
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 69 FC Enable ($ Port_Index + 0x12)

Bit	Name	Description	Type[1]	Default
Register Description: Indicates which flow control mode is used for the RX and TX MAC.				0x00000007
31:2	Reserved	Reserved	R	0x00000000
1	TX FDFC	0 = Disable TX full-duplex flow control [the MAC will not generate internally any flow control frames based on the RX FIFO watermarks or the Transmit Pause Control interface 1 = Enable TX full-duplex flow control [enables the MAC to send flow control frames to the link partner based on the RX FIFO programmable watermarks or the Transmit Pause Control interface]	R/W	1
0	RX FDFC	0 = Disable RX full-duplex flow control [the MAC will not respond to flow control frames sent to it by the link partner] 1 = Enable RX full-duplex flow control [MAC will respond to flow control frames sent by the link partner and will stop packet transmission for the time specified in the flow control frame]	R/W	1
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 70 Short Runts Threshold ($ Port_Index + 0x14)

Bit	Name	Description	Type[1]	Default
31:5	Reserved	Reserved	R	0x0000008
4:0	Short Runts Threshold	Holds the value in bytes, which applies to the threshold in determining between runts and short.	R/W	01000
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 71 Discard Unknown Control Frame ($ Port_Index + 0x15)

Bit	Name	Description	Type[1]	Default
31:1	Reserved	Reserved	R	0x00000000
0	Discard Unknown Control Frame	0 = Keep unknown control frames 1 = Discard unknown control frames.	R/W	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 72 Diverse Config ($ Port_Index + 0x18)

Bit	Name	Description	Type[1]	Default
Register Description: This register enables the padding of undersized frames on transmit and automatic CRC generation. For proper operation, if padding of undersized frames is enabled, the automatic CRC generation must be enabled.				0x0000110D
31:19	Reserved	Reserved	R	0x000
18:13	Reserved[2]	Write as 0, ignore on Read	R/W	000000
12	Reserved[2]	Write as 1, ignore on Read	R/W	1
11:9	Reserved[2]	Write as 0, ignore on Read	R/W	000
8	Reserved[2]	Write as 1, ignore on Read	R/W	1
7	pad_enable	Enable padding of undersized packets	R/W	0
6	crc_add	Enable automatic CRC appending	R/W	0
5:4	Reserved[2]	Write as 0, ignore on Read	R/W	00
3:2	Reserved[2]	Write as 1, ignore on Read	R/W	11
1	Reserved[2]	Write as 0, ignore on Read	R/W	0
0	Reserved[2]	Write as 1, ignore on Read	R/W	1
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write 2. Reserved bits must be written to the default value for proper operation				

Table 73 RX Packet Filter Control ($ Port_Index + 0x19) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: This register allows for specific packet types to be marked for filtering, and is used in conjunction with the RX FIFO Errored Frames Drop Enable Register				0x00000000
31:6	Reserved	Reserved	R	0x000000
5	CRC Error Pass[2]	This bit enables a Global filter on frames with a CRC Error. When CRCErrorPASS = 0, all frames with a CRC Error are marked as bad. **NOTE:** When used in conjunction with the RX FIFO ErroredFrameDropEnable[9:0] Register (see *RX FIFO Errored Frame Drop Enable ($ 0x59F)*). This allows the frame to be dropped in the RX FIFO. Otherwise, the frame is sent across the SPI4-2 interface but marked as an EOP Abort frame. When the CRC Error Pass Filter bit = 0, it takes precedence over the other filter bits. Any packet regardless if it is a Pause, Unicast, Multicast or Broadcast packet with a CRC error will be marked as bad frames when CRC Error Pass = 0 When CRCErrorPASS = 1, frames with a CRC Error are not marked as bad and are passed to the SPI4-2 interface for transfer as good frames, regardless of the state of the FrameDropEn[9:0] bits.	R/W	0
4	Pause Frame Pass	This bit enables a Global filter on Pause frames. When PauseFramePass = 0, all Pause frames are marked as bad. **NOTE:** When used in conjunction with the RX FIFO ErroredFrameDropEnable[9:0] Register (see *RX FIFO Errored Frame Drop Enable ($ 0x59F)*). This allows the frame to be dropped in the RX FIFO. Otherwise, the frame is sent across the SPI4-2 interface but marked as an EOP Abort frame. ***Note:*** When PauseFramePass = 1, all Pause frames are not marked as bad and are passed to the SPI4-2 interface for transfer as good frames, regardless of the state of the FrameDropEn[9:0] bits.	R/W	0
3	VLAN Drop En[2]	This bit enables a Global filter on VLAN frames. When VLANDropEn = 0, all VLAN frames are passed to the SPI4-2 Interface. When VLANDropEn = 1, all VLAN frames are dropped.[3]	R/W	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. Jumbo frames (1519 - 9600 bytes), matching the filter conditions, which would cause the frame to be dropped by the RX FIFO, will not be dropped. Instead, jumbo frames that are marked to be dropped by the RX FIFO, based on the filter setting in this register, will still be sent across the SPI4-2 interface, but will be marked as an EOP abort frame. Thus, jumbo frames matching the filter conditions will not be counted in the RX FIFO Number of Frames Removed Register because they are not removed by the RX FIFO. Only standard packet sizes (64 - 1518 bytes) meeting the filter conditions set in this register will actually be dropped by the RX FIFO and counted in the RX FIFO Number of Frames Removed.
3. Frames are dropped only when the appropriate bits are set in the RX FIFO Errored Frame Drop Enable Register (*RX FIFO Errored Frame Drop Enable ($ 0x59F)*). When the appropriate bits are not set, the frames are sent across the SPI4-2 interface and marked as EOP abort frames.

Table 73 RX Packet Filter Control ($ Port_Index + 0x19) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
2	B/Cast Drop En[2]	This bit enables a Global filter on Broadcast frames. When B/CastDropEn = 0, all broadcast frames are passed to the SPI4-2 Interface. When B/CastDropEn = 1, all broadcast frames are dropped.[3]	R/W	0
1	M/Cast Match En[2]	This bit enables a filter on multicast frames. If this bit = 0, all multicast frames are good and are passed to the SPI4-2 Interface. If this bit = 1, only multicast frames with a destination address that matches the PortMulticastAddress is forwarded. All other multicast frames are dropped.[3]	R/W	0
0	U/Cast Match En[2]	This bit enables a filter on unicast frames. If this bit = 0, all unicast frames are good and are passed to the SPI4-2 interface. If this bit = 1, only unicast frames with a destination address that matches the Station Address is forwarded. All other unicast frames are dropped.[3] ***Note:*** The VLAN filter overrides the Unicast filter. Thus, a VLAN frame cannot be filtered based on the Unicast address.	R/W	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. Jumbo frames (1519 - 9600 bytes), matching the filter conditions, which would cause the frame to be dropped by the RX FIFO, will not be dropped. Instead, jumbo frames that are marked to be dropped by the RX FIFO, based on the filter setting in this register, will still be sent across the SPI4-2 interface, but will be marked as an EOP abort frame. Thus, jumbo frames matching the filter conditions will not be counted in the RX FIFO Number of Frames Removed Register because they are not removed by the RX FIFO. Only standard packet sizes (64 - 1518 bytes) meeting the filter conditions set in this register will actually be dropped by the RX FIFO and counted in the RX FIFO Number of Frames Removed.
3. Frames are dropped only when the appropriate bits are set in the RX FIFO Errored Frame Drop Enable Register (*RX FIFO Errored Frame Drop Enable ($ 0x59F)*). When the appropriate bits are not set, the frames are sent across the SPI4-2 interface and marked as EOP abort frames.

Table 74 Port Multicast Address Low ($ Port_Index + 0x1A)

Bit	Name	Description	Type[1]	Default
31:0	Port Multicast Address Low	This address is used to compare against multicast frames at the receiving side if multicast filtering is enabled. This register contains bits 31:0 of the address.	R/W	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 75 Port Multicast Address High ($ Port_Index + 0x1B)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	R	0x0000
15:0	Port Multicast Address High	This address is used to compare against multicast frames at the receiving side if Multicast filtering is enabled. This register contains bits 47:32 of the address.	R/W	0x0000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

8.5.2 MAC RX Statistics Register Overview

The MAC RX Statistics Registers contain the MAC receiver statistic counters and are cleared when read. The software polls these registers and accumulates values to ensure that the counters do not wrap. The 32-bit counters wrap after approximately 30 seconds.

Table 76 covers the MAC RX Statistics Registers for all 10 MAC ports. The address is identical to the port number.

Table 76 MAC RX Statistics ($ Port_Index + 0x20 - Port_Index + 0x39) (Sheet 1 of 3)

Name	Description	Address	Type[1]	Default
RxOctetsTotalOK	Counts the bytes received in all legal frames, including all bytes from the destination MAC address to and including the CRC. The initial preamble and SFD bytes are not counted.	Port_Index + 0x20	CoR	0x00000000
RxOctetsBAD[2]	Counts the bytes received in all bad frames of a size greater than or equal to 64 bytes. A bad frame is defined as a properly framed packet containing a CRC, alignment error, or code violation. The 64-byte value is measured from the destination address, up to and including CRC. The initial preamble and SFD are not included in this value. **Note:** This register does not increment the Bad Octet count on undersized receive packets.	Port_Index + 0x21	CoR	0x00000000
RxUCPkts	The total number of unicast packets received (excluding bad packets) **Note:** This count includes non-pause control and VLAN packets, which are also counted in other counters. These packet types are counted twice. Take care when summing register counts for reporting MIB information.	Port_Index + 0x22	CoR	0x00000000
RxMCPkts	The total number of multicast packets received (excluding bad packets) **Note:** This count includes pause control packets, which are also counted in the PauseMacControl-ReceivedCounter. These packet types are counted twice. Take care when summing register counts for reporting MIB information.	Port_Index + 0x23	CoR	0x00000000
RxBCPkts	The total number of Broadcast packets received (excluding bad packets)	Port_Index + 0x24	CoR	0x00000000
RxPkts64Octets	The total number of packets received (including bad packets) that were 64 octets in length. Incremented for tagged packets with a length of 64 bytes, including tag field	Port_Index + 0x25	CoR	0x00000000
RxPkts65to127 Octets	The total number of packets received (including bad packets) that were [65-127] octets in length. Incremented for tagged packets with a length of 65 - 127 bytes, including tag field	Port_Index + 0x26	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. When sending in large frames, the counters can only deal with certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*MaxFrameSize, dependent on where the MaxFrameSize variable is set. If MaxFrameSize sets greater than half of the available count in RxOctetsBad (2^14-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2^14-1. MaxFrameSize is determined by the settings in the *Max Frame Size ($ Port_Index + 0x0F)*, on page 118.

Table 76 MAC RX Statistics ($ Port_Index + 0x20 - Port_Index + 0x39) (Sheet 2 of 3)

Name	Description	Address	Type[1]	Default
RxPkts128to255 Octets	The total number of packets received (including bad packets) that were [128-255] octets in length. Incremented for tagged packets with a length of 128-255 bytes, including tag field	Port_Index + 0x27	CoR	0x00000000
RxPkts256to511 Octets	The total number of packets received (including bad packets) that were [256-511] octets in length. Incremented for tagged packets with a length of 256 - 511 bytes, including tag field	Port_Index + 0x28	CoR	0x00000000
RxPkts512to1023 Octets	The total number of packets received (including bad packets) that were [512-1023] octets in length. Incremented for tagged packets with a length of 512 - 1023 bytes, including tag field	Port_Index + 0x29	CoR	0x00000000
RxPkts1024to1518 Octets	The total number of packets received (including bad packets) that were [1024-1518] octets in length. Incremented for tagged packet with a length between 1024-1522, including the tag	Port_Index + 0x2A	CoR	0x00000000
RxPkts1519toMax Octets	The total number of packets received (including bad packets) that were >1518 octets in length. Incremented for tagged packet with a length between 1523-max frame size, including the tag	Port_Index + 0x2B	CoR	0x00000000
RxFCSErrors	Number of frames received with legal size, but with wrong CRC field (also called FCS field) **Note:** Legal size is 64 bytes through the value stored in the *Max Frame Size ($ Port_Index + 0x0F)*.	Port_Index + 0x2C	CoR	0x00000000
RxTagged	Number of frames with VLAN tag (Type field = 0x8100)	Port_Index + 0x2D	CoR	0x00000000
RxDataError	***Note:*** Number of frames received with legal length, containing a code violation (signaled with RX_ERR on RGMII)	Port_Index + 0x2E	CoR	0x00000000
RxAlignErrors	Number of frames with a legal frame size, but containing less than 8 additional bits. This occurs when a frame is not byte-aligned. The CRC of the frame is wrong when the additional bits are stripped. If the CRC is OK, the frame is not counted, but treated as an OK frame. ***Note:*** This counter increments in 100 Mbps RGMII mode only.	Port_Index + 0x2F	CoR	0x00000000
RxLongErrors[2]	Frames bigger than the maximum allowed, with both OK CRC and the integral number of octets Default maximum allowed is 1518 bytes untagged and 1522 bytes tagged, but the value can be changed by a register Frames bigger than the larger of 2*MaxFrameSize and 50000 bits are not counted here, but counted in the VeryLongError counter.	Port_Index + 0x30	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. When sending in large frames, the counters can only deal with certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*MaxFrameSize, dependent on where the MaxFrameSize variable is set. If MaxFrameSize sets greater than half of the available count in RxOctetsBad (2^14-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2^14-1. MaxFrameSize is determined by the settings in the *Max Frame Size ($ Port_Index + 0x0F)*, on page 118.

Table 76 MAC RX Statistics ($ Port_Index + 0x20 - Port_Index + 0x39) (Sheet 3 of 3)

Name	Description	Address	Type[1]	Default
RxJabberErrors	Frames bigger than the maximum allowed, with either a bad CRC or a non-integral number of octets. The default maximum allowed is 1518 bytes untagged and 1522 bytes tagged, but the value can be changed by a register. Frames bigger than the larger of 2*MaxFrameSize and 50000 bits are not counted here, but counted in the VeryLongError counter.	Port_Index + 0x31	CoR	0x00000000
RxPauseMac ControlCounter	Number of Pause MAC control frames received This statistic register increments on any valid 64byte Pause frame with valid CRC and will also increment on 64byte Pause Frames with an invalid CRC if bit 5 of the *RX Packet Filter Control ($ Port_Index + 0x19)* is set to 1.	Port_Index + 0x32	CoR	0x00000000
RxUnknownMac ControlFrame Counter	Number of MAC control frames received with an op code different from 0001 (Pause)	Port_Index + 0x33	CoR	0x00000000
RxVeryLongErrors[2]	Frames bigger than the larger of 2*MaxFrameSize and 50000 bits	Port_Index + 0x34	CoR	0x00000000
RxRuntErrors	The total number of packets received that are less than 64 octets in length, but longer than or equal to 96 bit times. **Note:** The "ShortRuntsThreshold" Register controls the byte count used to determine the difference between Runts and Shorts, and therefore controls which counter is incremented for a given frame size. This counter is only updated after receipt of two good frames.	Port_Index + 0x35	CoR	0x00000000
RxShortErrors	The total number of packets received that are less than 96 bit times, which corresponds to a 4-byte frame with a well formed preamble and SFD. This counter indicates fragment sizes illegal in all modes, and is only fully updated after reception of a good frame following a fragment.	Port_Index + 0x36	CoR	0x00000000
RxCarrierExtend Error	Gigabit half-duplex event only Note: N/A - half-duplex only	Port_Index + 0x37	CoR	0x00000000
RxSequenceErrors	Records the number of sequencing errors that occur. **Note:** The IXF1010 MAC does not support fiber.	Port_Index + 0x38	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. When sending in large frames, the counters can only deal with certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*MaxFrameSize, dependent on where the MaxFrameSize variable is set. If MaxFrameSize sets greater than half of the available count in RxOctetsBad (2^14-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2^14-1. MaxFrameSize is determined by the settings in the *Max Frame Size ($ Port_Index + 0x0F)*, on page 118.

8.5.3 MAC TX Statistics Register Overview

The MAC TX Statistics Registers contain all the MAC transmit statistic counters and are cleared when read. The software must poll these registers to accumulate values and ensure that the counters do not wrap. The 32-bit counters wrap after approximately 30 seconds.

Table 77 covers the MAC TX Statistics Registers for all 10 MAC ports. The address is identical to the port number.

Table 77 MAC TX Statistics ($ Port_Index + 0x40 - Port_Index + 0x58) (Sheet 1 of 4)

Name	Description	Address	Type[1]	Default
TXOctetsTotalOK	Counts the bytes transmitted in all legal frames. The count includes all bytes from the destination MAC address to and including the CRC. The initial preamble and SFD bytes are not counted.	Port_Index + 0x40	CoR	0x00000000
TXOctetsBad	Counts the bytes transmitted in all bad frames. The count includes all bytes from the destination MAC address to and including the CRC. The initial preamble and SFD bytes are not counted. TX underrun counted: The count is expected to match the number of bytes actually transmitted before the frame is discarded. TX CRC error counted: All bytes not sent with success are counted by this counter	Port_Index + 0x41	CoR	0x00000000
TXUCPkts	The total number of unicast packets transmitted (excluding bad packets)	Port_Index + 0x42	CoR	0x00000000
TXMCPkts	The total number of multicast packets transmitted (excluding bad packets) **Note:** This count includes pause control packets which are also counted in the TxPauseFrames Counter. Thus, these types of packets are counted twice. Take care when summing register counts for reporting MIB information.	Port_Index + 0x43	CoR	0x00000000
TXBCPkts	The total number of broadcast packets transmitted (excluding bad packets)	Port_Index + 0x44	CoR	0x00000000
TXPkts64Octets	The total number of packets transmitted (including bad packets) that were 64 octets in length. Incremented for tagged packets with a length of 64 bytes, including tag field	Port_Index + 0x45	CoR	0x00000000
TXPkts65to127Octets	The total number of packets transmitted (including bad packets) that were [65-127] octets in length. Incremented for tagged packets with a length of 65 - 127 bytes, including tag field	Port_Index + 0x46	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 77 MAC TX Statistics ($ Port_Index + 0x40 - Port_Index + 0x58) (Sheet 2 of 4)

Name	Description	Address	Type[1]	Default
TXPkts128to255Octets	The total number of packets transmitted (including bad packets) that were [128-255] octets in length. Incremented for tagged packets with a length of 128 - 255 bytes, including tag field	Port_Index + 0x47	CoR	0x00000000
TXPkts256to511Octets	The total number of packets transmitted (including bad packets) that were [256-511] octets in length. Incremented for tagged packets with a length of 256 - 511 bytes, including tag field	Port_Index + 0x48	CoR	0x00000000
TXPkts512to1023Octets	The total number of packets transmitted (including bad packets) that were [512 - 1023] octets in length. Incremented for tagged packets with a length of 512 - 1023 bytes, including tag field	Port_Index + 0x49	CoR	0x00000000
TXPkts1024to1518Octets	The total number of packets transmitted (including bad packets) that were [1024-1518] octets in length. Incremented for tagged packet with a length between 1024-1522, including the tag	Port_Index + 0x4A	CoR	0x00000000
TXPkts1519toMaxOctets	The total number of packets transmitted (including bad packets) that were >1518 octets in length. Incremented for tagged packet with a length between 1523-max frame size, including the tag	Port_Index + 0x4B	CoR	0x00000000
TXDeferred	Number of times the initial transmission attempt of a frame is postponed due to another frame already being transmitted on the Ethernet network. **Note**: N/A - half-duplex only	Port_Index + 0x4C	CoR	0x00000000
TXTotalCollisions	Sum of all collision events **Note**: N/A - half-duplex only	Port_Index + 0x4D	CoR	0x00000000
TXSingleCollisions	A count of successfully transmitted frames on a particular interface where the transmission is inhibited by exactly one collision. A frame that is counted by an instance of this object is also counted by the corresponding instance of either the UnicastPkts, MulticastPkts, or BroadcastPkts, and is not counted by the corresponding instance of the MultipleCollisionFrames object. **Note**: N/A - half-duplex only	Port_Index + 0x4E	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 77 MAC TX Statistics ($ Port_Index + 0x40 - Port_Index + 0x58) (Sheet 3 of 4)

Name	Description	Address	Type[1]	Default
TXMultipleCollisions	A count of successfully transmitted frames on a particular interface for which transmission is inhibited by more than one collision. A frame that is counted by an instance of this object is also counted by the corresponding instance of either the UnicastPkts, MulticastPkts, or BroadcastPkts, and is not counted by the corresponding instance of the SingleCollisionFrames object. **Note**: N/A - half-duplex only	Port_Index + 0x4F	CoR	0x00000000
TXLateCollisions	The number of times a collision is detected on a particular interface later than 512 bit-times into the transmission of a packet. Such frame are terminated and discarded. **Note**: N/A - half-duplex only	Port_Index + 0x50	CoR	0x00000000
TXExcessiveCollisionErrors	A count of frames, which collides 16 times and is then discarded by the MAC. Not effecting xMultipleCollisions Note: N/A - half-duplex only	Port_Index + 0x51	CoR	0x00000000
TXExcessiveDeferralErrors	Number of times frame transmission is postponed more than 2*MaxFrameSize due to another frame already being transmitted on the Ethernet network. This causes the MAC to discard the frame. **Note**: N/A - half-duplex only	Port_Index + 0x52	CoR	0x00000000
TXExcessiveLengthDrop	Frame transmissions aborted by the MAC because the frame is longer than maximum frame size. These frames are truncated by the MAC when the maximum frame size violation is detected by the MAC.	Port_Index + 0x53	CoR	0x00000000
TXUnderrun	Internal TX error which causes the MAC to end the transmission before the end of the frame because the MAC did not get the needed data in time for transmission. The frames are lost and a fragment or a CRC error is transmitted.	Port_Index + 0x54	CoR	0x00000000
TXTagged	Number of OK frames with VLAN tag. (Type field = 0x8100).	Port_Index + 0x55	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 77 MAC TX Statistics ($ Port_Index + 0x40 - Port_Index + 0x58) (Sheet 4 of 4)

Name	Description	Address	Type[1]	Default
TXCRCError	Number of frames transmitted with a legal size, but with the wrong CRC field (also called FCS field)	Port_Index + 0x56	CoR	0x00000000
TXPauseFrames	Number of pause MAC frames transmitted	Port_Index + 0x57	CoR	0x00000000
TXFlowControlCollisions Send	Collisions generated on purpose on incoming frames, to avoid reception of traffic, while the port is in half-duplex and has flow control enabled, and do not have sufficient memory to receive more frames. Note: Due to the internal counting technique, a last frame might have to be transmitted after last flow control collision send to get the correct statistic. **Note**: N/A - half-duplex only	Port_Index + 0x58	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

8.5.4 PHY Autoscan Registers

Note: These register hold the current values of the PHY registers only when Autoscan is enabled for more information on Autoscan operation refer to Section 5.4.8, *Autoscan Operation*, on page 72.

Table 78 PHY Control ($ Port_Index + 0x60) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	R	0
15	Reset	PHY Soft Reset. Resets the PHY registers to their default value. This register bit self-clears after the reset is complete. 1 = PHY reset 0 = Normal Operation	R	0
14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R	0
13	Speed Selection	0.6 (Speed<1> 0.13 (Speed<0>) 1 1 = Reserved 1 0 = 1000 Mbps (manual mode not allowed) 0 1 = 100 Mbps 0 0 = Reserved	R	0[2]
12	Auto-Negotiation Enable	1 = Enable auto-negotiation process 0 = Disable auto-negotiation process This register bit must be enabled for 1000BASE-T operation	R	1
11	Power-Down	1 = Power-down 0 = Normal operation	R	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. This register is ignored if auto-negotiation is enabled.

Table 78 PHY Control ($ Port_Index + 0x60) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
10	Isolate	1 = Electrically isolate PHY from GMII	R	0
9	Restart Auto-Negotiation	1 = Restart auto-negotiation process 0 = Normal operation	R	0
8	Duplex Mode	1 = Full-duplex mode 0 = Half-duplex mode	R	1[2]
7	Collision Test	1 = Enable COL signal test 0 = Disable COL signal test This register bit is ignored unless loopback is enabled (Register bit 0.14 = 1)	R	0
6	Speed Selection 1000 Mbps	0.6 (Speed<1>) 0.13 (Speed<0>) 1 1 = Reserved 1 0 = 1000 Mbps (manual mode now allowed) 0 1 = 100 Mbps 0 0 = Reserved	R	0[2]
5:0	Reserved	Reserved	R	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. This register is ignored if auto-negotiation is enabled.

Table 79 PHY Status ($ Port_Index + 0x61) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	R	0x0000
15	100BASE-T4	0 = PHY not able to operate in 100BASE-T4 1 = PHY able to operate in 100BASE-T4	R	0
14	100BASE-X Full-Duplex	0 = PHY not able to operate in 100BASE-X in full-duplex mode 1 = PHY able to operate in 100BASE-X in full-duplex mode	R	1
13	100BASE-X Half-Duplex	0 = PHY not able to operate in 100BASE-X in half duplex mode 1 = PHY able to operate in 100BASE-X in half-duplex mode	R	1
12	10 Mbps Full-Duplex	0 = PHY not able to operate in 10 Mbps in full-duplex mode 1 = PHY able to operate in 10 Mbps in full-duplex mode	R	1
11	10 Mbps Half-Duplex	0 = PHY not able to operate in 10 Mbps in half-duplex mode 1 = PHY able to operate in 10 Mbps in half-duplex mode	R	1
10	100BASE-T2 Full-Duplex	0 = PHY not able to operate in 10BASE-T2 in full-duplex mode (not supported) 1 = PHY able to operate in 100BASE-T2 in full-duplex mode	R	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 79 PHY Status ($ Port_Index + 0x61) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
9	100BASE-T2 Half-Duplex	0 = PHY not able to operate in 100BASE-T2 in half-duplex mode 1 = PHY able to operate in 100BASE-T2 in half-duplex mode	R	0
8	Extended Status	0 = No extended status information in Register 15 1 = Extended status information in Register 15	R	1
7	Reserved	Reserved	R	0
6	MF Preamble Suppression	0 = PHY will not accept management frames with preamble suppressed 1 = PHY will accept management frames with preamble suppressed	R	0
5	Reserved	Reserved	R	0
4	Remote Fault	0 = No remote fault condition detected 1 = Remote fault condition detected	R	0
3	Auto-Negotiation Ability	0 = PHY is not able to perform auto-negotiation 1 = PHY is able to perform auto-negotiation	R	1
2	Link Status	0 = Link is down 1 = Link is up	R	0
1	Jabber Detect	0 = Jabber condition not detected 1 = Jabber condition detected	R	0
0	Extended Capability	0 = No extended register capabilities 1 = Extended register capabilities	R	1

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 80 PHY ID 1 (Addr: Port_Index + 0x62)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	R	0
15:0	PHY ID Number	The PHY identifier is composed of Register bits 18.3 of the OUI (Organizationally Unique Identifier)	R	na

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 81 PHY ID 2 ($ Port_Index + 0x63)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	R	0
15:10	PHY ID Number	The PHY identifier is composed of Register bits 24:19 of the OUI (Organizationally Unique Identifier)	R	011110
9:4	Manufacturer's Model	Six bits containing the manufacturer's part number	R	010000
3:0	Manufacturer's Revision Number	Four bits containing the manufacturer's revision number	R	0000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 82 Auto-Negotiation Advertisement ($ Port_Index + 0x64) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	R	0
15	Next Page	0 = No manual control of Next Page (software) 1 = Manual control of Next Page (software)	R	0
14	Reserved	Reserved	R	0
13	Remote Fault	0 = No remote fault 1 = Remote fault	R	0
12	Reserved	Reserved	R	0
11	ASM_DIR	Advertise Asymmetric Pause Direction Register bit. This register bit is used in conjunction with Pause (Register bit 4.10) 0 = Link partner is not capable of asymmetric pause 1 = Link partner is capable of asymmetric pause	R	1
10	Pause	Advertise to link partner that Pause operation is desired (IEEE 802.3x Standard)	R	0
9	100BASE-T4	0 = 100BASE-T4 capability is not available 1 = 100BASE-T4 capability is available	R	0
8	100BASE-TX Full-Duplex	0 = DTE is not 100BASE-TX, full-duplex mode capable 1 = DTE is 100BASE-TX, full-duplex mode capable	R	1
7	100BASE-TX Half-Duplex	0 = DTE is not 100BASE-TX, half-duplex mode capable 1 = DTE is 100BASE-TX, half-duplex mode capable	R	1

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 82 Auto-Negotiation Advertisement ($ Port_Index + 0x64) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
6	10BASE-T Full-Duplex	0 = DTE is not 10BASE-T, full duplex mode capable 1 = DTE is 10BASE-T, full-duplex mode capable	R	1
5	10BASE-T Half-Duplex	0 = DTE is not 10BASE-T, half-duplex mode capable 1 = DTE is 10BASE-T, half-duplex mode capable	R	1
4:0	Selector Field, S[4:0]	00000 =Reserved for future auto-negotiation development 00001 =IEEE 802.3 00010 =IEEE 802.9 ISLAN-16T 11111 =Reserved for future auto-negotiation development Unspecified or reserved combinations should not be transmitted. Setting this field to a value other than 00001 will most likely cause auto-negotiation to fail.	R	00001

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 83 Auto-Negotiation Base Page Ability ($ Port_Index + 0x65) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	R	0
15	Next Page	0 = Link partner has no ability to send multiple pages 1 = Link partner has the ability to send multiple pages	R	N/A
14	Acknowledge	0 = Link partner has not received Link Code Word from IXF1010 MAC 1 = Link partner has received Link Code Word from IXF1010 MAC	R	N/A
13	Remote Fault	0 = No remote fault 1 = Remote fault	R	N/A
12	Reserved	Reserved	R	0
11	ASM_DIR	Advertise Asymmetric Pause Direction Register bit. This register bit is used in conjunction with Pause (Register bit 4.10) 0 = Link partner is not capable of asymmetric pause 1 = Link partner is capable of asymmetric pause	R	1
10	Link Partner Pause	Link partner wants to utilize Pause Operation as defined in IEEE 802.3x Standard	R	0
9	1000BASE-T4	0 = Link partner is not 100BASE-T4 capable 1 = Link partner is 100BASE-T4 capable	R	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 83 Auto-Negotiation Base Page Ability ($ Port_Index + 0x65) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
8	100BASE-TX Full-Duplex	0 = Link partner is not 100BASE-TX, full-duplex mode capable 1 = Link partner is 100BASE-TX, full-duplex mode capable	R	1
7	100BASE-TX Half-Duplex	0 = Link partner is not 100BASE-TX, half-duplex mode capable 1 = Link partner is 100BASE-TX, half-duplex mode capable	R	1
6	10BASE-T Full-Duplex	0 = Link partner is not 10BASE-T, full duplex mode capable 1 = Link partner is 10BASE-T, full-duplex mode capable	R	1
5	10BASE-T Half-Duplex	0 = Link partner is not 10BASE-T, half-duplex mode capable 1 = Link partner is 10BASE-T, half-duplex mode capable	R	1
4:0	Selector Field, S[4:0]	00000 =Reserved for future auto-negotiation development 00001 =IEEE 802.3 00010 =IEEE 802.9 ISLAN-16T 11111 =Reserved for future auto-negotiation development Unspecified or reserved combinations should not be transmitted. Setting this field to a value other than 00001 will most likely cause auto-negotiation to fail.	R	00001

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 84 Auto-Negotiation Expansion ($ Port_Index + 0x66) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
31:6	Reserved	Reserved	R	0
5	Base Page	This register bit indicates the status of the auto-negotiation variable, base page. It flags synchronization with the auto-negotiation state diagram allowing detection of interrupted links. This register bit is only used if Register bit 16.1 (alternate Next Page feature) is set. 0 = base_page = false 1 = base_page = true	R	0
4	Parallel Detection Fault	0 = Parallel detection fault has not occurred 1 = Parallel detection fault has occurred	R	0
3	Link Partner Next Page Able	0 = Link partner is not Next Page able 1 = Link partner is Next Page able	R	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 84 Auto-Negotiation Expansion ($ Port_Index + 0x66) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
2	Next Page Able	0 = Local device is not Next Page able 1 = Local device is Next Page able	R	0
1	Page Received	Indicates that a new page has been received and the received code word has been loaded into Register 5 (base pages) or Register 8 (next pages) as specified in the EEE 802.3 Standard. This bit clears on Read.	R	0
0	Link Partner Auto-Negotiation Able	0 = Link partner is not auto-negotiation able 1 = Link partner is auto-negotiation able	R	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 85 Auto-Negotiation Next Page Transmit ($ Port_Index + 0x67)

Bit	Name	Description	Type[1]	Default
Register Description: Need one-sentence descriptions of register				0x0000000
31:16	Reserved	Reserved	R	0
15	Next Page (NP)	0 = Last page 1 = Additional Next Pages follow	R	0
14	Reserved	Reserved	R	0
13	Message Page (MP)	0 = Unformatted page 1 = Message page	R	0
12	Acknowledge 2	0 = Cannot comply with message 1 = Complies with message	R	0
11	Toggle (T)	0 = Previous value of the transmitted Link Code Word was logic one 1 = Previous value of the transmitted Link Code Word was logic zero	R	0
10:0	Message/ Unformatted Code Field	11-bit message code field See IEEE 802.3 Annex 28C	R	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

8.5.5 Global Status and Configuration Register Overview

Table 86 through Table 94 on page 140 provide an overview of the Global Control and Status Registers.

Table 86 Port Enable ($ 0x500)

Bit	Name	Description	Type[1]	Default
Register Description: A control register for each port in the IXF1010 MAC. Port ID = bit position in the register. To make a port active, the bit must be set High (for example, port 4 active implies register value = 0001.0000). Setting the bit to 0 disables the port. The default state for this register is for all 10 ports to be active.				0x000003FF
31:10	Reserved	Reserved	R	0x00000
9	Port 9 Enable	Port 9 0 = Disable 1 = Enable	R/W	1
8	Port 8 Enable	Port 8 0 = Disable 1 = Enable	R/W	1
7	Port 7 Enable	Port 7 0 = Disable 1 = Enable	R/W	1
6	Port 6 Enable	Port 6 0 = Disable 1 = Enable	R/W	1
5	Port 5 Enable	Port 5 0 = Disable 1 = Enable	R/W	1
4	Port 4 Enable	Port 4 0 = Disable 1 = Enable	R/W	1
3	Port 3 Enable	Port 3 0 = Disable 1 = Enable	R/W	1
2	Port 2 Enable	Port 2 0 = Disable 1 = Enable	R/W	1
1	Port 1 Enable	Port 1 0 = Disable 1 = Enable	R/W	1
0	Port 0 Enable	Port 0 0 = Disable 1 = Enable	R/W	1
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 87 Link LED Enable ($ 0x502)

Bit	Name	Description	Type[1]	Default
Register Description: Per-port bit should be set upon detection of link by system CPU to enable proper operation of the link LEDs.				0x00000000
31:10	Reserved	Reserved	R	0x00000
9	Link LED Enable Port 9	Port 9 link 0 = No link 1 = Link	R/W	0
8	Link LED Enable Port 8	Port 8 link 0 = No link 1 = Link	R/W	0
7	Link LED Enable Port 7	Port 7 link 0 = No link 1 = Link	R/W	0
6	Link LED Enable Port 6	Port 6 link 0 = No link 1 = Link	R/W	0
5	Link LED Enable Port 5	Port 5 link 0 = No link 1 = Link	R/W	0
4	Link LED Enable Port 4	Port 4 link 0 = No link 1 = Link	R/W	0
3	Link LED Enable Port 3	Port 3 link 0 = No link 1 = Link	R/W	0
2	Link LED Enable Port 2	Port 2 link 0 = No link 1 = Link	R/W	0
1	Link LED Enable Port 1	Port 1 link 0 = No link 1 = Link	R/W	0
0	Link LED Enable Port 0	Port 0 link 0 = No link 1 = Link	R/W	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 88 Core Clock Soft Reset ($ 0x504)

Bit	Name	Description	Type[1]	Default
Register Description: A soft reset register for the core clock system (for example, the SYS125 clock).				0x00000000
31:1	Reserved	Reserved	R	0x00000000
0	Core Soft Reset	0 = CoreSoftReset reset is inactive 1 = CoreSoftReset reset is active	R/W	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 89 MAC Soft Reset ($ 0x505) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: Per-port software activated reset of the MAC core.				0x00000000
31:10	Reserved	Reserved	R	0x00000
9	MAC Soft Reset Port 9	Port 9 0 = Reset inactive 1 = Reset active	R/W	0
8	MAC Soft Reset Port 8	Port 8 0 = Reset inactive 1 = Reset active	R/W	0
7	MAC Soft Reset Port 7	Port 7 0 = Reset inactive 1 = Reset active	R/W	0
6	MAC Soft Reset Port 6	Port 6 0 = Reset inactive 1 = Reset active	R/W	0
5	MAC Soft Reset Port 5	Port 5 0 = Reset inactive 1 = Reset active	R/W	0
4	MAC Soft Reset Port 4	Port 4 0 = Reset inactive 1 = Reset active	R/W	0
3	MAC Soft Reset Port 3	Port 3 0 = Reset inactive 1 = Reset active	R/W	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 89 MAC Soft Reset ($ 0x505) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
2	MAC Soft Reset Port 2	Port 2 0 = Reset inactive 1 = Reset active	R/W	0
1	MAC Soft Reset Port 1	Port 1 0 = Reset inactive 1 = Reset active	R/W	0
0	MAC Soft Reset Port 0	Port 0 0 = Reset inactive 1 = Reset active	R/W	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 90 MDIO Soft Reset ($ 0x506)

Bit	Name	Description	Type[1]	Default
Register Description: Software activated reset of the MDIO module.				0x00000000
31:1	Reserved	Reserved	R	0x00000000
0	MDIO Soft Reset	0 = Reset inactive 1 = Reset active	R/W	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 91 CPU Interface ($ 0x508)

Bit	Name	Description	Type[1]	Default
Register Description: CPU interface Endian select. This register allows the user to select the Endian of the CPU interface to allow various different CPUs to be connected to the IXF1010 MAC.				0x00000000
31:1	Reserved	Reserved	R	0x00000000
0	Endian	0 = Little Endian 1 = Big Endian	R/W	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 92 LED Control ($ 0x509) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: Globally selects and enables the LED mode.				0x00000000
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 92 LED Control ($ 0x509) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
31-2	Reserved	Reserved	R	0x00000000
1	LED Enable	0 = Disable LEDs 1 = Enable LEDs	R/W	0
0	LED_SEL_MODE	0 = Enable LED Mode 0 for use with SGS Thompson M5450 LED driver (Default) 1 = LED Mode 1 for use with Standard Octal Shift Register	R/W	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 93 LED Flash Rate ($ 0x50A)

Bit	Name	Description	Type[1]	Default
Register Description: Globally selects and enables the flash rate.				0x00000000
31:3	Reserved	Reserved	R	0x00000000
2:0	LED Flash Rate	000 = 100 ms flash rate 001 = 200 ms flash rate 010 = 300 ms flash rate 011 = 400 ms flash rate 100 = 500 ms flash rate 101 = Reserved 110 = Reserved 111 = Reserved	R/W	000
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 94 LED Fault Disable ($ 0x50B) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: Per-port fault disable: Disables the LED flashing for local or remote faults				0x00000000
31:10	Reserved	Reserved	R	0x000000
9	LED Fault Disable Port 9	Port 9 0 = Fault enabled 1 = Fault disabled	R/W	0
8	LED Fault Disable Port 8	Port 8 0 = Fault enabled 1 = Fault disabled	R/W	0
7	LED Fault Disable Port 7	Port 7 0 = Fault enabled 1 = Fault disabled	R/W	0
6	LED Fault Disable Port 6	Port 6 0 = Fault enabled 1 = Fault disabled	R/W	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 94 LED Fault Disable ($ 0x50B) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
5	LED Fault Disable Port 5	Port 5 0 = Fault enabled 1 = Fault disabled	R/W	0
4	LED Fault Disable Port 4	Port 4 0 = Fault enabled 1 = Fault disabled	R/W	0
3	LED Fault Disable Port 3	Port 3 0 = Fault enabled 1 = Fault disabled	R/W	0
2	LED Fault Disable Port 2	Port 2 0 = Fault enabled 1 = Fault disabled	R/W	0
1	LED Fault Disable Port 1	Port 1 0 = Fault enabled 1 = Fault disabled	R/W	0
0	LED Fault Disable Port 0	Port 0 0 = Fault enabled 1 = Fault disabled	R/W	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 95 JTAG ID Revision ($ 0x50C)

Bit	Name	Description	Type	Default
Register Description: The value of this register follows the same scheme as the device identification register found in the IEEE 1149.1 specification. The upper 4 bits correspond to silicon stepping. The next 16 bits store a Part ID Number. The next 11 bits contain a JEDEC Manufacturer ID. Bit zero = 1 if the chip is the first in a stack. The encoding scheme used for the Product ID field is implementation dependent.				0x403F2013
31:28	Version[2]	Version[2]	R	0100
27:12	Part ID	Part ID	R	0000001111110010
11:8	JEDEC Cont.	JEDEC Cont.	R	0000
7:1	JEDEC ID	JEDEC ID	R	0001001
0	Reserved	Reserved	R	1

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. See the IXF1010 MAC Specification Update for the latest version.

8.5.6 Global RX Block Register Overview

Table 96 through Table 101 on page 149 provide an overview of the RX Block Registers, which include the RX FIFO High and Low watermarks.

Table 96 RX FIFO High Watermark Ports 0 to 9 ($ 0x580 - 0x589)

Name[2]	Description	Address	Type[1]	Default
RX FIFO High Watermark Port 0	High watermark for RX FIFO port 0. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x580	R/W	0x00000740
RX FIFO High Watermark Port 1	High watermark for RX FIFO port 1. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x581	R/W	0x00000740
RX FIFO High Watermark Port 2	High watermark for RX FIFO port 2. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x582	R/W	0x00000740
RX FIFO High Watermark Port 3	High watermark for RX FIFO port 3. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x583	R/W	0x00000740
RX FIFO High Watermark Port 4	High watermark for RX FIFO port 4. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x584	R/W	0x00000740
RX FIFO High Watermark Port 5	High watermark for RX FIFO port 5. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x585	R/W	0x00000740
RX FIFO High Watermark Port 6	High watermark for RX FIFO port 6. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x586	R/W	0x00000740
RX FIFO High Watermark Port 7	High watermark for RX FIFO port 7. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x587	R/W	0x00000740
RX FIFO High Watermark Port 8	High watermark for RX FIFO port 8. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC	0x588	R/W	0x00000740
RX FIFO High Watermark Port 9	High watermark for RX FIFO port 9. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x589	R/W	0x00000740

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. For all RX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:15 - Reserved and R.
   Bits 14:0 - Described above.

Table 97 RX FIFO Low Watermark Ports 0 to 9 ($ 0x58A - 0x593)

Name[2]	Description	Address	Type[1]	Default
RX FIFO Low Watermark Port 0	Low watermark for RX FIFO port 0. The default value is 1840 bytes. When the port is in flow control, and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58A	R/W	0x00000730
RX FIFO Low Watermark Port 1	Low watermark for RX FIFO port 1. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58B	R/W	0x00000730
RX FIFO Low Watermark Port 2	Low watermark for RX FIFO port 2. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58C	R/W	0x00000730
RX FIFO Low Watermark Port 3	Low watermark for RX FIFO port 3. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58D	R/W	0x00000730
RX FIFO Low Watermark Port 4	Low watermark for RX FIFO port 4. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58E	R/W	0x00000730
RX FIFO Low Watermark Port 5	Low watermark for RX FIFO port 5. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58F	R/W	0x00000730
RX FIFO Low Watermark Port 6	Low watermark for RX FIFO port 6. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x590	R/W	0x00000730
RX FIFO Low Watermark Port 7	Low watermark for RX FIFO port 7. The default value is 1840 bytes.When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x591	R/W	0x00000730
RX FIFO Low Watermark Port 8	Low watermark for RX FIFO port 8. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x592	R/W	0x00000730
RX FIFO Low Watermark Port 9	Low watermark for RX FIFO port 9. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x593	R/W	0x00000730

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. For all RX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:15 - Reserved and R.
   Bits 14:0 - Described above.

Table 98 RX FIFO Number of Frames Removed Ports 0 to 9 ($ 0x594 - 0x59D) (Sheet 1 of 3)

Name[2]	Description	Address	Type[1]	Default
RX FIFO Number of Frames Removed on Port 0	This register counts all frames removed from the RX FIFO for port 0 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (*RX FIFO Errored Frame Drop Enable ($ 0x59F)*) • Frames are greater than the MaxFrameSize (*Max Frame Size ($ Port_Index + 0x0F)*)	0x594	CoR	0x00000000
RX FIFO Number of Frames Removed on Port 1	This register counts all frames removed from the RX FIFO for port 1 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (*RX FIFO Errored Frame Drop Enable ($ 0x59F)*) • Frames are greater than the MaxFrameSize (*Max Frame Size ($ Port_Index + 0x0F)*)	0x595	CoR	0x00000000
RX FIFO Number of Frames Removed on Port 2	This register counts all frames removed from the RX FIFO for port 2 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (*RX FIFO Errored Frame Drop Enable ($ 0x59F)*) • Frames are greater than the MaxFrameSize (*Max Frame Size ($ Port_Index + 0x0F)*)	0x596	CoR	0x00000000
RX FIFO Number of Frames Removed on Port 3	This register counts all frames removed from the RX FIFO for port 3 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (*RX FIFO Errored Frame Drop Enable ($ 0x59F)*) • Frames are greater than the MaxFrameSize (*Max Frame Size ($ Port_Index + 0x0F)*)	0x597	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write.
2. For all Number of Frames Removed Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:22 - Reserved and R.
   Bits 21:0 - Described above.

Table 98 RX FIFO Number of Frames Removed Ports 0 to 9 ($ 0x594 - 0x59D) (Sheet 2 of 3)

Name[2]	Description	Address	Type[1]	Default
RX FIFO Number of Frames Removed on Port 4	This register counts all frames removed from the RX FIFO for port 4 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (*RX FIFO Errored Frame Drop Enable ($ 0x59F)*) • Frames are greater than the MaxFrameSize (*Max Frame Size ($ Port_Index + 0x0F)*)	0x598	CoR	0x00000000
RX FIFO Number of Frames Removed on Port 5	This register counts all frames removed from the RX FIFO for port 5 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (*RX FIFO Errored Frame Drop Enable ($ 0x59F)*) • Frames are greater than the MaxFrameSize (*Max Frame Size ($ Port_Index + 0x0F)*)	0x599	CoR	0x00000000
RX FIFO Number of Frames Removed on Port 6	This register counts all frames removed from the RX FIFO for port 6 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (*RX FIFO Errored Frame Drop Enable ($ 0x59F)*) • Frames are greater than the MaxFrameSize (*Max Frame Size ($ Port_Index + 0x0F)*)	0x59A	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write.
2. For all Number of Frames Removed Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:22 - Reserved and R.
   Bits 21:0 - Described above.

Table 98 RX FIFO Number of Frames Removed Ports 0 to 9 ($ 0x594 - 0x59D) (Sheet 3 of 3)

Name[2]	Description	Address	Type[1]	Default
RX FIFO Number of Frames Removed on Port 7	This register counts all frames removed from the RX FIFO for port 7 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (*RX FIFO Errored Frame Drop Enable ($ 0x59F)*) • Frames are greater than the MaxFrameSize (*Max Frame Size ($ Port_Index + 0x0F)*)	0x59B	CoR	0x00000000
RX FIFO Number of Frames Removed on Port 8	This register counts all frames removed from the RX FIFO for port 8 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (*RX FIFO Errored Frame Drop Enable ($ 0x59F)*) • Frames are greater than the MaxFrameSize (*Max Frame Size ($ Port_Index + 0x0F)*)	0x59C	CoR	0x00000000
RX FIFO Number of Frames Removed on Port 9	This register counts all frames removed from the RX FIFO for port 9 by meeting one of the following conditions: • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (*RX FIFO Errored Frame Drop Enable ($ 0x59F)*) • Frames are greater than the MaxFrameSize (*Max Frame Size ($ Port_Index + 0x0F)*)	0x59D	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write.
2. For all Number of Frames Removed Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:22 - Reserved and R.
   Bits 21:0 - Described above.

Table 99 RX FIFO Port Reset ($ 0x59E) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: The soft reset register for each port in the RX block. Port ID = bit position in the register. To make the reset active, the bit must be set High. For example, reset of port 4 implies register value = 0001.0000. Setting the bit to 0 de-asserts the reset.				0x00000000
31:10	Reserved	Reserved	R	0x000000
9	RXFIFOPort 9 Reset	Port 9 0 = De-assert reset 1 = Reset	R/W	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 99 RX FIFO Port Reset ($ 0x59E) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
8	RXFIFOPort 8 Reset	Port 8 0 = De-assert reset 1 = Reset	R/W	0
7	RXFIFOPort 7 Reset	Port 7 0 = De-assert reset 1 = Reset	R/W	0
6	RXFIFOPort 6 Reset	Port 6 0 = De-assert reset 1 = Reset	R/W	0
5	RXFIFOPort 5 Reset	Port 5 0 = De-assert reset 1 = Reset	R/W	0
4	RXFIFOPort 4 Reset	Port 4 0 = De-assert reset 1 = Reset	R/W	0
3	RXFIFOPort 3 Reset	Port 3 0 = De-assert reset 1 = Reset	R/W	0
2	RXFIFOPort 2 Reset	Port 2 0 = De-assert reset 1 = Reset	R/W	0
1	RXFIFOPort 1 Reset	Port 1 0 = De-assert reset 1 = Reset	R/W	0
0	RXFIFOPort 0 Reset	Port 0 0 = De-assert reset 1 = Reset	R/W	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 100 RX FIFO Errored Frame Drop Enable ($ 0x59F) (Sheet 1 of 3)

Bit	Name	Description	Type[1]	Default
Register Description: This register is used in conjunction with the RX Packet Filter Control Register bits to select whether errored or filtered frames are to be dropped.				0x00000000
31:10	Reserved	Reserved	R	0x000000
9	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the *RX Packet Filter Control ($ Port_Index + 0x19)* bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 9: 0 = Do not drop frames 1 = Drop frames	R/W	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 100 RX FIFO Errored Frame Drop Enable ($ 0x59F) (Sheet 2 of 3)

Bit	Name	Description	Type[1]	Default
8	RX FIFO Errored Frame Drop Enable Port 8	These bits are used in conjunction with the *RX Packet Filter Control ($ Port_Index + 0x19)* bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 8: 0 = Do not drop frames 1 = Drop frames	R/W	0
7	RX FIFO Errored Frame Drop Enable Port 7	These bits are used in conjunction with the *RX Packet Filter Control ($ Port_Index + 0x19)* bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 7: 0 = Do not drop frames 1 = Drop frames	R/W	0
6	RX FIFO Errored Frame Drop Enable Port 6	These bits are used in conjunction with the *RX Packet Filter Control ($ Port_Index + 0x19)* bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 6: 0 = Do not drop frames 1 = Drop frames	R/W	0
5	RX FIFO Errored Frame Drop Enable Port 5	These bits are used in conjunction with the *RX Packet Filter Control ($ Port_Index + 0x19)* bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 5: 0 = Do not drop frames 1 = Drop frames	R/W	0
4	RX FIFO Errored Frame Drop Enable Port 4	These bits are used in conjunction with the *RX Packet Filter Control ($ Port_Index + 0x19)* bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 4: 0 = Do not drop frames 1 = Drop frames	R/W	0
3	RX FIFO Errored Frame Drop Enable Port 3	These bits are used in conjunction with the *RX Packet Filter Control ($ Port_Index + 0x19)* bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 3: 0 = Do not drop frames 1 = Drop frames	R/W	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 100 RX FIFO Errored Frame Drop Enable ($ 0x59F) (Sheet 3 of 3)

Bit	Name	Description	Type[1]	Default
2	RX FIFO Errored Frame Drop Enable Port 2	These bits are used in conjunction with the *RX Packet Filter Control ($ Port_Index + 0x19)* bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 2: 0 = Do not drop frames 1 = Drop frames	R/W	0
1	RX FIFO Errored Frame Drop Enable Port 1	These bits are used in conjunction with the *RX Packet Filter Control ($ Port_Index + 0x19)* bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 1: 0 = Do not drop frames 1 = Drop frames	R/W	0
0	RX FIFO Errored Frame Drop Enable Port 0	These bits are used in conjunction with the *RX Packet Filter Control ($ Port_Index + 0x19)* bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 0: 0 = Do not drop frames 1 = Drop frames	R/W	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 101 RX FIFO Overflow Event ($ 0x5A0) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: This register provides a status if a FIFO-full situation has occurred (for example, a FIFO overflow). The bit position equals the port number. This register is cleared on Read.				0x00000000
31:10	Reserved	Reserved	R	0x000000
9	RX FIFO Overflow Event Port 9	Port 9 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
8	RX FIFO Overflow Event Port 8	Port 8 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
7	RX FIFO Overflow Event Port 7	Port 7 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
6	RX FIFO Overflow Event Port 6	Port 6 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
5	RX FIFO Overflow Event Port 5	Port 5 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 101 RX FIFO Overflow Event ($ 0x5A0) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
4	RX FIFO Overflow Event Port 4	Port 4 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
3	RX FIFO Overflow Event Port 3	Port 3 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
2	RX FIFO Overflow Event Port 2	Port 2 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
1	RX FIFO Overflow Event Port 1	Port 1 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
0	RX FIFO Overflow Event Port 0	Port 0 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

8.5.7 TX Block Register Overview

Table 102 through Table 108 on page 159 provide an overview of the TX Block Registers, which include the TX FIFO High and Low Watermark.

Table 102 TX FIFO High Watermark Ports 0 to 9 ($ 0x600 - 0x609) (Sheet 1 of 2)

Name[2]	Description	Address	Type[1]	Default
TX FIFO High Watermark Port 0	High watermark for TX FIFO port 0. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x600	R/W	0x00000630
TX FIFO High Watermark Port 1	High watermark for TX FIFO port 1. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x601	R/W	0x00000630
TX FIFO High Watermark Port 2	High watermark for TX FIFO port 2. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x602	R/W	0x00000630

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. For all TX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and R.
   Bits 12:0 - Described above.

Table 102 TX FIFO High Watermark Ports 0 to 9 ($ 0x600 - 0x609) (Sheet 2 of 2)

Name[2]	Description	Address	Type[1]	Default
TX FIFO High Watermark Port 3	High watermark for TX FIFO port 3. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x603	R/W	0x00000630
TX FIFO High Watermark Port 4	High watermark for TX FIFO port 4. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x604	R/W	0x00000630
TX FIFO High Watermark Port 5	High watermark for TX FIFO port 5. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x605	R/W	0x00000630
TX FIFO High Watermark Port 6	High watermark for TX FIFO port 6. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x606	R/W	0x00000630
TX FIFO High Watermark Port 7	High watermark for TX FIFO port 7. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x607	R/W	0x00000630
TX FIFO High Watermark Port 8	High watermark for TX FIFO port 8. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x608	R/W	0x00000630
TX FIFO High Watermark Port 9	High watermark for TX FIFO port 9. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x609	R/W	0x00000630

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. For all TX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and R.
   Bits 12:0 - Described above.

Table 103 TX FIFO Low Watermark Ports 0 to 9 ($ 0x60A - 0x613) (Sheet 1 of 2)

Name[2]	Description	Address	Type[1]	Default
TX FIFO Low Watermark Port 0	Low watermark for TX FIFO port 0. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60A	R/W	0x000001D0
TX FIFO Low Watermark Port 1	Low watermark for TX FIFO port 1. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60B	R/W	0x000001D0
TX FIFO Low Watermark Port 2	Low watermark for TX FIFO port 2. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60C	R/W	0x000001D0
TX FIFO Low Watermark Port 3	Low watermark for TX FIFO port 3. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60D	R/W	0x000001D0
TX FIFO Low Watermark Port 4	Low watermark for TX FIFO port 4. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60E	R/W	0x000001D0
TX FIFO Low Watermark Port 5	Low watermark for TX FIFO port 5. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60F	R/W	0x000001D0
TX FIFO Low Watermark Port 6	Low watermark for TX FIFO port 6. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x610	R/W	0x000001D0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. For all TX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and R.
   Bits 12:0 - Described above.

Table 103 TX FIFO Low Watermark Ports 0 to 9 ($ 0x60A - 0x613) (Sheet 2 of 2)

Name[2]	Description	Address	Type[1]	Default
TX FIFO Low Watermark Port 7	Low watermark for TX FIFO port 7. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x611	R/W	0x000001D0
TX FIFO Low Watermark Port 8	Low watermark for TX FIFO port 8. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x612	R/W	0x000001D0
TX FIFO Low Watermark Port 9	Low watermark for TX FIFO port 9. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x613	R/W	0x000001D0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. For all TX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and R.
   Bits 12:0 - Described above.

Table 104 TX FIFO MAC Transfer Threshold Ports 0 to 9 ($ 0x614 - 0x61D) (Sheet 1 of 3)

Name[2]	Description[3]	Address	Type[1]	Default
TX FIFO MAC Transfer Threshold Port 0	Sets the value at which the FIFO begins to transfer data to the MAC. The bottom 3 bits of this register are ignored, and the threshold is set in increments of 8-byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x614	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 1	Sets the value at which the FIFO begins to transfer data to the MAC. The bottom 3 bits of this register are ignored, and the threshold is set in increments of 8-byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x615	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 2	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x616	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 3	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x617	R/W	0x00000100

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. For all MAC Transfer Threshold Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and R.
   Bits 12:0 - Described above.
3. For proper operation of the IXF1010 MAC, the MAC transfer threshold must be set to greater than the MaxBurst1 on the SPI4-2.

Table 104 TX FIFO MAC Transfer Threshold Ports 0 to 9 ($ 0x614 - 0x61D) (Sheet 2 of 3)

Name[2]	Description[3]	Address	Type[1]	Default
TX FIFO MAC Transfer Threshold Port 4	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x618	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 5	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x619	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 6	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x61A	R/W	0x00000100

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. For all MAC Transfer Threshold Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and R.
   Bits 12:0 - Described above.
3. For proper operation of the IXF1010 MAC, the MAC transfer threshold must be set to greater than the MaxBurst1 on the SPI4-2.

Table 104 TX FIFO MAC Transfer Threshold Ports 0 to 9 ($ 0x614 - 0x61D) (Sheet 3 of 3)

Name[2]	Description[3]	Address	Type[1]	Default
TX FIFO MAC Transfer Threshold Port 7	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x61B	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 8	Sets the value at which the FIFO begins to transfer data to the MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x61C	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 9	Sets the value at which the FIFO begins to transfer data to the MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x61D	R/W	0x00000100

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. For all MAC Transfer Threshold Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and R.
   Bits 12:0 - Described above.
3. For proper operation of the IXF1010 MAC, the MAC transfer threshold must be set to greater than the MaxBurst1 on the SPI4-2.

Table 105 TX FIFO Overflow Event ($ 0x61E) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: This register provides status that a FIFO- full situation has occurred (for example, a FIFO overflow). The bit position equals the port number. This register is cleared on Read.				0x00000000
31:10	Reserved	Reserved	R	0x000000
9	TX FIFO Overflow Event Port 9	Port 9 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
8	TX FIFO Overflow Event Port 8	Port 8 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 105 TX FIFO Overflow Event ($ 0x61E) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
7	TX FIFO Overflow Event Port 7	Port 7 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
6	TX FIFO Overflow Event Port 6	Port 6 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
5	TX FIFO Overflow Event Port 5	Port 5 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
4	TX FIFO Overflow Event Port 4	Port 4 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
3	TX FIFO Overflow Event Port 3	Port 3 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
2	TX FIFO Overflow Event Port 2	Port 2 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
1	TX FIFO Overflow Event Port 1	Port 1 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0
0	TX FIFO Overflow Event Port 0	Port 0 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	CoR	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 106 TX FIFO Drain ($0x620) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: This register enables the TX FIFO drain mode for the selected port by holding the TX FIFO for that port in reset. All data stored in the TX FIFO is lost when this bit is set to 1. When this bit is set to 1, the TX FIFO status for the selected port is STARVING.				0x00000000
31:10	Reserved	Reserved	R	0x000000
9	TX FIFO Drain Port 9	Port 9 0 = Disable TX FIFO drain mode 1 = Enable TX FIFO drain mode	R/W	0
8	TX FIFO Drain Port 8	Port 8 0 = Disable TX FIFO drain mode 1 = Enable TX FIFO drain mode	R/W	0
7	TX FIFO Drain Port 7	Port 7 0 = Disable TX FIFO drain mode 1 = Enable TX FIFO drain mode	R/W	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 106 TX FIFO Drain ($0x620) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
6	TX FIFO Drain Port 6	Port 6 0 = Disable TX FIFO drain mode 1 = Enable TX FIFO drain mode	R/W	0
5	TX FIFO Drain Port 5	Port 5 0 = Disable TX FIFO drain mode 1 = Enable TX FIFO drain mode	R/W	0
4	TX FIFO Drain Port 4	Port 4 0 = Disable TX FIFO drain mode 1 = Enable TX FIFO drain mode	R/W	0
3	TX FIFO Drain Port 3	Port 3 0 = Disable TX FIFO drain mode 1 = Enable TX FIFO drain mode	R/W	0
2	TX FIFO Drain Port 2	Port 2 0 = Disable TX FIFO drain mode 1 = Enable TX FIFO drain mode	R/W	0
1	TX FIFO Drain Port 1	Port 1 0 = Disable TX FIFO drain mode 1 = Enable TX FIFO drain mode	R/W	0
0	TX FIFO Drain Port 0	Port 0 0 = Disable TX FIFO drain mode 1 = Enable TX FIFO drain mode	R/W	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 107 TX FIFO Info Out-of-Sequence ($ 0x621) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: This register signals when out-of-sequence data is detected in the TX FIFO. Events such as SOP followed by another SOP cause this bit to be set and remain so until read. This register is cleared on Read.				0x00000000
31:10	Reserved	Reserved	R	0x000000
9	TX FIFO Info Out-of-Sequence Port 9	Port 9 0 = FIFO out-of-sequence event did not occur 1 = FIFO out-of-sequence event occurred	CoR	0
8	TX FIFO Info Out-of-Sequence Port 8	Port 8 0 = FIFO out-of-sequence event did not occur 1 = FIFO out-of-sequence event occurred	CoR	0
7	TX FIFO Info Out-of-Sequence Port 7	Port 7 0 = FIFO out-of-sequence event did not occur 1 = FIFO out-of-sequence event occurred	CoR	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 107 TX FIFO Info Out-of-Sequence ($ 0x621) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
6	TX FIFO Info Out-of-Sequence Port 6	Port 6 0 = FIFO out-of-sequence event did not occur 1 = FIFO out-of-sequence event occurred	CoR	0
5	TX FIFO Info Out-of-Sequence Port 5	Port 5 0 = FIFO out-of-sequence event did not occur 1 = FIFO out-of-sequence event occurred	CoR	0
4	TX FIFO Info Out-of-Sequence Port 4	Port 4 0 = FIFO out-of-sequence event did not occur 1 = FIFO out-of-sequence event occurred	CoR	0
3	TX FIFO Info Out-of-Sequence Port 3	Port 3 0 = FIFO out-of-sequence event did not occur 1 = FIFO out-of-sequence event occurred	CoR	0
2	TX FIFO Info Out-of-Sequence Port 2	Port 2 0 = FIFO out-of-sequence event did not occur 1 = FIFO out-of-sequence event occurred	CoR	0
1	TX FIFO Info Out-of-Sequence Port 1	Port 1 0 = FIFO out-of-sequence event did not occur 1 = FIFO out-of-sequence event occurred	CoR	0
0	TX FIFO Info Out-of-Sequence Port 0	Port 0 0 = FIFO out-of-sequence event did not occur 1 = FIFO out-of-sequence event occurred	CoR	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 108 TX FIFO Number of Frames Removed Ports 0-9 ($ 0x622 - 0x62B) (Sheet 1 of 2)

Name	Description	Address	Type[1]	Default
TX FIFO Number of Frames Removed on Port 0	This register counts the number of frames removed on port 0 due to a TX FIFO overflow.	0x622	CoR	0x00000000
TX FIFO Number of Frames Removed on Port 1	This register counts the number of frames removed on port 1 due to a TX FIFO overflow.	0x623	CoR	0x00000000
TX FIFO Number of Frames Removed on Port 2	This register counts the number of frames removed on port 2 due to a TX FIFO overflow.	0x624	CoR	0x00000000
TX FIFO Number of Frames Removed on Port 3	This register counts the number of frames removed on port 3 due to a TX FIFO overflow.	0x625	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 108 TX FIFO Number of Frames Removed Ports 0-9 ($ 0x622 - 0x62B) (Sheet 2 of 2)

Name	Description	Address	Type[1]	Default
TX FIFO Number of Frames Removed on Port 4	This register counts the number of frames removed on port 4 due to a TX FIFO overflow.	0x626	CoR	0x00000000
TX FIFO Number of Frames Removed on Port 5	This register counts the number of frames removed on port 5 due to a TX FIFO overflow.	0x627	CoR	0x00000000
TX FIFO Number of Frames Removed on Port 6	This register counts the number of frames removed on port 6 due to a TX FIFO overflow.	0x628	CoR	0x00000000
TX FIFO Number of Frames Removed on Port 7	This register counts the number of frames removed on port 7 due to a TX FIFO overflow.	0x629	CoR	0x00000000
TX FIFO Number of Frames Removed on Port 8	This register counts the number of frames removed on port 8 due to a TX FIFO overflow.	0x62A	CoR	0x00000000
TX FIFO Number of Frames Removed on Port 9	This register counts the number of frames removed on port 9 due to a TX FIFO overflow.	0x62B	CoR	0x00000000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

8.5.8 MDIO Block Register Overview

Table 109 through Table 112 on page 161 provide an overview of the MDIO Block Registers

Table 109 MDI Single Command ($ 0x680) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: This register contains the PHY address and the register within the PHY with which the IXF1010 MAC is communicating. The MDI Single command and address register also contain the operation that the IXF1010 MAC is attempting (for example, Read or Write across the MDIO) and the status of the MDIO [operation in progress or operation complete].				0x00000000
31:21	Reserved	Reserved	R	00000000000
20	MDI Command	Performs an MDIO access. When set, this bit self clears upon completion of the access. 0 = MDIO access completed 1 = Performs an MDIO access	R/W	0
19:18	Reserved	Reserved	R	00
17:16	OP Code	MDIO Op Code 00 = Reserved 01 = Write Access 10 = Read Access 11 = Reserved	R/W	01
15:13	Reserved	Reserved	R	000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write

Table 109 MDI Single Command ($ 0x680) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
12:8	PHY Address	Address of external PHY device	R/W	00000
7:5	Reserved	Reserved	R	000
4:0	REG Address	Address of register within external PHY	R/W	00000
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 110 MDI Single Read and Write Data ($ 0x681)

Bit	Name	Description	Type[1]	Default
Register Description: This register contains the MDI Data read from the external device and the data the IXF1010 MAC is writing to the external PHY.				0x00000000
31:16	MDI Read Data	Read Data from external device	R	0x0000
15: 0	MDI Write Data	Write data for MDI Writes to the external device.	R/W	0x0000
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 111 Autoscan PHY Address Enable ($ 0x682)

Bit	Name	Description	Address	Type[1]	Default
Register Description: This register enables and disables the autoscan on a per-port basis					0x000003FF
31:0	Autoscan PHY Address Enable	Defines valid PHY addresses Each bit enables the corresponding PHY address for autoscan operation: 0 = Disable this PHY Address 1 = Enable this PHY Address	0x682	R/W	0x000003FF
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write					

Table 112 MDI Control ($ 0x683) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: This register contains the information on the progress of the MDIO, the speed of the clock (MDC) and whether autoscan is enabled				0x00000000
31:4	Reserved	Reserved	R	0x0000000
3	MDIO in Prog	Status of MDIO single transaction 0 = MDIO single command not in progress (Default) 1 = MDIO single command in progress	R/W	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 112 MDI Control ($ 0x683) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
2	MDIO in Prog Enable	Enable the MDIO IN PROG Register bit 0 = MDIO IN PROG Register bit disabled (Default) 1 = MDIO IN PROG Register bit enabled	R/W	0
1	Autoscan Enable	Enable continuous Autoscan operation 0 = Autoscan disabled (default) 1 = Autoscan enabled	R/W	0
0	MDC Speed	Selects speed of MDC clock 0 = MDC runs at 2.5 MHz 1 = MDC runs at 17.8 MHz	R/W	0
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

8.5.9 SPI4-2 Block Register Overview

Table 113 through Table 116 on page 164 provide an overview of the SPI4-2 Block Registers.

Table 113 SPI4-2 RX Burst Size ($ 0x700)

Bit	Name	Description	Type[1]	Default
Register Description: SPI4-2 RX interface start-up parameters for burst size.				0x00060002
31	idles	0 = Zero idle insertion between transfer bursts 1 = Inserts four idle control words between each burst. (This occurs not only on an EOP, but also at the end of every MaxBurst1 or MaxBurst2.	R/W	0x0
30:25	Reserved	Reserved	R	0x00
24:16	MaxBurst1	Maximum number of 16-byte blocks that the FIFO in the receive path, external to the IXF1010 MAC, can accept when the FIFO Status channel indicates STARVING. ***Note:*** Do not program these bits below 0x2 (32 byte burst).	R/W	0x006
15:9	Reserved	Reserved	R	0x00
8:0	MaxBurst2	Maximum number of 16-byte blocks that the FIFO in the receive path, external to the IXF1010 MAC, can accept when the FIFO Status channel indicates HUNGRY. ***Note:*** Do not program these bits below 0x2 (32 byte burst).	R/W	0x002
1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write				

Table 114 SPI4-2 RX Training ($ 0x701)

Bit	Name	Description	Type[1]	Default
Register Description: SPI4-2 RX interface start-up parameters for training sequences				0x00000000
31:24	Reserved	Reserved	R	0x00
23:16	REP_T	Number of repetitions of the data training sequence that must be scheduled every DATA_MAX_T cycles	R/W	0x00
15:0	DATA_MAX_T[2]	Maximum interval (in number of cycles) between scheduling of training sequences on receive data path interface An all zero value disables periodic training sequences.	R/W	0x0000

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. The value of DATA_MAX_T is the Most Significant 16 bits of a 24-bit counter value. The Least Significant 8 bits are always 0x00. This allows for a much larger DAT_MAX_T time-out period and provides a more than adequate granularity of selection.

Table 115 SPI4-2 RX Calendar ($ 0x702) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default Value
Register Description: SPI4-2 RX interface start-up parameters for FIFO status calendar operation.				0x00010300
31:30	RX Train Test Modes	00 = Normal mode 01 = Do not enter training based on a repeating “11” pattern on RSTAT[1:0] 1x = Train continuously	R/W	0x0
29	RSCLK_invert	0 = The FIFO status is captured on the rising edge of the RSCLK as per the SPI4-2 specification 1 = The FIFO status is captured on the falling edge of RSCLK ***Note:*** For proper operation, set this bit to the desired setting before the RSCLK is applied to the device.	R/W	0
28	TSCLK_invert	0 = The FIFO status is launched on the rising edge of the TSCLK as per the SPI4-2 specification 1 = The FIFO status is launched on the falling edge of TSCLK	R/W	0
27:21	Reserved	Reserved	R	0x000
20	DIP2_Error	Set based on an incorrect RX DIP2 result. This bit is cleared upon a read	CoR	0x0
19:16	DIP-2_Thr	Defines how many consecutive correct DIP-2s are required to disable sending of training sequences on the RX SPI4-2.	R/W	0x1
15:14	Reserved	Reserved	R	00

1. R = Read Only; CoR = Clear on Read; W = Write only; R/W = Read/Write

Table 115 SPI4-2 RX Calendar ($ 0x702) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default Value
13	RX SPI4-2 Sync	0 = RX SPI4 In Training (RDAT = training) ***Note:*** RX SPI4 Out Of Training (RDAT = idles)	R	0
12	TX SPI4 Sync	0 = TX SPI4-2 Calendar is in constant Framing ***Note:*** The TX SPI4-2 has received the valid training patterns on TDAT and is now sending a 10 port Calendar on TSAT with valid FIFO information	R	0
11:8	Loss_of_Sync	Loss-of-Sync is a parameter specifying the number of consecutive framing calendar cycles required to indicate a loss of synchronization and restart training sequences.	R/W	0x3
7:4	Reserved	Reserved	R	0x0
3:0	Reserved	Write as 0, ignore on Read.	R/W	0x0

1. R = Read Only; CoR = Clear on Read; W = Write only; R/W = Read/Write

Table 116 SPI4-2 TX Synchronization ($ 0x703)

Bit	Name	Description	Type[1]	Default
Register Description: SPI4-2 synchronization DIP-4 counters.				0x00000420
31:16	DIP4_Errors	DIP4_Errors is the total number of DIP4 errors detected since this register was last read.	CoR	0x0000
15:8	DIP4_UnLock[2]	DIP-4_Unlock is a SPI4-2 parameter specifying the number of incorrect DIP4 fields to be detected to declare loss of synchronization and drive the TSTAT[1:0] bus with framing.	R/W	0x04
7:0	DIP4_Lock	Number of consecutive correct DIP4 results to achieve synchronization and end training	R/W	0x20

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. When Periodic Training is enabled, the actual count of DIP4 errors required to lose synchronization is 1 less than the programmed value in this register. Therefore, this value should always be programmed to be 1 more than the desired value and should never be programmed to either 0 or 1.

9.0 Mechanical Specifications

CBGA packages are suited for applications requiring high I/O counts and high electrical performance. They are recommended for high-power applications, having high noise immunity requirements.

9.1 Features

- Flip chip die attach; surface mount second-level interconnect
- High electrical performance
- High I/O counts
- Area array I/O options
- Multiple power zone offering supports core and four additional voltages
- JEDEC-compliant package

9.2 IXF1010 MAC Package Specifics

The IXF1010 MAC uses the following packaging (see Figure 45, *552-Ceramic Ball Grid Array (CBGA) Package Specifications*, on page 167):

- 576-ball BGA package with 6 balls removed diagonally from each corner, for a total of 552 balls used measuring 25 mm x 25 mm
- Ball pitch of 1.0 mm
- Overall package dimensions of 25 mm x 25 mm

9.2.1 Markings

Figure 44 illustrates the IXF1010 MAC top label marking.

In contrast to the Pb-Free (RoHS-compliant) package, the non-RoHS-compliant package does not have the “e1” symbol.

Figure 44 Markings

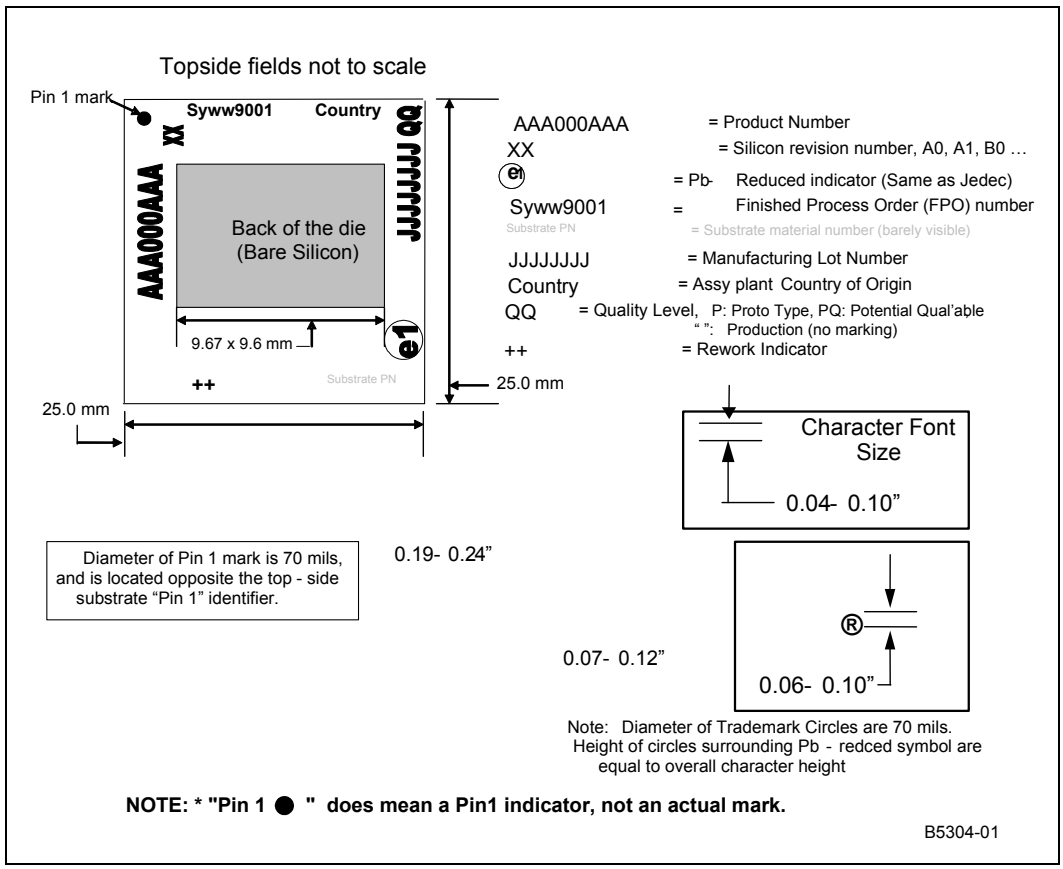
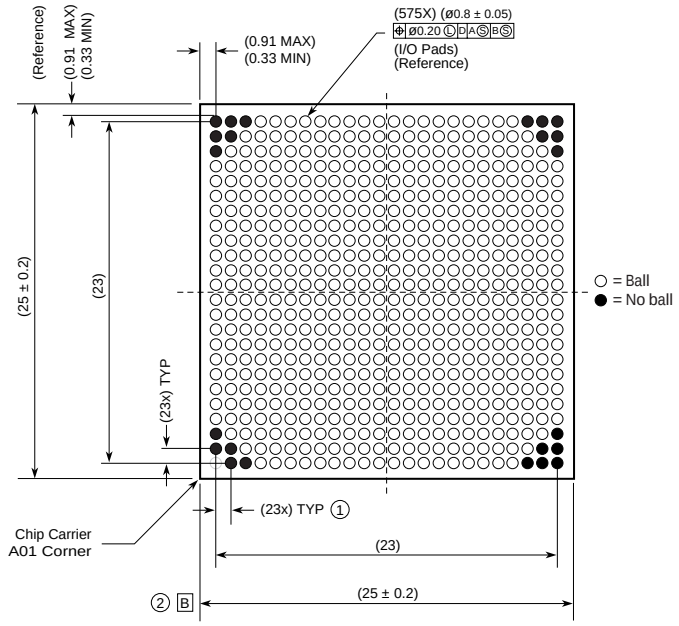
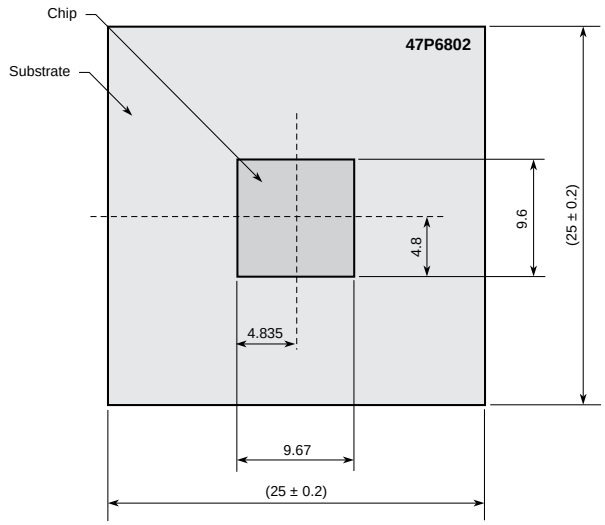


Figure 45 552-Ceramic Ball Grid Array (CBGA) Package Specifications



Note: All dimensions are in mm.

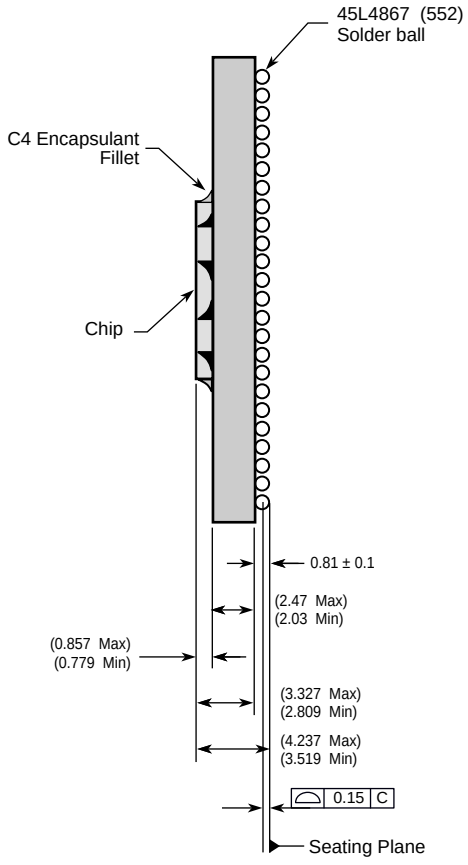
B0611-02



Note: All dimensions are in mm.

B0612-01

Figure 46 CBGA Package Side View Diagram



Note: All dimensions are in mm.

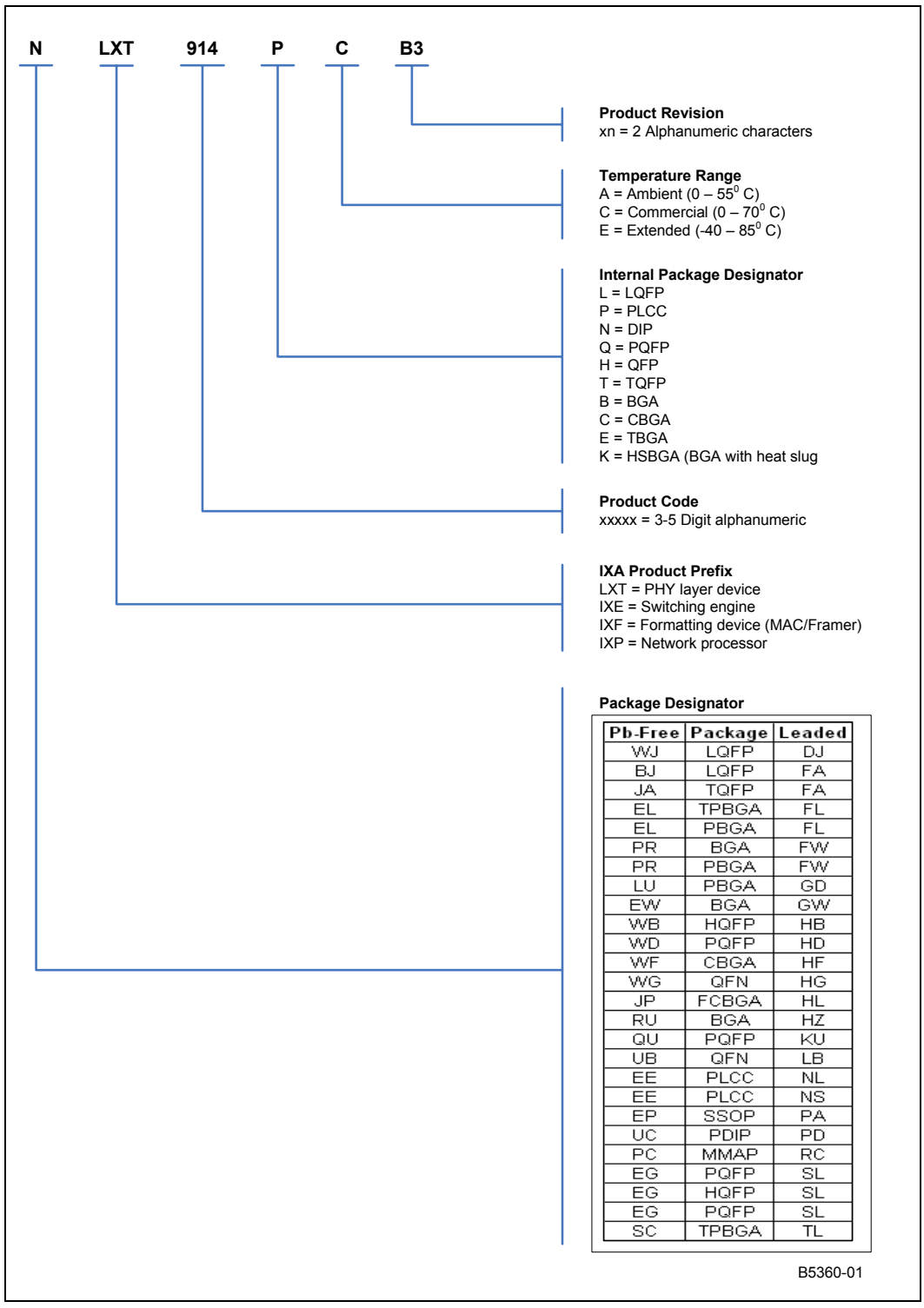
B0610-01

10.0 Product Ordering Information

Table 117 Product Ordering Information

Number	Revision	Ship Media	RoHS-Compliant
HFIXF1010CC.B2	B2	Tray	N
WFIXF1010CC.B2	B2	Tray	Y

Figure 47 Ordering Information - Sample



Pb-Free	Package	Leaded
WJ	LQFP	DJ
BJ	LQFP	FA
JA	TQFP	FA
EL	TPBGA	FL
EL	PBGA	FL
PR	BGA	FW
PR	PBGA	FW
LU	PBGA	GD
EW	BGA	GW
WB	HQFP	HB
WD	PQFP	HD
WF	CBGA	HF
WG	QFN	HG
JP	FCBGA	HL
RU	BGA	HZ
QU	PQFP	KU
UB	QFN	LB
EE	PLCC	NL
EE	PLCC	NS
EP	SSOP	PA
UC	PDIP	PD
PC	MMAP	RC
EG	PQFP	SL
EG	HQFP	SL
EG	PQFP	SL
SC	TPBGA	TL

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