CX86810

DFX214/DFX209
14400/9600 bps Fax Modem

Design Guide (Preliminary)

Conexant Proprietary Information

Doc. No. 102366B
April 29, 2004

CONEXANT®

Ordering Information: DFX214/DFX209 Modem Models and Features

Order/Model/Part Numbers		Supported Functions		
Modem Part No.	**Marketing Name**	**V.17 Fax up to 14,400 bps**	**V.29 Fax up to 9,600 bps**	**Russian Caller ID Supported**
CX86810-22	DFX214-C	Yes	Yes	Yes
CX86810-12	DFX214	Yes	Yes	No
CX86810-21	DFX209-C	No	Yes	Yes
CX86810-11	DFX209	No	Yes	No

Revision History

Revision	Date	Comments
B	4/29/2004	Rev. B release
A	3/11/2004	Initial release.

Reader Response: Conexant strives to produce quality documentation and welcomes your feedback. Please send comments and suggestions to conexant.tech.pubs@conexant.com. For technical questions, contact your local Conexant sales office or field applications engineer.

Contents

Figures

Tables

1. Introduction

1.1 Summary

The Conexant® CX86810 DFX214 and DFX209 facsimile modem family offers 14400 bps and 9600 bps half-duplex capability with functions supporting Type I and Type II Caller ID, Russian Caller ID (-C option), and V.23 full duplex modes. The modem models are identified in Table 1-1.

These functions are supplied in a single device. The Conexant CX86810 facsimile modem family is packaged in a 100-pin low-profile quad flat pack (LQFP) containing a Digital Signal Processor (DSP), and a Primary Integrated Analog (PIA) codec (Figure 1-1).

The modem can operate at 14400, 12000 (DFX214 family only), 9600, 7200, 4800, 2400, or 300 bps, and can perform HDLC framing for T.30 at all rates. A programmable DTMF detector, three programmable tone detectors, V.21 Channel 2 FSK 7E flag detector, Caller ID demodulator and ring detector are provided.

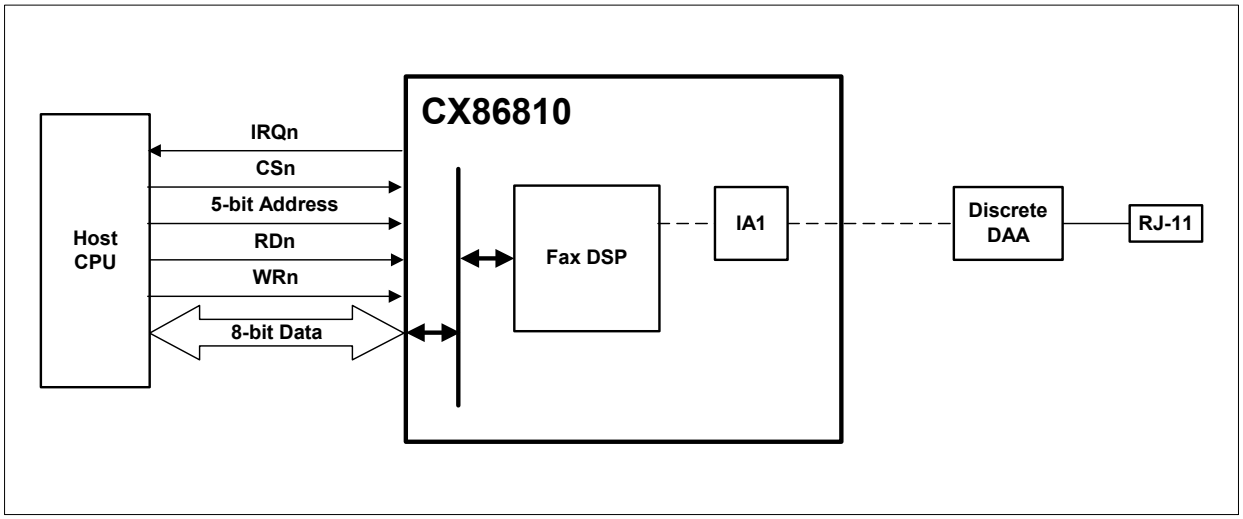
Both full-duplex transmit and receive (with asymmetric 1200/75 bps connection) and half-duplex (1200 bps) asynchronous V.23 are supported, as well as parallel interface to the modem. The V.23 algorithm includes a programmable receive compromise equalizer which is active in both V.23 and Caller ID (V.23 Receive only) modes. The modem can also optionally support Russian Caller ID.

Common applications for V.23 include France's Minitel and Japan's Lowest Cost Routing.

Table 1-1. Modem Models and Supported Features

Order/Model/Part Numbers		Supported Functions		
Modem Part No.	**Marketing Name**	**V.17 Fax up to 14,400 bps**	**V.29 Fax up to 9,600 bps**	**Russian Caller ID Supported**
CX86810-22	DFX214-C	Yes	Yes	Yes
CX86810-12	DFX214	Yes	Yes	No
CX86810-21	DFX209-C	No	Yes	Yes
CX86810-11	DFX209	No	Yes	No

Figure 1-1. CX86810 Block Diagram



102366_001

1.2 Features

- Group 3 facsimile transmission/reception
  - ITU-T V.17 (DFX214 models)
  - ITU-T V.29, V.27 ter, V.21 Channel 2
  - HDLC framing at all speeds
  - Receive dynamic range: 0 dBm to –43 dBm
  - Automatic adaptive equalization
  - Fixed and programmable digital compromise equalization
  - DTMF detect and tone detect
  - ITU-T V.21 Channel 2 FSK 7E Flag Detect
  - Ring detector
  - Programmable transmits level
  - Programmable single/dual tone transmission
- DTMF detect, tone detect and tone transmit
- Type II Caller ID CAS detection
- Russian Caller ID detection (optional)
- V.23 and Type I Caller ID
  - Full-duplex modes:
    - TX = 75 bps, RX = 1200 bps
    - TX = 1200 bps, RX = 75 bps
  - Half-duplex mode:
    - TX = RX = 1200 bps
  - Parallel data modes
  - 5, 6, 7, or 8 data bits
  - 1 or 2 Stop bits
  - Mark, Space, Even, or Odd Parity
  - Break function
  - Transmitter squelch
  - Compromise equalizer
- Programmable interface memory interrupt
- Three General Purpose Input (GPI) and two General Purpose Output (GPO) pins for host assignment
- TTL and CMOS compatible
- 3.3V operation
- Power consumption
  - Operating Mode: TBD
  - Sleep Mode: TBD
- Packaging
  - 100-pin LQFP

1.3 Technical Specifications

1.3.1 Modem

1.3.1.1 Configurations, Signaling Rates and Data Rates

The selectable modem configurations, along with the corresponding symbol (baud) rates and data rates, are listed in Table 1-3.

1.3.1.2 Scrambler/Descrambler

The modem incorporates a self-synchronizing scrambler/descrambler in accordance with ITU-T V.17 (DFX214 models), V.29, and V.27 ter recommendations, depending on the selected configuration.

1.3.1.3 Data Encoding

Data encoding conforms to ITU-T recommendations V.17 (DFX214 models), V.29, V.27 ter, V.21 Channel 2, V.23 and CID receive.

1.3.1.4 Fixed Digital Cable Compromise Equalizer

Compromise equalization can improve performance when operating over low quality lines. The modem has a selectable fixed digital compromise cable equalizer in the high speed receive and transmit data paths.

The modem includes an optional host programmable Receive Compromise Equalizer for V.23 1200 bps reception and Caller ID mode.

1.3.1.5 Transmitted Data Spectrum

Transmitted data spectrum is shaped in the baseband by an excess bandwidth finite impulse response filter (FIR) with the following characteristics:

When operating at 2400 baud, the transmitted spectrum is shaped by a square root of 20% raised cosine filter.

When operating at 1600 baud, the transmitted spectrum is shaped by a square root of 50% raised cosine filter.

When operating at 1200 baud, the transmitted spectrum is shaped by a square root of 90% raised cosine filter.

The out-of-band transmitter energy levels in the 4 kHz – 50 kHz frequency range is below –55 dBm.

1.3.1.6 Transmit Level

The transmitter output (TXA) level is programmable in the DSP RAM from 0 dBm to -15 dBm. The modem adjusts the output level by digitally scaling the output to the transmitter's digital-to-analog converter.

1.3.1.7 Turn-on Sequence

Transmitter turn-on sequence times are shown in Table 1-4.

1.3.1.8 Receive Dynamic Range

The receiver satisfies PSTN performance requirements for received line signal levels from 0 dBm to –43 dBm measured at the Receiver Analog Input (RXA) input. An external input buffer with 6 dB loss must be supplied between RXA and IA1_RXP/IA1_RXM.

The default values of the programmable Carrier Detector (CDET [register:bit 07:0]) turn-on and turn-off threshold levels are –43 dBm and –48 dBm, respectively. The CDET threshold levels can be programmed over the following range:

Turn on: –10 dBm to –47 dBm

Turn off: –10 dBm to –52 dBm

1.3.1.9 Automatic Adaptive Equalizer

An adaptive equalizer in ITU-T V.17 (DFX214 models), V.29, and V.27 ter modes compensates for transmission line amplitude and group delay distortion.

1.3.1.10 Receiver Timing

The timing recovery circuit can track a ±0.01% frequency error in the associated transmit timing source.

1.3.1.11 Carrier Recovery

The carrier recovery circuit can track a ±7 Hz frequency offset in the received carrier.

1.3.1.12 Turn-off Sequence

Transmitter turn-off sequence times are shown in Table 1-5.

1.3.1.13 V.23 Modem

The modem can transmit and detect Break signals (continuous Space).

The Mark and Space frequencies are 1300 Hz and 2100 Hz, respectively, for 1200 bps, and 390 Hz and 450 Hz, respectively, for 75 bps.

The modem transmitter output can be forced to zero.

The modem includes an optional host programmable Receive Compromise Equalizer for V.23 1200 bps reception and Caller ID Mode.

Default transmitter turn-on sequence time is shown in Table 1-2. See Section 4 for programming information.

Table 1-2. V.23 Default Turn-On and Turn-Off Sequences

Configuration	RTSP On to CTSP On	RTSP Off to CTSP Off
V.23 FDX	10.5 ms	2.2 ms

1.3.2 Tone Detectors and Generators

The tone detector signal path is separate from the main received signal path thus enabling tone detection to be independent of the receiver status. The tone detectors operate in all modes. The filter coefficients of each filter are host programmable in RAM.

The modem can generate voice-band single or dual tones from 0 Hz to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3400 Hz are attenuated. Dual tone generation allows the modem to operate as a programmable DTMF dialer.

Table 1-3. Configurations, Signaling Rates, and Data Rates

Configuration	Modulation[1]	Carrier Frequency (Hz) ±0.01%	Data Rate (bps) ±0.01%	Baud (Symbols/Sec.)	Bits/ Symbol	Constellation Points
V.17 14400 [2]	TCM	1800	14400	2400	6	128
V.17 12000 [2]	TCM	1800	12000	2400	5	64
V.17 9600 [2]	TCM	1800	9600	2400	4	32
V.17 7200 [2]	TCM	1800	7200	2400	3	16
V.29 9600	QAM	1700	9600	2400	4	16
V.29 7200	QAM	1700	7200	2400	3	8
V.29 4800	QAM	1700	4800	2400	2	4
V.27 ter 4800	DPSK	1800	4800	1600	3	8
V.27 ter 2400	DPSK	1800	2400	1200	2	4
V.21 Channel 2 300	FSK	1650, 1850	300	300	1	–
V.23 receive HDX	FSK	1300, 2100	1200	1200	1	–
V.23 1200/75	FSK	1300, 2100, 390, 450	1200/75	1200/75	1	–
Type I Caller ID	FSK	1200, 2200	1200	1200	1	–

Notes:

1. Modulation legend:
   - QAM: Quadrature Amplitude Modulation
   - DPSK: Differential Phase Shift Keying
   - FSK: Frequency Shift Keying
   - TCM: Trellis-Coded Modulation
2. DFX214 models only.

Table 1-4. Turn-On Sequence Times

	RTSP bit On to CTSP bit On	
Configuration	**Echo Protector Tone Disabled**	**Echo Protector Tone Enabled**
V.17	1395 ms	1602 ms
V.17 Short Train	144 ms	351 ms
V.29 Long Train	255 ms	443 ms
V.27 ter 4800 bps Long Train	710 ms	917 ms
V.27 ter 4800 bps Short Train	52 ms	259 ms
V.27 ter 2400 bps Long Train	945 ms	1152 ms
V.27 ter 2400 bps Short Train	69 ms	276 ms
V.21 Channel 2 300 bps	≤14 ms	≤ 14 ms

Table 1-5. Turn-Off Sequence Times

Configuration	Data and Scrambled Ones	No Transmitted Energy	Total
V.17	13.3 ms	20 ms	33.3 ms
V.29 Long Train	5 ms	20 ms	25 ms
V.27 ter 4800 bps Long and Short Train	7 ms	20 ms	27 ms
V.27 ter 2400 bps Long and Short Train	10 ms	20 ms	30 ms
V.21 Channel 2 300 bps	7 ms	0 ms	7 ms
Note: In HDLC mode, the turn-off sequence may be extended by more than 8-bit times.			

This page is intentionally blank.

2. Hardware Interface Signals

2.1 Hardware Interface

A functional interconnect diagram is shown in Figure 2-1.

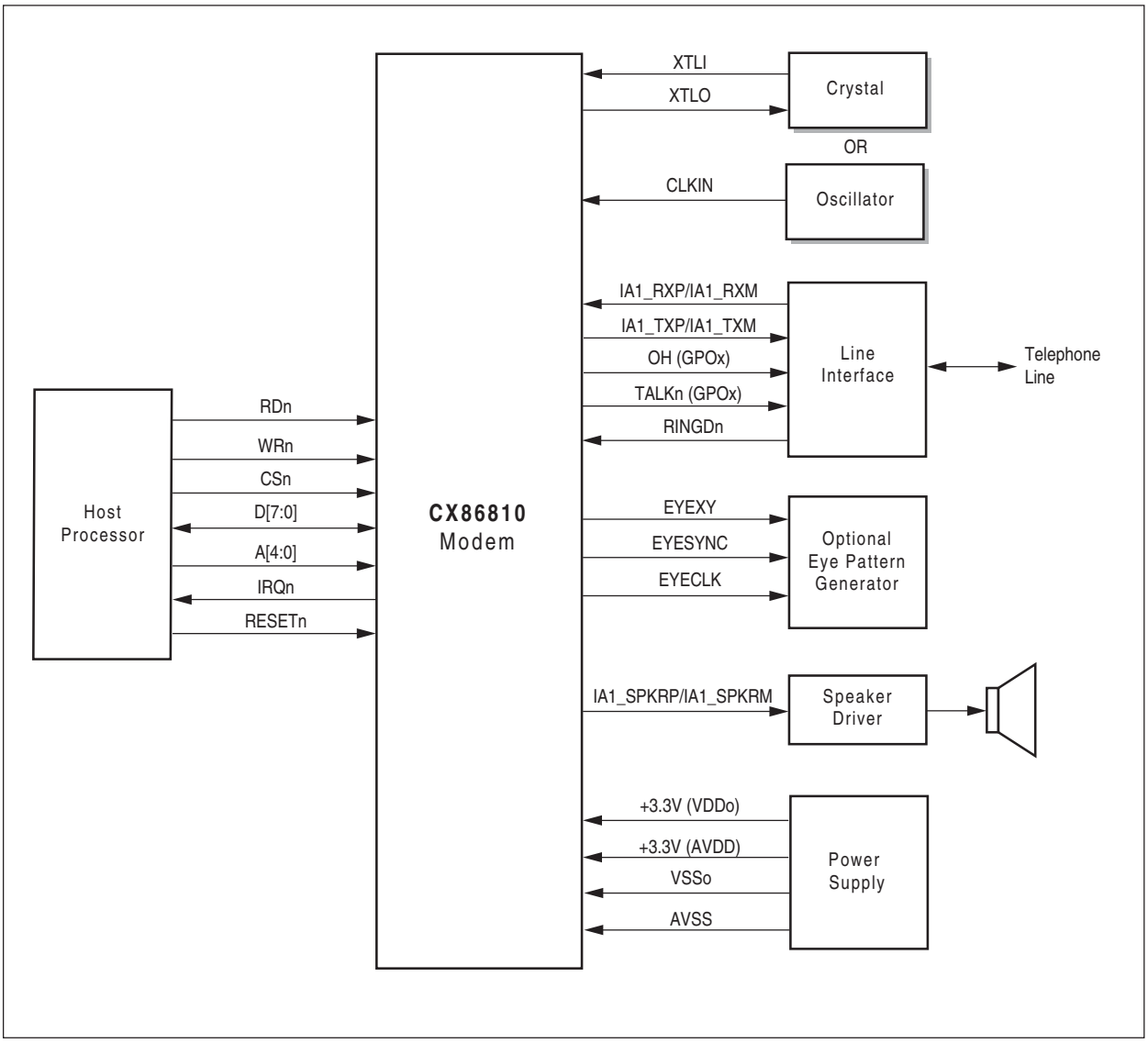
Pin assignments for the 100-pin LQFP package are shown in Figure 2-2 and are listed in Table 2-1.

Hardware interface signals are described in Table 2-2.

Digital signal characteristics are defined in Table 2-3.

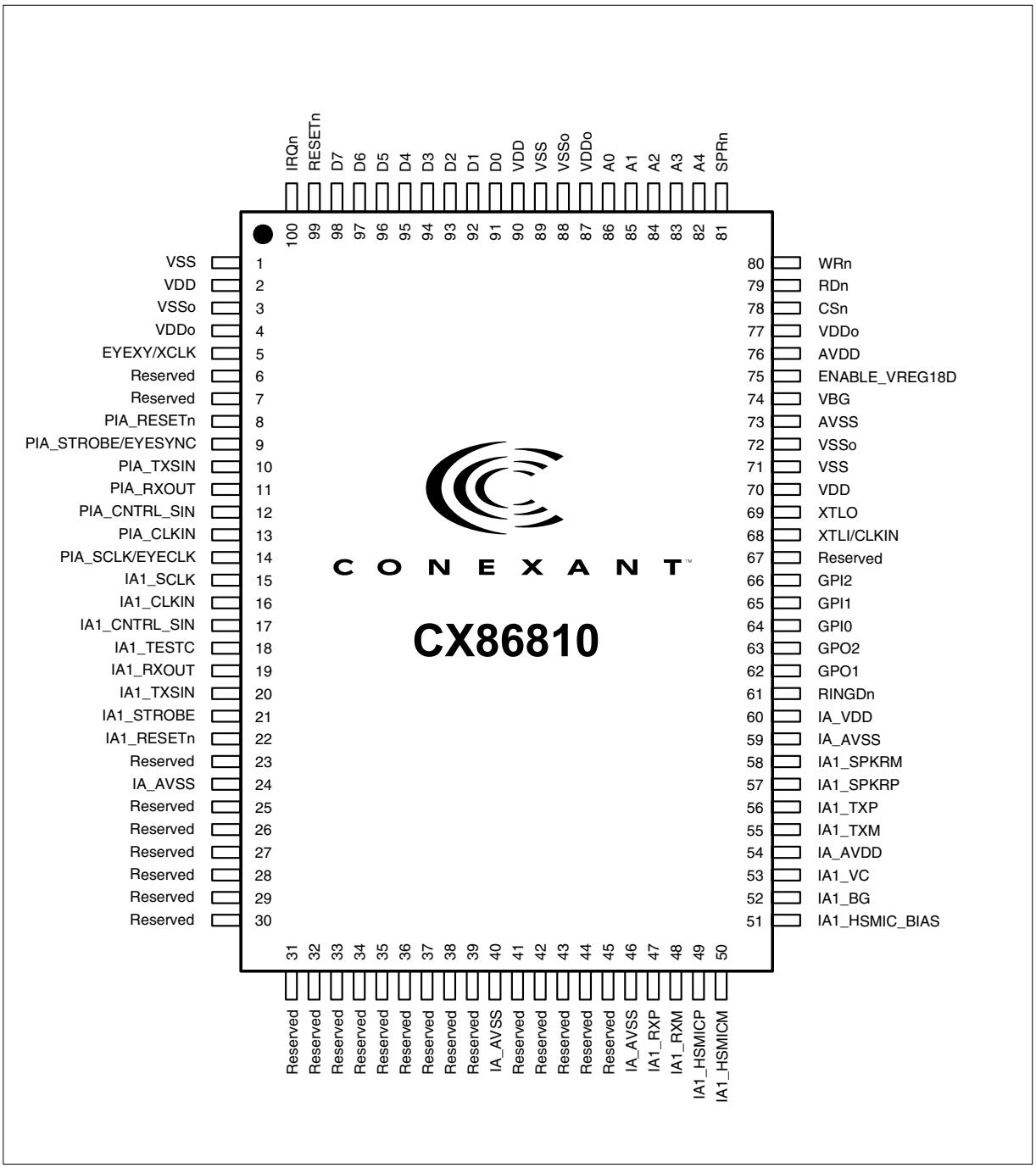
Analog signal characteristics are defined in Table 2-4.

Figure 2-1. Modem Functional Interconnect Diagram



102366_002

Figure 2-2. Modem Pin Signals - 100-Pin LQFP



102366_003

Table 2-1. Modem Pin Signals - 100-Pin LQFP

Pin	Signal Label	I/O	Interface	Pin	Signal Label	I/O	Interface
1	VSS	-	Digital Core GND	51	IA1_HSMIC_BIAS	I	Handset Mic. Bias
2	VDD	-	Digital Core Power 1.8V	52	IA1_BG	-	IA Internal Voltage Reference
3	VSSo	-	Digital Pad GND	53	IA1_VC	-	IA Bias Voltage
4	VDDo	-	Digital Pad Power 3.3V	54	IA_AVDD	-	IA Analog Power 3.3V
5	EYEXY/XCLK		Diagnostic	55	IA1_TXM	O	IA Line Out
6	Reserved	-	-	56	IA1_TXP	O	IA Line Out
7	Reserved	-	-	57	IA1_SPKRP	O	IA Speaker Out
8	PIA_RESETn	O	Power-On Reset	58	IA1_SPKRM	O	IA Speaker Out
9	PIA_STROBE/ EYESYNC	I	IA Interface	59	IA_AVSS	-	IA Analog GND
10	PIA_TXSIN	O	IA Interface	60	IA_VDD	-	IA Digital Power 3.3V
11	PIA_RXOUT	I	IA Interface	61	RINGDn	O	Ring Detect Indicate
12	PIA_CNTRL_SIN	O	IA Interface	62	GPO1	O	Host Interface
13	PIA_CLKIN	O	IA Interface	63	GPO2	O	Host Interface
14	PIA_SCLK/ EYECLK	I	IA Interface	64	GPI0	I	Host Interface
15	IA1_SCLK	O	IA Interface	65	GPI1	I	Host Interface
16	IA1_CLKIN	I	IA Interface	66	GPI2	I	Host Interface
17	IA1_CNTRL_SIN	I	IA Interface	67	Reserved	-	-
18	IA1_TESTC	I	IA Interface	68	XTLI/CLKIN	I	Clock Interface
19	IA1_RXOUT	O	IA Interface	69	XTLO	O	Clock Interface
20	IA1_TXSIN	I	IA Interface	70	VDD	-	Digital Core Power 1.8V
21	IA1_STROBE	O	IA Interface	71	VSS	-	Digital Core GND
22	IA1_RESETn	I	IA Interface	72	VSSo	-	Digital Pad Ground
23	Reserved	-		73	AVSS	-	Analog GND
24	IA_AVSS	-	IA Analog GND	74	VBG	-	Bandgap Reference
25	Reserved	-	-	75	ENABLE_VREG18D	I	Internal Regulator Enable
26	Reserved	-	-	76	AVDD	-	Analog Power 3.3V
27	Reserved	-	-	77	VDDo	-	Digital Pad Power 3.3V
28	Reserved	-	-	78	CSn	I	Host Interface
29	Reserved	-	-	79	RDn	I	Host Interface
30	Reserved	-	-	80	WRn	I	Host Interface
31	Reserved	-	-	81	SPRn	I	Host Interface
32	Reserved	-	-	82	A4	I	Host Interface
33	Reserved	-	-	83	A3	I	Host Interface
34	Reserved	-	-	84	A2	I	Host Interface
35	Reserved	-	-	85	A1	I	Host Interface
36	Reserved	-	-	86	A0	I	Host Interface
37	Reserved	-	-	87	VDDo	-	Digital Pad Power 3.3V
38	Reserved	-	-	88	VSSo	-	Digital Pad Ground
39	Reserved	-	-	89	VSS	-	Digital Core GND
40	IA_AVSS	-	IA Analog GND	90	VDD	-	Digital Core Power 1.8V
41	Reserved	-	-	91	D0	I/O	Host Interface
42	Reserved	-	-	92	D1	I/O	Host Interface
43	Reserved	-	-	93	D2	I/O	Host Interface
44	Reserved	-	-	94	D3	I/O	Host Interface
45	Reserved	-	-	95	D4	I/O	Host Interface
46	IA_AVSS	-	IA Analog GND	96	D5	I/O	Host Interface
47	IA1_RXP	I	IA Line In	97	D6	I/O	Host Interface
48	IA1_RXM	I	IA Line In	98	D7	I/O	Host Interface
49	IA1_HSMICP	I	IA Handset Mic	99	RESETn	I	Host Interface
50	IA1_HSMICM	I	IA Handset Mic	100	IRQn	O	Interrupt Request

Notes:

1. I/O:
   I = Input
   O = Output
   I/O = Input/Output

Table 2-2. Modem Hardware Interface Signal Definitions

Table Pin Name	Pin No	Pin I/O	I/O Type	Interface Signal Definition
Power/Ground, Reset, and Clock Pins				
XTLI/CLKIN	68	I	OSC	**Crystal Input/External Clock Input.** 32.256 MHz crystal/clock input. It includes a 1 MΩ bias register internally.
XTLO	69	O	OSC	**Crystal Output.** 32.256 MHz crystal output.
RESETn	99	I	GPH	**Reset.** After application of power to the modem, RESETn must be held low for at least 15 ms after the power reaches operating range. The modem is ready to use 25 ms after the low-to-high transition of RESETn. The reset sequence initializes the modem interface memory.
AVDD	76	-	-	**Voltage Regulator Power 3.3 V.**
AVSS	73	-	-	**Voltage Regulator Ground.**
VDDo	4, 77, 87	-	-	**Digital Pad Power 3.3 V.**
VDD	2, 70, 90	-	-	**Digital Core Power 1.8 V.** The VDD pins must be decoupled to VSS even if the internal 1.8V regulator is used.
VSSo	3, 72, 88	-	-	**Digital Pad Ground.**
VSS	1, 71, 89	-	-	**Digital Core Ground**
Host Interface Signals				
D[7:0]	91-98	I/O	GP	**Data Bus.** Eight bi-directional data lines (D0–D7) provide parallel transfer of data between the host and the modem. The most significant bit is D7.
A[4:0]	82-86	I	GP	**Address Bus.** Five active high inputs (A0–A4) address interface memory registers within the DSP when CSn is low.
CSn	78	I	GPH	**Chip Select.** The active low CSn input selects and enables the modem DSP for parallel data transfer between the DSP and the host over the microprocessor bus.
SPRn	81	I	GPH	**Select Program RAM.** Active low select used to access Program RAM (PRAM).
RDn	79	I	GPH	**Read Enable.** Reading is controlled by the host pulsing RDn input low during the microprocessor bus access cycle.
WRn	80	I	GPH	**Write Enable.** Writing is controlled by the host pulsing WRn input low during the microprocessor bus access cycle.
IRQn	100	O	GP	**Interrupt Request.** IRQn interrupt request output may be connected to the host processor interrupt request input to interrupt host program execution for immediate modem service. IRQn use is optional depending upon modem application. The IRQn output can be enabled in DSP interface memory. The IRQn signal can be connected with other active low, open-drain IRQ sources to form a single interrupt request in a wire-OR configuration. An external resistor to +3.3V is required on the line and should be located near the receiver of the IRQ.
IA1 Interface signals on DSP				
PIA_CLKIN	13	O	GP	Connect to IA1_CLKIN.
PIA_CNTRL_SIN	12	O	GP	Connect to IA1_CNTRL_SIN.
PIA_TXSIN	10	O	GP	Connect to IA1_TXSIN.
PIA_RESETn	8	O	GP	Connect to IA1_RESETn.
PIA_SCLK/EYECLK	14	I	GPH	Connect to IA1_SCLK. **Serial Eye Pattern Clock.** EYECLK is a 2.016 MHz output clock for use by the serial-parallel converters on an external eye pattern circuit.
PIA_RXOUT	11	I	GP	Connect to IA1_RXOUT.
PIA_STROBE/EYESYNC	9	I	GPH	Connect to IA1_STROBE. **Serial Eye Pattern Strobe.** EYESYNC is a strobe for loading the D/A converters on an external eye pattern circuit. The EYESYNC frequency is the same as the modem configuration sample rate.

Table 2-2. Modem Hardware Interface Signal Definitions

Table Pin Name	Pin No	Pin I/O	I/O Type	Interface Signal Definition
IA Signals On IA1				
IA1_CLKIN	16	I	PD	Connect to PIA_CLKIN.
IA1_CNTRL_SIN	17	I	PD	Connect to PIA_CNTRL_SIN.
IA1_TXSIN	20	I	PD	Connect to PIA_TXSIN.
IA1_RESETn	22	I	PU	Connect to PIA_RESETn.
IA1_SCLK	15	O	O	Connect to PIA_SCLK.
IA1_RXOUT	19	O	O	Connect to PIA_RXOUT.
IA1_STROBE	21	O	O	Connect to PIA_STROBE.
IA1_RXP IA1_RXM	47 48	I	IA	**Receive Analog Positive and Negative**. IA1_ RXM and IA1_RXP inputs are differential inputs that are 180 degrees out of phase with each other.
IA1_SPKRM IA1_SPKRM	57 58	O	OA	**Speaker Analog Output Positive and Negative.** IA1_SPKRM and IA1_SPKRP output are differential outputs, 180 degrees out of phase with each other. The IA1_SPKRM and IA1_SPKRP output can drive an impedance as low as 300 Ω.
IA1_TXP IA1_TXM	56 55	O	OA	**Transmit Analog Positive and Negative**. IA1_TXP and IA1_TXM outputs are differential outputs, 180 degrees out of phase with each other.
IA1_HSMICP IA1_HSMICM	49 50	I	IA	**Handset Mic input Positive and Negative.** IA1_HSMICP and IA1_HSMICM are differential inputs, 180 degrees out of phase with each other. Analog data input for handset.
IA1_HSMIC_BIAS	51	O	OA	**Handset Mic. Bias.** Microphone voltage bias output. It can be +2.2 V (default) or +2.5 V.
IA_VDD	60	-	-	**+3.3V Digital Power for IA.**
IA_AVDD	54	-	-	**+3.3V Analog Power for PIA.** Connect to +3.3V.
IA_AVSS	24, 40, 46, 59		-	**Ground for IA_AVDD.** Connect to Analog Ground.
IA1_TESTC	18	I	-	**IA Test**. Connect to GND.
IA1_BG	52	-	-	**Internal Voltage Reference.** Minimum 2.15 V, normal 2.2 V, and maximum 2.25 V. This signal should be tied through a 0.1 µF capacitor to analog VSS.
IA1_VC	53	-	-	**Analog Ground Bias Voltage**. 1.5 V for power supplies in the 3.0 V to 3.6 V range. This signal should be tied through a 0.1 µF capacitor to analog VSS.
General Purpose Input/Output Lines				
GPI0-GPI2	64, 65, 66	I	GPH	**General Purpose Inputs.** Three general purpose input (GPI) pins are available to the host for programming via the modem interface memory.
GPO1-GPO2	62, 63	O	GPH	**General Purpose Outputs**. Two general purpose output (GPO) pins are available to the host for programming via the modem interface memory.

Table 2-2. Modem Hardware Interface Signal Definitions

Table Pin Name	Pin No	Pin I/O	I/O Type	Interface Signal Definition
Diagnostic/Test				
EYEXY/XCLK	5	O	PLB03	**Serial Eye Pattern X/Y Output/X Clock Output.** EYEXY is a serial output containing two 16-bit diagnostic words for display on an oscilloscope X (EYEX) axis and Y axis (EYEY), using an external eye pattern circuit. XCLK is a 32.256 MHz clock. EYEX data is the first 16 bits, MSB first, that are shifted out on the high portion of the EYESYNC clock. EYEX is a serial bit stream that is the equivalent of modem interface memory register XDAM followed by XDAL. EYEY data is the second 16 bits, MSB first, that are shifted out on the low portion of the EYESYNC clock. EYEY is a serial bit stream that is the equivalent of modem interface memory register YDAM followed by YDAL. X Clock is 32.256 MHz.
Ring Indicator Signal				
RINGDn	61	I	GPH	**Ring Frequency Detected.** The Ring signal from the DAA, when connected to the RINGDn input, is monitored for pulses in the range of 15 Hz to 68 Hz. The frequency detection range may be changed by the host in DSP RAM. The circuit driving RINGDn should be a 4N35 optoisolator or equivalent. The circuit driving RINGDn should not respond to momentary bursts of ringing less than 125 ms in duration, or less than 40 VRMS (15 Hz to 68 Hz) across TIP and RING. The RI status bit in the interface memory reflects the logic level on the RINGDn pin.
Control and Reference				
VBG	74	-	-	**Bandage Reference Voltage (1.2 V).** Tie to ground through 0.1 µF capacitor.
ENABLE_VREG18D	75	I	PU	**Digital 1.8 Regulator Enable.** To enable the internal regulator, tie this pin directly to +3.3V (high) without a resistor. To disable the internal regulator, tie this pin directly to ground (low).
Reserved				
Reserved	6-7, 23, 25-39, 41-45, 67	-	-	**Reserved.** Leave open. No external connection allowed.

Table 2-3. Digital Electrical Characteristics

Parameter	Symbol	Min.	Max.	Units	Test Conditions
Pad Power Supply	VDDo	3.0	3.6	VDC	
Core Power Supply	VDD	1.65	1.95	VDC	
CMOS Input Low Voltage	VIL				
3V CMOS (GP)		0	0.8	VDC	
3V CMOS with Hysteresis (GPH)		0	0.3*VDDo	VDC	
CMOS Input High Voltage	VIH				
3V CMOS (GP)		2.0	VDDo	VDC	
3V CMOS with Hysteresis (GPH)		0.7*VDDo	VDDo	VDC	
CMOS Output Low Voltage (GP, GPH)	Vol				
Drive Strength = 125 – 500 Ω			0.4	VDC	IOL = 0.8 mA
Drive Strength = 45 – 180 Ω			0.4	VDC	IOL = 2.5 mA
Drive Strength = 25 – 95 Ω			0.4	VDC	IOL = 4.5 mA
Drive Strength = 22 – 85 Ω			0.4	VDC	IOL = 5 mA
Drive Strength = 16 – 65 Ω			0.4	VDC	IOL = 6.8 mA
Drive Strength = 18 – 55Ω (PLB03)			0.4	VDC	IOL = +7 mA
CMOS Output High Voltage (GP, GPH)					
Drive Strength = 125 – 500 Ω			VDDo-0.4	VDC	IOH = -0.8 mA
Drive Strength = 45 – 180 Ω			VDDo-0.4	VDC	IOH= -2.5 mA
Drive Strength = 25 – 95 Ω			VDDo-0.4	VDC	IOH = -4.5 mA
Drive Strength = 22 – 85 Ω			VDDo-0.4	VDC	IOH = -5 mA
Drive Strength = 16 – 65 Ω			VDDo-0.4	VDC	IOH = -6.8 mA
Input Hysteresis (H)	H	0.5		VDC	
Pull Up Resistance (PU)	PU	120	500	KΩ	DCCTL = 11
Pull Down Resistance (PD)	PD	120	500	KΩ	DCCTL = 01
XO Output Low Voltage (OSC)	VOL		0.4	VDC	IOL = +1.5 mA
XO Output High Voltage (OSC)	VOH	VDDo-0.4		VDC	IOH = -7.3 mA
XI Input Low Voltage (OSC)	VIL	0	0.3*VDDo	VDC	
XI Input Output Voltage (OSC)	VIH	0.7*VDDo	VDDo	VDC	

Table 2-4. Analog Electrical Characteristics

Signal Name	Characteristic	Value
IA1_RXM/IA1_RXP	Input Impedance	> 70K Ω
	AC Input Voltage Range	1.1 VP-P
	Reference Voltage	+1.35 VDC
IA1_TXM/IA1_TXP	Minimum Load	300 Ω
	Maximum Capacitive Load	0 µF
	Output Impedance	10 Ω
	AC Output Voltage Range	1.4 VP-P (with reference to ground and a 600 Ω load)
	Reference Voltage	+1.35 VDC
	DC Offset Voltage	± 200 mV
IA1_SPKRM/IA1_SPKRP	Minimum Load	300 Ω
	Maximum Capacitive Load	0.01 µF
	Output Impedance	10 Ω
	AC Output Voltage Range	1.4 VP-P
	Reference Voltage	+1.35 VDC
	DC Offset Voltage	± 20 mV
Test Conditions unless otherwise stated: VDDo = +3.3 ± 0.3 VDC; IA_AVDD = +3.3 ± 0.3 VDC, TA = 0°C to 70°C		

2.2 Electrical and Environmental Specifications

Modem operating conditions are specified in Table 2-5.

Modem absolute maximum ratings are stated in Table 2-5 .

Modem current and power requirements are listed in Table 2-7.

Table 2-5. Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Core Supply Voltage	VDD	1.65	1.8	1.95	VDC
I/O Supply Voltage	VDDo	3.0	3.3	3.6	VDC
Analog Supply Voltage	AVDD, IA_AVDD	3.0	3.3	3.6	VDC
Operating Ambient Temperature	T_A	0	25	70	°C

Table 2-6. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Comments
Pad Supply Voltage	VDDo		4.6	VDC	
Core Supply Voltage	VDD		2.5	VDC	
3V Only Pin Voltage				VDC	
Input, High Z	VIN3	-0.5	VDDo + 0.5	VDC	Not to exceed 4.6 V
Output, Low Z	VOUT3	-0.5	VDDo + 0.5	VDC	Not to exceed 4.6 V
Operating Temperature Range	T	0	+70	°C	
Storage Temperature Range	Tstg	-55	+125	°C	
Voltage Applied to Outputs in High Z State	VHz	-0.5	4.6	V	
Static Discharge Voltage (25°C) - HBM	ESD	-2500	+2500	V	
Static Discharge Voltage (25°C) - CDM	ESD2	250	250	V	
Latch-up Current (25°C)	Itrig	-300	+300	mA	

Table 2-7. Current and Power Requirements

Power Supply	Typical Current @ 25°	Maximum Current @ 0°C
Normal Mode		
VDDo	25 mA	
AVDD	2 mA	
IA_AVDD		
Sleep Mode		
VDDo		
AVDD		
IA_AVDD		

Notes:

1. Test conditions: VDDo, AVDD, and IA_AVDD = 3.3 VDC for typical values;
   VDDo, AVDD, and IA_AVDD = 3.6 VDC for maximum values.
2. Input Ripple less than 0.1 Vpeak-peak.
3. Data based on 32.256 MHz crystal frequency.

2.3 Scratchpad and PRAM I/O Interface

To write to a register, the host must send valid chip select and address. The address bus is held by using the latest falling edge of the CSn and WRn signals. The data is registered into the device on the rising edge of the write signal. To read a register, the host must send valid chip select and address. The address is decoded and used to multiplex data from the scratchpad so that is can be stored in an output register.

2.3.1 PRAM Access

The SPRn signal along with A0, CSn, RDn, WRn, and D[0:7] are used for PRAM accesses.

When SPRn is low, the data will go to/from the PRAM, otherwise, the data will go to/from the scratchpad interface.

When host wants to read PRAM continuously through the data bus, it should be noted that the PRAM address is incremented 2 cycles after the first data is read out. Therefore, in the first 2 cycles, the data from the same location will be read out. After that, each cycle will access different locations. Since the read bus is a 32-bit bus, it takes 5 accesses to retrieve the first set of data. After the initial 5 accesses, 4 accesses are required to retrieve each subsequent 32-bit set of data.

When the host wants to write data to the PRAM continuously through the data bus, since the write bus is 16-bit, it takes 2 writes to write to the lower (A0 = 0) and upper byte (A0 = 1) of 16-bit word. No dummy access is required in the write case.

2.3.2 Host Download Mode

In this mode the host can read/write to program memory through the scratchpad interface. Signal SPRn should be set low in this mode in order for the host to read/write to program memory. The starting address will be loaded into address generator by the modem. For the write case, the data from the program memory address is read out the host port. After the read or write, the address in the address generator will be automatically incremented. Since the input data bus has only 8-bit and the program memory data bus has 16-bit, the lower byte is latched first when the host wants to write the program RAM, A0=0 (host address bit 0). Toggling A0 to a logic one means the host is sending the upper byte of data. Only after the upper byte has been latched, the address is incremented in the address generator. A0 has the same function in the read interface except that the read data is 32-bit.

2.3.3 Scratchpad and PRAM I/O Interface Waveforms and Timing

Host write timing and host read timing are illustrated in Figure 2-3 and Figure 2-4, respectively.

PRAM write timing and PRAM read timing are illustrated in Figure 2-5 and Figure 2-6, respectively. Also see Function 4:41 in Section 4.

Host and PRAM interface timing parameters are listed in Table 2-8.

Figure 2-3. Host Write Timing

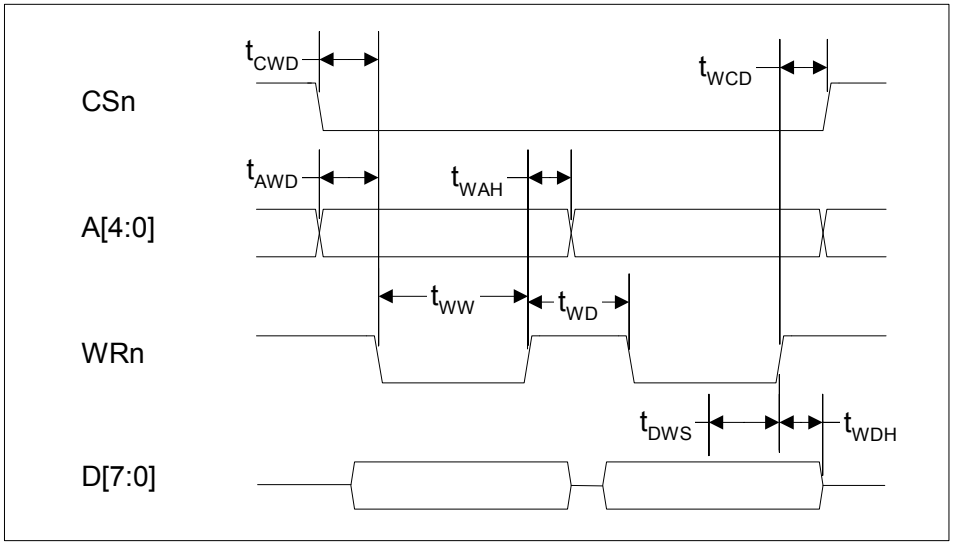


Figure 2-4. Host Read Timing

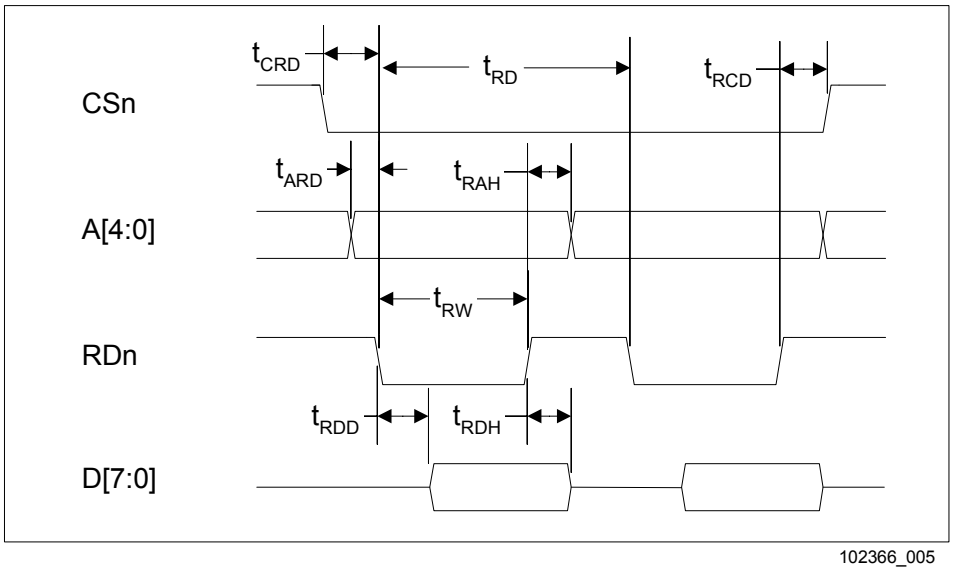


Figure 2-5. PRAM Write Timing

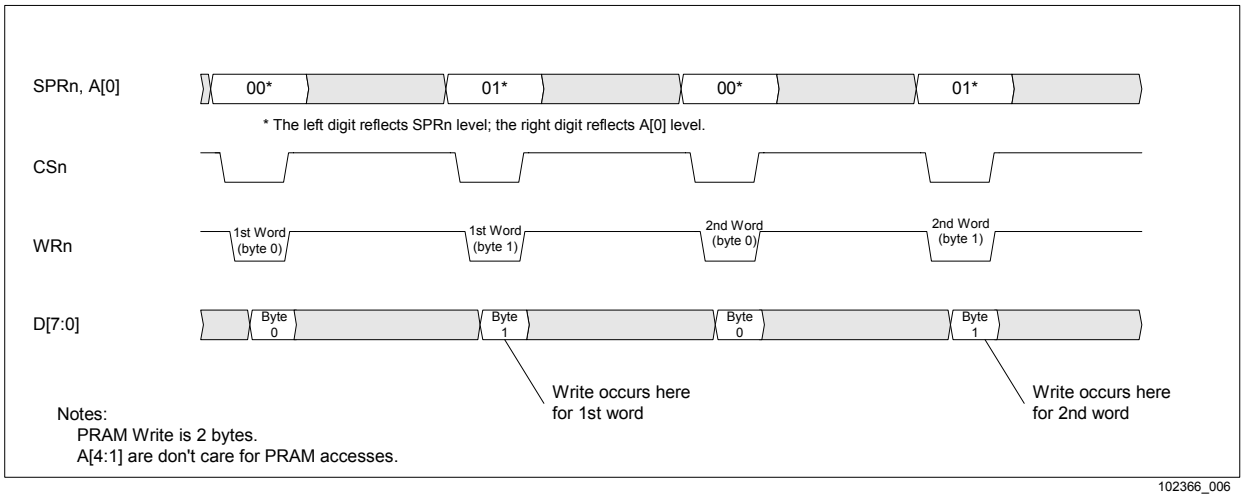


Figure 2-6. PRAM Read Timing

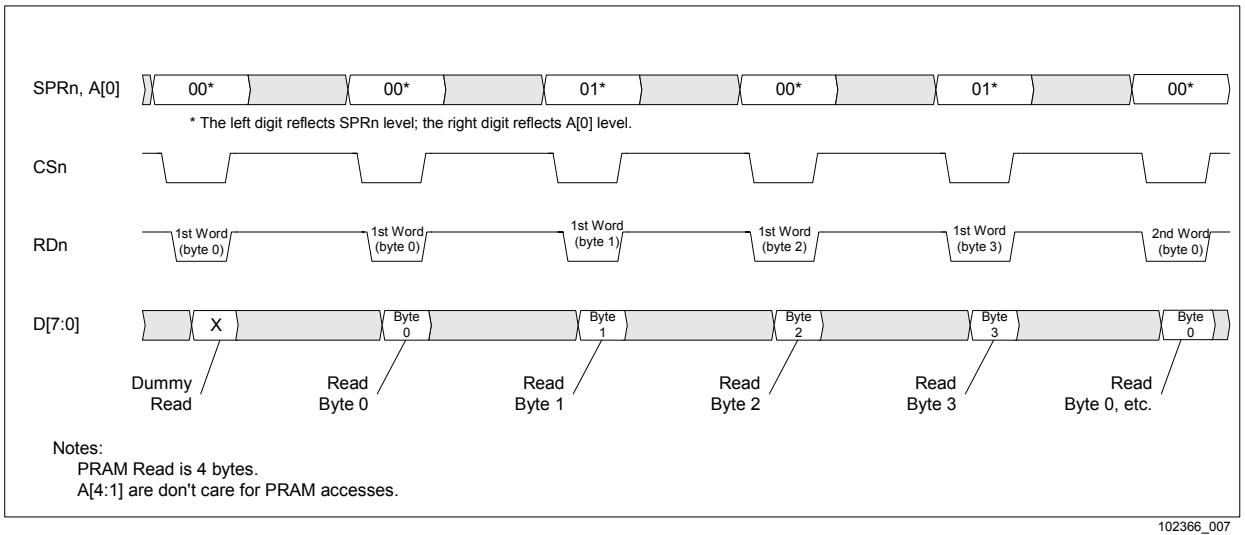


Table 2-8. Host and PRAM Interface Timing Parameters

Parameter	Symbol	Min	Max	Units
CSn Setup Time	t_{CWD}/t_{CRD}	0	—	ns
Address Setup Time	t_{ARD}	0	—	ns
CSn Hold Time	t_{WCD} / t_{RCD}	0	—	ns
Address Hold Time	t_{WAH} / t_{RAH}	0	—	ns
Read Pulse Width	t_{RW}	70	—	ns
Read Data Delay	t_{RDD}	—	70	ns
Read Data Hold Time	t_{RDH}	3	—	ns
Time between Reads (falling edge to falling edge)	t_{RD}	140	—	ns
Write Data Setup Time	t_{WDS}	5	—	ns
Write Data Hold Time	t_{WDH}	2	—	ns
Write Strobe Width	t_{WW}	30	—	ns
Time between Writes	t_{WD}	125	—	ns

2.4 Eye Pattern Waveforms and Circuit

Eye pattern waveforms are illustrated in Figure 2-7.

An eye pattern interface circuit is shown in Figure 2-8.

Figure 2-7. Eye Pattern Timing

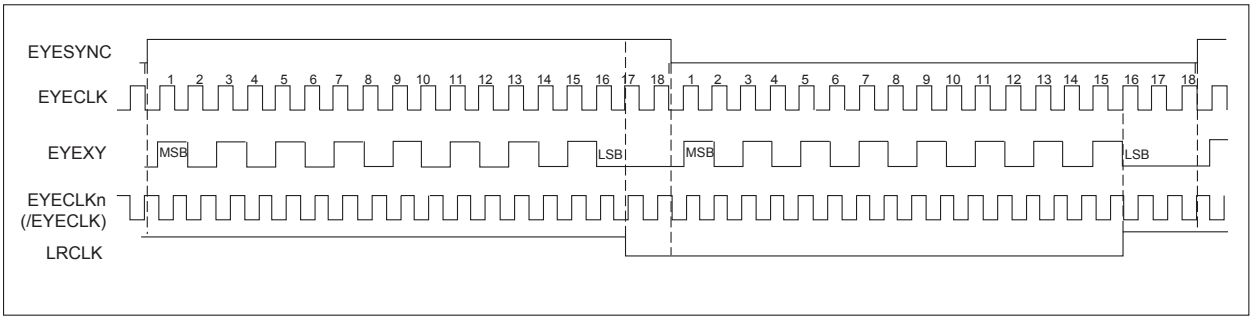
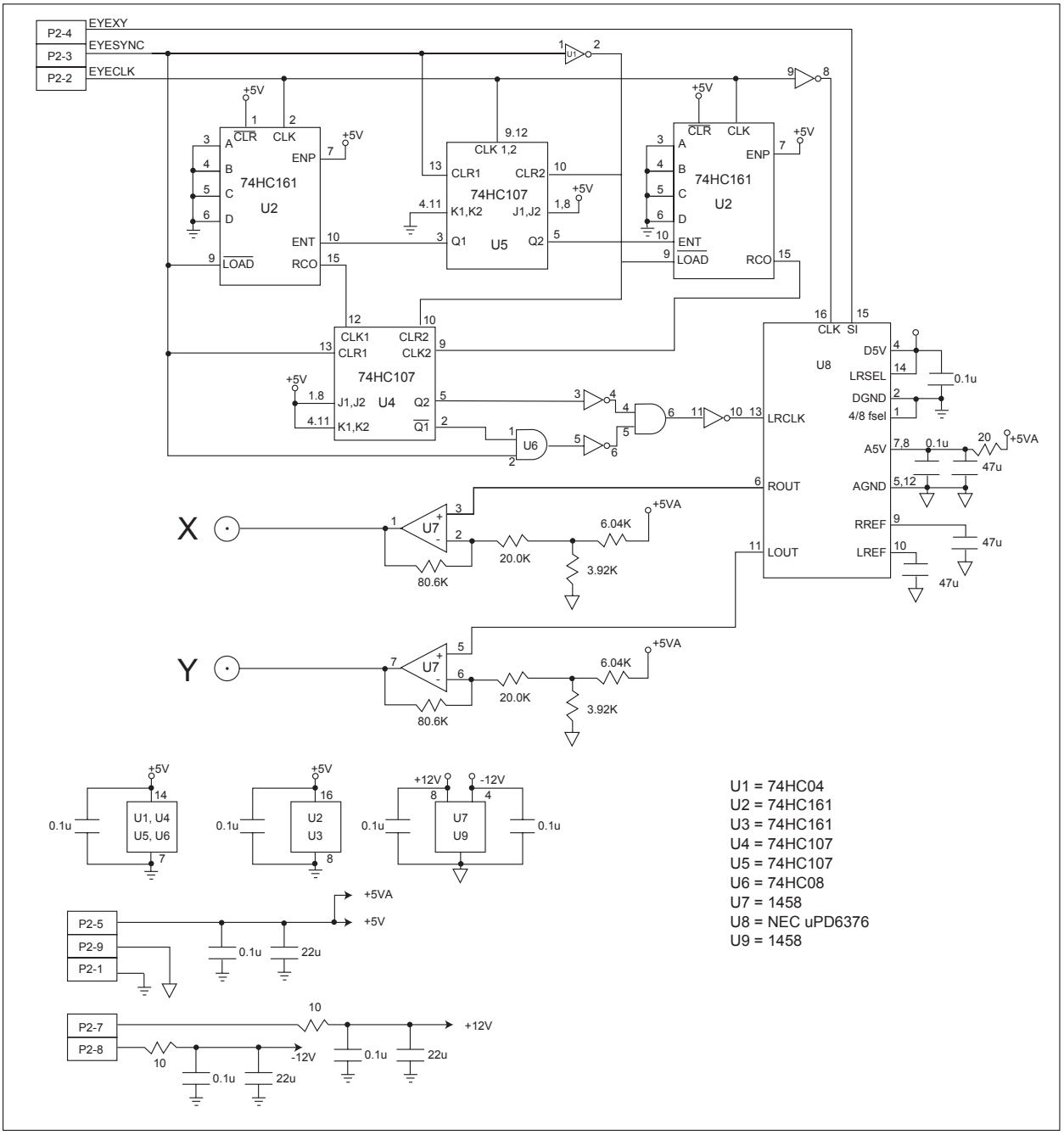


Figure 2-8. Eye Pattern Circuit



102366_008b

3. Software Interface

Modem functions are implemented in firmware executing in the DFX209/214 modem's digital signal processor (DSP).

The DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory in the DSP contains 32 8-bit registers, labeled register 00 through 1F (Table 3-1). Each register can be read from, or written to, by both the host and the DSP.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through the DSP interface memory. The host monitors modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

Writing parameter values to DSP RAM and reading parameter values from DSP RAM is described in Section 4.

3.1 Interface Memory Map

A memory map of the 32 addressable registers in the modem is shown in Table 3-1. These 8-bit registers may be read or written to during any host read or write cycle. To operate on a single bit or a group of bits in a register, the host must read a register and then mask out unwanted data. When writing a single bit or group of bits to a register, the host must perform a read-modify-write operation. The entire register (8-bits) must be read, the necessary bits must be set or reset without altering the other register bits, then the byte (8-bits) containing both the unaltered and modified bits must be written back into the interface memory.

3.1.1 Conventions

The following conventions are used throughout this document:

The individual bits in the interface memory are referred to using the format $Z:Q. The register number is specified by Z (00 through 1F) and the bit number by Q (7 through 0, 0=LSB).

For example. the register and bit for PIE is shown as $1F:4 (See Table 3-1).

Multiple bit fields are shown as Z:MSB-LSB (See Table 3-2)

DBUFF = 10:7-0

Addresses are shown as $xxx. A value used by an address is shown as xxxh.

Functions are shown as Function 4:1.

Where: 4 = Section 4

1 = First function in the section.

Functions for the remaining sections are described in the same manner.

Table 3-1. Interface Memory Map

Register Function	Reg. Addr.	Bit 7	6	5	4	3	2	1	0	Default
Interrupt Handling	1F	PIA	—	—	PIE	PIREQ	—	—	SETUP	-xx0-xx0
	1E	B2IA	B1IA	B2I1E	—	B2A	B1I1E	—	B1A	--00-00-
High Speed Control & Status	1D	SHPR*	ASPEED*	PR*	PRDET*	—	—	—	—	0000xxxx
DTMF Status/RCID Status	1C	EDET	DTDET/ RCIDIllegal	OTS/ ANIDET	DTMFD/ ANIDROP	DTMF/RCIDW				--------
General Purpose Outputs	1B	EYEXY/ XCLK	—	—	—	—	GPO2	GPO1	GPO0	00000001
Ring Detector Control/ RCID Control	1A	—	—	—	—	—	RCID3rd	RCIDDIS	RNGDIS	00000000
Reserved	19	—	—	—	—	—	—	—	—	x00--000
V.23 Control	18	—	—	—	—	—	—	TDBE	—	xxxxxx1x
Ring/Tone Status	17	EDETC	DTDETC/ RCIDIllegalC	OTSC/ ANIDETC	DTMFDC/ ANIDROPC	—	RI	FRx	—	--------
General Purpose Inputs	16	—	—	—	—	—	GPI2	GPI1	GPI0	--------
V.23 and HDLC Control	15	—	—	AEOF	—	CEQ	ANS	—	V23HDX	00000000
V.23 Control	14	TXSQ	BRKS	PARSL		PEN	STB	WDSZ		00000000
Reserved	13	—								--------
Reserved	12	—								--------
Reserved	11	—								--------
Data	10	DATA BUFFER (DBUFF)								--------
High Speed Status	0F	FED		—	—	—	—	CTSP	CDET	--xxxx--
	0E	FSKFLS	—	—	—	—	—	—	—	-xxxxxxx
	0D	RX	PNDET	—	—	—	HPFEN	—	—	--xxx0xx
	0C	—	—	DATA	SCR1	PN	P2	P1	—	xx-----x
Programmable Interrupt Control	0B	ITBMSK								00000000
	0A	TRIG		ANDOR	ITADRS					00000000
High Speed Control, V.23, and HDLC Control & Status	09	OVRUN/ OE	EQSV	EQFZ	ZEROC	ABIDL	EOF BRKD	CRC/ FE	FLAG/ PE	-000----
Tone Detect, V.23, & High Speed Control & Status	08	FR3	FR2	FR1	12TH	PNSUC/ CASD/UE	FSK7E	DCABLE	PDEQZ	0000-000
Mode Control**	07	RTSP	TDIS	—	SHTR	EPT	SQEXT	—	HDLC	00001000
	06	CONF								00010100
RAM Access Control and Programmable Interrupt Control	05	ACC	AREX	—	—	IO	BR	WRT	CR	10000101
RAM Access Address/Data	04	RAM ADDRESS (ADD)								00010111
	03	X RAM DATA MSB (XDAM)								--------
	02	X RAM DATA LSB (XDAL)								--------
	01	Y RAM DATA MSB (YDAM)								--------
	00	Y RAM DATA LSB (YDAL)								--------

Notes:

* DFX214 only.

** A changed value in these registers (except RTSP and TDIS) require setting SETUP to become active.

— This symbol in the “Bit” columns indicates that the bit is reserved for modem use only (do not alter X value in “Default Value” column).

- This symbol in the “Default Value” column indicates that the value is determined by operating conditions.

3.1.2 Interface Memory Bit Definitions

The interface memory bits are defined in Table 3-2.

Table 3-2. Interface Memory Bit Definitions

Mnemonic	Location	Default	Name/Description
12TH	08:4	0	**Select 12th Order.** When control bit 12TH is a 1, the tone detectors operate as one 12th order filter (uses FR3).When 12TH is a 0, the tone detectors operate as three parallel independent 4th order filters (FR1, FR2, FR3).The 12TH bit is valid in all reception modes.
ABIDL	09:3	–	**Abort/Idle.** In HDLC mode, when the modem is configured as a transmitter and control/status bit ABIDL is a 1, the modem will finish sending the current DBUFF byte. The modem will then send continuous ones if ZEROC is a 0, or continuous zeros if ZEROC is a 1. When ABIDL is a 0, the modem will not send continuous ones or zeros. If ABIDL is reset one DCLK cycle after being set, the modem will transmit eight continuous ones if ZEROC is a 0, or eight continuous zeros if ZEROC is a 1. ABIDL is also set by the modem when the underrun condition occurs (bit OVRUN is a 1) and the modem will send at least eight continuous ones (if ZEROC is a 0) or eight continuous zeros (if ZEROC is a 1).To stop continuous ones or zeros transmission, ABIDL must be reset by the host. In HDLC mode, when the modem is configured as a receiver and status bit ABIDL is a 1, the modem has received a minimum of seven consecutive ones. To recognize further occurrences of this abort condition, ABIDL must be reset by the host.
ACC	05:7	1	**RAM Access.** When control bit ACC is a 1, the modem accesses the RAM associated with the address in ADD, and the AREX and CR bits. WRT determines if a read or write is performed.
ADD	04:7-0	17	**RAM Address.** ADD, in conjunction with AREX, contains the RAM address used to access the modem's X and Y Data RAM (CR = 0) or X and Y Coefficient RAM (CR = 1) via the X RAM Data least significant byte (LSB) and most significant byte (MSB) words ($02:7-0 and $03:7-0, respectively) and the Y RAM Data LSB and MSB words ($00:7-0 and $01:7-0, respectively).
AEOF	15:5	0	**Automatic End of Frame.** When the modem is configured as an HDLC transmitter and AEOF control bit is a 1, the modem interprets an underrun condition as an end of frame and outputs the FCS and at least one ending flag. (HDLC mode.)
ANDOR	0A:5	0	**AND/OR Bit Mask Function.** When control bit ANDOR is a 1 and the programmable interrupt is enabled (PIE bit = 1), the modem will assert IRQn if all the bits in the register specified by ITADRS and masked by ITBMSK trigger the interrupt and control bit PIREQ has been previously reset by the host. When ANDOR is a 0 and the programmable interrupt is enabled, the modem will assert IRQn if any one of the bits in the register specified by ITADRS and masked by ITBMSK trigger the interrupt and control bit PIREQ has been previously reset by the host.
ANIDET	1C:5	0	**Russian Caller ID Detected.** When configured as RCID detector, the modem sets status bit ANIDET when a valid RCID digit is detected. The modem resets ANIDET when the RCID digit is no longer detected.
ANIDETC	17:5	0	**Russian Caller ID Detected Copy.** Copy of ANIDET bit for programmable interrupt control (RCID detector).
ANIDROP	1C:4	0	**Russian Caller ID Silence Detected.** When configured as RCID detector, the modem will set status bit ANIDROP when silence is detected. The silence interval is host programmable. The host resets ANIDROP.
ANIDROPC	17:4	0	**Russian Caller ID Silence Detected Copy.** Copy of ANIDROPC bit for programmable interrupt control (RCID detector).
ANS	15:2	0	**Answer.** When configuration bit ANS is set, the modem is in answer mode; when reset, the modem is in originate mode. If the modem is in Answer Mode (ANS= 1), then the transmit data rate is 1200 bps, and the receive data rate is 75 bps. If the modem is in Originate mode, the transmit data rate is normally 75 bps, and the receive data rate is 1200 bps. (V.23). When V.23 Half Duplex mode is selected (V23HDX = 1), ANS should be set to 0 to configure 1200 bps transmit and receive data rates. Since this is a configuration bit, the SETUP bit ($1F:0) must be set after any change in the ANS bit.
AREX	05:6	0	**RAM Access Code Extension Select.** When control bit AREX is a 1, the upper part (80h-FFh) of the RAM is selected. When AREX is a 0, the lower part (00-7Fh) is selected.

Table 3-2. Interface Memory Bit Definitions (Continued)

Mnemonic	Location	Default	Name/Description
ASPEED	1D:6	0	**Auto Speed Change Enable.** When control bit ASPEED is a 0, the modem transmitter sends the default V.17 rate sequence. The modem receiver stores the rate sequence in RAM. (V.17 modes.) **ASPEED** / **Data Rate** / **Rate Sequence Pattern** 0 / V.17, all rates / 0111h 1 / 14400 bps / 0171h 1 / 12000 bps / 01B1h 1 / 9600 bps / 01F1h 1 / 7200 bps / 0331h When set to a 1, the modem transmitter sends a different rate sequence depending on the selected TCM configuration. When receiving in a TCM configuration, the modem reconfigures to the received rate sequence. The new configuration is reflected in the receiver CONF register.
B1A	1E:0	–	**Buffer 1 Available.** When set to a 1, status bit B1A signifies that the modem has either written diagnostic data to, or read diagnostic data from, the Y RAM DATA LSB (YDAL) register ($00:7-0). This condition can also cause IRQn to be asserted. The host writing to or reading from register 00 resets the B1A and B1IA bits to 0. (See B1I1E, B1I2E, and B1IA.)
B1I1E	1E:2	0	**Buffer 1 Interrupt 1 Enable.** When control bit B1I1E is a 1, IRQn is enabled for Buffer 1, the modem will assert IRQn and set B1IA to a 1 when B1A is set to 1 by the modem. When B1I1E is a 0, B1A has no effect on IRQn and B1IA. (See B1A and B1IA.)
B1IA	1E:6	–	**Buffer 1 Interrupt Active.** When Buffer 1 interrupt is enabled (B1I1E is a 1) and B1A is set to a 1 by the modem, the modem asserts IRQn and sets status bit B1IA to a 1 to indicate that B1A caused the interrupt. The host writing to or reading from register 00 resets B1IA to a 0. (See B1I1E and B1A.)
B2A	1E:3	–	**Buffer 2 Available.** When set to a 1, status bit B2A signifies that it has read register $10:7-0 (DBUFF) when transmitting (buffer becomes empty), or it has written register $10:7-0 (DBUFF) when receiving (buffer becomes full). The modem setting B2A can also cause IRQn to be asserted. The host writing to or reading from register 10h resets the B2A and B2IA bits to 0. (See B2I1E and B2IA.)
B2I1E	1E:5	0	**Buffer 2 Interrupt 1 Enable.** When control bit B2I1E is a 1, IRQn is enabled for Buffer 2, the modem will assert IRQn and set B2IA to a 1 when B2A is set to a 1 by the modem. When B2I1E is a 0, B2A has no effect on IRQn and B2IA. (See B2A and B2IA.)
B2IA	1E:7	–	**Buffer 2 Interrupt Active.** When Buffer 2 interrupt is enabled (B2I1E is a 1) and B2A is set to a 1 by the modem, the modem asserts IRQn and sets status bit B2IA to a 1 to indicate that B2A caused the interrupt. The host writing to or reading from register 10 resets B2IA to a 0. (See B2I1E and B2A.)
BR	05:2	1	**Baud Rate.** In high-speed modem modes, when control bit BR is a 1, RAM access for ADD occurs at the baud rate regardless of the state of DR. When BR is a 0, RAM access occurs at the sample rate or data rate (See DR).
BRKD	09:2	–	**Break Detect.** When set, status bit BRKD indicates that the V.23 receiver has detected a Break sequence (continuous Space). (V.23)
BRKS	14:6	0	**Break Send.** When control bit BRKS is set, the modem will send continuous Space. When BRKS is reset, the modem will transmit data from the DBUFF. (V.23)
CASD	08:3	0	**CAS Detected.** When status bit CASD is a 1, the Type II Caller ID CAS signal has been detected. When CASD is a 0 Type II Caller ID CAS signal has not been detected. The host must reset CASD after each detection.
CDET	0F:0	–	**Carrier Detected.** When status bit CDET is a 1, the receiver has finished receiving the training sequence, or has turned on due to detecting energy above threshold, and is receiving data. When CDET is a 0, the receiver is in the idle state or is in the process of training.
CEQ	15:3	0	**Receive Compromise Equalizer Enable (1200 bps only).** When control bit CEQ is set, the receiver's digital compromise equalizer is inserted into the receive path (1200 bps receive only). The compromise equalizer taps are programmable through RAM. (V.23)

Table 3-2. Interface Memory Bit Definitions (Continued)

Mnemonic	Location	Default	Name/Description
CONF	06:7-0	14	**Configuration.** The CONF control bits select one of the following configurations: **CONF (Hex.) Configuration** 31 V.17 14400 bps. (DFX214.) 32 V.17 12000 bps. (DFX214.) 34 V.17 9600 bps. (DFX214.) 38 V.17 7200 bps. (DFX214.) 14 V.29 9600 bps. 12 V.29 7200 bps. 11 V.29 4800 bps. 0A V.27 ter 4800 bps. 09 V.27 ter 2400 bps. 20 RTSP on: V.21 Ch. 2 300 bps FSK transmit. RTSP off: V.21 Ch. 2 300 bps FSK receive and tone detect. 21 RTSP on: V.21 Ch. 2 300 bps FSK transmit. RTSP off: V.21 Ch. 2 300 bps FSK receive, tone detect, and DTMF detect. 24 V.23, tone detect. 22 V.23 receive 1200 bps (Caller ID), tone detect. 80 RTSP on: Dual/single tone transmit. RTSP off: Tone detect. RCID Detect 90 CAS Detection for CID Type II **Configuration Definitions: (Continued)** **V.17.** The modem operates as specified in ITU-T Recommendation V.17. **V.29.** The modem operates as specified in ITU-T Recommendation V.29. **V.27 ter.** The modem operates as specified in ITU-T Recommendation V.27 ter. **V.23.** The modem operates as specified in ITU-T Recommendation V.23. **V.23 Receive.** The modem operates as specified in ITU-T Recommendation V.23. **V.21 Channel 2.** The modem operates as specified in ITU-T Recommendation V.21 Channel 2. **High Speed Modes.** The 2400 bps through 14400 bps modes. **DTMF Detect.** The modem detects DTMF transmissions. **Tone Transmit.** The modem transmits single or dual frequency tones in response to the RTSP bit. Tone frequencies and amplitudes are programmable in the DSP RAM. **Tone Detect.** When the Tone Detect configuration is selected and 12TH is a 1, the three 4^{th} order tone detect filters are combined into a single 12^{th} order tone detect filter (FR3). If 12TH is not set to a 1, the three tone detect filters are placed in parallel and are independent (FR1, FR2, and FR3). All tone detect filters are programmable.
CR	05:0	1	**Coefficient RAM Select.** When control bit CR is a 1, AREX and ADD address Coefficient RAM. When CR is a 0, AREX and ADD address Data RAM. This bit must be set according to the desired RAM address.
CRC	09:1	–	**Cyclic Redundancy Check Error.** In HDLC mode, when status bit CRC is a 1 and status bit EOF is a 1, the received frame is in error. When CRC is a 0 and EOF is a 1, the received frame is correct. CRC changes immediately before EOF is set to a 1. In Caller ID mode (CONF = 22h), the modem sets the CRC bit if the stop bit is detected to be a 1.
CTSP	0F:1	–	**Clear to Send Parallel**. When set to a 1, status bit CTSP indicates to the DTE that the training sequence has been completed and any data presented at DBUFF will be transmitted.
DATA	0C:5	–	**Data Mode.** When status bit DATA is a 1, the high speed transmitter/receiver is in the data mode.

Table 3-2. Interface Memory Bit Definitions (Continued)

Mnemonic	Location	Default	Name/Description
DBUFF	10:7-0	–	**Data Buffer.** The host obtains received data from the modem by reading a data byte from DBUFF; the host sends data to the modem to be transmitted by writing a data byte to DBUFF. The data is received and transmitted bit 0 first. The modem reading (taking data) or writing (sending data) to this register sets the B2A bit. The host reading (taking data) or writing (sending data) to this register resets the B2A bit. By setting B2I1E, the host can enable the assertion of IRQn upon the setting of B2A. Bit 0 of DBUFF is the first bit of the 8-bit input or output. In the V.23 configuration (CONF = $24), the host obtains received data from the modem by reading a data byte from DBUFF. The modem writing (sending data) to this register sets the B2A bit ($1E:3). The host reading (taking data) from this register resets the B2A bit ($1E:3).
DCABLE	08:1	0	**Digital Cable Equalizer Enable.** Control bit DCABLE enables (1) or disables (0) insertion of the digital cable equalizer into the receive and transmit paths.
DTDET	1C:6	–	**Dual Tone Detected.** When configured as an DTMF receiver, the modem sets status bit DTDET to a 1 when a signal is received that satisfies all DTMF criteria except on-time, off-time, and cycle-time. The encoded DTMF Output Word ($1C:3-0) value is available when DTDET is a 1. If the received signal is a valid DTMF signal, then DTDET will be set to a 1 approximately 11 ms following EDET setting to a 1. The DTDET bit is reset by the modem after DTMFD is set to a 1 or if the received signal fails to satisfy any subsequent DTMF criteria.
DTDETC	17:6	–	**Dual Tone Detected Copy.** In DTMF modes, DTDETC is a copy of the DTDET bit for programmable interrupt control.
DTMF	1C:3-0	–	**DTMF Output Word.** When configured as an DTMF receiver and a DTMF signal is present such that status bit DTDET is set by the modem, the encoded DTMF output is written to $1C:3-0. The DTMF symbol codes are: **DTMF Symbol / Encoded Output (Hex.) / DTMF Symbol / Encoded Output (Hex.)** 1 0 3 8 4 1 6 9 7 2 9 A * 3 # B 2 4 A C 5 5 B D 8 6 C E 0 7 D F
DTMFD	1C:4	–	**DTMF Signal Detected.** When configured as a DTMF receiver, the modem sets status bit DTMFD to a 1 when a DTMF signal has been detected that satisfies all specified DTMF detect criteria. The host must reset this bit after reading the DTMF Output Word ($1C:7-0), otherwise the same symbol may be missed by the host.
DTMFDC	17:4	–	**DTMF Detected Copy.** In DTMF modes, DTMFDC is a copy of the DTMFD bit for programmable interrupt control.
EDET	1C:7	–	**DTMF Early Detection.** When configured as a DTMF receiver, the modem sets status bit EDET to a 1 approximately 20 ms after the DTMF signal energy is detected to indicate that the received signal is probably a DTMF signal. This bit is reset by the modem after DTMFD is set to a 1 or if the received signal fails to satisfy any subsequent DTMF criteria.

Table 3-2. Interface Memory Bit Definitions (Continued)

Mnemonic	Location	Default	Name/Description
EDETC	17:7	–	**Early Detection Copy.** In DTMF modes, EDETC is a copy of the EDET bit for programmable interrupt control.
EOF	09:2	–	**End of Frame.** In HDLC mode, when the modem is configured as a transmitter and bit AEOF is a 0, the EOF bit is a control bit. When AEOF is a 0, to convey to the modem that it is time to send the 16-bit FCS and ending flag of an HDLC frame, the host must set the EOF bit after the modem has taken the last byte of data (resides in DBUFF) of the frame (B2A sets again). EOF will then be reset by the modem after it has recognized the setting of EOF by the host. When the modem is configured as a transmitter and bit AEOF is a 1, EOF is a status bit. In this case, the modem will interpret the underrun condition as the end of the frame, set EOF, and will output the 16-bit FCS and at least one ending flag. EOF is reset whenever a flag is transmitted. When the modem is configured as a receiver and bit AEOF is a 1, the modem has received a frame ending flag and the CRC bit is updated. EOF must be reset by the host before receiving the ending flag of a following frame.
EPT	07:3	1	**Echo Protector Tone Enable.** When control bit EPT is a 1, an unmodulated carrier is transmitted for 187.5 ms followed by 20 ms of no transmitted energy prior to the transmission of the training sequence. When EPT is a 0, neither the echo protector tone nor the 20 ms of no energy are transmitted prior to the transmission of the training sequence except in V.29 long train which transmits 20 ms of silence at the beginning of training. (See status bit P1.) The setting of the EPT bit must be followed by the setting of the SETUP bit to become active.
EQFZ	09:5	0	**Equalizer Freeze.** When control bit EQFZ is a 1, updating of the receiver's adaptive equalizer taps is inhibited.
EYEXY/ XCLK	1B:7	0	**Serial Eye Pattern X/Y Output.** When the EYEXY/XCLK bit is a 1, serial data containing two 16-bit diagnostic words (EYEX and EYEY) is output on the EYEXY/XCLK pin. When the EYEXY/XCLK bit is a 0, the XCLK (32.256 MHz) clock is output on the EYEXY/XCLK pin.
EQSV	09:6	0	**Equalizer Save.** When control bit EQSV is a 1, the adaptive equalizer taps are not zeroed when reconfiguring the modem or when entering the training state. Adaptive equalizer taps are also not updated during training. For short train only, this bit is used in conjunction with the SHTR bit.
FE	09:1	0	**Framing Error.** When set, status bit FE indicates that more than 1 in 8 characters were received without a Stop bit in asynchronous mode. When reset, no framing error is detected. (V.23)
FED	0F:7-6	–	**Fast Energy Detector.** Status bits FED indicates the level of the received signal according to the following codes: **Bit 7** / **Bit 6** / **Energy Level** 0 / 0 / No energy (idle mode) 0 / 1 / Invalid 1 / 0 / Above Turn-off Threshold 1 / 1 / Above Turn-on Threshold
FLAG	09:0	–	**FLAG Mode**. When the modem is configured as a transmitter and status bit FLAG is a 1, the modem is transmitting a flag sequence. When the modem is configured as a receiver and status bit FLAG is a 1, the modem has received a flag sequence. (HDLC mode)
FR1	08:5	–	**Frequency No. 1.** The modem sets status bit FR1 to a 1 when energy above tone detector 1's turn-on threshold is detected. The default detection range = 2100 Hz ± 25 Hz for 9600 Hz sample rate.
FR2	08:6	–	**Frequency No. 2.** The modem sets status bit FR2 to a 1 when energy above tone detector 2's turn-on threshold is detected. The default detection range = 1100 Hz ± 30 Hz for 9600 Hz sample rate.
FR3	08:7	–	**Frequency No. 3.** The modem sets status bit FR3 to a 1 when energy above tone detector 3's turn-on threshold is detected. The default detection range = 462 Hz ± 14 Hz for 9600 Hz sample rate.
FRx	17:1	–	**Frequency No. 1, 2, or 3.** Status bit FRx is set by the modem if FR1, FR2, FR3 or CASD is set. FRx is reset by the modem if FR1, FR2, FR3 and CASD are reset.
FSK7E	08:2	–	**FSK FLAG (7E) Detected.** The modem sets status bit FSK7E to a 1 when FSK flags have been detected in a high-speed receiver mode. FSK7E is valid after bit FSKFLS transitions from 1 to 0. FSK7E is not valid in V.27 ter short train modes.

Table 3-2. Interface Memory Bit Definitions (Continued)

Mnemonic	Location	Default	Name/Description
FSKFLS	0E:7	0	**FSK FLAG (7E) Search.** When status bit FSKFLS is a 1, the modem is searching for FSK flags in high speed receiver modes except V.27 ter short train. This bit is reset by the modem when the FSK flag search is completed.
GPIx	16:2-0	–	**General Purpose Inputs.** The modem sets/resets bits 2-0 in the GPIx register to represent the corresponding logic level (1 = high, 0 = low) appearing on signals GPI0 – GPI2, respectively, within 125 µs of signal transition. RINGDn is typically connected to the DAA ring detection circuitry, and bit RI in the interface memory represents a valid ring frequency if it is so connected.
GPOx	1B:2-0	001	**General Purpose Outputs.** Bits 2-0 in the GPOx register, set/reset by the host, are reflected by logic level outputs (1 = high, 0 = low) appearing on signals GPO0 – GPO2, respectively, within 125 µs of bit transition. GPO0 is internally connected to IA_RESETn.
HDLC	07:0	0	**HDLC Mode.** When control bit HDLC is a 1, the modem performs HDLC framing. When the HDLC bit is a 0, the modem does not perform HDLC framing. In data modes, changing the value of the HDLC bit requires setting the SETUP bit to become active.
HPFEN	0D:2	0	**High Pass Filter Enable.** When control bit HPFEN is a 1, the Pre-AGC high pass filter is enabled in the receive path.
IO	05:3	0	**Input/Output RAM Select**. When control bit IO is a 1, ADD addresses IO RAM. When IO is a 0, ADD addresses either coefficient or data RAM depending on the state of the CR bit. This bit must be set according to the desired RAM address.
ITADRS	0A:4-0	0	**Interrupt Address.** These 5 bits specify the register upon which the programmable interrupt and ITBMSK will take effect. The address of the byte on which the modem asserts IRQn on a bit or bits in that byte is: **Host Register (Hex.) / ITADRS (Hex.) / Host Register (Hex.) / ITADRS (Hex.)** 00 00 10 08 01 10 11 18 02 01 12 09 03 11 13 19 04 02 14 0A 05 12 15 1A 06 03 16 0B 07 13 17 1B 08 04 18 0C 09 14 19 1C 0A 05 1A 0D 0B 15 1B 1D 0C 06 1C 0E 0D 16 1D 1E 0E 07 1E 0F 0F 17 1F 1F
ITBMSK	0B:7-0	00	**Interrupt Bit Mask.** This byte performs a bit mask on the register specified in ITADRS for the programmable interrupt processing. A one in any position in ITBMSK will cause the modem to assert IRQn on the corresponding bit or bits in the register specified by ITADRS according to the ANDOR bit and the TRIG bits if PIE is set by the host and PIREQ is reset by the host.
OTS	1C:5	–	**On-Time Satisfied.** When configured as an DTMF receiver, the modem sets status bit OTS to 1 after the DTMF on-time criteria is satisfied. This bit is reset by the modem after DTMFD is set to a 1 or if the received signal fails to satisfy the DTMF off-time criteria.
OTSC	17:5	–	**On-Time Satisfied Copy.** In DTMF modes, OTSC is a copy of the OTS bit for programmable interrupt control.
OVRUN	09:7	–	**Overrun/Underrun.** In HDLC mode, when configured as a transmitter and control bit AEOF is a 0, the modem sets status bit OVRUN to a 1 if a transmit underrun condition occurs. If the host does not load in a new byte of data in DBUFF within eight bit times of loading the previous byte into DBUFF, OVRUN and ABIDL bits will be set. The modem will then automatically send eight continuous ones. The transmission of these ones will continue until the host resets ABIDL. The modem will then finish sending the current group of eight ones and will either start sending another frame (if B2A is a 0) or will transmit continuous flags. The modem will reset OVRUN every time it sets B2A. If AEOF is a 1, OVRUN is disabled. When configured as a receiver, the modem sets the OVRUN bit to a 1 if a receive overrun condition occurs. To detect the next overrun condition, the host must reset this bit.

Table 3-2. Interface Memory Bit Definitions (Continued)

Mnemonic	Location	Default	Name/Description
P1	0C:1	–	**P1 Sequence.** When the modem is configured as a high-speed transmitter, status bit P1 = 1 indicates the P1 sequence is being sent. When P1 = 0, the P1 sequence is not being sent. The P1 sequence is an echo protection tone. When the modem is configured as a receiver, the P1 bit has no meaning.
P2	0C:2	–	**P2 Sequence.** When the modem is configured as a high-speed transmitter, status bit P2 = 1 indicates the P2 sequence is being sent. When P2 = 0, the P2 sequence is not being sent. When the modem is configured as a high-speed receiver, status bit P2 = 1 indicates the search for the P2 to PN transition is occurring. When P2 = 0, the P2 to PN transition search is not occurring.
PARSL	14:5-4	00	**Parity Select.** In V.23 mode, control bits PARSL select the method by which parity is generated and checked during asynchronous parallel data mode. The options are: **Bit 5** / **Bit 4** / **Parity Selected** 0 / 0 / Mark Parity 0 / 1 / Space Parity 1 / 0 / Even Parity 1 / 1 / Odd Parity
PDEQZ	08:0	0	**Programmable Digital Equalizer.** When the host has configured the modem as a receiver or transmitter and has set control bit PDEQZ, the programmable digital equalizer is enabled. When control bit PDEQZ is a 0, the programmable digital equalizer is disabled. The programmable digital equalizer defaults to a Japanese 2 link delay equalizer.
PE	09:0	0	**Parity Error.** When set, status bit PE indicates that a character with bad parity was received. When reset, a character with good parity was received. (V.23)
PEN	14:3	0	**Parity Enable.** When control bit PEN is set, parity generation and checking is enabled. When PEN is a 0, parity generation and checking is disabled. (V.23) **Note:** Parity bit is NOT masked out in the receive buffer (DBUFF). The Parity bit is the MSB of the character contained in DBUFF. Start and Stop bit(s) are stripped from the data before it is written to DBUFF.
PIA	1F:7	–	**Programmable Interrupt Active.** When control bit PIE is enabled (PIE is a 1) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the modem asserts IRQn if PIREQ has been previously reset by the host (usually after servicing the previous interrupt). Status bit PIA is set by the modem when the above occurs. PIA is reset when the host resets PIREQ.
PIE	1F:4	0	**Programmable Interrupt Enable.** When control bit PIE is enabled (PIE is a 1) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the modem asserts IRQn if PIREQ has been previously reset by the host (usually after servicing the previous interrupt). Status bit PIA is set by the modem when the above occurs. When PIE is a 0 (interrupt disabled), ITBMSK, ITADRS, TRIG, ANDOR, and PIREQ have no effect on IRQn and PIA.
PIREQ	1F:3	–	**Programmable Interrupt Request.** When control bit PIE is enabled (PIE is a 1) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the modem asserts IRQn if control bit PIREQ has been previously reset by the host. PIREQ is set by the modem when the programmable interrupt condition is true. The host must reset PIREQ after servicing the interrupt since the modem does not reset PIREQ. If PIREQ is not reset when the interrupt condition occurs again, the modem will not assert IRQn.

Table 3-2. Interface Memory Bit Definitions (Continued)

Mnemonic	Location	Default	Name/Description
PN	0C:3	–	**PN Sequence.** When the modem is configured as a high-speed transmitter, status bit PN = 1 signals that the PN sequence is being sent. When PN = 0, the PN sequence is not being transmitted. When the modem is configured as a high-speed receiver, status bit PN = 1 indicates the PN portion of the training sequence is being received. When PN = 0, the PN portion of training is not being received.
PNDET	0D:6	–	**PN Detected.** When status bit PNDET is a 1, the receiver has detected the PN portion of the training sequence. When PNDET is a 0, PN has not been detected.
PNSUC	08:3	–	**PN Success.** When status bit PNSUC is a 1, the receiver has successfully trained at the end of the PN portion of the high speed training sequence. When PNSUC is a 0, a successful training has not occurred. PNSUC is still valid after the CDET bit is set to a 1.
PR	1D:5	–	**Rate Sequence Period.** When status bit PR is a 1 during transmit, the modem is sending the rate sequence (PR). When reset to a 0, the rate sequence (PR) is not being sent. When set to a 1 during receive, the modem is receiving the rate sequence (PR). When reset to a 0, the rate sequence (PR) is not being received. (V.17 mode.)
PRDET	1D:4	–	**Rate Sequence Detection.** When status bit PRDET is a 1, the modem receiver has detected a rate sequence pattern containing a proper synchronization bit pattern. (V.17 mode.)
RCID3rd	1A:2	0	**Russian Caller ID 3rd Tone Rejection Enable.** When configured as RCID detector, the host sets control bit RCID3rd to enable 3rd tone rejection.
RCIDDIS	1A:1	-	**Russian Caller ID Disable.** Setting control bit RCIDDIS disables Russian Caller ID detection. RCIDDIS is set/reset by host before setting SETUP.
RCIDIllegal	1C:6	0	**Russian Caller ID Illegal Tone Detected.** When configured as RCID detector, the modem will set status bit RCIDIllegal when an illegal symbol detection occurs. The modem will reset RCIDIllegal when there is no illegal symbol detection.
RCIDIllegalC	17:6	0	**Russian Caller ID Illegal Tone Detected Copy.** Copy of RCIDIllegal bit for programmable interrupt control (RCID detector).
RCIDW	1C:3-0	-	**Russian Caller ID Output Word.** When status bit ANIDET is set the modem has written the detected RCID symbol to RCIDW. The host reads RCIDW. **RCID Encoded Code** / **Encoded RCID Output (Hex)** 0 → 0 (6) 1 → 1 (7) 2 → 2 (8) 3 → 3 (9) 4 → 4 (Start) (A) 5 → 5 (Repeat) (B)
RNGDIS	1A:0	0	**Ring Detector Disable.** When control bit RNGDIS is a 0, the Ring Detector is enabled. When RNGDIS is a 1, Ring Detector is disabled. **Note:** The host may set this bit to avoid false ring detection after off-hook. The delay between activation and actual toggling of the external control line will be two sample periods.
RI	17:2	–	**Ring Indicator.** Status bit RI is set when a valid ringing signal is being detected. RI is reset when a valid ringing signal is not being detected. Ringing is selected if pulses are present on RINGDn input in the 15-68 Hz frequency range (default frequency range). The RI bit follows the ringing signal with a 1 during the ON time and a 0 during the OFF time. The minimum and maximum valid ring frequencies are host programmable in DSP RAM.
RTSP	07:7	0	**Request To Send Parallel.** The one state of control bit RTSP begins a transmit sequence. The modem will continue to transmit until RTSP is reset to a 0 and the turn-off sequence has been completed.
RX	0D:7	–	**Receive State.** In high-speed modes, the modem is in the receive state when status bit RX is a 1; the modem is in the transmit state when RX is a 0.

Table 3-2. Interface Memory Bit Definitions (Continued)

Mnemonic	Location	Default	Name/Description
SCR1	0C:4	–	**Scrambled Ones.** When the modem is configured as a high speed transmitter, status bit SCR1 = 1 indicates scrambled ones are being sent. When SCR1 = 0, scrambled ones are not being sent. When the modem is configured as a high speed receiver, status bit SCR1 = 1 indicates scrambled ones are being received. When SCR1 = 0, scrambled ones are not being received.
SETUP	1F:0	0	**Setup.** Control bit SETUP must be set to a 1 by the host after the host writes a configuration code into the CONF bits ($06:7-0) or changes any of bits 0 through 6 in register 07 ($07:6-0). This informs the modem to implement the configuration change. The modem resets the SETUP bit to a 0 when the configuration change request is recognized.
SHPR	1D:7	0	**Short Train Rate Sequence.** When control bit SHPR is a 1, the V.17 rate sequence is included in the short training sequence, which extends the training by 64 baud.
SHTR	07:4	0	**Short Train Mode.** When control bit SHTR is a 1 and the modem is configured as a high-speed receiver (see CONF), the modem will perform a short training sequence. A successful long train at the same data rate must precede its short train. **Note**: For V.17, a successful long train at any data rate must precede its short train. Setting SHTR bit must be followed by the setting of the SETUP bit. The EQSV bit must be set and the EQFZ bit may optionally be set for Short Train operation.
SQEXT	07:2	0	**Squelch Extend.** Control bit SQEXT determines the length of time the modem receiver is inhibited from receiving any signal after transmitter turn-off. The length of time is either 20 ms (SQEXT = 0) or 140 ms (SQEXT = 1). The setting of the SQEXT bit must be followed by the setting of the SETUP bit to become active.
STB	14:2	0	**Stop Bit Number.** When control bit STB is reset, one stop bit is selected; when set, two stop bits are selected. (V.23)
TDBE	18:1	1	**Transmit Data Buffer Empty**. When set, status bit TDBE signifies that the modem has read DBUFF and the host can write new data into DBUFF. This condition can also cause an IRQ to be asserted using the programmable interrupt. The host must clear the bit to transmit data. (V.23)
TDIS	07:6	0	**Training Disable.** When control bit TDIS is a 1, the modem as a receiver is prevented from recognizing a training sequence and entering the training state; as a transmitter the modem will not transmit the training sequence when the RTSP bit is activated.
TRIG	0A:7-6	0	**Interrupt Triggering.** These two bits select how the programmable interrupt is to occur if this interrupt is enabled (PIE bit = 1). The host has the option to be continuously interrupted whenever the interrupt condition is true (DC level triggered), to be interrupted only when the interrupt condition transitions from false to true (positive edge triggered), to be interrupted only when the interrupt condition transitions from true to false (negative edge triggered), or to be interrupted when the interrupt condition transitions from false to true or from true to false (edge triggered): **Bit 7 / Bit 6 / Description** 0 / 0 / DC Level Triggered 0 / 1 / Positive Edge Triggered 1 / 0 / Negative Edge Triggered 1 / 1 / Edge Triggered
TXSQ	14:7	0	**Transmitter Squelch.** When control bit TXSQ is set, the transmitter analog output is squelched (forced to zero); all other transmitter functions continue to operate as normal. When TXSQ is reset, the transmitter output functions normally. (v.23)
UE	08:3	0	**Underrun Error.** If the host does not load in a new byte of data within X bit times of the modem setting bit TDBE, an underrun condition occurs and UE is set by the modem, The actual number of bit times depends upon the number of stop bits and word size selected. (V.23) The modem will reset UE whenever it sets TDBE.

Table 3-2. Interface Memory Bit Definitions (Continued)

Mnemonic	Location	Default	Name/Description
V23HDX	15:0	0	**V.23 Half Duplex.** When control bit V23HDX is set, the modem operates in V.23/1200 half duplex. The transmitter and receiver must be set to the same V.23 configuration, 1200 bps (CONF = 24h). Carrier is under RTSP control. The RTSP-CTSP delay is adjustable in DSP RAM. ANS should also be set to zero.
WDSZ	14:1-0	--	**Data Word Size.** In V.23 mode, the WDSZ bits set the number of data bits per character as follows: **Bit 1 / Bit 0 / Data Bits/Character** 0 / 0 / 5 0 / 1 / 6 1 / 0 / 7 1 / 1 / 8
WRT	05:1	0	**RAM Write.** When control bit WRT is a 1 and ACC is a 1, the modem writes the data from the Y RAM Data registers into its internal RAM at the location addressed by AREX, ADD, and CR. (When the most significant bit of ADD is a 0, the write is performed to the X RAM location; when a 1, the write is to the Y RAM location.) When WRT is a 0 and ACC is set to a 1, the modem reads data from its internal RAM from the locations addressed by AREX, ADD, and CR, and stores the data into the X RAM Data registers and Y RAM Data registers, respectively.
XDAL	02:7-0	–	**X RAM Data LSB.** XDAL is the LSB of the 16-bit X RAM data word used in reading X RAM locations.
XDAM	03:7-0	–	**X RAM Data MSB.** XDAM is the most significant byte of the 16-bit X RAM data word used in reading X RAM locations.
YDAL	00:7-0	–	**Y RAM Data LSB.** YDAL is the LSB of the 16-bit Y RAM data word used in reading Y RAM locations, or writing X or Y RAM locations in the modem.
YDAM	01:7-0	–	**Y RAM Data MSB.** YDAM is the MSB of the 16-bit Y RAM data word used in reading Y RAM locations, or writing X or Y RAM locations in the modem.
ZEROC	09:4	0	**Zero Clamp.** In HDLC mode, when control bit ZEROC is a 1 and ABIDL is a 1, the modem will transmit continuous zeros. When ZEROC is a 0 and ABIDL is a 1, the modem will transmit continuous ones. If ABIDL is a 0, ZEROC is disabled.

3.2 Software Interface Considerations

3.2.1 Parallel Data Transfer

Register 10 in the interface memory is the Data Buffer (DBUFF). The modem and host synchronize data transfer by observing the state of the Buffer 2 Available bit, B2A ($1E:3). The flowchart in Figure 3-1 is used for data transfer.

3.2.2 Receiving Data

The modem writes to register DBUFF every eight bit times. The modem sets the B2A bit when received data is available. The host resets the B2A bit by reading DBUFF. After the modem sets B2A, the host must respond within eight bit times or else the modem will write over register DBUFF.

While receiving, if the energy drops below the turn-off threshold for a sufficient period of time, the modem writes the last bits of received data to register DBUFF before terminating the receive process.

The modem writes the first bit of received data to the least significant bit of register DBUFF, and writes the last bit of received data to the most significant bit of register DBUFF.

3.2.3 Transmitting Data

The modem reads register DBUFF every eight bit times when transmitting. The modem sets the B2A bit when requesting transmit data. The host resets the B2A bit by writing to DBUFF. After the modem sets B2A, the host must respond within eight bit times or else the modem will retransmit the data in register DBUFF.

If RTSP bit is reset, or SETUP bit is set while transmitting, the modem sends all of the data previously read from register DBUFF before terminating the transmit process.

The modem transmits the least significant bit of register DBUFF first, and transmits the most significant bit of register DBUFF last.

3.2.4 Programmable Interrupt Feature

The interface memory interrupt feature enables the host to select an interrupt to occur on any combination of bits within an interface memory register.

3.2.5 Programmable Interrupt Bits

The programmable interrupt routine runs at the sample rate in all transmit and receive modes. If the host sets the Programmable Interrupt Enable bit, PIE ($1F:4), the modem sets the Programmable Interrupt Active bit, PIA ($1F:7), and IRQn goes low when the interrupt condition is true. The Programmable Interrupt Request bit, PIREQ ($1F:3), is set by the modem whenever the interrupt condition is true. The host must reset PIREQ after servicing the interrupt.

An interrupt may occur only within a single interface memory register based upon any combination of bits. For example, the host may select register 09h and generate an

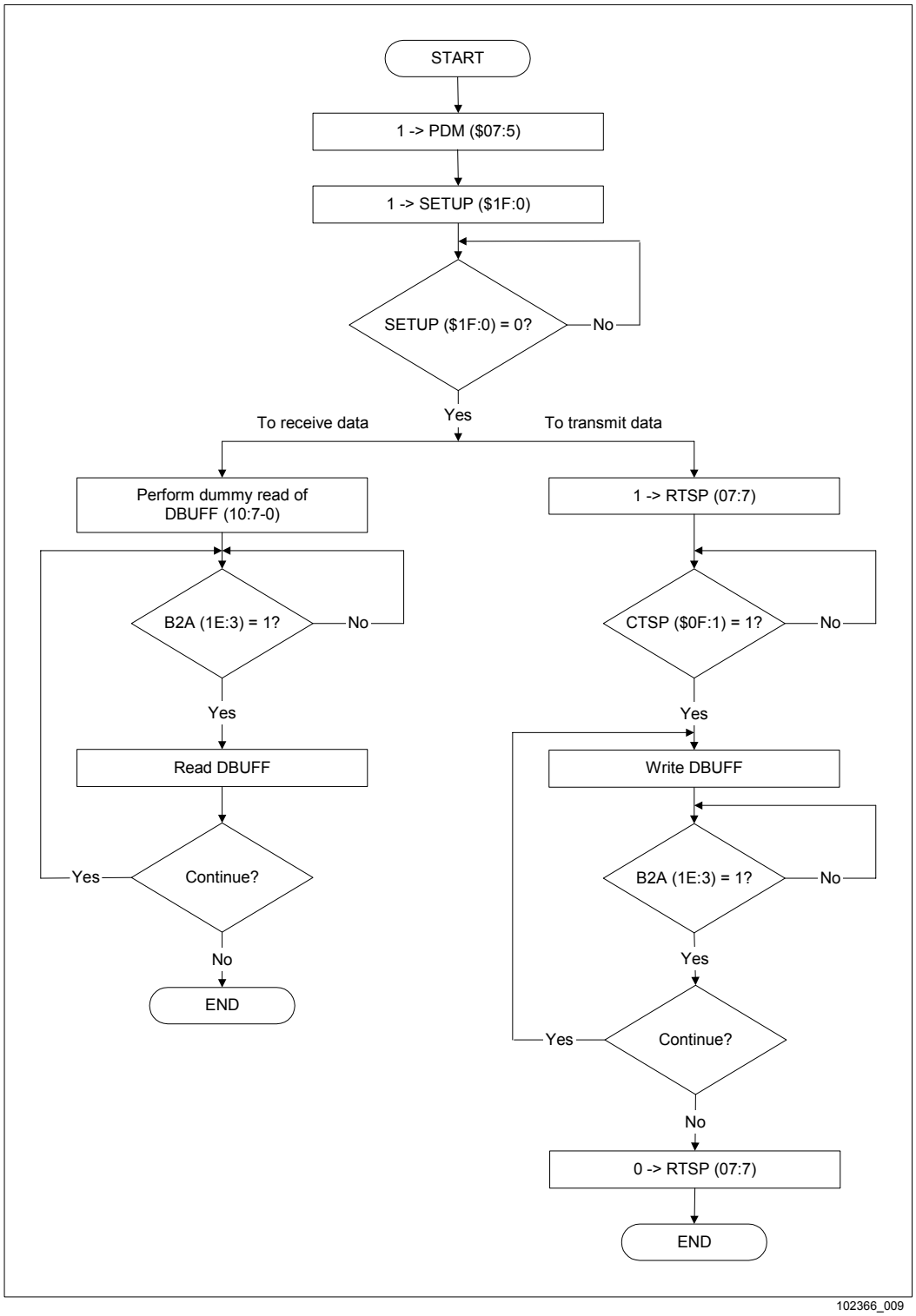
interrupt whenever bits $09:7, $09:4, and/or $09:3 are set, but may not select bits $08:7 and $09:2 to generate an interrupt. The register is selected by specifying the Interrupt Address, ITADRS ($0A:4-0). (See ITADRS)

The Interrupt Bit Mask register, ITBMSK ($0B:7-0), selects the bits to be tested in the interface memory register specified by ITADRS. For example, if ITBMSK is equal to FFh, all the bits are selected; if ITBMSK is equal to 0Fh, the four least significant bits are selected.

3.2.6 Programmable Interrupt Operating Modes

There are two operating modes with each mode having four trigger options. The ANDOR ($0A:5) bit selects the operating mode. The TRIG bits ($0A:7-6) select the triggering option.

Figure 3-1. Parallel Data Transfer Routine



3.2.7 DTMF Receiver

3.2.7.1 Mode Selection and Description

The DTMF receiver operates concurrently with the FSK receiver and the three tone detectors.

The encoded DTMF receiver output is written into the four least significant bits of register 1C.

The modem sets the DTMF Signal Detected status bit, DTMFD ($1C:4), to a 1 whenever a DTMF signal is successfully detected. The host must reset DTMFD after reading the register, otherwise, two or more successive detections of the same symbol may go unnoticed.

3.2.7.2 DTMF Reception Status Bits

Other status bits have been included in register 1C to facilitate host DTMF detection, primarily when used with the programmable interrupt. The Early Detection bit, EDET ($1C:7), may set to a 1 approximately 20 ms after signal energy is detected. Setting this bit informs the host that the received signal appears to be a DTMF signal, but the modem has not yet completed its processing.

The Dual Tone Detected bit, DTDET ($1C:6), may set to a 1 approximately 11 ms following EDET setting. DTDET is set when the received signal satisfies all DTMF criteria except on-time, off-time, and cycle-time. At this time the encoded DTMF receiver output is made available to the host in the DTMF Output Word ($1C:3-0). If DTDET is not set to a 1, then the received signal has failed one or more criteria, and consequently the modem resets EDET and resumes its search.

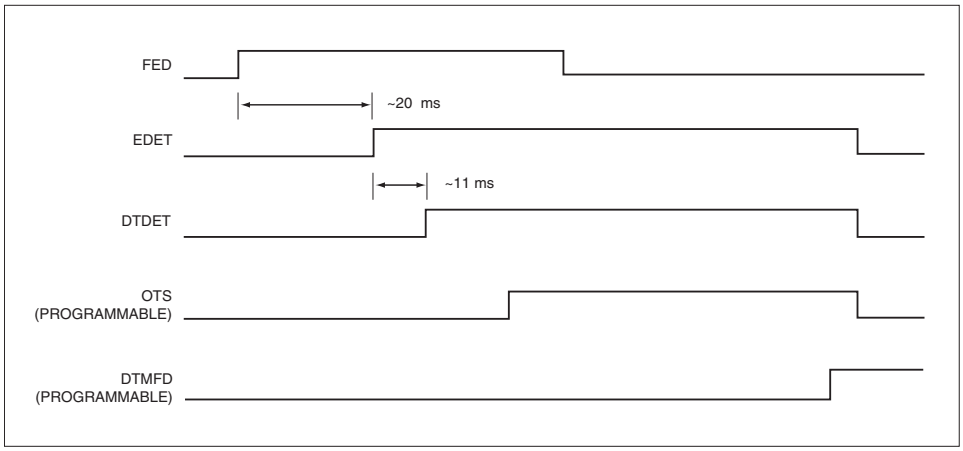
After the on-time criteria is satisfied, the modem sets the On-Time Satisfied bit, OTS ($1C:5), to a 1. If the on-time is not satisfied, the modem resets bits EDET and DTDET and resumes its search. As soon as both the off-time and cycle-time are satisfied, DTMFD is set to a 1. If these times are not satisfied, then EDET, DTDET, and OTS are reset and the receiver resumes its search. Also following DTMFD setting, EDET, DTDET, and OTS are reset. The relationship between these status bits for a valid DTMF signal is illustrated in Figure 3-2.

If, after DTDET is set to a 1, the host resets DTDET before OTS sets to a 1, then the DTMF receiver is reset to its initial state except for the programmable DTMF parameters which retain their present values (see Section 4).

If, after OTS is set to a 1, the host resets OTS before DTMFD sets to a 1, then the DTMF receiver is reset to its initial state except for the programmable DTMF parameters which retain their present values (see Section 4). See Table 11-1 for DTMF receiver performance characteristics.

***Note**: The DTMF copy bits (EDETC, DTDETC, OTSC, and DTMFDC in register 17) copy the corresponding actual DTMF status bits (EDET, DTDET, OTS, and DTMFD, respectively, in register 1C). The copy bits are located in the same register as the status bits for tone detection, Type II Caller ID detection, and ring detection status bits to facilitate programmable interrupt service. Clearing the DTMFD status bit will automatically clear the corresponding DTMFDC copy bit within one sample time.*

Figure 3-2. DTMF Receiver Status Bit Timing



3.2.8 V.21 Channel 2 FSK 7E Flag Detector

The V.21 Channel 2 FSK 7E flag detector can be used to detect the presence of the energy produced by the T.30 FSK 7E flag preamble while the modem is configured in any high speed receiver mode except for V.27 ter short train. FSKFLS and FSK7E bits indicate the status of the detection process (see Table 3-2 for bit descriptions). The detection process starts after the modem enters its receiver idle mode and a waiting period of 8 bauds has elapsed after FED turns on (Figure 3-3). The modem receiver normally enters the idle mode after any of the following events:

1. The host setting of SETUP bit.
2. After FED turns off with enough lapse time (about 30 ms in V.29) in data mode to return to the idle mode.
3. After the modem detects a significant gain hit in the data mode (CDET on). The presence of an FSK signal when noise is above turn-on threshold will generate such a hit.

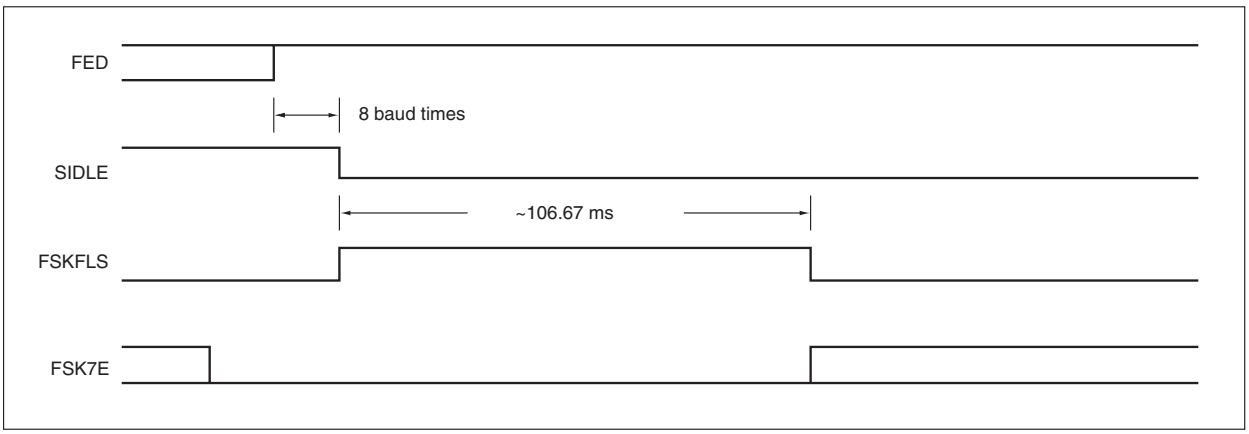
After the modem enters the idle mode, the modem will reset FSKFLS and FSK7E bits to a 0. If FED is on, then the modem will set FSKFLS to a 1 and start the detection process. After the completion of the detection process, if the FSK 7E signal is present the modem will set FSK7E bit to a 1 and reset the FSKFLS bit to a 0. The FSK7E bit will remain at this state until the modem enters the idle mode again or the host resets the bit to a 0.

The detector will not work properly if the modem is not allowed to complete the detection process, which lasts about 106.7 ms after FSKFLS goes to a 1.

In the event that the host sets the control bit TDIS to a 1 after the modem enters its idle mode, the modem will quickly enter the data mode after FED turns on and, hence, not allow enough time for the detector to complete its detection process. Therefore, the TDIS bit must be reset to a 0 to assure the proper function of the FSK 7E flag detector.

An example of the FSK 7E flag detector in a signal recognition algorithm is illustrated in Figure 8-26.

Figure 3-3. FSK 7E Flag Detector Timing



3.2.9 V.23 Mode Operation

The V.23 mode operates when CONF = 24h. DSP RAM Access 2 does not operate in this mode.

3.2.9.1 V.23 Mode Transmitter and Receiver

In both V.23 Full-duplex and Half-duplex operation, the transmitter is activated by RTSP = 1. CTSP will respond as described in Table 1-2, and data may then be sent using the DBUFF. V.23 data received by the modem will be presented to the host at DBUFF.

During V.23 communication, the transmitter squelch (TXSQ), break send (BRKS), and Receive Compromise Equalizer (CEQ) may be activated at any time. All other changes to the V.23 configuration (word size, parity, stop bit selection, parallel data mode, half duplex mode) require the host to set the SETUP bit before any action is taken by the modem.

Start, stop, data length, and parity selection is done via the modem interface memory. During transmission, the host need only provide data bits to the DBUFF register, and the modem will add the requested start, stop, and parity bits. During reception, start and stop bits are always stripped by the modem. The parity bit is NOT, in general, stripped from the data by the modem, and remains with the data as the most significant bit, for backward compatibility with previous Conexant products. In parallel mode, the modem senses overrun, underrun, framing, and parity errors.

Figure 3-4 shows how to setup various V.23 transmit and receive modes.

3.2.10 Caller ID Mode Operation

The Caller ID (V.23 Receive only) mode operates when CONF = 22h.

3.2.10.1 Control Bits

The Receive Compromise Equalizer included in V.23 mode also functions in Caller ID mode. It may be enabled at any time during Caller ID reception by setting CEQ to a 1.

The V.23 control bits ANS (Answer) and V23HDX must be set to zero in Caller ID mode. Figure 3-5 shows Caller ID setup.

Figure 3-4. V.23 Modes Setup Procedure

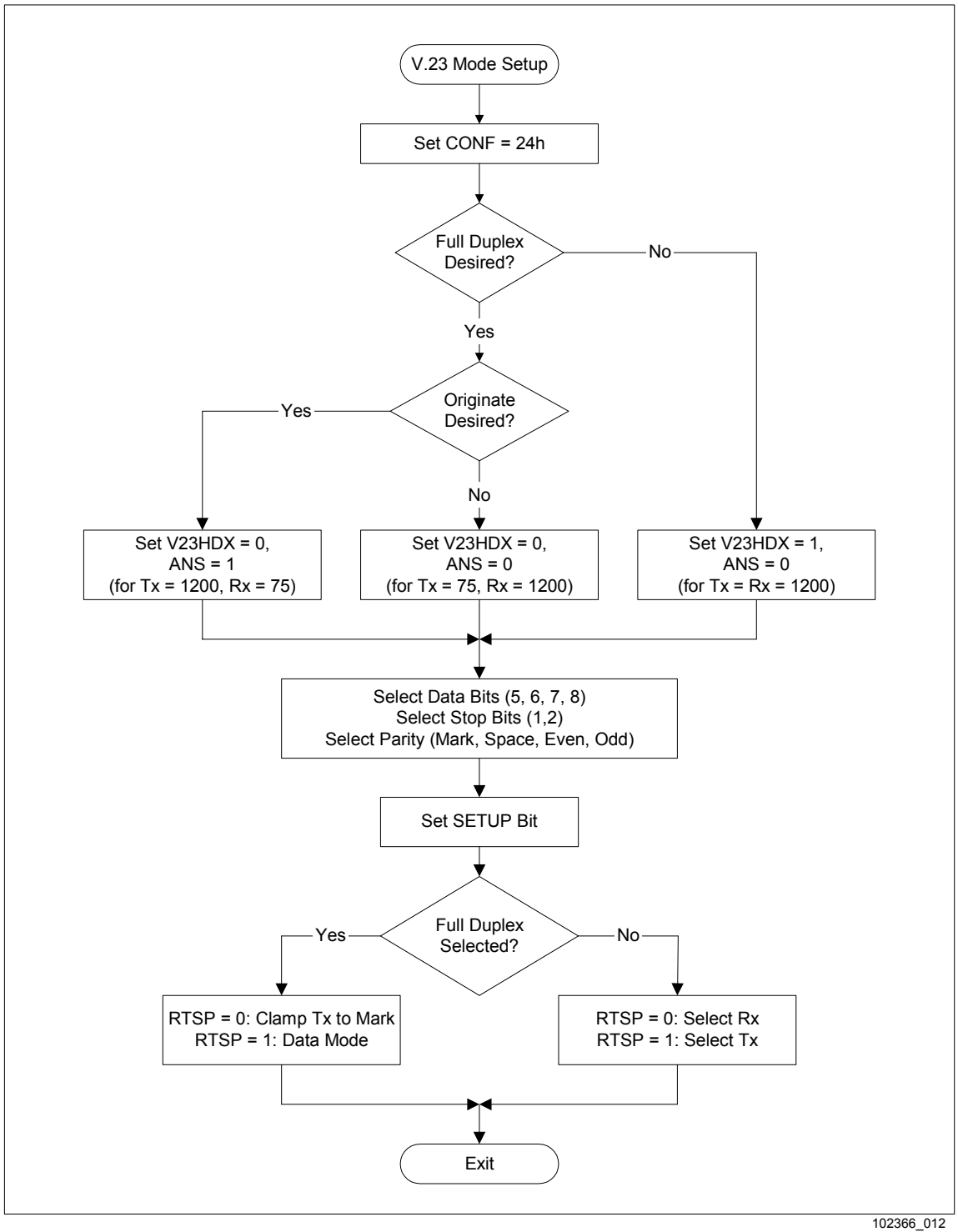
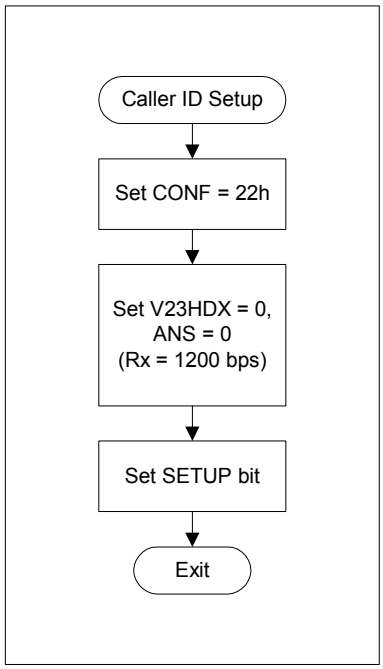


Figure 3-5. Caller ID Mode Setup Procedure



3.2.11 High Speed Timing

Several status bits in the DSP interface memory are useful to the host for monitoring various receiver conditions. These bits are significant during training and data reception/transmission. Figure 3-6 illustrates the timing relationships between these bits. Table 3-3 lists the timing values.

Table 3-3. High Speed Status Bit Timing

Mode	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11[2]	T13	Units
V.17	187.5	20.0	106.7	15.8	0[1]	20.0	4.6	4.2	10.9	13	20	40	ms
V.29 Long	187.5	20.0	53.3	160	0	20.0	6.3	4.2	4.2	5	20	34	ms
V.29 Short	187.5	20.0	41.7	25.8	0	7.5	4.6	4.2	4.2	5	20	34	ms
V.27 ter, 4800 Long	187.5	20.0	31.2	671	0	5.0	9.4	6.3	6.3	7	20	19	ms
V.27 ter, 4800 Short	187.5	20.0	8.8	36.3	0	5.0	3.1	6.3	6.3	7	20	19	ms
V.27 ter, 2400 Long	187.5	20.0	41.6	895	0	6.6	12.5	8.3	8.3	10	20	24	ms
V.27 ter, 2400 Short	187.5	20.0	11.7	48.3	0	6.6	4.2	8.3	8.3	10	20	24	ms

Notes:

1. SHPR = 0; T5 = 26.5 ms for SHPR = 1.
2. 140 ms if SQEXT = 1.
3. With HDLC bit off, resetting the RTSP bit immediately after loading the last byte (see Section 3.): T12 = 8 bit times (see Figure 3-6).
   With HDLC bit on, resetting the RTSP bit after loading the last byte (see Section 5): T12 = 32 bit times.

Figure 3-6. High Speed Mode Status Bit Timing

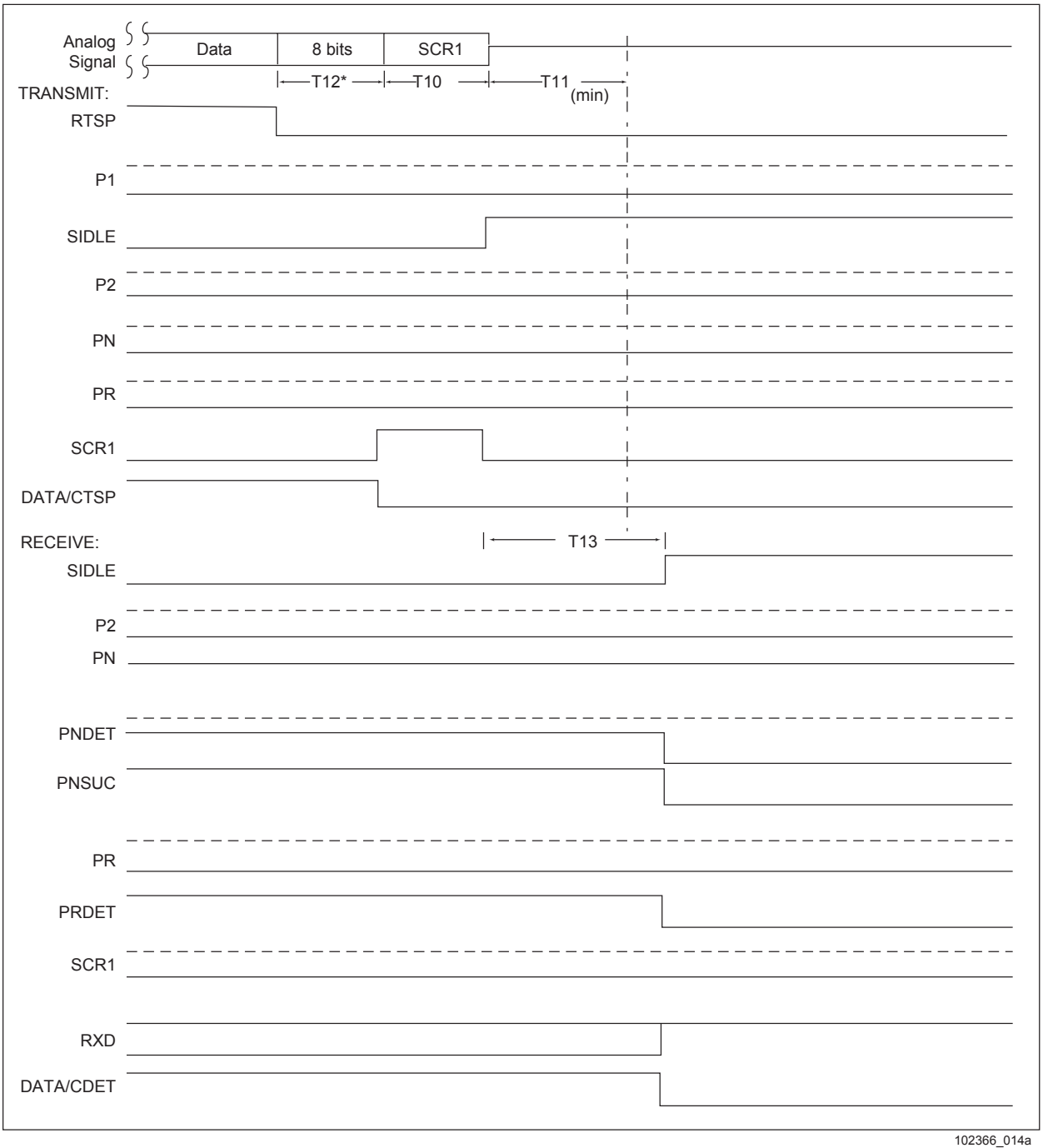
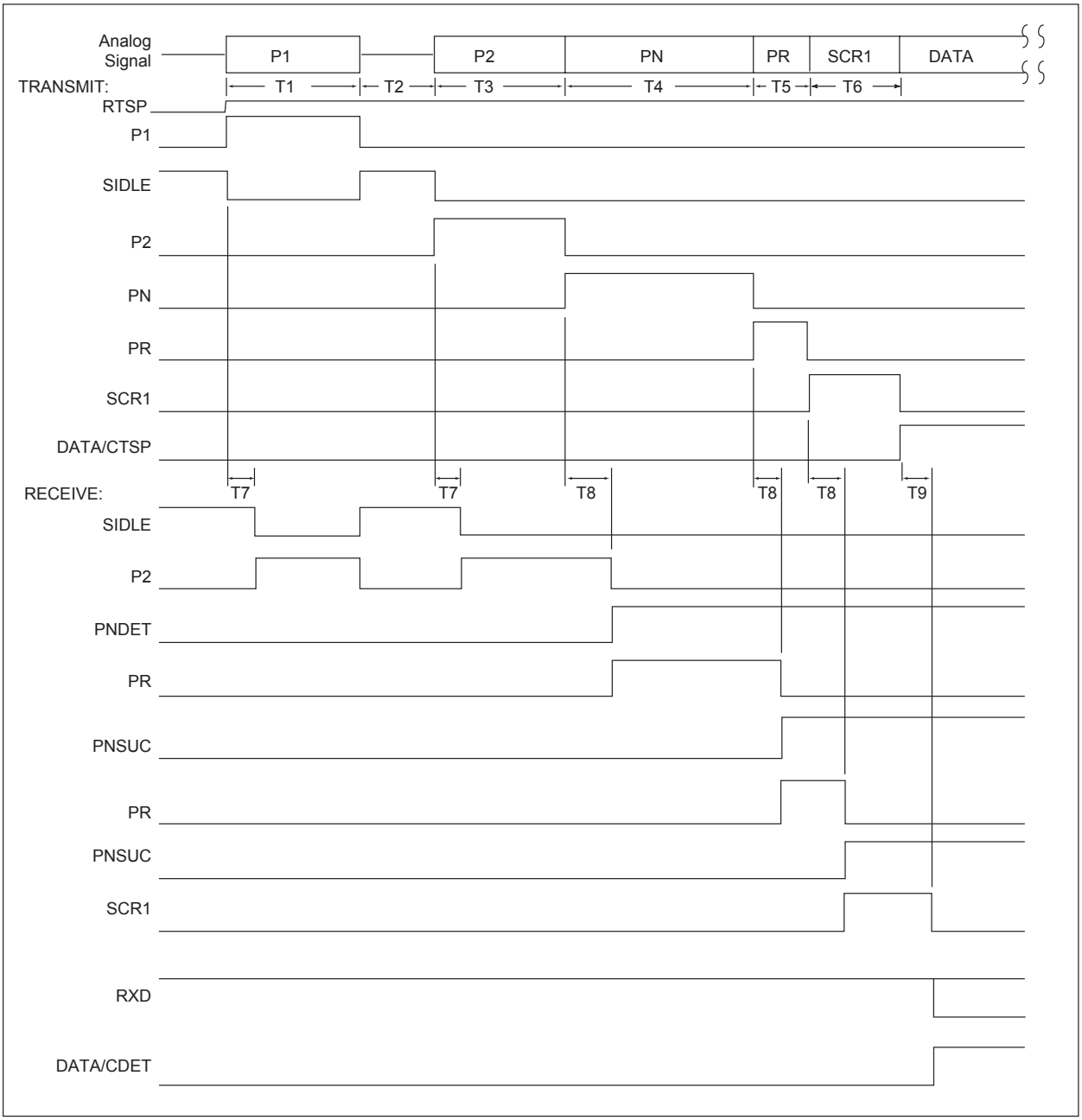


Figure 3-6. High Speed Mode Status Bit Timing (Continued)



102366_014b

3.2.12 Power-On/Reset DSP Test Mode

After Power-On Reset (POR), the modem enters into a test mode and calculates checksums on ROM, RAM and multiplier sections. The results of the checksums and ASCII values corresponding to the DSP device part number and code revision letter are written to the interface memory registers 10h through 19h approximately 20 ms after POR signal deactivates (see Table 3-4). The contents will remain in these registers for about 2.5 ms or until register 10 is read by the host.

Table 3-4. Power-On Reset Self-Test Values

Contents	Register (Hex)	Value (Hex)
Multiplier checksum upper word	19	46
Multiplier checksum lower word	18	EE
RAM checksum upper word	17	81
RAM checksum lower word	16	5C
ROM checksum upper word	15	C8
ROM checksum lower word	14	68
DSP device upper number ASCII	13	68
DSP device lower word ASCII	12	00
ASCII value for " " (space)	11	20
DSP device code revision number (example = "A")	10	41

After POR, the contents of these registers are read using the following RAM Access Codes:

Table 3-5. RAM Access Codes

Function	BR	CR	IO	AREX	ADD	Read Reg. No.
DSP Device Number	0	0	1	0	9F	0,1
DSP Device Code Revision Number	0	0	1	0	9E	0,1
ROM Checksum	0	0	1	0	9D	0,1
Multiplier Checksum	0	0	1	0	9C	0,1
RAM Checksum	0	0	1	0	9B	0,1

This page is intentionally blank.

4. DSP RAM Access

The DSP RAM contains 16-bit words. Since the DSP is optimized for performing complex arithmetic, the RAM is organized into real (X RAM) and imaginary (Y RAM) parts. The host processor reads or writes X RAM and Y RAM.

The DSP interface memory is an intermediary during data exchanges between the host and the DSP RAM. The address stored in the interface memory RAM address registers by the host determines the DSP RAM address for data access.

The 16-bit words are transferred between DSP RAM and DSP interface memory once each baud or sample time, as selected by the BR bit.

A RAM Access bit in the DSP interface memory tells the DSP to access the X RAM and/or Y RAM. The transfer is initiated by the host setting the ACC bit. The DSP tests this bit each baud or sample period.

4.1 Host Programmable Data

The DSP RAM access functions, codes, and registers are identified in Table 4-1.

4.1.1 Host DSP RAM Read And Write Procedures

The modem main RAM has four RAM banks: Data RAM Real, Data RAM Imaginary, Coefficient RAM Real, and Coefficient RAM Imaginary.

To access the main RAM, write the desired RAM access code into ADD. Bits 0 through 6 and AREX of the access code specify the RAM location and bit 7 of the access code specifies a real or imaginary RAM location. The CR bit controls whether the coefficient RAM or data RAM is accessed.

4.1.2 DSP RAM Read Procedure

The DSP RAM read procedure is a 32-bit transfer from DSP RAM to the interface memory which transfers both the X RAM and Y RAM simultaneously (Figure 4-1).

1. Before reading from the DSP, reset ACC to a 0, then read YDAL to reset B1A.
2. Reset WRT to a 0 to inform the DSP that a RAM read will occur when ACC is set to a 1.
3. For main RAM access, write the RAM address into ADD and AREX, then set CR and IO to chosen values.
4. Set ACC to a 1 to signal the DSP to perform the RAM read.
5. The DSP sets B1A after transferring the contents of RAM into the interface memory registers.
6. If B1I1E is a 1, the DSP asserts IRQn and sets B1IA to a 1 to inform the host that setting of B1A is the cause.
7. Read XDAM, XDAL, YDAM, and YDAL in this order.

Note: *Reading YDAL clears B1IA, which causes IRQn to return high if no other interrupt requests are pending.*

4.2 DSP RAM Write Procedure

The RAM write procedure is a 16-bit transfer from interface memory to DSP RAM allowing the transfer of X RAM data or Y RAM data to occur each baud data or sample time (Figure 4-1).

1. Before writing to DSP interface memory, reset ACC to a 0, then read YDAL to reset B1A.
2. For main RAM access, write the RAM address into ADD and AREX, then set CR and IO to the chosen values.
3. Set WRT to a 1 to inform the DSP that a RAM write will occur when ACC is set to a 1.
4. Write the desired data into the interface memory RAM Data registers YDAL and YDAM.
5. Set ACC to a 1 to signal the DSP to perform the RAM write.
6. The DSP sets B1A after transferring the contents of the interface memory registers into RAM.
7. If B1I1E is a 1, IRQn is also asserted and B1IA is set to a 1 when B1A is set to a 1 by the DSP.
8. Clear B1IA by writing into YDAL, which causes IRQn to return high if no other interrupt requests are pending.

Table 4-1. Modem DSP RAM Access Codes

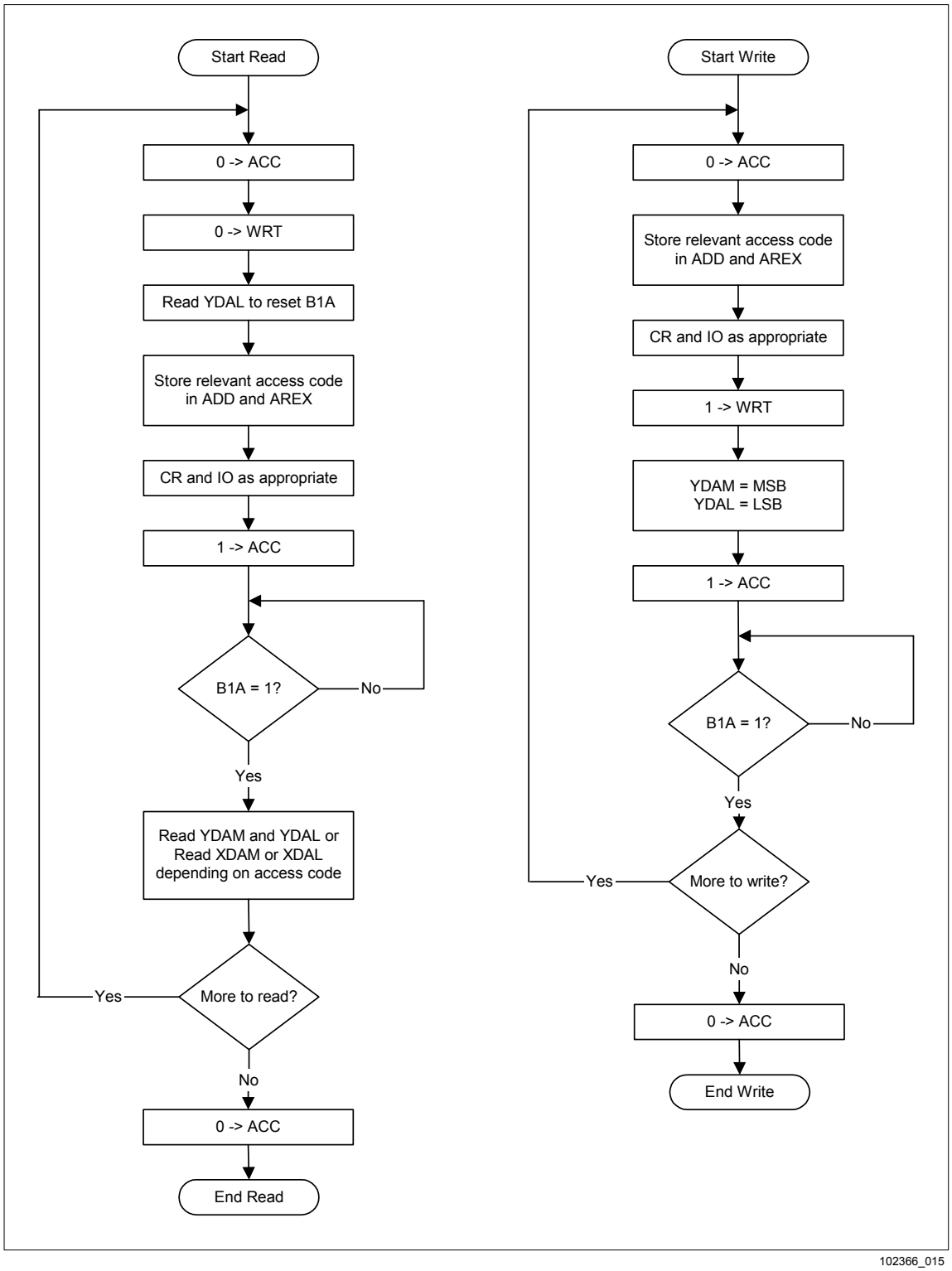
Function [1]	Description	BR	CR	IO	AREX	ADD	Read Reg. No.
4:1	Tone 1 Frequency	0	1	0	0	21	2,3
4:2	Tone 2 Frequency	0	1	0	0	22	2,3
4:3	Tone 1 Transmit Output Level	0	0	0	0	22	2,3
4:4	Tone 2 Transmit Output Level	0	0	0	0	23	2,3
4:5	Transmit Output Level/Scaling	0	0	0	0	21	2,3
4:6	Equalizer Tap Coefficients	1	1	0	1	50 - 7F	0,1,2,3
4:7	Rotated Equalizer Output, Eye Pattern	1	1	0	0	17	0,1,2,3
4:8	Decision Points, Ideal	1	0	0	0	17	0,1,2,3
4:9	Error Vector	1	1	0	0	1D	0,1,2,3
4:10	Rotation Angle	1	1	0	0	8C	0,1
4:11	Frequency Correction	1	1	0	0	18	2,3
4:12	Eye Quality Monitor (EQM), Hard Decision	1	1	0	0	0D	2,3
4:13	Eye Quality Monitor (EQM), TCM Min. Metric	1	1	0	0	B8	0,1
4:14	CDET Turn-on Threshold	0	1	0	0	37	2,3
4:15	CDET Turn-off Threshold	0	1	0	0	B7	0,1
4:16	Receiver Sensitivity, MAXG	0	1	0	0	24	2,3
4:17	Minimum On Time (DTMF)	0	1	0	0	1F	2,3
4:18	Minimum Off Time (DTMF)	0	0	0	0	1F	2,3
4:19	Minimum Cycle Time (DTMF)	0	0	0	0	9F	0,1
4:20	Maximum Dropout Time (DTMF)	0	1	0	0	9F	0,1
4:21	Maximum Speech Energy (DTMF)	0	1	0	0	1E	2,3
4:22	Frequency Deviation, Low Group (DTMF)	0	0	0	0	1D	2,3
4:23	Frequency Deviation, High Group (DTMF)	0	1	0	0	1D	2,3
4:24	Negative Twist Control (DTMF)	0	0	0	0	1E	2,3
4:25	Positive Twist Control (DTMF)	0	0	0	0	9E	0,1
4:26	Maximum Energy Hit Time (DTMF)	0	1	0	0	A3	0,1
4:27	Number of Additional Flags, NFLAG (HDLC)	0	1	0	0	85	0,1
4:28	Transmitter Rate Sequence Pattern 3	0	0	0	0	6B	2,3
4:29	Receiver Rate Sequence Pattern 3	0	1	0	0	9A	0,1
4:30	FR1 Tone Detector Coefficients	0	1	0	0	25-2A	2,3
	FR1 Tone Detector Coefficients	0	1	0	0	A5-AA	0,1
4:31	FR2 Tone Detector Coefficients	0	1	0	0	2B-30	2,3
	FR2 Tone Detector Coefficients	0	1	0	0	AB-B0	0,1
4:32	FR3 Tone Detector Coefficients	0	1	0	0	31-36	2,3
	FR3 Tone Detector Coefficients	0	1	0	0	B1-B6	0,1
4:33	Tone Detector Threshold	0	0	0	0	9D	0,1
4:34	Maximum Samples per Ring Frequency Period	0	0	0	0	53	2,3
4:35	Minimum Samples per Ring Frequency Period	0	0	0	0	52	2,3
4:36	Sleep Mode Enable	0	0	1	0	3E	0,1
4:37	V.23 Receive Compromise Equalizer Taps	0	1	0	1	18-4F	2,3
4:38	V.23 RTSP to CTSP Turn On Transition Time	0	0	1	0	12	1,2
		0	1	0	1	D3	1,2
		0	1	0	1	D2	1,2
		0	1	0	1	DC	1,2
		0	1	0	1	DE	1,2
4:39	V.23 Number of Bits (Caller ID only)	0	1	0	1	EB	0,1
4:40	Set Start Address for PRAM Read/Write	0	0	1	0	B4	0,1

Table 4-2. Modem DSP RAM Access Codes

Function [1]	Description	BR	CR	IO	AREX	ADD	Read Reg. No.
4:41	Received Signal Sample (Pre-AGC)	0	1	0	0	55	2,3
4:42	Received Signal Sample (Post-AGC)	0	0	0	0	15	2,3
4:43	AGC Gain Word	0	1	0	0	15	2,3
4:44	AGC Slew Rate Word	0	0	0	0	95	0,1

Notes:
1. Parameter numbers refer to corresponding numbers in this section.

Figure 4-1. Host Flowchart - RAM Data Read and Write



4.3 Diagnostic Data Scaling

Function 4:1 **Tone 1 Frequency**
Function 4:2 **Tone 2 Frequency**

Format: 16 bits, unsigned

Equation: N = 6.8267 x Frequency (in Hz)

Convert N to hexadecimal, then store in RAM.

Function 4:3 **Tone 1 Transmit Output Level**
Function 4:4 **Tone 2 Transmit Output Level**

Format: 16-bits, positive, twos complement

Calculate the transmit output level (power) of each tone independently by using the equation for Transmit Output Level.

Total power transmitted in tone configuration is the result of both tone 1 power and tone 2 power.

Function 4:5 **Transmit Output Level/Scaling**

Format: 16-bits, positive, twos complement

Equation: Transmit Output Level = $18426\ [10^{(Po/20)}]$ or $18426\ [10^{(P_s/20)}]$

Where: Po = output power in dBm with a 600 ohm load termination.
Ps = output power in dBm with a series 600 ohm resistor into a 600 ohm load (Ps = Po – 6).

Convert Transmit Output Level to hexadecimal and store in RAM.

Default Value: 7FFFh

Function 4:6 **Equalizer Tap Coefficients**

Access codes 50h through 7Fh represent 48 complex taps.

The equalizer tap coefficients can be useful for restoring modem operation after loss of equalization without requesting a training sequence from the transmitter. Since the equalizer tap coefficients are complex numbers, they require two write operations per tap, one for the real part and one for the imaginary part. When writing the imaginary part, the access codes 50h through 7Fh must be changed to D0h through FFh. When writing the real part, or when reading the complex number, the access codes 50h through 7Fh are appropriate.

Format: 16 bits, signed, twos complement, real

16 bits, signed, twos complement, imaginary

Function 4:7 **Rotated Equalizer Output (Eye Pattern)**
Function 4:8 **Decision Points (Ideal)**

Format: 16 bits, signed, twos complement, real

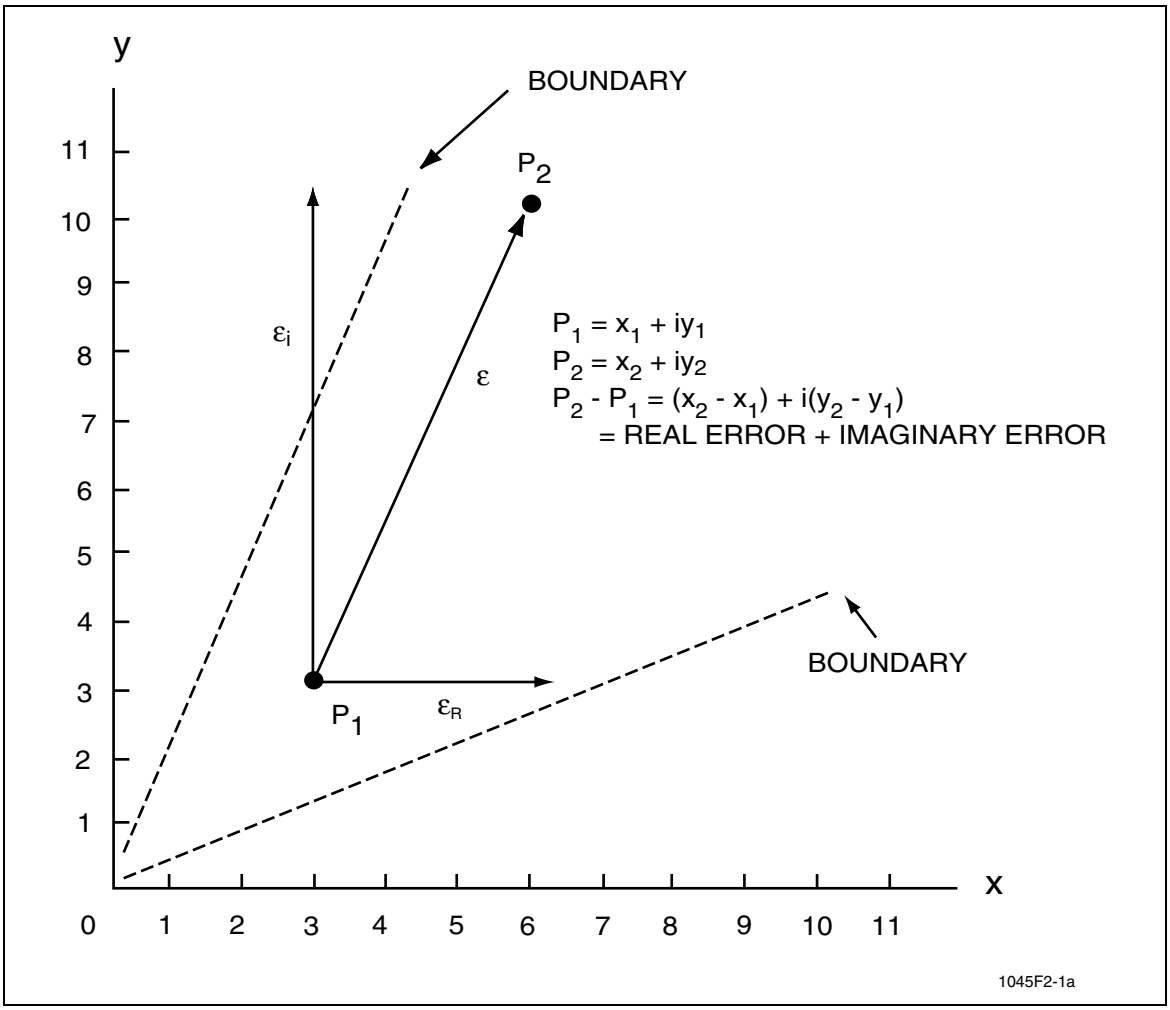
16 bits, signed, twos complement, imaginary

Function 4:9 **Error Vector**

Represents the difference between the received point (P2) and the nearest ideal point (P1).

Format: 16 bits, signed, twos complement, real

16 bits, signed, twos complement, imaginary



Error Vector Maximum Values:

Configuration	Bit Rate	Registers 3 and 2 Real Error (Re) (Hex)	Registers 1 and 0 Imaginary Error (Im) (Hex)	Magnitude $\sqrt{(Re^2 + Im^2)}$ (Hex)
V.29	9600	<0C00	<0C00	<0E66
V.29	9200	<2400	<2400	<1AD4
V.29	4800	<1C00	<1C00	<1C00
V.27 ter	4800	<1C00	<1C00	<1C00
V.27 ter	2400	<1C00	<1C00	<1C00

Function 4:10 **Rotation Angle**

Represents instantaneous correction for phase and frequency errors.

Format: 16-bits, twos complement

Equation: Rotation Angle (degrees) = [(Rotation Angle Word)h/10000h] x 180

Function 4:11 **Frequency Correction**

Represents component of rotation angle caused by frequency error.

Format: 16 bits, twos complement

Equation: Frequency Correction (Hz) = [(Freq. Correction Word)h/10000h] x Baud Rate in Hz

Range: FC00h to 0400h representing ±37.5 Hz

Function 4:12 **Eye Quality Monitor (EQM) Hard Decision**

Equals the filtered squared magnitude of the error vector. Proportionality to bit error rate is determined by the particular application. Stabilizes in approximately 700 baud times from CDET going active.

Format: 16 bits, positive, twos complement

Function 4:13 **Eye Quality Monitor (EQM) TCM Minimum Metric (DFX214 models)**

Equals the filtered squared magnitude of the path length for TCM modes. Stabilizes in approximately 1200 baud times from CDET going active.

Format: 16 bits, positive, twos complement

Function 4:14 **CDET Turn-On Threshold**
Function 4:15 **CDET Turn-Off Threshold**
Function 4:16 **Receiver Sensitivity (MAXG)**

Three parameters can be programmed by the host to control the CDET turn-on and turn-off thresholds: (1) Post-AGC Turn-on Threshold, (2) Post-AGC Turn-off Threshold, and (3) Receiver Sensitivity (MAXG) - AGC Gain Word Limit.

Format: 16 bits, positive, twos complement

Equation: CDET Turn-on Threshold
$= 2185 \times 10^{(TON + 50 - [(MAXG/64)0.098]/10)}$

CDET Turn-off Threshold
$= 2185 \times 10^{(TOFF + 50 - [(MAXG/64)0.098]/10)}$

Receiver Sensitivity (MAXG) = 655.36 [50 - Gain Limit (dB)]

Where: TON is the turn-on threshold in dBm.

TOFF is the turn-off threshold in dBm.

MAXG is programmable in RAM and defaults to 0FC0h (4032).

Function 4:17 **Minimum On-Time (DTMF)**

The on-time is defined as the minimum period of time of the DTMF signal, beginning when the signal is detected, and ending when the energy is below the turn-off threshold. The on-time parameter cannot be set below 29.6 ms (0000h). The default on-time parameter is set for 40.0 ±1 ms. The on-time will vary with signal level. To increase or decrease the on-time parameter value, convert the increase/decrease value into hex and then add/subtract that to/from the current value.

Format: 16-bits, positive, twos complement

Equation: Minimum On-Time ± [(Increase/Decrease in ms)9.6]h

Range: 0 to 7FFFh

Default Value: 007Ah

Function 4:18 **Minimum Off-Time (DTMF)**

The minimum off-time is defined as the minimum period of time of the DTMF signal beginning when the energy falls below the turn-off threshold and ending when a gain hit is detected. The off-time parameter is equal to the desired minimum off-time minus the drop out time. The default off-time is set for 40.0 ± 1 ms with a default drop out time parameter of 5.0 ms. To increase or decrease the off-time parameter value, convert the increase/decrease value into hex and then add/subtract that to/from the current value.

Format: 16-bits, positive, twos complement

Equation: Minimum Off-Time ± [(Increase/Decrease in ms)9.6]h
(drop out time equal to 5.0 ms).

Range: 0 to 7FFFh

Default Value: 013Eh

Function 4:19 **Minimum Cycle-Time (DTMF)**

The minimum cycle-time is defined as the minimum period of the DTMF signal beginning when the signal is detected and ending when the next signal begins. The cycle-time parameter is equal to the desired minimum cycle-time minus the drop out time. The default cycle-time parameter is set for 93.0 ±1 ms with a default drop out time parameter of 5.0 ms. To increase or decrease the cycle-time parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format: 16-bits, positive, twos complement

Equation: Minimum Cycle-Time ± [(Increase/Decrease in ms)9.6]h
(dropout time equal to 5.0 ms).

Range: 0 to 7FFFh

Default Value: 022Ah

Function 4:20 **Minimum Dropout-Time (DTMF)**

The minimum dropout time is defined as the maximum period of the DTMF signal beginning when the signal energy drops below the turn-off threshold and ending when the signal energy returns that is considered to be part of the on-time. The default dropout-time parameter is set to 5.0 ms.

Format: 16-bits, positive, twos complement

Equation: [(Desired Time in ms)9.6]h

Range: 0 to 7FFFh

Default Value: 0029h

Function 4:21 **Maximum Speech Energy (DTMF)**

This parameter specifies the maximum relative speech energy that may be detected and still receive DTMF signals. The speech energy is measured in the frequency region of second or third harmonics of the DTMF tones. To disable the speech energy detector, set this parameter to its full scale positive value 7FFFh. Decreasing the value of this parameter may degrade signal-to-noise ratio (SNR) performance, but may reduce false settings of status bit EDET due to speech signals. To increase or decrease the maximum speech energy parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format: 16-bits, positive, twos complement

Equation: Maximum Speech Energy ± (Increase/Decrease)h

Range: 0 to 7FFFh

Default Value: 0519h

Function 4:22 **Frequency Deviation, Low Group (DTMF)**

This parameter controls the acceptable frequency range for the low group DTMF tones. Increasing the value of this parameter increases the frequency range. The frequency range will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format: 16-bits, positive, twos complement

Equation: Frequency Deviation ±(Increase/Decrease)h

Range: 0 to 7FFFh

Default Value: 034Ah

Function 4:23 **Frequency Deviation, High Group (DTMF)**

This parameter controls the acceptable frequency range for the high group DTMF tones. Increasing the value of this parameter increases the frequency range. The frequency range will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format: 16-bits, positive, twos complement

Equation: Frequency Deviation ±(Increase/Decrease)h

Range: 0 to 7FFFh

Default Value: 0444h

Function 4:24 **Negative Twist Control (DTMF)**

This parameter controls the acceptable negative twist for the DTMF signals. Decreasing this parameter increases the acceptable negative twist level. The twist will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the default value.

Format: 16-bits, positive, twos complement

Equation: Negative Twist ±(Increase/Decrease)h

Range: 0 to 7FFFh

Default Value: 2800h

Function 4:25 **Positive Twist Control (DTMF)**

This parameter controls the acceptable positive twist for the DTMF signals. Decreasing this parameter increases the acceptable positive twist level. The twist will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the default value.

Format: 16-bits, positive, twos complement

Equation: Positive Twist ±(Increase/Decrease)h

Range: 0 to 7FFFh

Default Value: 1420h

Function 4:26 **Maximum Energy Hit Time (DTMF)**

This parameter is a counter value which represents the number of sample times (the duration) of an allowed energy impulse during the DTMF off-time measurement. A value of 0000h means no gain hits will be tolerated during the off time.

Format: 16-bits, positive, twos complement

Equation: [(Desired Time in ms)(9.6)]h

Range: 0 to 7FFFh

Default Value: 0

Function 4:27 **Number of Additional Flags (HDLC)**

This parameter controls the number of flags between frames or at the end of the final frame. See Section 5 for more information.

Format: 16-bits, positive, twos complement

Equation: Desired number of flags - 1

Default Value: 0

Function 4:28 **Transmitter Rate Sequence Pattern (DFX214 models only)**
Function 4:29 **Receiver Rate Sequence Pattern (DFX214 models only)**

The following rate sequence patterns can be sent and detected by the modem as enabled by the ASPEED bit (see ASPEED description in Table 3-2):

Encoding:

ASPEED	Data Rate	Rate Sequence Pattern (Hex)
0	V.17, all rates	0111*
1	14400 bps	0171*
1	12000 bps	01B1*
1	9600 bps	01F1*
1	7200 bps	0331*
* The most significant bit of the rate sequence pattern corresponds to bit 0 in the V.17 rate sequence pattern.		

Format: 16-bits, unsigned

Function 4:30 **FR1 Tone Detector Coefficients**
FR1 Tone Detector Coefficients

See Section 6 for scaling information.

Function 4:31 **FR2 Tone Detector Coefficients**
FR2 Tone Detector Coefficients

See Section 6 for scaling information.

Function 4:32 **FR3 Tone Detector Coefficients**
FR3 Tone Detector Coefficients

See Section 6 for scaling information.

Function 4:33 **Tone Detector Threshold**

This parameter represents the threshold value (1/8 by default) to compare with the output of the energy average in the tone detector. This parameter is used for all 3 filters.

Format: 16 bits, twos complement, positive value

Equation: 215 (1 - Threshold desired) h

Default Value: 7000h

Function 4:34 **Maximum Samples per Ring Frequency Period (RDMAXP)**

This parameter determines the maximum period on RINGDn that will be indicated on RI. The default value of 71.4 ms corresponds to the minimum ring frequency of 14 Hz. This allows proper detection of frequencies as low as 14 Hz.

Format: 16 bits, twos complement, positive value

Equation: Maximum period samples = Sampling frequency (samples/sec)/minimum ring frequency (Hz)

Convert to hex and store in RAM.

Default Value: 02B4h (71.4 ms) for 9600 Hz sample rate

Function 4:35 **Minimum Samples per Ring Frequency Period (RDMINP)**

This parameter determines the minimum period on RINGDn that will be indicated on RI. The default value of 13.9 ms corresponds to the maximum ring frequency of 72 Hz. This allows proper detection of frequencies as high as 72 Hz.

Format: 16 bits, twos complement, positive value

Equation: Minimum period samples = Sampling frequency (samples/sec)/maximum ring frequency (Hz)

Convert to hex and store in RAM.

Default Value: 0085h (13.9 ms) for 9600 Hz sample rate

Function 4:36 **Sleep Mode Enable**

Writing a 0 to this register puts the modem DSP into the Sleep Mode and the PIA into reset mode.

The modem will then go through its power-on sequence and resume normal operation with its default values in response to a hardware power-on reset.

Function 4:37 **V.23 Receive Compromise Equalizer Taps**

Access codes 18h through 4Fh represent 56 taps.

Format: 16 bits, signed, twos complement, real

Default Values: The default values of the Receive Compromise Equalizer provide 50% compensation (both amplitude and group delay) of a 1040 Tellindus line (which approximates a CCITT 1040/1025 line). Access code 4Fh is used for the first equalizer tap, and Access code 18h is used for the last equalizer tap.

Function 4:38 **V.23 RTSP to CTSP Turn On Transition Time**

These parameters control the transition time from RTSP On-to-CTSP On. The default value of this time is 10 ms.

This transition time can be controlled by following procedure:

1. Write 00h to address $12.
2. Write 00h to address $D3 and $D2.
3. Write desired value for RTSP On-to-CTSP On time to $DC and $DE (default is 64h).

   The equation of desired transition time = T * Fs

   Where: T = time in ms, Fs = 9600 Hz

Example for 10 ms transition time: 0.010 * 9600 = 96 (60h)

Write 60h to $DE and $DC for 10 ms RTSP On-to-CTSP On time.

Function 4:39 **V.23 Number of Bits (Caller ID only)**

This parameter selects the number of bits per character for Caller ID mode, including one start bit and one stop bit. Caller ID mode does not use a parity bit. Characters from 5 to 8 data bits (7 to 10 bits total) are supported. The start and stop bits will be stripped from received data before it is placed in DBUFF.

Format: 16 bits, positive, twos complement

Equation: [Desired number of bits per received character]h

Default Value: 000Ah (8 data bits, 1 start bit, 1 stop bit, no parity - standard for Caller ID)

Function 4:40 **Set Start Address for PRAM Read or Write**

Before the host reads or writes data from or to PRAM, the host must write the starting address to address $B4. The PRAM starts at address $00 and the size is 512 bytes. See Figure 2-5 and Figure 2-6 for PRAM write and read timing, respectively.

Format: 16 bits

Default Value: No default value

Function 4:41 **Received Signal Sample (Pre-AGC) = A/D Sample Word**

Format: 16 bits, signed, twos complement

Equation: V_{INT} (Volts)= [(A/D Sample Word x V_{MAX}/32768) + 2.5V

Where: V_{MAX} = 1.6V

V_{EXT} is the input to the IA

V_{INT} is the output of the IA and input to the DSP.

Function 4:42 **Received Signal Sample (Post-AGC) = A/D Sample Word**

Format: 16 bits, signed, twos complement

Equation: V_{INT} (Volts)= [(A/D Sample Word x V_{MAX}/32768) + 2.5V

VEXT = V_{INT}/LOG_{10}^{-1} [AGC Gain (dB)/20]

Where: V_{MAX} = 1.6V

V_{EXT} is the input to the IA

V_{INT} is the output of the IA and input to the DSP.

Function 4:43 **AGC Gain Word**

Format: 16-bits, unsigned

Equation: AGC Gain (dB) = 50 [1 - (AGC Gain Word)h/32768]

Function 4:44 **AGC Slew Rate Word**

Format: 16 bits, positive, twos complement

The AGC Slew Rate can be approximated by the following equation:

Equation: AGC Slew Rate = [19968/(Sample rate x AGC gain fall time constant in seconds)]h

Note: AGC gain tracks the input signal with an exponential function with respect to time, and its fall time is approximately 5 times faster than its rise time. The above equation was determined based upon a 40 dB change in input signal.

4.4 Integrated Analog Control Registers

The modem has an internal integrated analog (PIA) codec that provides gain, filtering, internal analog switching, and an internally sourced microphone bias output. The IA is controlled by three control registers and an address register located in internal RAM space which are accessed via the modem interface memory. These registers provide individual controls for the IA's inputs, outputs, gain, and switching. The registers are located in internal RAM. The LSB of each 16-bit address contents is used to control the PIA.

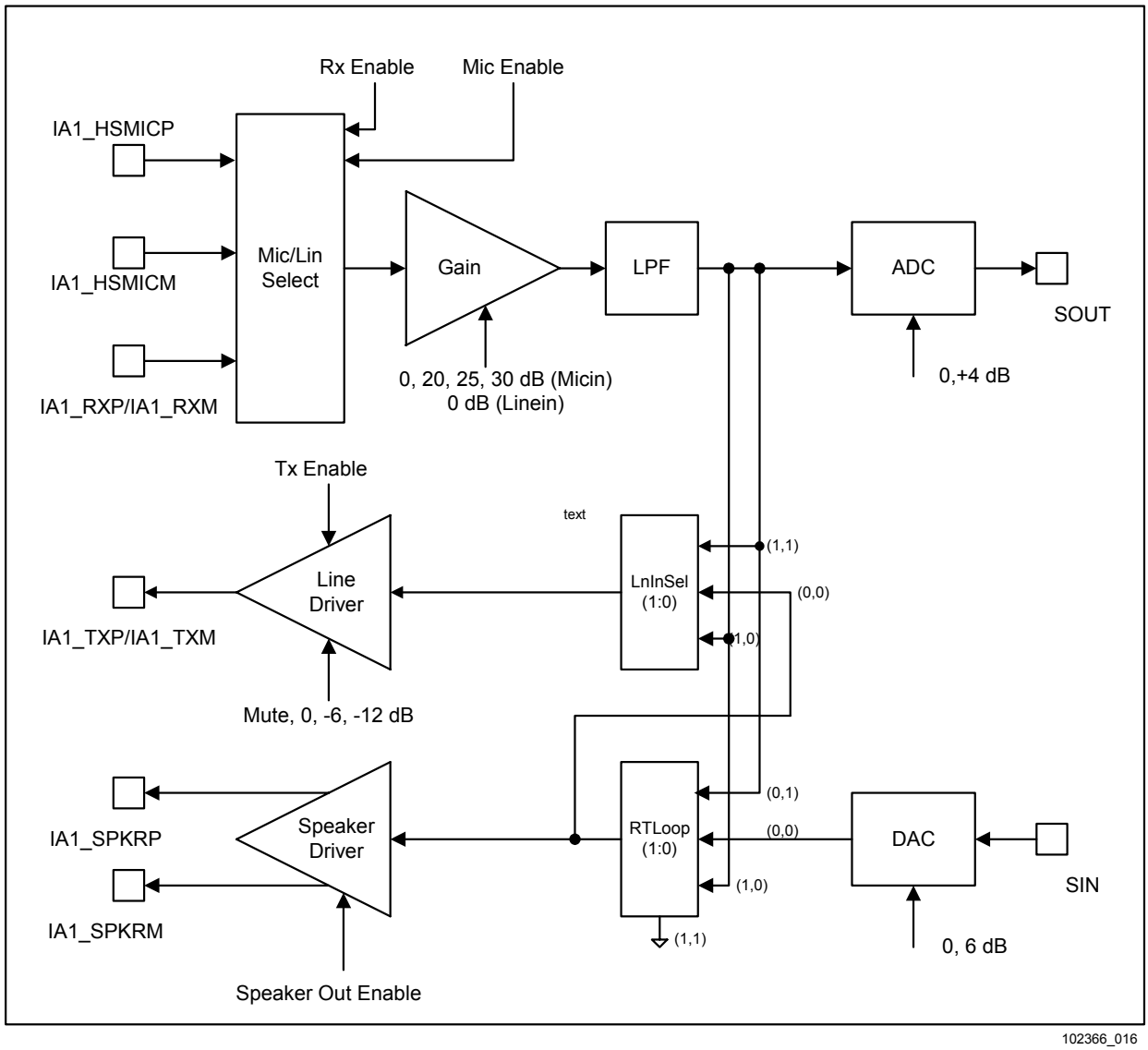
Figure 4-2 shows the PIA signal flow control.

Register	BR	CR	IO	AREX	ADD	PIA Register
IACR1	0	0	0	0	D0	0
IACR2	0	0	0	0	D4	0
IACR3	0	0	0	0	D5	0
IAADD	0	0	0	0	CE	0,1

For changes made to IACR1/IACR2/IACR3 to be effective, the host must write to IAADD with values 0002h/0006h/00007h, respectively. Configuration default values are shown below.

Configuration	Default Value (Hex)		
	IACR1	IACR2	IACR3
V.17	1D9E	0008	0000
V.29	1D9E	0008	0000
V.27ter	1D9E	0008	0000
V.21 Ch. 2	1D9E	0008	0000
V.23/Caller ID	1D9E	0008	0000
Tone Transmit/Detect	1D9E	0008	0000

Figure 4-2. PIA Signal Flow Control



102366_016

4.4.1 IACR1 IA Control Register 1

The bits in IA Control Register IACR1 control DAC gain, Mic gain, TX enable, SPKRP and SPKRM enable, ADC gain, RX enable, and MICP and MICM enable.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DAC Gain	Mic Gain		TX Enable	SPKR(P/M) Enable	ADC Gain	RX Enable	MIC(P/M) Enable

Bit 7 **DAC Gain Enable.** When control bit DAC Gain is a 1, the modem transmit output level is increased by 6 dB in the DAC. When control bit DAC Gain is a 0, the transmit output level is not increased in the DAC (0 dB).

Bits 6-5: **Mic Gain.** Control bits Mic Gain select one of four amplifications for the MIC(P/M) pins.

00 = 0 dB
01 = 20 dB
10 = 25 dB
11 = 30 dB

Bit 4 **TX Enable.** When SPKR(P/M) is a 1 and TX Enable is a 0, the IA line output driver is three-stated.

Bit 3 **SPKR(P/M) Enable.** When control bit SPKR(P/M) is a 1, the IA speaker output driver is enabled. When SPKR(P/M) is a 0 the IA speaker output driver is three-stated.

Bit 2 **ADC Gain.** When control bit ADC Gain is a 0, the ADC gain is +4 dB. When control bit ADC Gain is a 1, the ADC Gain is 0 dB.

Bit 1 **RX Enable.** When control bit RX Enable is a 1, the line differential input signal at pins IA1_RXP and IA1_RXM is routed to the ADC input. When control bit RX Enable is a 0, the line differential input signal at pins IA1_RXP and IA1_RXM is not routed to the ADC input.

Bit 0 **MIC(P/M) Enable.** When control bit MIC(P/M) Enable is a 1, the microphone differential input signal at pins IA1_HSMICM and IA1_HSMICP are routed to the ADC input. When control bit MIC(P/M) Enable is a 0, the microphone differential input signal at pins IA1_HSMICM and IA1_HSMICP are not routed to the ADC input.

Note: RX Enable and MIC(P/M) cannot be enabled at the same time.

4.4.2 IACR2 IA Control Register 2

The bits in IA Control Register IACR2 control the speaker driver output to microphone input loopback, line output driver attenuation, microphone input to speaker driver output loopback, line input to speaker driver output loopback, and microphone bias voltage.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxRxLoop	—	—	LINEOUT Attenuation		RxTxLoop		MICBIAS Select

Bit 7: **TxRxLoop.** When control bit TxRxLoop is a 1, the speaker driver transmit output signal is looped back to the microphone receiver input signal. When TxRxLoop is a 0, this transmit-receive loopback is disabled.

Bit 6: **Reserved.** Control bit 6 is reserved for modem use. Do not alter.

Bit 5: **Reserved.** Control bit 5 is reserved for modem use. Do not alter.

Bits 4-3: **LINEOUT Attenuation.** Control bits LINEOUT Attenuation select one of four attenuations for the line output driver.

00 = Analog Ground (Mute)
01 = 0 dB
10 = -6 dB
11 = -12 dB

Bits 2-1: **RxTxLoop.** Control bits RxTxLoop select and enable one of two receive-transmit loopback and speaker output driver mute.

00 = RxTx Loop disabled
01 = Microphone input looped back to speaker driver output
10 = Line input looped back to speaker driver output
11 = Speaker driver output connected to analog ground (Mute)

Note: The 01 and 10 settings have the same effect. The actual looped back signal at the speaker output pin is the enabled input signal. For example, when IA1_HSMIC(P/M) is enabled and RxTxLoop bits are set to a 01 or 10, the actual signal at IA1_SPKR(P/M) is the IA1_HSMIC(P/M) signal. When Rx is enabled and RxTxLoop bits are set to a 01 or 10, the actual signal at IA1_SPKR(P/M) is the Rx signal.

Bit 0: **MICBIAS Select.** When control bit MICBIAS Select is a 1 the voltage present at the MICBIAS output is analog ground (2.5V). When control bit MICBIAS Select is a 0 the voltage present at the MICBIAS output is 2.2V.

4.4.3 IACR3 IA Control Register 3

The bits in IA Control Register IACR3 control the line driver input selection.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
—	—	—	—	—	—	LnInSel	

Bit 7: **Reserved.** Control bit 7 is reserved for modem use. Do not alter.

Bit 6: **Reserved.** Control bit 6 is reserved for modem use. Do not alter.

Bit 5: **Reserved.** Control bit 5 is reserved for modem use. Do not alter.

Bit 4: **Reserved.** Control bit 4 is reserved for modem use. Do not alter.

Bit 2: **Reserved.** Control bit 2 is reserved for modem use. Do not alter.

Bits 1-0: **LnInSel**. Control bits LnInSel select one of three input signals for the Line Driver.

00 = DAC Filter Output
10 = LPF Output
11 = LPF Output

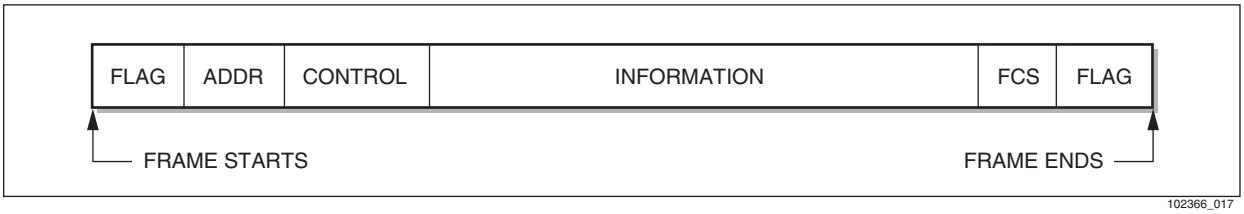
This page is intentionally blank.

5. HDLC Framing

The modem supports High Level Data Link Control (HDLC) framing. This protocol is a standard used for data communications. Synchronous Data Link Control (SDLC) is a bit-oriented protocol which is a subset of HDLC. The same format is used in both protocols although all SDLC fields must be eight-bit octets. The modem uses the SDLC eight-bit octet format.

Data and control information on a HDLC link are transmitted via frames. These frames organize the information into a format specified by an ISO standard that enables the transmitting and receiving station to synchronize with each other. This format is shown in Figure 5-1.

Figure 5-1. HDLC Frame



5.1 Frame Fields

5.1.1 Flags

All frames start and end with a flag sequence. The beginning flag and the ending flag are defined by the bit pattern 01111110 (7Eh). The ending flag for one frame can also serve as the beginning flag for the following frame. If separate ending and beginning flags are used, the final zero in the ending flag of one frame may also serve as the first zero of the beginning flag in the following frame. This process is known as “zero-sharing”. The zero-sharing bit pattern is 011111101111110.

5.1.2 Address Field

The address field informs the receiver where the information is to go (if the primary station is transmitting) or where the message originated (if a secondary station is transmitting). This field is eight bits in length for the “basic” format.

For the “extended” format, the length is N number of octets, each octet having the first bit a binary zero with the exception of the last octet that begins with a binary one.

Broadcast Address = 11111111

Null Address = 00000000

5.1.3 Control Field

The control field defines the function of the frame. It may contain a command or response. The control field might also contain send or/and receive sequence numbers. This field can be in one of the following formats:

1. Information Transfer Format
2. Supervisory Format
3. Unnumbered Format

This field is normally eight bits in length. However, certain protocols allow for an "extended" control field. For example, it is 16 bits in length for modulo 128 operation of the LAP and LAPB procedures.

5.1.4 Information Field

The modem treats the address field, the control field, and any other transmitted data, except for the flags and the Frame Check Sequence, as the information field. The information field does not have a set length; however, this field follows the SDLC protocol in being in the format of eight bit bytes.

5.1.5 Zero Insertion

Since flags mark the beginning and ending of a frame, some method must be implemented to inhibit or alter the transmission of data that appear as flags. The method used is called "zero insertion". HDLC procedures require that a zero be transmitted following any succession of five continuous ones. This includes all data in the address, control, information and Frame Check Sequence fields. Use of zero insertion denies any pattern of 01111110 to ever be transmitted between beginning and ending flags.

5.1.6 Zero Deletion

When transmitting flags, zero insertion is disabled. During reception of data, after testing for flag recognition, the receiver removes a zero that immediately follows five continuous ones. This is termed "zero deletion". A one that follows five continuous ones signifies either a frame abort (at least seven ones with no zero insertion) or a flag (01111110). The sixth one is, therefore, not removed.

5.1.7 Frame Check Sequence (FCS)

The purpose of the Frame Check Sequence (FCS) is to give a shorthand representation of the entire transmitted information field and to compare it to the identically generated shorthand representation of the received sequence. If any difference occurs, the received frame was in error and should be re-transmitted.

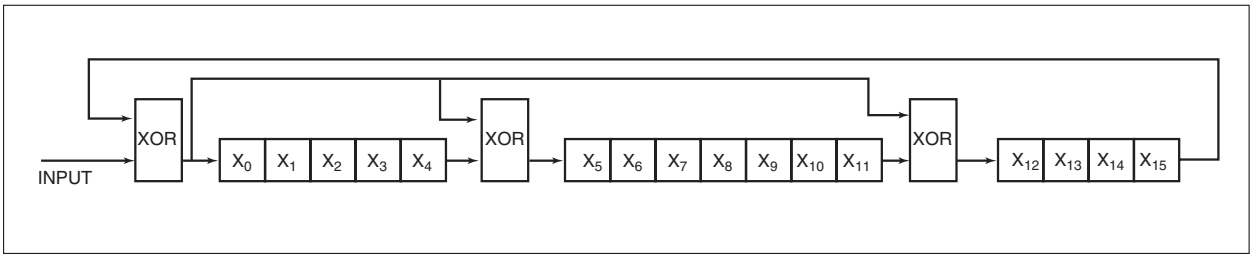
The FCS computation is done on all fields within the frame but does not include the flags. Cyclic Redundancy Check (CRC) is the method used. The polynomial is specified in ITU-T T.30 and X.25 as follows:

$$x^{16} + x^{12} + x^5 + 1$$

The polynomial is implemented as shown in Figure 5-2.

The FCS is sent as two bytes of data immediately preceding the ending flag of the frame. The FCS register is first preset to all binary ones. The register is then modified by shifting in the data (no flags) contained in the address, control, and information fields. Following the last bit of data, the ones complement of the FCS register is transmitted as the 16-bit FCS. The FCS is transmitted with the highest order bit (x15) first.

Figure 5-2. CRC Polynomial Implementation



5.1.8 Frame Abortion, Frame Idle, And Time Fill

Frame abortion prematurely finishes transmission of a frame. This occurs by sending at least seven consecutive ones with no zero insertion. This abort pattern terminates a frame immediately and does not require a FCS or an ending flag.

An abort pattern followed by a minimum of eight additional consecutive ones idles the data link. Thus, seven to fourteen ones establish the abort pattern; fifteen or more ones constitute an idle pattern.

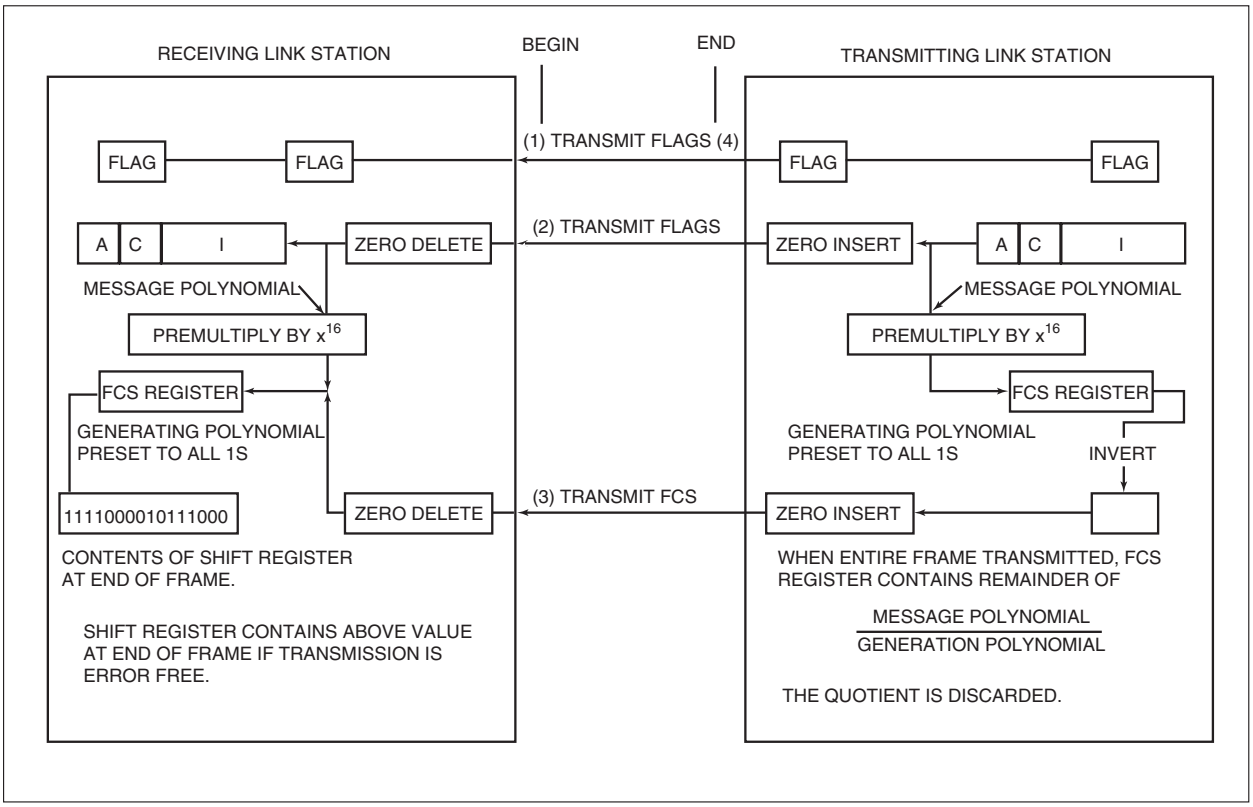
Interframe time fill is accomplished by transmitting continuous flags without zero-sharing between flags. Therefore, the transmitter must be capable of sending multiple flags to maintain the active state in the receiver if any time fill is required.

5.2 Implementation

A representation of the HDLC process is shown in Figure 5-3. The events are numbered in order of occurrence from one to four.

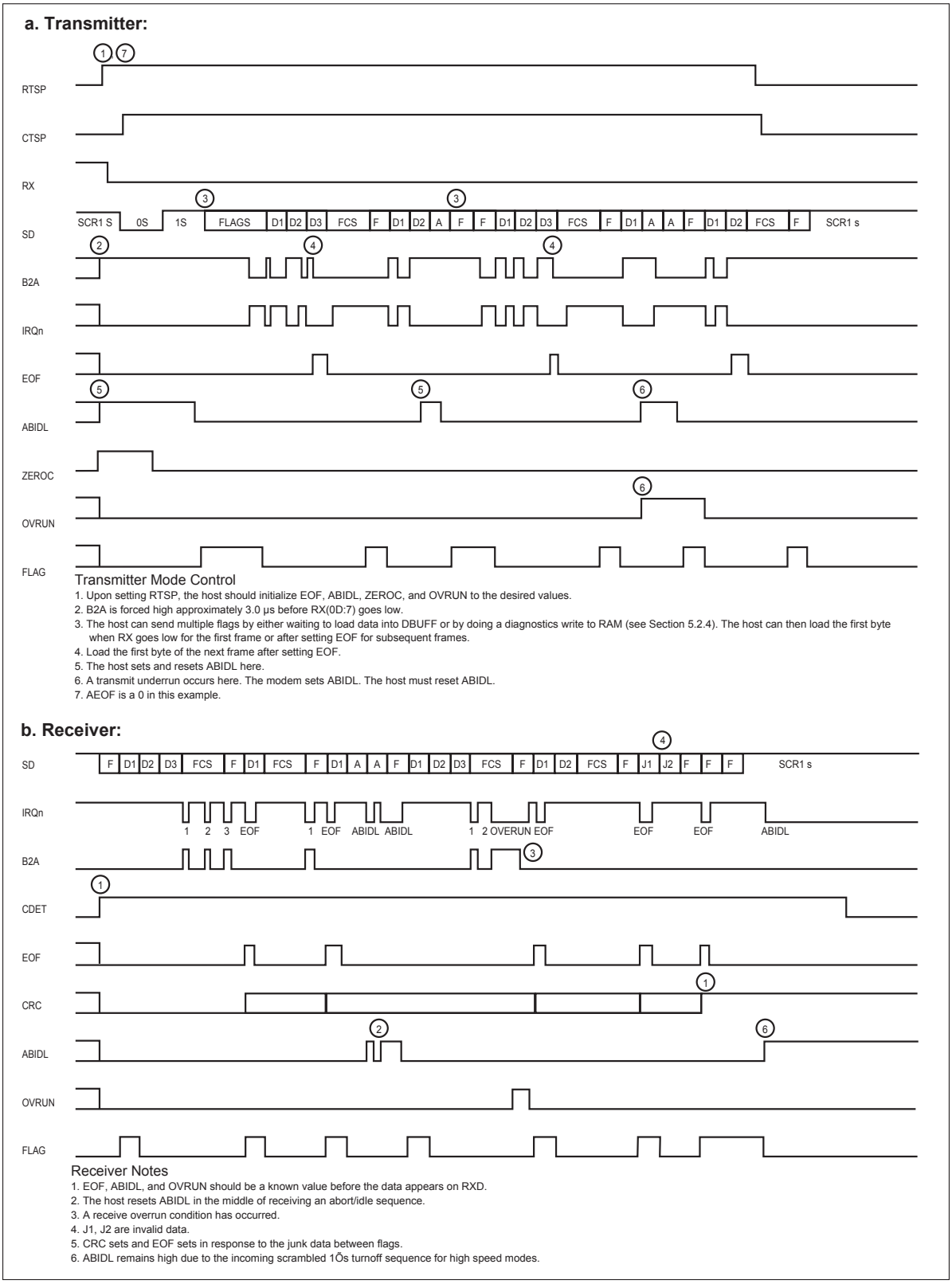
1. The beginning flag is transmitted. The receiver sees the flag and now becomes aligned with the transmitter. Both the receive and the transmitter FCS registers are preset to FFFFh.
2. The information field is transmitted. The data is also run through the FCS register before zero insertion. At the receive end, after the zero deletion algorithm, the data is presented to the user and then run through the FCS register.
3. The FCS is inverted and then transmitted. The transmitted FCS is passed through the receiver's FCS register. The shift register will contain 1111000010111000 if the frame has been received correctly.
4. The ending flag is transmitted. The signal timing is illustrated in Figure 5-4.

Figure 5-3. HDLC Process



102366_019

Figure 5-4. HDLC Signal Timing



102366_020

5.2.1 Mode Selection

To use HDLC in the modem, the host processor must:

1. Set up the modem configuration.
2. Set the HDLC mode bit.
3. Set the SETUP bit.

The format of the data input to the modem is in groups of 8-bit bytes. The least significant bit of the byte is transmitted first.

5.2.2 Transmission and Reception Rate

HDLC implemented in the modem runs under the following transmitter and receiver modes: V.17, V.29, V.27 ter, V.21, and V.21 with DTMF receiver.

5.2.3 Transmitter and Receiver Initialization

The HDLC transmitter and receiver is initialized differently than other modes upon power-up, reconfiguration, or setting the RTSP bit. Table 5-1 shows the states of the interface memory bits for HDLC initialization.

Table 5-1. Transmitter and Receiver Initialization

Parameter	Transmitter	Receiver
ABIDL	0 (Note 2)	0 (Note 2)
AEOF	0 (Note 2)	0 (Note 2)
B2A	1	Not initialized
CRC	0 (Note 1, 2)	0 (Note 2)
EOF	0 (Note 2)	0 (Note 2)
FLAG	0	0
OVRUN	0 (Note 2)	0 (Note 2)
ZEROC	0 (Note 2)	0 (Note 2, 3)
Notes: 1. Not applicable in the transmitter. 2. Zeroed only upon power-up; unchanged elsewhere. 3. Not applicable in the receiver.		

5.2.4 Flag Transmission and Reception

The modem transmitter sends at least one flag as the opening flag of the first frame. As long as the user does not load the 8-bit transmit data register, DBUFF (register 10h), with data, the modem sends continuous flags with no zero-sharing (0111111001111...). This facilitates transmission of the preamble as specified in T.30. Thus, the transmitter defaults to transmitting time-fill and, therefore, keeps the receiving link station active.

To assist the user in transmitting more than one flag between frames or at the end of the final frame, a counter can be accessed through modem diagnostics. This counter decrements directly in the signal processor's RAM. This means that the number written will only last for one group of flags. For example, FSK should have at least two beginning flags for the first frame and at least two ending flags for the final frame. However, frames between these two require only one flag. This is why the counter decrements directly and one flag is transmitted as a default. Diagnostics should be setup as shown below:

ADD = 85h

AREX = 0

BR = 0

CR = 1

WRT = 1

The value to write into YDAM and YDAL should be 1 less than the number of flags desired. This value can be written anytime after the RX bit returns to zero and before FLAG is set by the modem.

Using the FSK example above, assume three flags are to be transmitted at the beginning of the first frame and at the end of the final frame.

1. Turn on RTSP.
2. Wait until the RX bit is reset by the modem.
3. Disable diagnostics 1 (reset ACC).
4. Setup diagnostics 1 as above, write 00h into YDAM, and write 02h into YDAL.
5. Enable diagnostics 1 (set ACC).
6. Wait until B1A is set before resetting WRT.
7. For the ending flag of the final frame, immediately after loading in the final byte of data or after setting EOF, again setup diagnostics 1 as above, write 00h into YDAM, and write 02h into YDAL.

Another method exists for sending extra flags. The host must simply do nothing since flags are transmitted as the default condition. After the final zero in a flag is transmitted, the modem looks to see if the host has loaded new data into DBUFF (B2A is reset). If no new data is loaded before this time, another flag is sent. Therefore, if more than one flag is desired, the host must wait N-1 multiples of eight bit times after FLAG is set by the modem to load new data into DBUFF, where N is the number of flags. The host then has seven bit times in which to load new data and thus prevent another flag from being sent. For example, if three flags are desired between frames, the host must wait at least 16 bit times and not more than 23 bit times after FLAG is set by the modem.

As the default condition, the modem receiver continually searches for the flag data pattern. When one or more flags are detected, the interface memory status bit FLAG ($09:0) is set. The flags themselves are not presented to the host through the DBUFF

register. Therefore, as soon as a flag is observed, the modem examines the next byte of received data. If it is a flag, an abort/idle sequence, or a FCS, it is not given to the user. Instead, the appropriate status bits are set or reset.

The modem also has the capability to detect consecutive flags with zero-sharing.

5.2.5 Information Field Transmission and Reception

For information field transmission, the host should wait for CTSP ($0F:1) to transition high. The host must then load the data into DBUFF and then wait for the data available bit B2A ($1E:3) to be set by the modem before loading in the next byte of data. If AEOF is 0 and the next byte is not loaded into DBUFF within the next eight bit times, the modem will set OVRUN ($09:7), indicating an underrun condition has occurred. To tell the modem that the host wants to end the frame, the host must set EOF as soon as the modem has taken the last byte of the frame (B2A sets). When the modem recognizes EOF being high, the modem will reset EOF and will transmit the FCS and closing flag. Once the host sets EOF, the host may load in the first byte of data of the next frame into DBUFF. If the host wants to end transmission, the host must wait for EOF to return low before setting the RTSP bit.

The automatic frame ending feature can be used to more easily facilitate the use of a DMA interrupt system. With this feature, data is transmitted as described in the above paragraph. However, when AEOF ($15:5) is set by the host, the ending of the frame occurs “automatically,” without the host having to perform any handshaking. When the host is finished sending the data in the frame, the host should wait until EOF is set to a 1 by the modem. The modem will then send the 16-bit FCS and at least one ending flag. When EOF is set to a 1 by the modem, the host can then load in the first byte of data of the next frame. EOF will be set to a 0 by the modem at the beginning of flag transmission. Therefore, the underrun condition as described in the previous paragraph is the exact same condition that causes the 16-bit FCS and ending flag to be transmitted when AEOF is set to 1.

In the receiver, only the information field data between flags is passed to the user through the DBUFF register by the use of the handshaking bit B2A. The user must wait for B2A to be set by the modem and then take the data. If AEOF is 0 and the host does not read the data within eight bit times, OVRUN will set indicating an overrun condition, and the data in DBUFF will be overwritten by the next byte.

Furthermore, no flags, abort/idle sequence, or FCSs are given to the user via the DBUFF register. Since these fields are not presented to the user, there is at least a 16-bit time delay in the reception of data when receiving these fields. This allows the FCS and ending flag, continuous flags, or the abort/idle sequence to be flushed out of the internal buffers.

5.2.6 FCS and Ending Flag Transmission and Reception

If AEOF is 0, the host ends a frame by loading in his last byte of data into DBUFF, waiting until the modem has taken it (B2A sets), and then setting EOF. After setting EOF, the host may load in the first byte of data of the next frame into DBUFF. When the modem recognizes that the host wants to end the frame, the modem will reset EOF. To terminate data transmission, the host may turnoff RTSP when the modem resets EOF. After resetting EOF, the modem will automatically transmit the 16-bit FCS and at least one flag that signifies the end of the current frame and, if another frame follows, the beginning of the next frame.

For the case when AEOF is set to 1 (automatic end of frame), the host ends a frame by loading the last byte of data and waiting until EOF is set to 1 by the modem. The host

may then load in the byte of data of the next frame. To terminate data transmission, the host may turn off RTSP when the modem sets EOF to 1. The modem will then automatically transmit the 16-bit FCS and at least one flag that signifies the end of the current frame and, if another frame follows, the beginning of the next frame. The modem will set EOF to 0 upon sending a flag.

Upon the receipt of an ending flag in the current frame (which may also be the beginning flag of the next frame), the modem examines the data in the FCS register and compares it to the remainder. If the FCS register remainder is correct, CRC ($09:1) is reset. Conversely, if the remainder is incorrect, the CRC bit is set. This is the only time CRC is updated (except upon power-up). Following this determination, the modem sets EOF. Thus, once the modem sets EOF, the host can examine CRC to determine whether or not an erred frame was received. It is left to the host to reset the EOF bit. If the user does not reset EOF before the end of the next frame, the host will not get any indication that the following frame has ended.

5.2.7 Abort/Idle Sequence Transmission and Reception

An abort/idle sequence can be sent by the host setting the bit ABIDL ($09:3) in the interface memory. This stops any normal frame transmission, as well as continuous flag transmission, and sends continuous ones. After the setting of ABIDL is detected, the modem first completes the transmission of the current byte of data. Immediately after this transmission, the modem sends eight consecutive ones. After these eight bit times, if ABIDL is still set, eight ones are sent again. To discontinue this sequence, ABIDL must be reset. Then, if no new data is loaded into DBUFF, continuous flags are sent. If new data is loaded into DBUFF (B2A is reset), the modem sends a beginning flag and then the data in DBUFF. The modem will also recognize the setting of ABIDL while transmitting the FCS, thereby allowing the receiver to recognize that the transmitted frame should be discarded.

The modem has the ability to send continuous zeros. To accomplish this, ABIDL and ZEROC ($09:4) must be set. The modem completes the transmission of the current byte and then sends eight consecutive zeros. After this time, if ABIDL remains set, eight zeros are sent again. To discontinue this sequence, ABIDL must be reset or, if continuous ones are desired, ZEROC only must be reset. However, if no new data is loaded in DBUFF and ABIDL is reset, continuous flags are sent regardless of the state of ZEROC. Then, if new data is loaded into DBUFF (B2A is reset), the modem sends a beginning flag and then the data in DBUFF.

The modem in HDLC mode not only continually searches for flags, but also continually searches for an abort/idle sequence. When the receive modem encounters this data pattern, it sets the abort/idle receive bit ABIDL. It is left up to the host to reset this bit. However, receiver processing will continue unaffected by the state of this bit.

The reception of data immediately following the abort/idle sequence is treated as invalid and is not presented to the user. Therefore, to re-establish transmitter and receiver synchronization, the receiver must see at least one flag. At least one flag and three bytes of data must be received following the abort sequence before any data is given to the host.

5.2.8 Underrun and Overrun Conditions

A bit in the interface memory OVRUN ($09:7) is used to indicate to the host processor that a transmit underrun condition has occurred. If the host does not load in a new byte of data within eight bit times, OVRUN and ABIDL will be set by the modem and the modem will automatically send a minimum of eight continuous ones. This abort sequence

will continue until the host resets ABIDL. After the host resets ABIDL, the modem will finish sending the current byte of ones and will then send a flag. At the end of sending a flag, if B2A is reset, the modem will interpret the data in DBUFF as being the first byte of the next frame. After uploading this data for the first byte of the frame, the modem will reset OVRUN. The modem will always reset OVRUN every time it sets B2A, except upon transmitter HDLC initialization. (The underrun condition is not applicable when AEOF = 1.)

In the receiver, the OVRUN bit will inform the host that an overrun condition occurred. The overrun condition takes place when the receiver fails to take the byte of data in DBUFF within eight bit times. The modem will thus overwrite the data in DBUFF and, if the host has not taken the data (B2A is not reset), the modem will set OVRUN. To detect further overrun occurrences, the host must reset this bit.

5.2.9 Transmit Mode Control

After power-up, reconfiguration, or setting the RTSP bit, the host must wait for the CTSP bit to turn on before starting frame transmission.

There are two ways in which the user can signal the modem to exit current HDLC execution. The first way is by setting the SETUP bit which tells the modem that a new configuration is desired. The second way is by resetting the RTSP bit in the interface memory. In both cases, the following events will occur:

1. When AEOF is set to a 0 and if exiting after making sure the modem took the data in DBUFF, setting EOF to a 1, and then waiting for EOF to be set to a 0 by the mode, the modem sends the last byte of data followed by the 16-bit FCS sequence and a closing flag. The modem then either goes through the turn-off sequence (if the RTSP bit is turned off), or sets up the new configuration (if SETUP is set to 1).
2. When AEOF is a set to a 1 and if exiting after making sure the modem sets EOF to a 1, the modem sends the last byte of data followed by the 16-bit FCS sequence and a closing flag. The modem then either goes through the turn-off sequence (if the RTSP bit is turned off), or sets up the new configuration (if SETUP is set to 1).
3. Exiting during the transmission of an abort sequence, the modem finishes sending the last byte of the abort sequence, then either goes through the turn-off routine or sets up to a new configuration.

5.3 Example Application

Refer to Section 3 for a description of the bits associated with the HDLC and programmable interrupt functions.

5.3.1 Transmitter Example

1. The modem configuration to the desired speed for transmitting, enable HDLC and set RTSP. (AEOF defaulted to 0).
2. Wait until CTSP goes low and returns to a high level.
3. Place the first byte of data into DBUFF. The modem transmits a flag followed by this byte of data.
4. As soon as B2A is set, load in the next byte of data. This must occur within eight bit times of B2A being set.
5. After all information but the last byte is given to the modem, load in the last byte of data in the frame as in step 4.
6. To end the frame, the host must load in the last byte of data into DBUFF, wait for B2A to be set, and then set EOF.
7. Repeat steps 3 through 6 for all frames to be transmitted.
8. When the last byte of the final frame is loaded into register DBUFF, wait for B2A to return high. Then set EOF and wait for EOF to return low before resetting RTSP. The modem transmits the last byte followed by the 16-bit FCS and at least one closing flag, depending upon if diagnostics was used to write into the flag counter RAM location as mentioned previously. The modem then goes through its normal turn-off routine.

5.3.2 Receiver Example

The steps to perform a typical HDLC reception are:

1. Set the modem configuration to the desired speed for receiving and enable HDLC.
2. Perform a dummy read of DBUFF to reset B2A.
3. Wait until the modem has properly configured.
4. Monitor, through interrupts, the EOF, ABIDL, and B2A bits in the interface memory.
5. Wait for an interrupt. If it is caused by B2A being set, read the data in DBUFF. This indicates that the first byte of the first frame is ready for host reading. If the interrupt is caused by EOF being set, check CRC to determine if the current frame is in error and reset EOF. If the interrupt is caused by ABIDL, the modem is receiving the abort/idle sequence. The current frame that was aborted is invalid. The modem does not set the CRC bit or the EOF bit in this case since no FCS checking is done.
6. Continue waiting for interrupts and take appropriate action when the interrupts are received.

This page is intentionally blank.

6. Tone Detector Filter Tuning

This section describes a method of tuning the filters in the modem for tone detection.

The modem includes three independently programmable tone detectors (F1, F2, and F3). Upon power-up, the tone detectors are centered at 2100 Hz (F1), 1100 Hz (F2), and 462 Hz (F3).

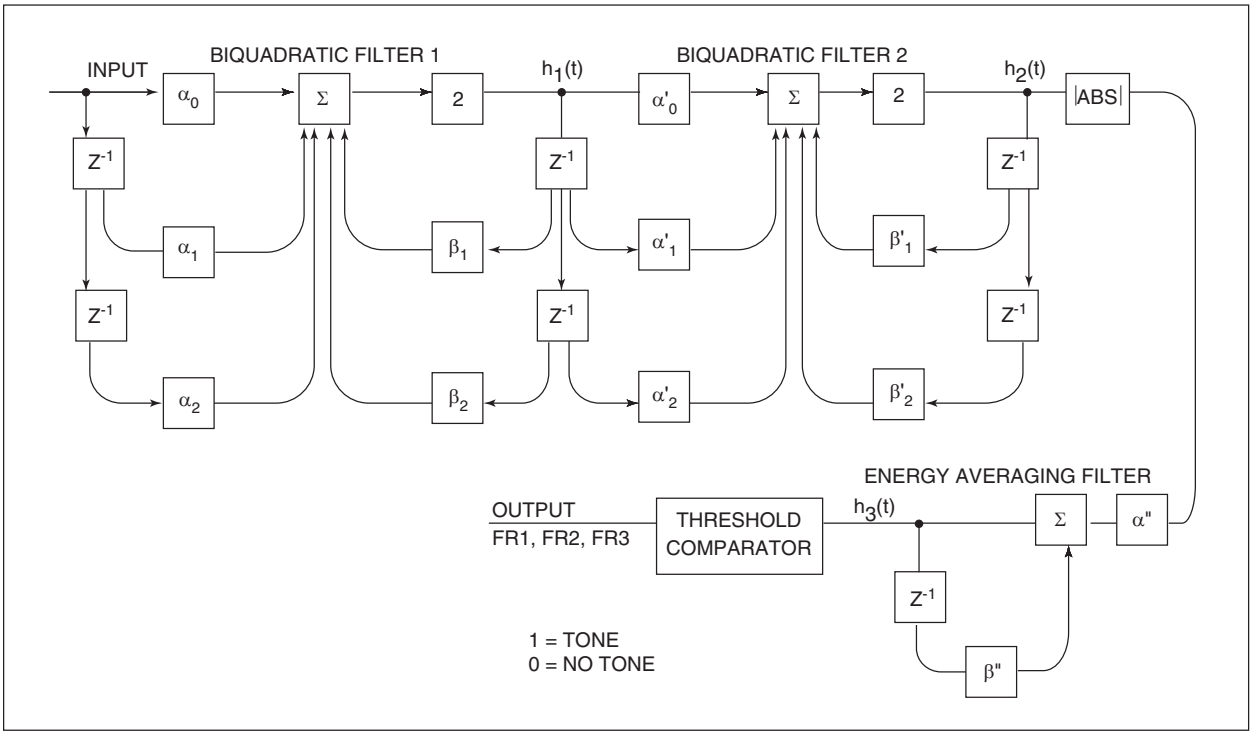
In each of the three detectors, two second-order biquadratic filters can be programmed for a variety of frequency responses. The modem sets interface memory bits FR1, FR2, and FR3 to a 1 when tone detectors 1, 2, and 3 detect energy above their respective threshold. This Designer's Guide presents a method of tuning these detectors to any frequency in the 400 Hz–3000 Hz band.

By setting bit 12TH to a 1 in the interface memory, the three tone detectors are cascaded to form a programmable 12^{th}-order filter. The modem sets the FR3 bit to a 1 when energy is above the threshold.

6.1 Computation of Tone Detector Coefficients

Each tone detector consists of two cascaded second-order filters, an energy averaging filter, and a threshold comparator. A diagram of a tone detector is shown in Figure 6-1.

Figure 6-1. Modem Tone Detection Diagram



Filter 1 has a transfer function:

$$H_1(Z) = 2(\alpha_0 + \alpha_1 Z^{-1} + \alpha_2 Z^{-2})/(1 - 2\beta_1 Z^{-1} - 2\beta_2 Z^{-2}) \quad \text{(Eq. 1)}$$

Filter 2 has a transfer function:

$$H_2(Z) = 2(\alpha'_0 + \alpha'_1 Z^{-1} + \alpha'_2 Z^{-2})/(1 - 2\beta'_1 Z^{-1} - 2\beta'_2 Z^{-2}) \quad \text{(Eq. 2)}$$

The energy averaging filter has a transfer function:

$$H_3(Z) = \alpha''/(1 - \beta'' Z^{-1}) \quad \text{(Eq. 3)}$$

The output of the energy average is fed to a threshold comparator that sets interface memory bit FR1, FR2, or FR3 to a 1 if the output is equal to or greater than the Tone Detector threshold (default value = 1/8 of full scale), otherwise, the bits are set to a 0.

Filters 1 and 2 have frequency response as shown in Figure 6-2. When cascaded, they form a bandpass filter with a narrow bandwidth as shown in Figure 6-3.

Given the transfer functions $H_1(Z)$ and $H_2(Z)$, an analytical method is provided to compute their coefficients for any frequency in the 400 Hz – 3000 Hz band. First, consider $H_1(Z)$. This transfer function can be rewritten as:

$$H_1(Z) = 2(\alpha_0 Z^2 + \alpha_1 Z + \alpha_2)/(Z^2 - 2\beta_1 Z - 2\beta_2) \quad \text{(Eq. 4)}$$

which has a conjugate pair of poles:

$$P_1 = \beta_1 + \sqrt{(\beta_1 2 + 2\beta_2)}$$

and

$$P_2 = \beta_1 - \sqrt{(\beta_1 2 + 2\beta_2)}$$

Upon power up, these poles lie on a circle of radius 0.994030884 on the Z-plane. The radius of the tone detector circle was chosen so that each filter has a high Q without being unstable (poles must lie inside the unit circle for stability). Figure 6-4 shows a Z-plane pole-zero diagram for an arbitrary conjugate pole pair on the tone detector circle. The angle $\theta = 360\ f_O/f_S$, where f_O is the desired center frequency and f_S is the sampling rate.

The following equations are derived from the angle and magnitude of the position vector pointing to a pole pair located at the desired angle:

$$\cos^{-1}(\beta_1/r) = \theta = 360° \times f_O/f_S \quad \text{(Eq. 5)}$$

$$\sqrt{[\beta_1 2 + (-\beta_1 2 - 2\beta_2)]} = r = 0.994030884 \quad \text{(Eq. 6)}$$

Solving for β_1 and β_2:

$$\beta_1 = r \cos(360° \times f_O/f_S) \quad \text{(Eq. 7)}$$

$$\beta_2 = -r^2/2 \quad \text{(Eq. 8)}$$

In deriving these equations, only $H_1(Z)$ was considered. However, the tone detector consists of two identical filters in cascade. Referring to Figure 6-3, shifting filter 1 and filter 2 above and below the desired center frequency, a response with the desired bandwidth is achieved. Furthermore, since the α_1, α'_1, α_2, and α'_2 coefficients default to zero upon power-up, α_0 controls the amplitude response, and one may set $\alpha_0 = \alpha'_0$ to uniformly raise or lower the overall cascade response.

From Equation 8:

$$\beta_2 = \beta'_2 = -r^2/2 = -0.494048699$$

Rewriting Equation 7 in terms of the offsets f_A and f'_A:

$$\beta_1 = r \cos [360° (f_O - f_A)/f_S] \text{ (Eq. 9)}$$

$$\beta'_1 = r \cos [360° (f_O + f'_A)/f_S] \quad \text{(Eq. 10)}$$

The frequency offset is approximately 72% of B/2 (half the bandwidth) for most applications:

$$\beta'_2 \cong 0.72 (B/2) \quad \text{(Eq. 11)}$$

The value of f_A should be equal to f'_A. However, f_A may be chosen 1% smaller than f'_A to compensate for the fact that the overall cascade response is not perfectly symmetrical, near DC (see Figure 6-5).

The values for the coefficients α_0 and α'_0 that set $|H(f_O)| = 0$ dB in equations 1 and 2 were measured and plotted versus center frequency f_O as shown in Figure 6-6. Three equations corresponding to three linear approximations result:

$$\alpha_0 = \alpha'_0 = [(104/319)f_O - 78.62]/32767$$

$$400 = f_O \leq 1100 \text{ Hz} \quad \text{(Eq. 12a)}$$

$$\alpha_0 = \alpha'_0 = [(44/275)f_O + 104]/32767$$

$$1100 \leq f_O \leq 1650 \text{ Hz (Eq. 12b)}$$

$$\alpha_0 = \alpha'_0 = [(4/45)f_O + 221]/32767$$

$$1650 \leq f_O \leq 3000 \text{ Hz (Eq. 12c)}$$

6.1.1 Energy Averaging Filter

The coefficients of the energy averaging filter are determined by a Z-domain approximation to an RC circuit of transfer function $H(S) = 1/(1 + S\tau)$:

$$\alpha'' = 1/(1 + f_S\tau) \quad \text{(Eq. 13)}$$

$$\beta'' = 1/[1 + (1/f_S\tau)] \quad \text{(Eq. 14)}$$

Upon power up, α'' and β'' are set for $\tau = 0.1$ seconds. Unless different tone detector response times are required, these coefficients need not be changed.

The Tone Detector Threshold value is programmable in DSP RAM (see Section 4).

Figure 6-2. Typical Single Filter Response

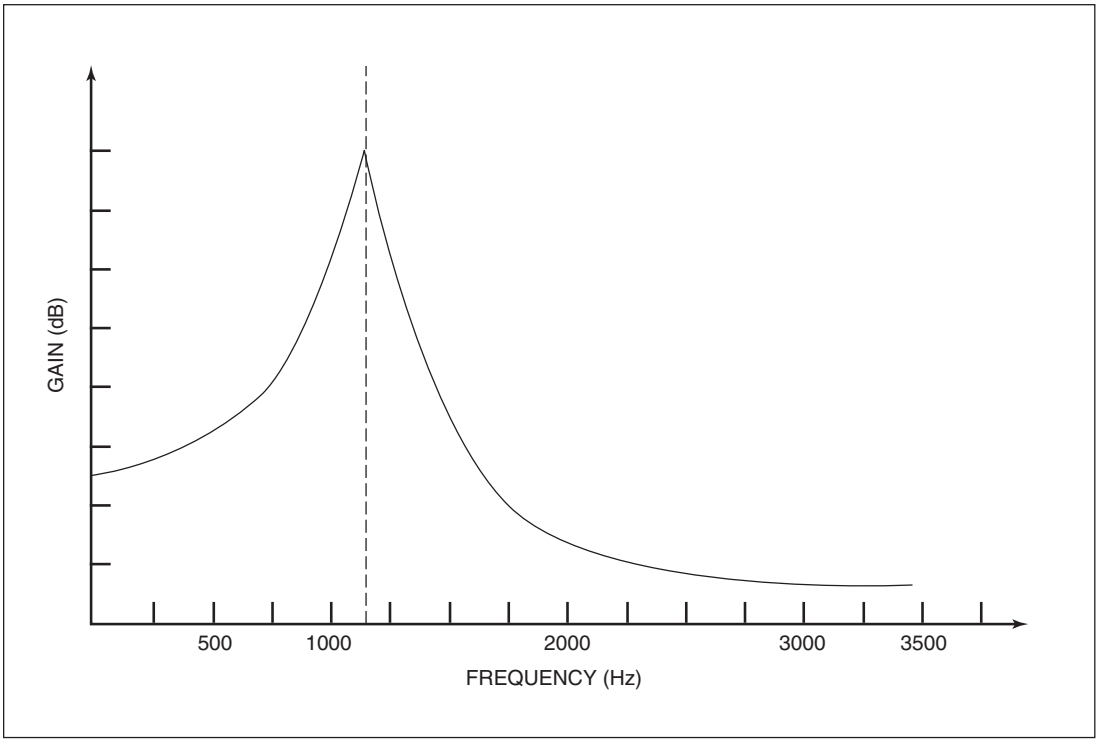


Figure 6-3. Typical Cascade Filter Response

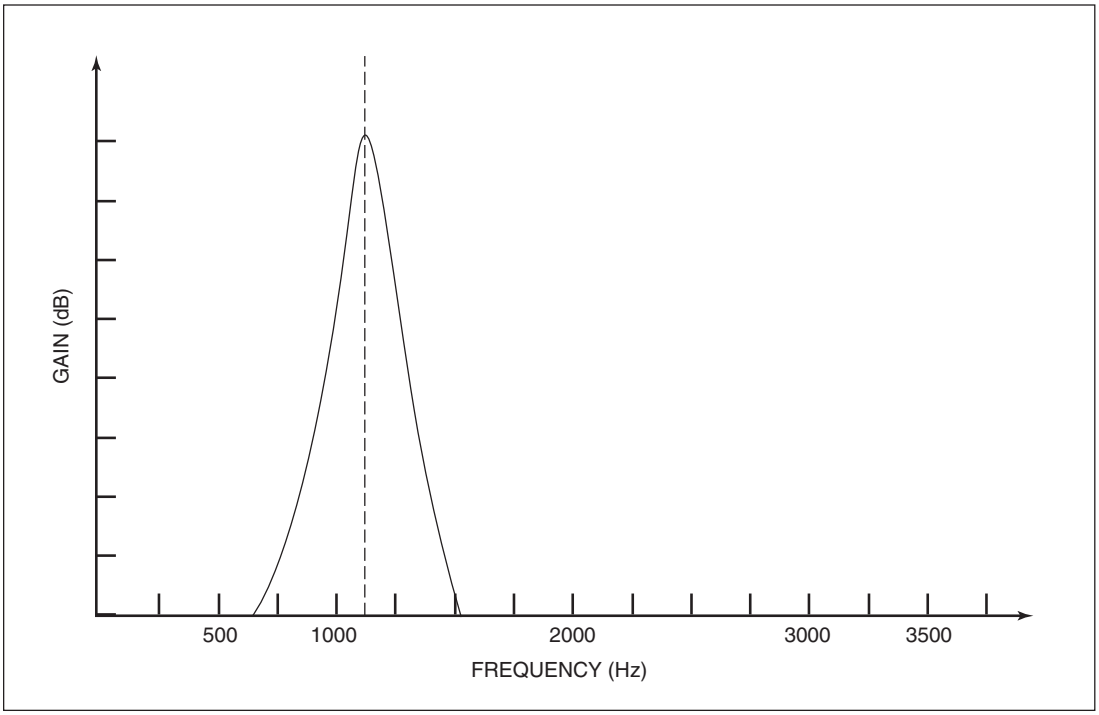
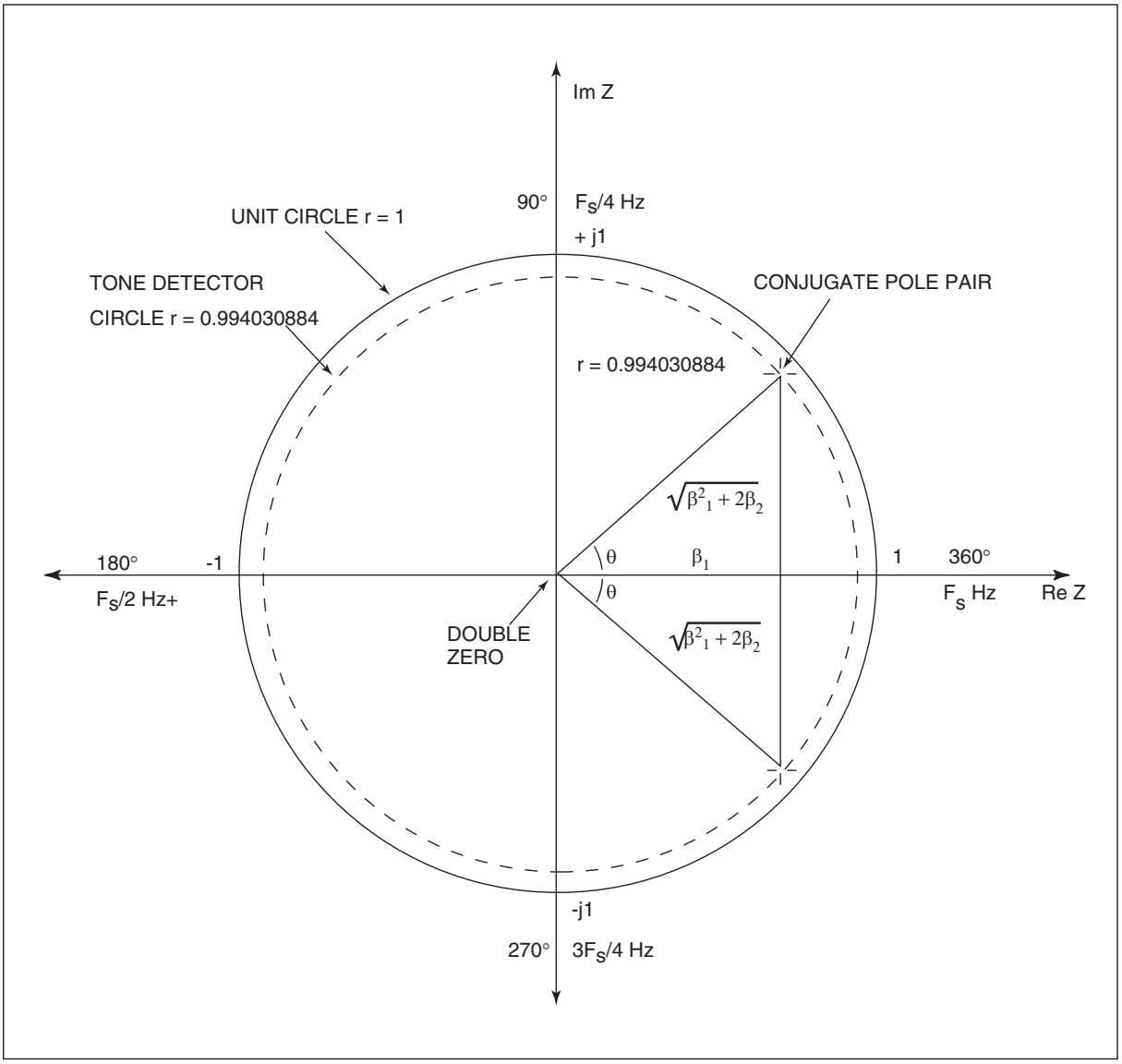


Figure 6-4. Z-Plane Pole-Zero Diagram



102366_024

Figure 6-5. Bandwidth and Offset Frequencies

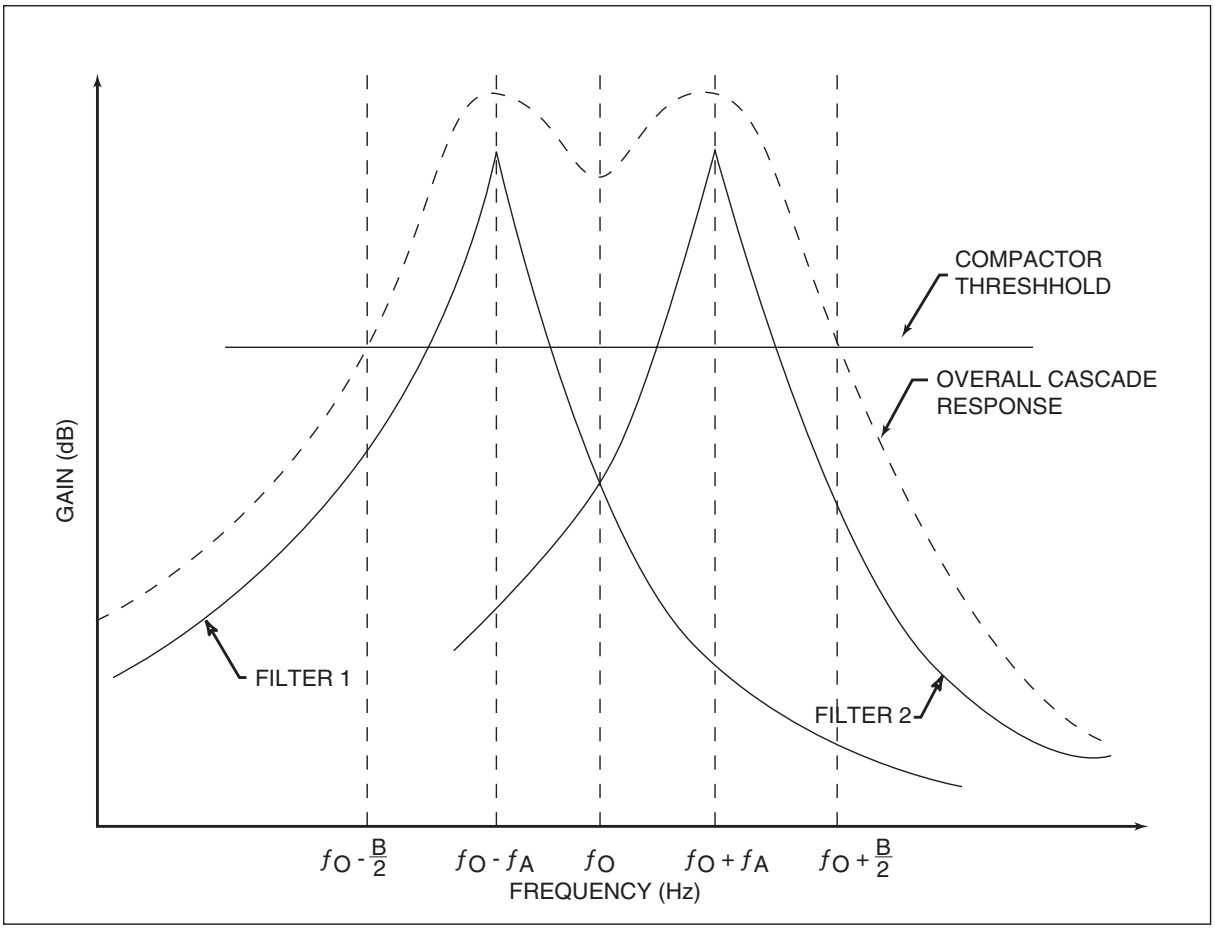
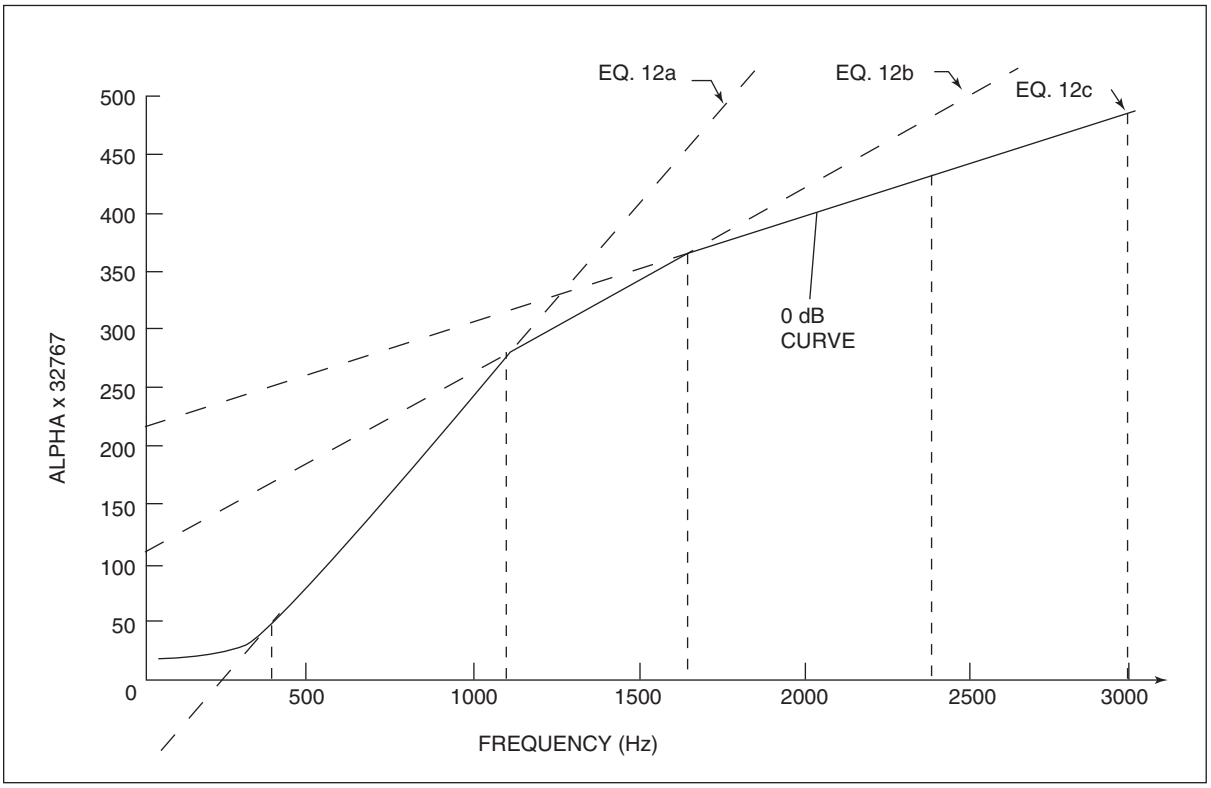


Figure 6-6. Alpha-zero Center Frequency



6.1.2 Filter Coefficients

Table 6-1 contains the RAM access codes for all filter coefficients. Refer to the Section 4 for the proper procedure for writing new coefficients into the RAM locations.

Table 6-2 contains the computed values of the filter coefficients, including those of default frequencies 462 Hz, 1100 Hz, and 2100 Hz. The value 32767 (7FFFh) is full scale in the DSP's machine units (32767 = unity). Coefficients may range from –1 to +1 (8000h to 7FFFh) in machine units.

Table 6-1. Filter Coefficient RAM Access Codes

Coefficient Name	RAM Write Access Code (Hex)		
	Tone 1	Tone 2	Tone 3
α_0	25	2B	31
α_1	26	2C	32
α_2	27	2D	33
α'_0	28	2E	34
α'_1	29	2F	35
α'_2	2A	30	36
β_1	A6	AC	B2
β_2	A7	AD	B3
β'_1	A9	AF	B5
β'_2	AA	B0	B6
α''	A8	AE	B4
β''	A5	AB	B1

Notes:

In all cases: AREX is a 0, CR is a 1, and BR is a 0

If the most significant bit (MSB) of the address is a 0, the data is written to XRAM; if the MSB is a 1, the data is written to YRAM.

Table 6-2. Calculated Coefficient Values, 9600 Hz Sample Rate

Frequency Detected	Coefficient Name	Coefficient Value (Hex.)	Coefficient Value (Dec.)
2100 Hz ±25 Hz; $f_A \cong$18 Hz	$\alpha_0 = \alpha'_0$	0198	0.01245117
	$\alpha_1 = \alpha'_1 = \alpha_2 = \alpha'_2$	0000	0.00000000
	β_1	1A4A	0.20538330
	β'_1	175A	0.18243408
	$\beta_2 = \beta'_2$	C0C4	–0.49401855
1850 Hz ±24 Hz; $f_A \cong$18 Hz	$\alpha_0 = \alpha'_0$	0180	0.01171875
	$\alpha_1 = \alpha'_1 = \alpha_2 = \alpha'_2$	0000	0.00000000
	β_1	2E37	0.36105347
	β'_1	2B69	0.33914184
	$\beta_2 = \beta'_2$	C0C4	-0.49401855
1650 Hz ±23 Hz; $f_A \cong$18 Hz	$\alpha_0 = \alpha'_0$	0170	0.01123047
	$\alpha_1 = \alpha'_1 = \alpha_2 = \alpha'_2$	0000	0.00000000
	β_1	3D48	0.47875977
	β'_1	3AA6	0.45819092
	$\beta_2 = \beta'_2$	C0C4	-0.49401855
1100 Hz ±30 Hz; $f_A \cong$ 19 Hz	$\alpha_0 = \alpha'_0$	0118	0.00854492
	$\alpha_1 = \alpha'_1 = \alpha_2 = \alpha'_2$	0000	0.00000000
	β_1	60BE	0.75579834
	β'_1	5E9C	0.73913574
	$\beta_2 = \beta'_2$	C0C4	-0.49401855
462 Hz ±14 Hz; $f_A \cong$ 10 Hz	$\alpha_0 = \alpha'_0$	0048	0.00219726
	$\alpha_1 = \alpha'_1 = \alpha_2 = \alpha'_2$	0000	0.00000000
	β_1	79F3	0.95272827
	β'_1	7974	0.95152405
	$\beta_2 = \beta'_2$	C083	–0.49601733

This page is intentionally blank.

7. DTMF Dialing with Auto Dialer

The modem includes tunable oscillators that can be used to perform dual-tone multi-frequency (DTMF) dialing. The frequency and amplitude of each oscillator output is under host control. A programmable tone detector can also be used in call establishment to recognize an answer tone.

This section describes the method of oscillator and filter tuning by the host processor and provides an example of an auto dialer routine that may be programmed into the host.

7.1 DTMF Requirements

EIA Standard RS-496, (Section 4), specifies requirements that ensure proper DTMF signaling through the public switched telephone network (PSTN). These tones consist of two sinusoidal signals, one from a high group of frequencies and one from a low group of frequencies, that represent each of the pushbutton telephone characters shown in Table 7-1.

Table 7-1. DTMF Signals

Low	High Frequency			
Frequency	**1209 Hz**	**1336 Hz**	**1477 Hz**	**1633 Hz**
697 Hz	1	2	3	A
770 Hz	4	5	6	B
852 Hz	7	8	9	C
941 Hz	*	0	#	D

Signal power is defined for the combined tones as well as for the individual tones. Both maximum and minimum power requirements are functions of loop current. By combining the various requirements of RS-496, compromise power levels can be determined that meet the power specification for all U.S. lines (when driving the PSTN from a 600 ohm resistive source). The high frequency tone should be at a higher power level than the low frequency tone by approximately 2 dB. The maximum combined power, averaged over the pulse duration, should not exceed +1 dBm. The minimum steady state power of the high frequency tone should not be less than –8 dBm.

When connecting the modem circuit to the PSTN by means of a data access arrangement (DAA) set for permissive mode, the DAA gain is –9 dB. The modem circuit must, therefore, drive the DAA input with +1 dBm of steady state high frequency power and -1 dBm of steady state low frequency power to meet all of the listed conditions. Since +0.5 dBm is the maximum undistorted power level for individual tones generated by the modem, the user may need to add gain in front of the DAA during DTMF dialing.

The required duration of the DTMF pulse is 50 ms minimum. By experience, a pulse duration of approximately 95 ms is more reliable. The required interval between DTMF pulses is 45 ms minimum and 3 seconds maximum. Again, by experience, an interdigit delay of approximately 70 ms is preferred.

The remaining requirements of RS-496, relative to DTMF dialing, are not influenced by the host processor. These requirements are all met by the modem's oscillators.

7.2 Setting Oscillator Parameters

The oscillator frequency and output power are set by the host computer in DSP RAM using the microprocessor bus and diagnostic data routine. For a description of the microprocessor bus and other interface considerations, refer to Sections 2, 3 and 4.

To generate a DTMF tone, place the modem into TONE configuration (CONF = 80h). The user must program the frequencies and the levels of each tone. To set the frequency of tone 1, write a 16-bit hexadecimal number into RAM using RAM access code 21h with AREX = 0, BR = 0, and CR = 1. When setting the frequency of tone 2, use the same procedure with the RAM access code 22h with AREX = 0, BR = 0, and CR = 1. Set the power levels of tone 1 by writing a 16-bit hexadecimal number into RAM using RAM access code 22h with AREX = 0, BR = 0, and CR = 0. The RAM access code for the power level of tone 2 is 23h with AREX = 0, BR = 0, and CR = 0.

The hexadecimal numbers written into these RAM locations are scaled as follows:

Frequency number = 6.8267 x (desired frequency in Hz)

Power number = $18426\ [10^{(Po/20)}]$

Where Po = output power in dBm with a 600 ohm load termination. If terminating with a series 600 ohm resistor into a 600 ohm load, add 6 dB to the output power before using the above equation.

These decimal numbers must be converted to hexadecimal form then stored in RAM (see RAM data write routine).

Hexadecimal numbers for DTMF generation are listed in Table 7-2. Power levels are selected to give the desired output power for each tone (–1 dBm for the high frequency tone and –3 dBm for the low frequency tone if terminated with a series 600 Ω resistor into a 600 Ω load) while compensating for modem filter characteristics.

7.3 Detecting Answer Tone

Frequency detector bit FR1 ($08:5) can be used to detect a 2100 Hz answer tone when connection to the remote modem is successful. Bit FR1 goes active (one) when energy above the turn-on threshold is present at 2100 Hz ±25 Hz. At the end of the answer tone, FR1 returns to zero and data transmission can begin.

7.4 Complete Calling Sequence

A complete calling sequence consists of several steps including modem configuration, telephone number selection, DTMF transmission, and answer tone detection. A sample flow chart for implementing an auto-dialer in host software is illustrated in Figure 7-1.

The auto-dialer routine may be entered at one of two points; either AUTO DIAL or REDIAL. When entering at AUTO DIAL, the host prompts the user to enter a phone number, which is then stored in the phone number buffer. When entering at REDIAL, the routine dials the number previously stored in the phone number buffer and does not issue a user prompt.

Interrupts not required during dialing are disabled to prevent errors in real time delays. Interrupt status is saved to allow restoring these interrupts when dialing is complete. The current modem configuration is saved prior to selecting the DTMF Transmit

configuration, then restored at the completion of the auto-dialer routine to allow data transfer.

The commands for off-hook and request coupler cut through are typical of signals required by data access arrangements that may be connected to the modem for switched network operation.

Since the number to be dialed varies in length depending on the requirements of various PBX equipment, domestic telephone companies, and foreign PTTs, the number buffer must allow for numbers of different length. The method used in Figure 7-1 determines the end of valid bytes in the buffer is zero recognition. After the last digit is entered, the carriage return must place a 00h (ASCII NUL character) in the buffer. All other bytes must be non-NUL ASCII characters. Only numeric characters (ASCII 30 through 39) are printed and dialed. Non-numeric characters are tested for comma and NUL. Comma causes a 2-second pause in dialing to allow for known delays in the telephone network or PBX. NUL ends the dialing portion of the routine and begins the answer tone detection portion. All other characters are ignored.

The answer tone detection logic allows 30 seconds for 2100 Hz recognition. If answer tone is not recognized within this time limit, the call is aborted. If answer tone is recognized, the routine jumps to the data handling software.

Table 7-2. DTMF Parameters

Digit	AREX	ADD (Hex.)	CR	BR	Value (Hex)
0	0	21	1	0	1918
	0	22	1	0	23A0
	0	22	0	0	65AB
	0	23	0	0	7FFF
1	0	21	1	0	1296
	0	22	1	0	203D
	0	22	0	0	65AB
	0	23	0	0	7FFF
2	0	21	1	0	1296
	0	22	1	0	23A0
	0	22	0	0	65AB
	0	23	0	0	7FFF
3	0	21	1	0	1296
	0	22	1	0	2763
	0	22	0	0	65AB
	0	23	0	0	7FFF
4	0	21	1	0	1488
	0	22	1	0	203D
	0	22	0	0	65AB
	0	23	0	0	7FFF
5	0	21	1	0	1488
	0	22	1	0	23A0
	0	22	0	0	65AB
	0	23	0	0	7FFF
6	0	21	1	0	1488
	0	22	1	0	2763
	0	22	0	0	65AB
	0	23	0	0	7FFF
7	0	21	1	0	16B8
	0	22	1	0	203D
	0	22	0	0	65AB
	0	23	0	0	7FFF
8	0	21	1	0	16B8
	0	22	1	0	23A0
	0	22	0	0	65AB
	0	23	0	0	7FFF
9	0	21	1	0	16B8
	0	22	1	0	2763
	0	22	0	0	65AB
	0	23	0	0	7FFF

Table 7-2. DTMF Parameters (Continued)

Digit	AREX	ADD (Hex.)	CR	BR	Value (Hex.)
*	0	21	1	0	1918
	0	22	1	0	203D
	0	22	0	0	65AB
	0	23	0	0	7FFF
#	0	21	1	0	1918
	0	22	1	0	2763
	0	22	0	0	65AB
	0	23	0	0	7FFF
A	0	21	1	0	1296
	0	22	1	0	2B8C
	0	22	0	0	65AB
	0	23	0	0	7FFF
B	0	21	1	0	1488
	0	22	1	0	2B8C
	0	22	0	0	65AB
	0	23	0	0	7FFF
C	0	21	1	0	16B8
	0	22	1	0	2B8C
	0	22	0	0	65AB
	0	23	0	0	7FFF
D	0	21	1	0	1918
	0	22	1	0	2B8C
	0	22	0	0	65AB
	0	23	0	0	7FFF

7.5 Single Tone Generation

In OEM equipment that combines the features of a modem with those of a telephone handset, the tone generators may be used to generate a caller reassurance tone (or even music) while the caller is kept on hold. To generate a single tone, make sure one of the oscillators is set to zero frequency or zero amplitude while the other oscillator is set to the desired frequency and amplitude. Common parameters for single tone generation are listed in Table 7-3.

Table 7-3. Common Single Tone Parameters

Parameter	Frequency	Value (Hex.)
CED	2100 Hz	3800
CNG	1100 Hz	1D55

Figure 7-1. Autodialer Flowchart

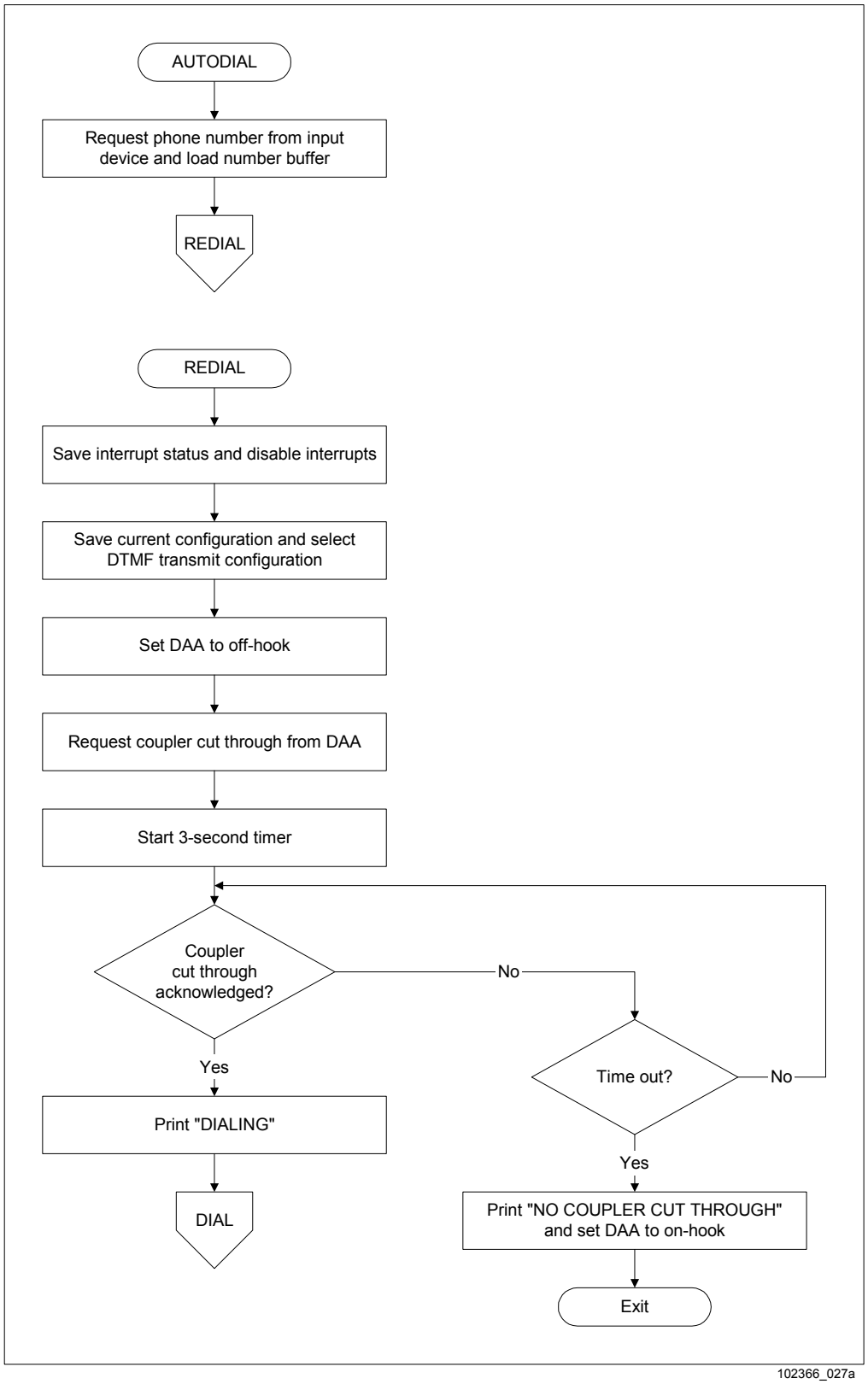


Figure 7-1. Autodialer Flowchart (Continued)

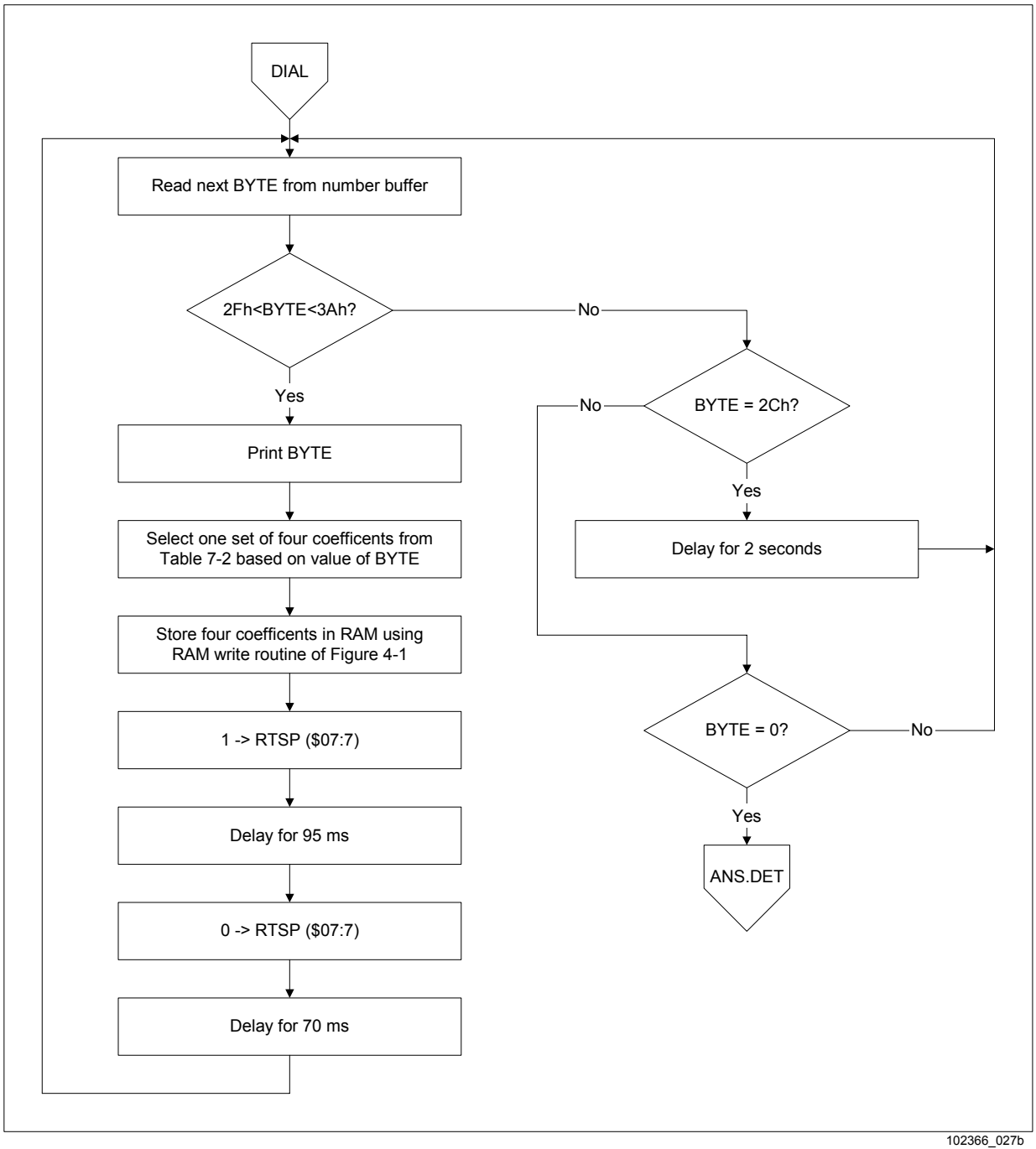
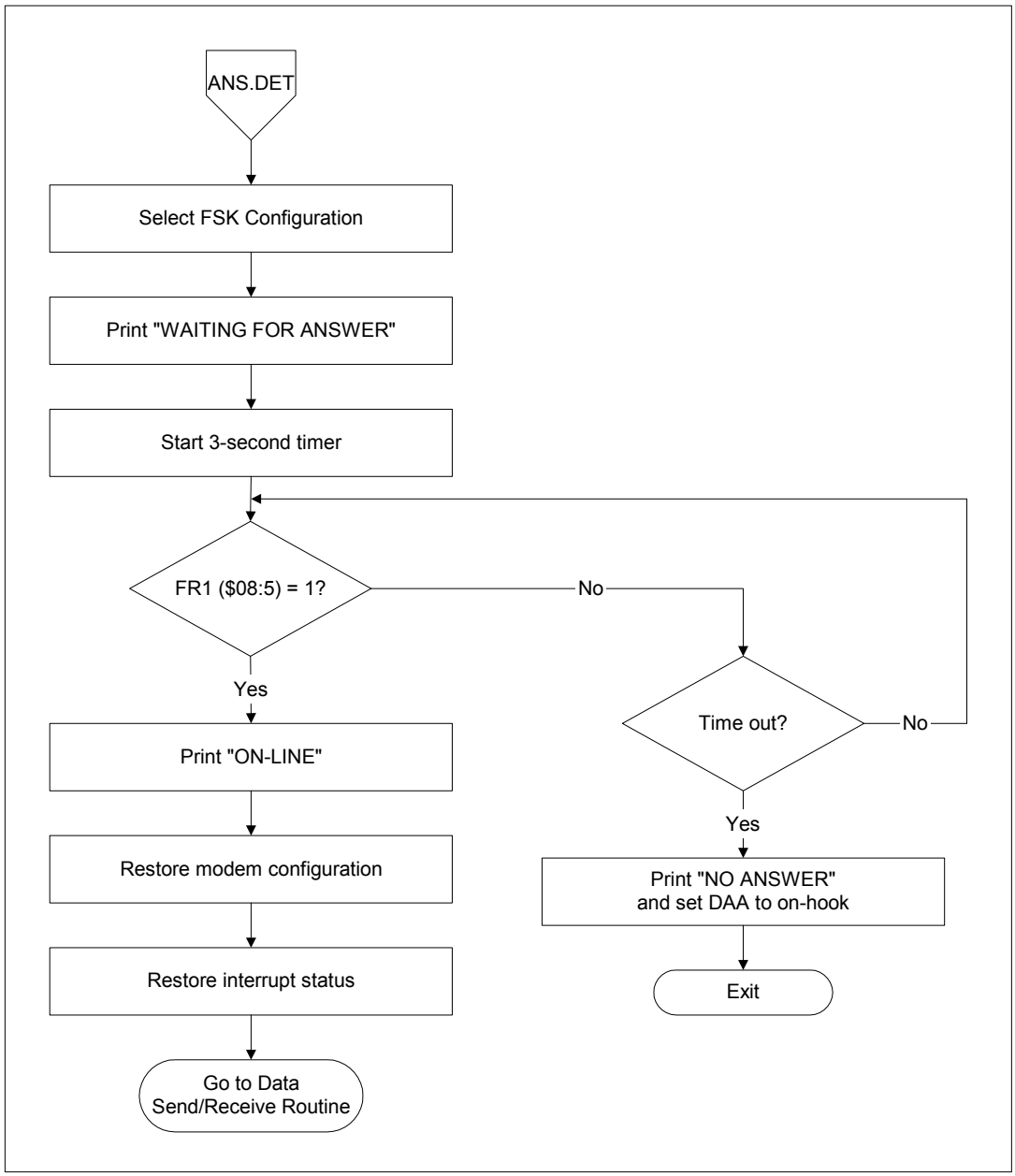


Figure 7-1. Autodialer Flowchart (Continued)



8. T.30 Implementation

ITU-T Recommendation T.30 details procedures for facsimile transmission over the PSTN. This standard describes how to initiate, complete, and end a fax transmission. This section describes methods to set up host software to implement T.30.

A block diagram of a Group 3 facsimile machine is shown in Figure 8-1. The modem performs the modulation/demodulation process. The fax machine manufacturer must implement the interface between the modem (T.30), the data compression/decompression (T.4), and the interface to the scanner and printer.

There are five phases (A-E) to the T.30 facsimile protocol. Phase A is the call setup, in which both facsimile machines connect to the line. Phase B is a pre-message procedure which consists of identification and command sections. The actual high speed message transmission occurs during Phase C. This is followed by the post-message procedure or Phase D. Both facsimile machines release the line in Phase E.

Figure 8-2 illustrates a typical Group 3 facsimile procedure. This T.30 example describes a facsimile call where the calling unit (originate) transmits a documents to a called unit (answer). Phase E is not included in this example since it is the call release and both ends hang up.

8.1 T.30 Phases

8.1.1 Phase A

T.30 specifies that call establishment can be realized one of four ways. The four methods of call establishment are: manual-to-manual, manual-to-automatic, automatic-to-manual, and automatic-to-automatic. Manual corresponds to operator or human intervention while automatic means machine only. The explanation describes an automatic-to-automatic example.

The calling unit, or originating fax, first transmits a calling tone (CNG) to indicate it is a non-speech terminal.

Figure 8-3 describes how to set up the modem to generate a 1100 Hz (CNG) tone. Figure 8-4 describes how to set up the modem to detect a 1100 Hz tone. The called unit, or answering fax, then responds with a called station ID (CED). Figure 8-5 and Figure 8-6 describe how to accomplish this task. The end of Phase A is signified after the called unit sends a 2100 Hz (CED) tone and the calling unit has detected this tone. Some facsimile manufacturers do not configure the modem to detect these tones. In this case, the modem looks for the preamble of flags (see Phase B).

8.1.2 Phase B

The pre-message procedure consists of the handshake. One machine sends an identification signal and the other machine responds with a command signal. A training check is sent at a high speed and the receiving machine informs the transmitting machine if the training check was successful. This usually occurs at V.21 300 bps Frequency Shift Keying (FSK) modulation in HDLC format.

HDLC stands for High level Data Link Control. It is a standard procedure used for data communications. HDLC is a bit-oriented protocol (normally used in synchronous communications) that defines how the data being sent over the data link is organized and arranged.

When using the HDLC protocol, the data is transmitted via frames. These frames organize the data into a format specified by an ISO (International Standards Organization) standard that enables the transmitting and receiving station to synchronize with each other. Figure 8-7 illustrates the HDLC frame structure used for the facsimile protocol.

The preamble is a series of HDLC Flags for one second ±15%. The purpose of the 7E flags is to condition the line. The flag sequence defines the beginning and ending of a frame. The address field is required to provide identification for multi-point addressing. For PSTN the format is 11111111. The control field's purpose is to provide the capability of encoding the commands and responses. The format is 1100X000 (X=0 non-final frame; X=1 final frame).

The HDLC information field provides the specific information for the control and message interchange between the two stations. In the fax protocol the format for the information field consists of two parts, the Facsimile Control Field (FCF) and the Facsimile Information Field (FIF).

The FCF contains information regarding the type of information being exchanged and the position in the overall sequence. The acronyms, functions, and format for FCF commands are defined in the T.30 Recommendation. The FIF contains additional information which further clarifies the facsimile procedure. Some examples of some information communicated with the FIF are: group capability, data rate, vertical resolution, coding scheme, recording width, recording length, and minimum scan line time.

The Frame Check Sequence (FCS) follows the FIF. The modem automatically generates the FCS or Cyclic Redundancy Check (CRC). The frame ends with an ending 7E flag. It is recommended that more than one ending flag be transmitted.

Figure 8-1. Basic Block Diagram of G3 Facsimile

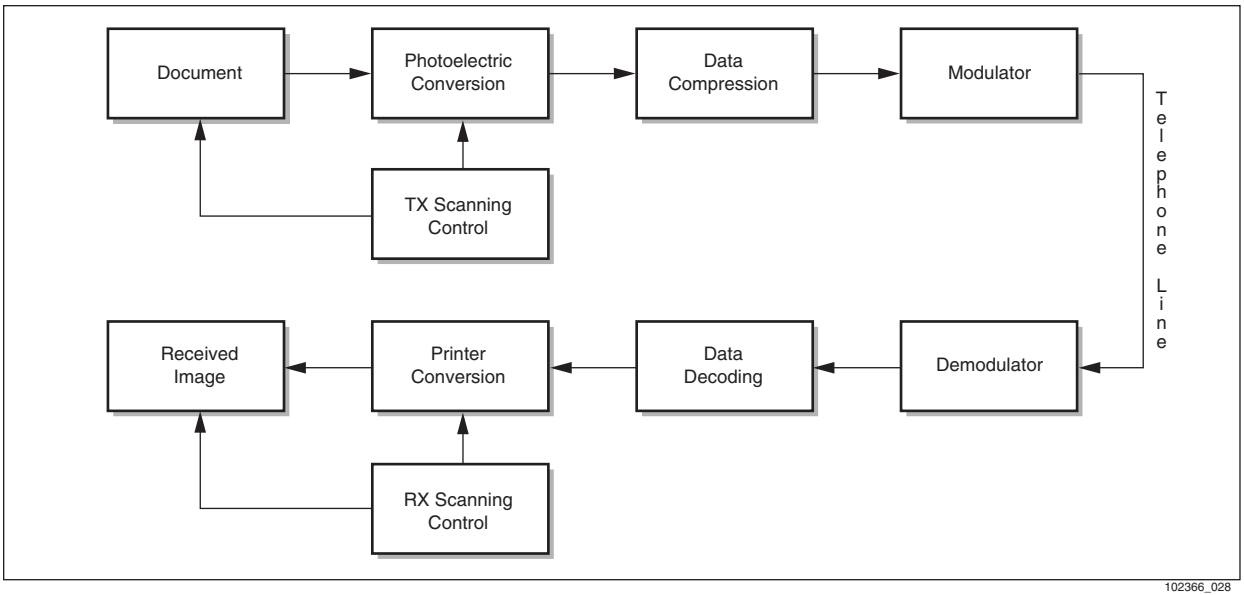


Figure 8-2. G3 Facsimile Procedure

CALLING UNIT	CALLED UNIT
CNG PHASE A	CALLING TONE: 1100 Hz, 0.5 SEC ON/0.3 SEC OFF INDICATE NON-SPEECH TERMINAL CED CALLED STATION ID: 2100 Hz, 2.6 SEC < ON < 4 SEC
DCS TCF PHASE B	DIS DIGITAL ID SIGNAL: 300 BPS FSK, HDLC FORMAT DIGITAL COMMAND SIGNAL: 300 BPS FSK, HDLC FORMAT TRAINING CHECK: HIGH SPEED TRAIN FOLLOWED BY 1.5 SEC OF ZEROS CONFIRMATION TO RECEIVE: 300 BPS FSK, HDLC FORMAT CFR
MESS PHASE C	TRANSMITS DOCUMENT
EOM PHASE D	END OF MESSAGE: 300 BPS FSK, HDLC FORMAT EOP, MPS OR PRI-Q MAY BE SENT MESSAGE CONFIRMATION: 300 BPS, HDLC FORMAT POST-MESSAGE RESPONSE OF MCF RTP, RTN, PIP OR PIN MAY BE SENT

102366_029

Figure 8-3. Transmit Calling Tone (CNG) (1100 Hz)

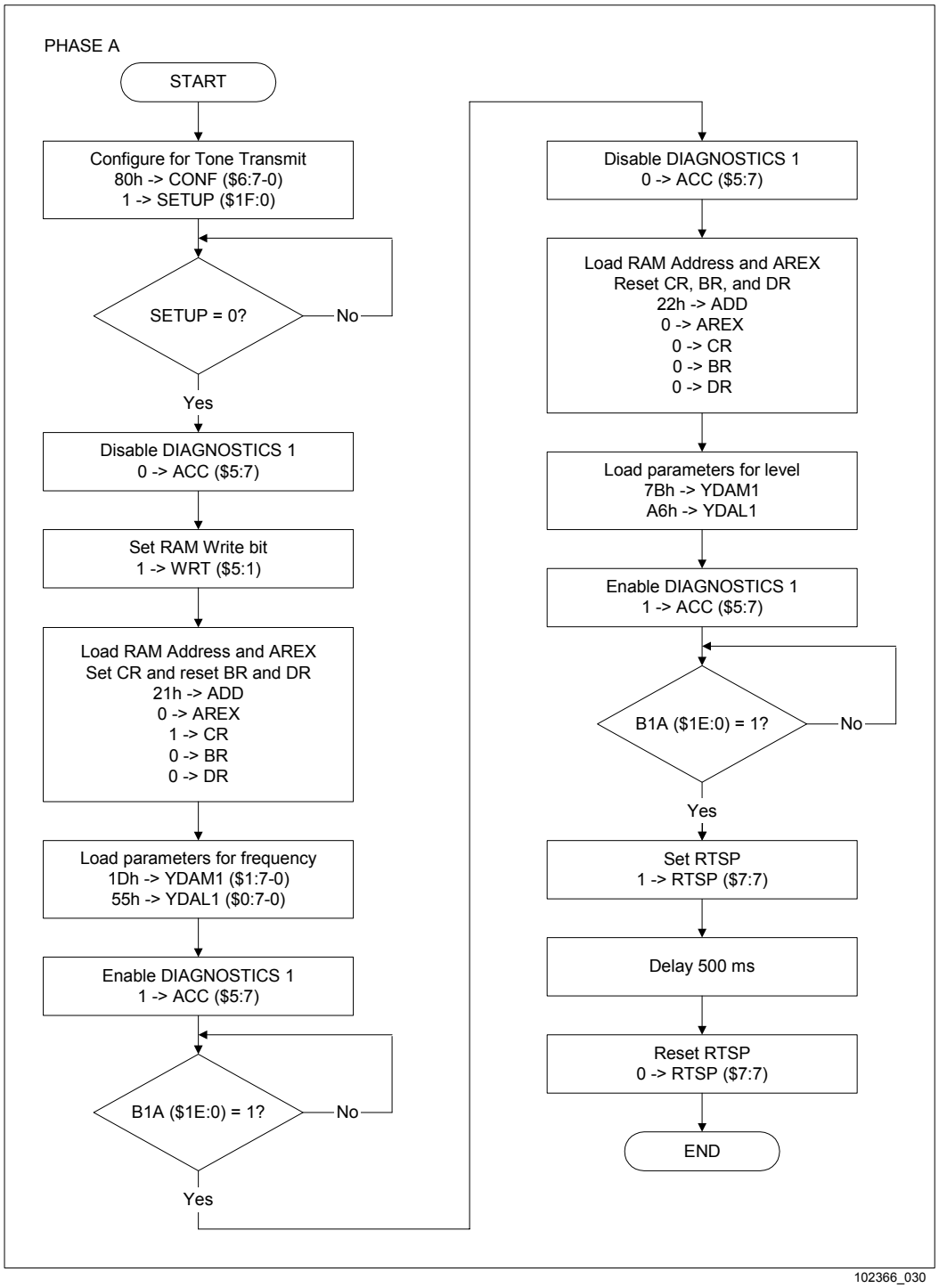


Figure 8-4. Detecting CNG Tone (1100 Hz)

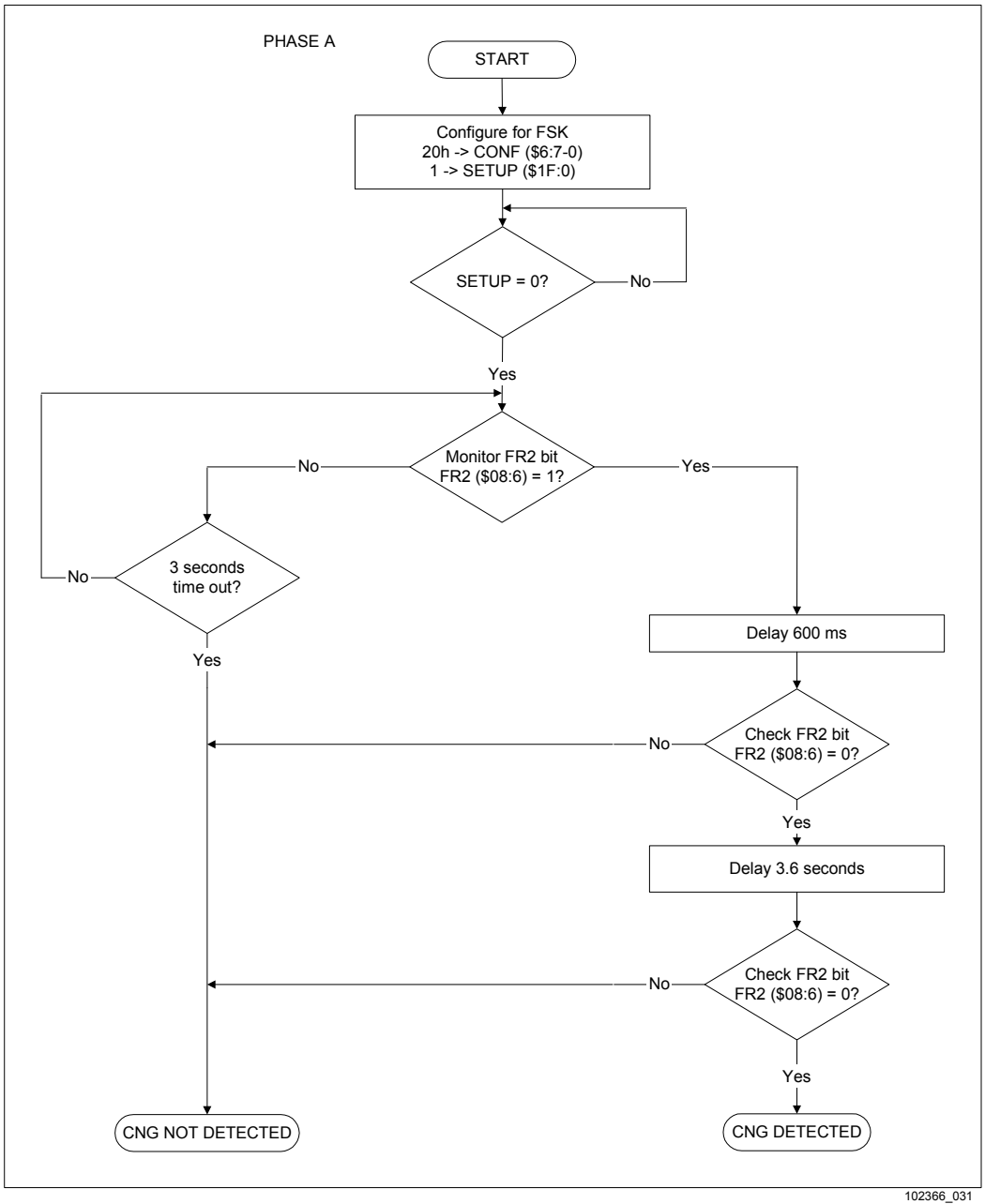


Figure 8-5. Transmit Called Tone (CED) (2100 Hz)

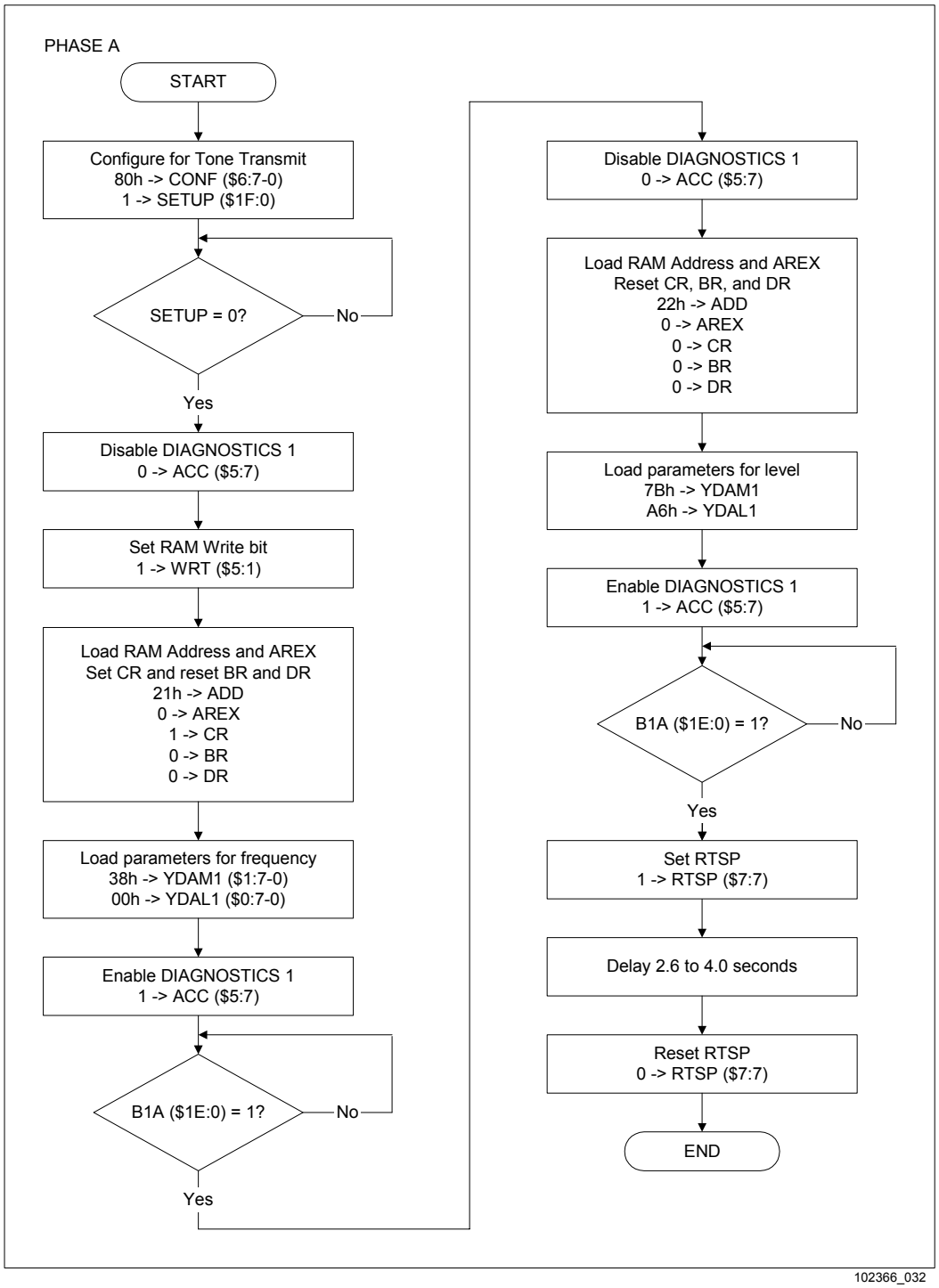


Figure 8-6. Detecting CED Tone (2100 Hz)

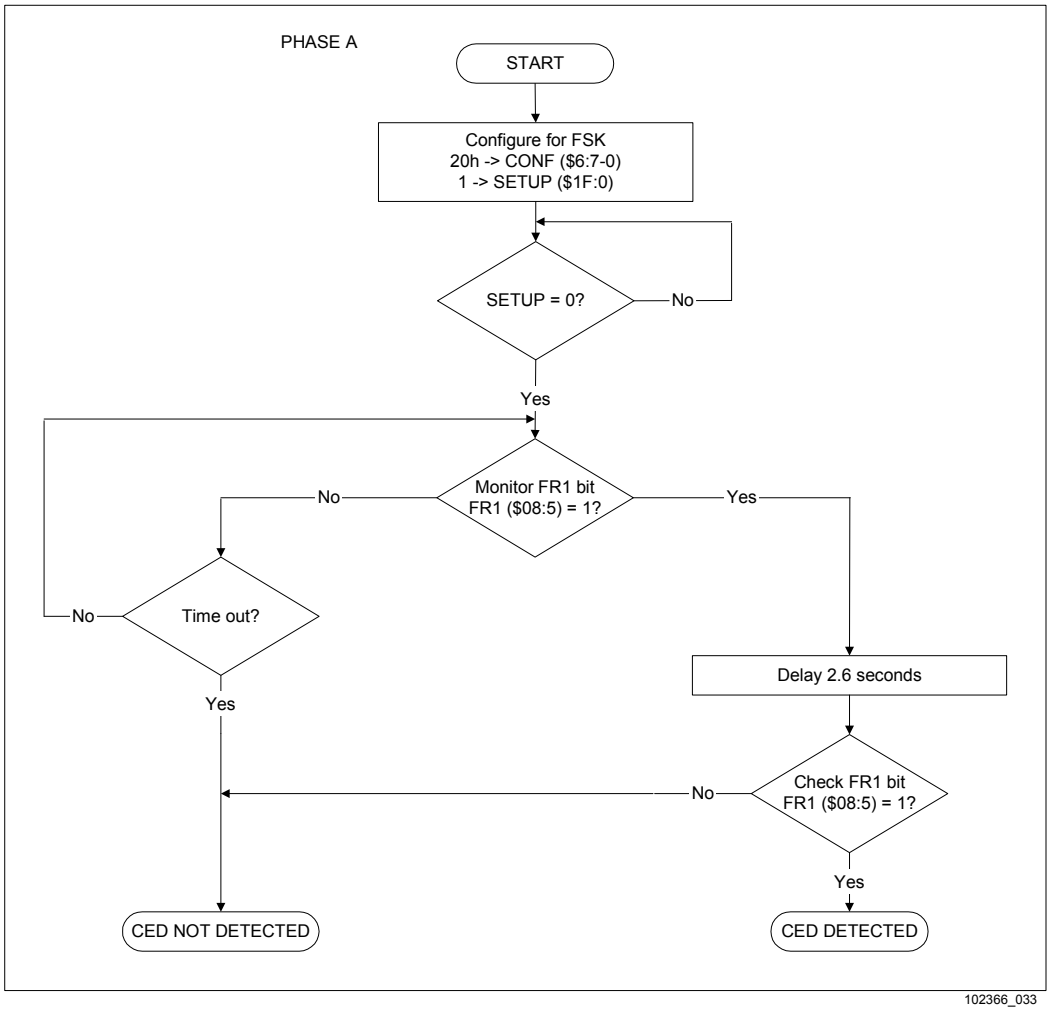
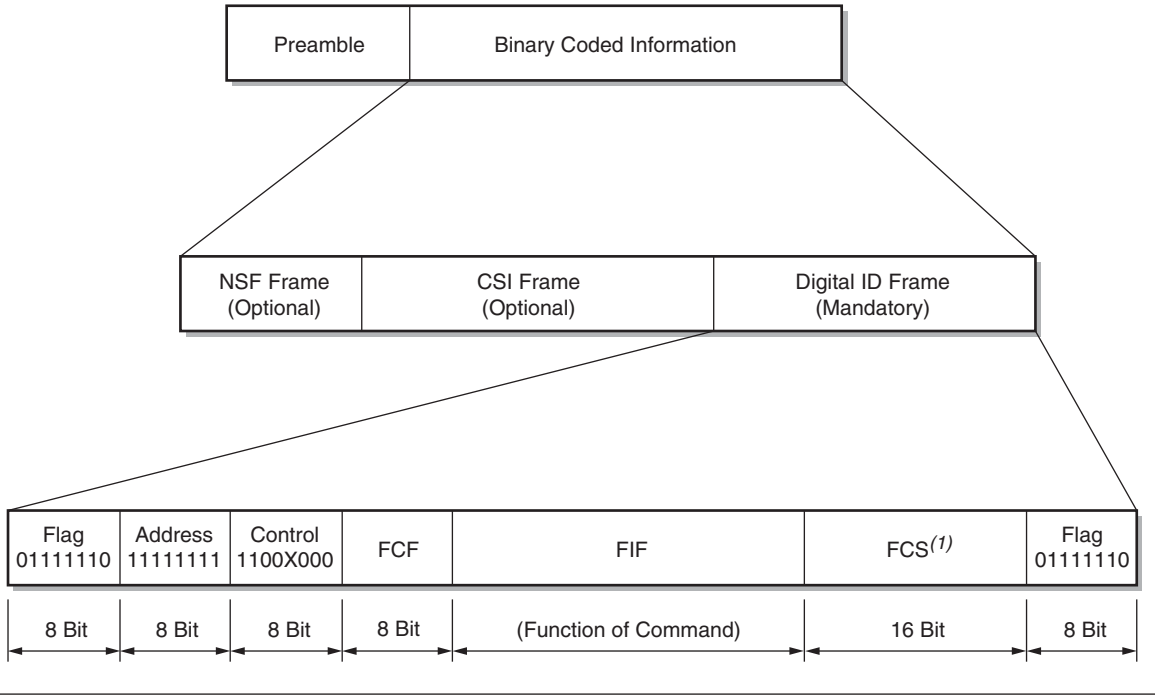


Figure 8-7. HDLC Frame Structure



NOTE(S):
(1) FCS: Frame Check Sequence; ITU-T V.41 CRC-16 is used.

102366_034

After the modem has been configured for FSK, the Digital Identification Signal (DIS) is transmitted by the called unit. The DIS informs the calling unit about the called unit's capabilities such as group capability (G1, G2, G3), data rate, vertical resolution, coding scheme (Modified Huffman, Modified Read), recording width, recording length, and minimum scan line time. The calling unit then responds with a Digital Command Signal (DCS) which informs the called unit which options are chosen to complete this facsimile call.

After the DCS is transmitted, both the calling unit and the called unit set up for the high speed configuration that was chosen and transmitted via the DCS. A Training Check (TCF) is transmitted by the calling unit to verify training and give an indication of channel acceptability for the selected data rate. The TCF consists of a series of zeros for 1.5 seconds ±10%. Since the called unit knows it will be receiving 1.5 seconds of zeros, the host can make a decision whether the line is good enough at the chosen data rate or fallback to a slower speed.

After completing the TCF, the calling unit and the called unit re-configures for FSK, HDLC format. The called unit then transmits either a Confirmation to Receive (CFR) or a Failure To Train (FTT). The CFR is a response informing the calling unit of a successful pre-message procedure completion. A FTT informs the calling unit that the training signal was rejected and requests re-training. If a FTT is received by the calling unit, the fax protocol jumps back to the transition of DCS and continues until finally a CFR is received or the calling unit host decides to terminate the call.

The fallback criterion based upon the modem performance information during TCF reception, for example, may consist of monitoring the number of bit errors or EQM number. If EQM is to be used as a fallback criterion for an acceptable BER performance,

the minimum metric EQM number should be used for V.17 mode and the hard decision EQM number should be used for V.29 and V.27 ter modes (see Table 4-1 for RAM access codes and Section 4 for scaling information). Refer to the EQM and BER vs. S/N charts. The EQM numbers shown in the charts are the decimal equivalent to the 16-bit hexadecimal numbers divided by 256.

During TCF, EQMs that represent acceptable BERs can be used to determine whether or not to fallback. If a fallback is necessary, EQM can be used to choose the appropriate fallback mode for a desired BER.

8.1.3 Phase C

Phase C occurs after both facsimile machines have set up for the high speed configuration decided upon in phase B. The T.30 Error Correction Mode is addressed in a following section. This high speed message information is usually compressed data using a Modified Huffman (MH) or Modified Read (MR) algorithm. The host processor must perform the MH or MR compression before loading the data into the modem. On the receive end, the host processor must perform the MH or MR decompression.

The start of phase C is denoted by an End Of Line (EOL) 8-bit code. The data follows this first EOL character until the end of the line. Another EOL character is transmitted to indicate a new line. A minimum transmission time of a total coded scan line is measured from the beginning of the EOL to the beginning of the following EOL. If the transmitted data requires less time than the minimum transmission time, fill bits must be transmitted. Six consecutive EOL character constitute a Return To Control (RTC) command meaning end of document transmission. Figure 8-8 illustrates the phase C format.

8.1.4 Phase D

The post-message phase D procedure uses FSK and HDLC format. The calling station will typically send an End Of Message (EOM) signal. This FCF command (EOM) informs the called station that this is the end of the page and return to Phase B. A Multi-Page Signaling (MPS) or End Of Procedure (EOP) signal may be sent instead of EOM. The MPS signal informs the called unit that there are more pages in this facsimile transmission. EOP signals the end of the facsimile transmission. Procedure Interrupt-EOM (PRI-EOM), Procedure Interrupt-MPS (PRI-MPS), and Procedure Interrupt-EOP (PRI-EOP) indicate the same as EOM, MPS, and EOP, respectively, with the additional optional capability of requesting operator intervention. If operator intervention is required, further facsimile procedures commence at the beginning of phase B.

The called station might respond to an EOM, MPS, or EOP signal with a Message Confirmation (MCF) command. This FCF command indicates to the calling unit that the complete message was received. One of the following FCF commands may be sent instead of the MCF: Re-Train Positive (RTP), Re-Train Negative (RTN), Procedure Interrupt Positive (PIP), or Procedure Interrupt Negative (PIN). RTP indicates that a complete message has been received and that additional messages may follow after retransmission of TCF and CFR. RTN indicates that the previous message has not been satisfactorily received, however, further receptions may be possible provided there is a retransmission of TCF and CFR. PIP and PIN indicate that the previous message was received satisfactorily or not satisfactorily, respectively, and operator intervention is required for further transmissions.

8.1.5 Phase E

Call Release, or phase E, occurs after the last post-message signal of the procedure or under certain conditions such as a time-out, procedural interrupt, or a Disconnect (DCN) command. The DCN command indicates the initiation of phase E. This command requires no response.

Figure 8-9 through Figure 8-15 illustrate how to implement certain phase B procedures. The examples show how the modem can be set up using the internal HDLC framing capabilities.

Figure 8-9 describes how to transmit FSK/HDLC signals such as DIS, DCS, DTC, CFR, FTT, etc. Three subroutines are called out: the low speed configuration, the transmit preamble, and interrupt-driven transmit routine. A Programmable Interrupt set-up is required in the receiver to determine if it is the end of the frame and if the frame was received correctly. See Figure 8-10 for setup instructions. The Low Speed Configuration subroutine is shown on Figure 8-11. Since the HDLC function is being used, the parallel data mode is enabled. The Transmit Preamble routine is shown on Figure 8-12. When the modem is configured in HDLC mode by setting RTSP, the modem will automatically transmit flags. The Interrupt-Driven Transmit routine is illustrated in Figure 9-13.

The hardware IRQn pin must be monitored for interrupts. The IRQn pin will become active (go low) when the modem is ready for a byte of data. This data should be loaded into the Data Buffer Register, DBUFF. When the IRQn returns low, the modem is ready for the next byte of data.

Figure 8-14 describes how to receive FSK/HDLC signals. The Interrupt-Driven Low Speed Receive routine is shown on Figure 8-15.

After IRQn is low, the Buffer 2 Available (B2A) bit is polled to determine if the next byte must be read by the host. If B2A is a 0, the Programmable Interrupt Request (PIREQ) bit is polled to determine if one of the programmable interrupt bits caused the interrupt. If Abort/Idle (ABIDL) is a 1, then an abort or idle sequence is being received. If ABIDL is a 0, then a Return from Subroutine is executed and the End of Frame bit is checked to see if it is the end of the frame. The Cyclic Redundancy Check (CRC) bit is looked at to determine if the current frame was received correctly. Figure 8-16 shows how to re-configure the modem to a high speed configuration. This procedure will be used again when entering phase C. Figure 8-17 describes how to transmit the TCF or one second of zeros. Figure 8-18 describes the High Speed Message Transmission. This procedure is similar to the Low Speed Message Transmission. The High Speed Configuration is located at Figure 8-16.

The High Speed Interrupt-Driven Transmit routine is in Figure 8-19. This is also similar to the low speed procedure.

The High Speed Message Reception procedure is illustrated in Figure 8-20. The High Speed Interrupt-Driven Receive subroutine is in Figure 8-21. Included in the High Speed Message Reception procedure is an optional Ensure Valid Train subroutine (Figure 8-22). This procedure is recommended to ensure that a valid training sequence is accomplished when noise is above the CDET turn-on threshold.

Figure 8-8. Phase C Format

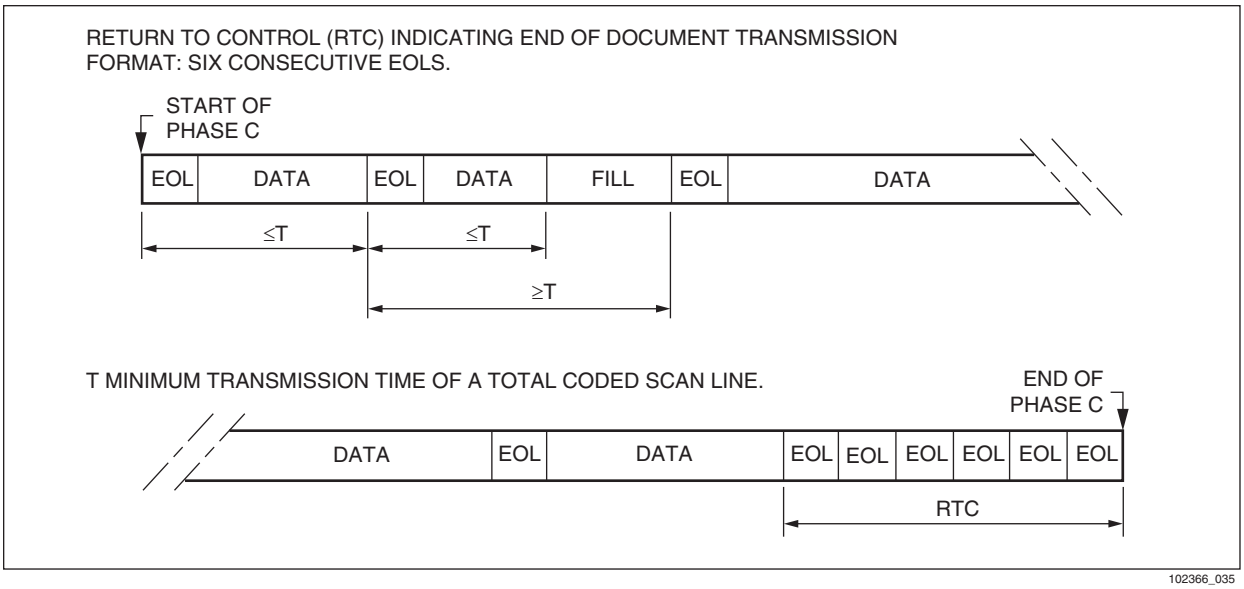


Figure 8-9. Transmit FSK/HDLC Signals

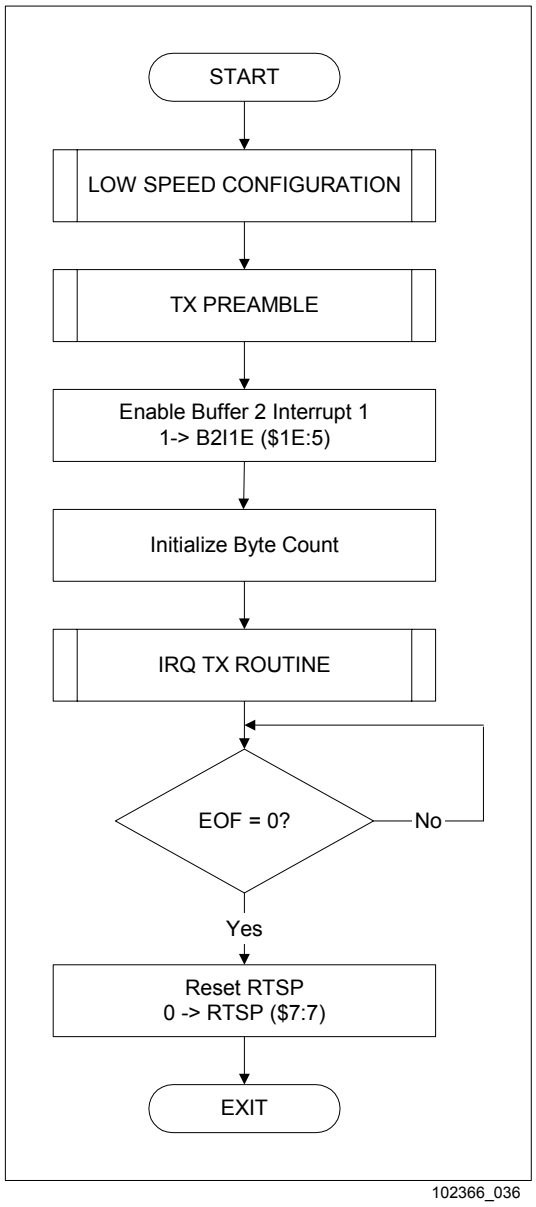


Figure 8-10. Setup for Programmable Interrupt

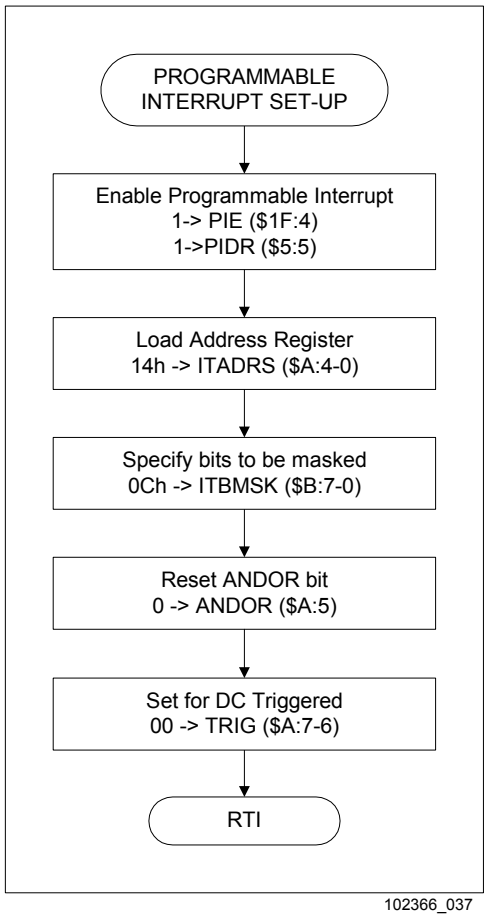


Figure 8-11. Low Speed Configuration Subroutine

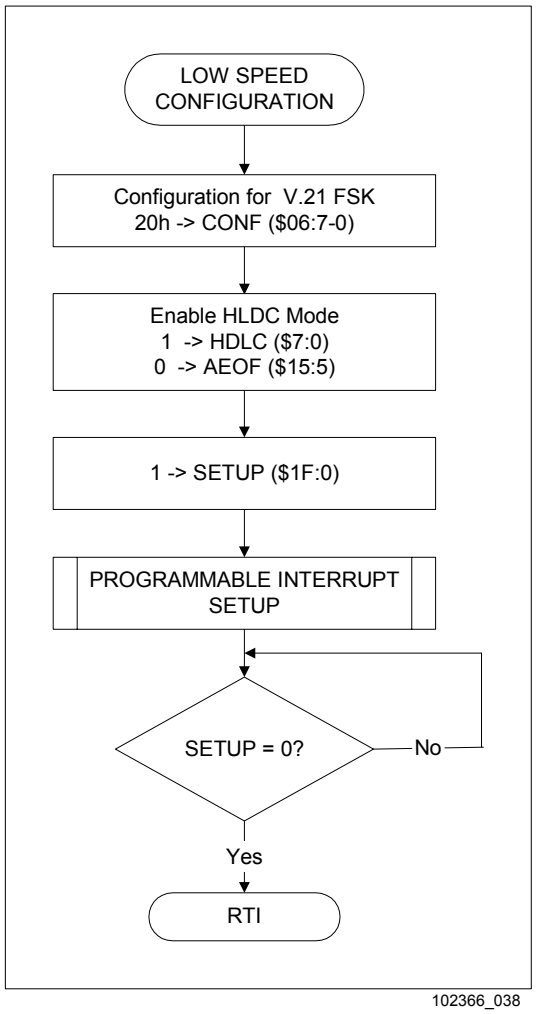


Figure 8-12. Transmit Preamble

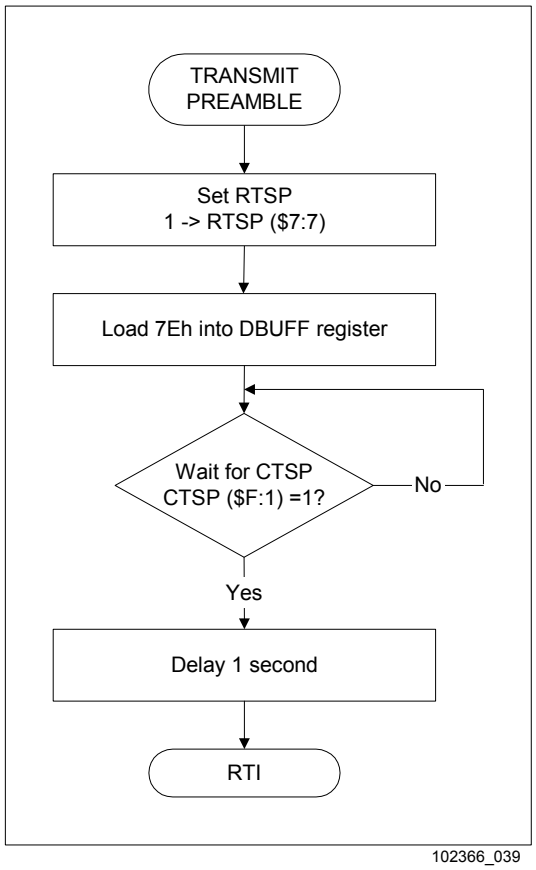


Figure 8-13. Low Speed Interrupt-Driven Transmit

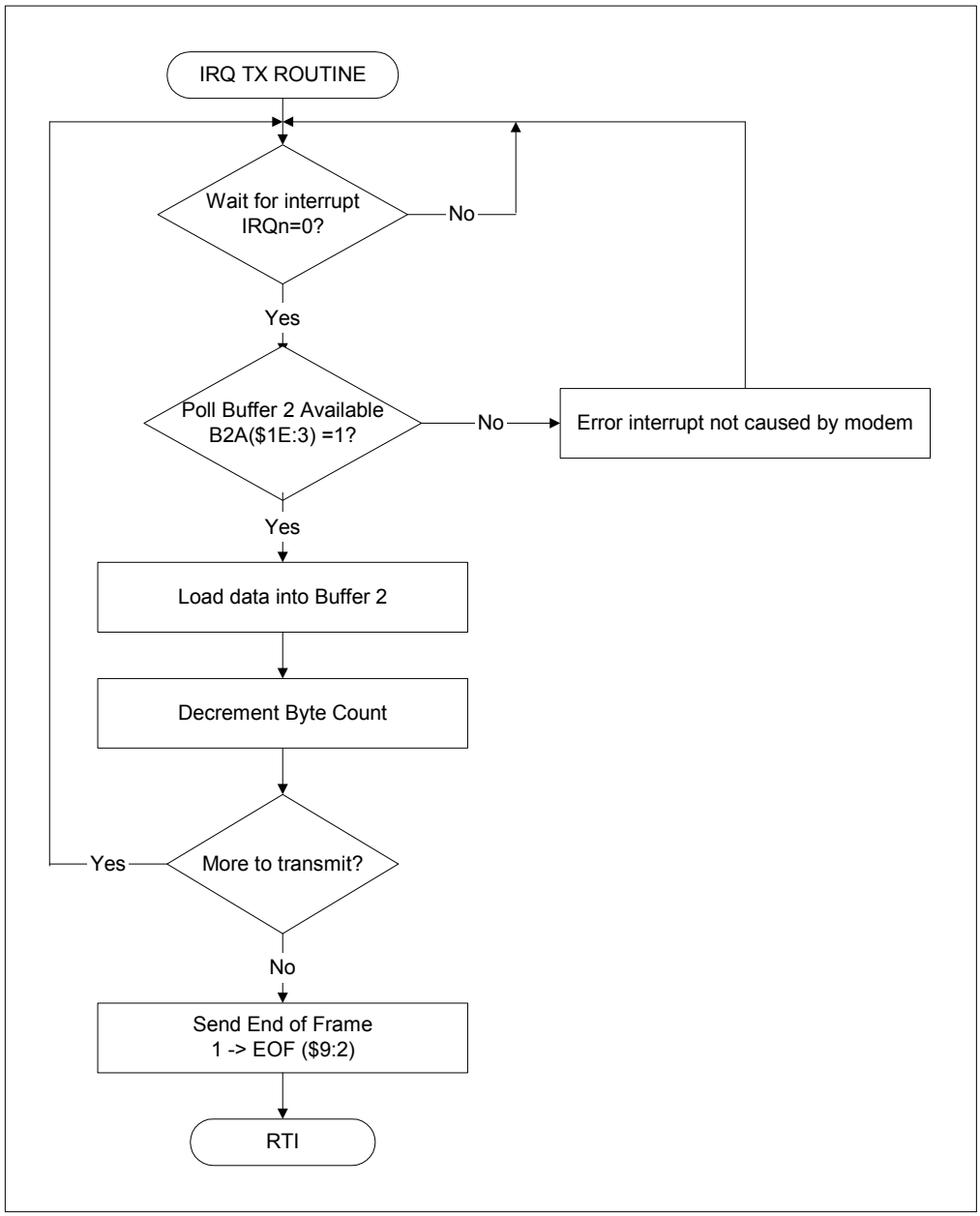


Figure 8-14. Receive FSK/HDLC Signals

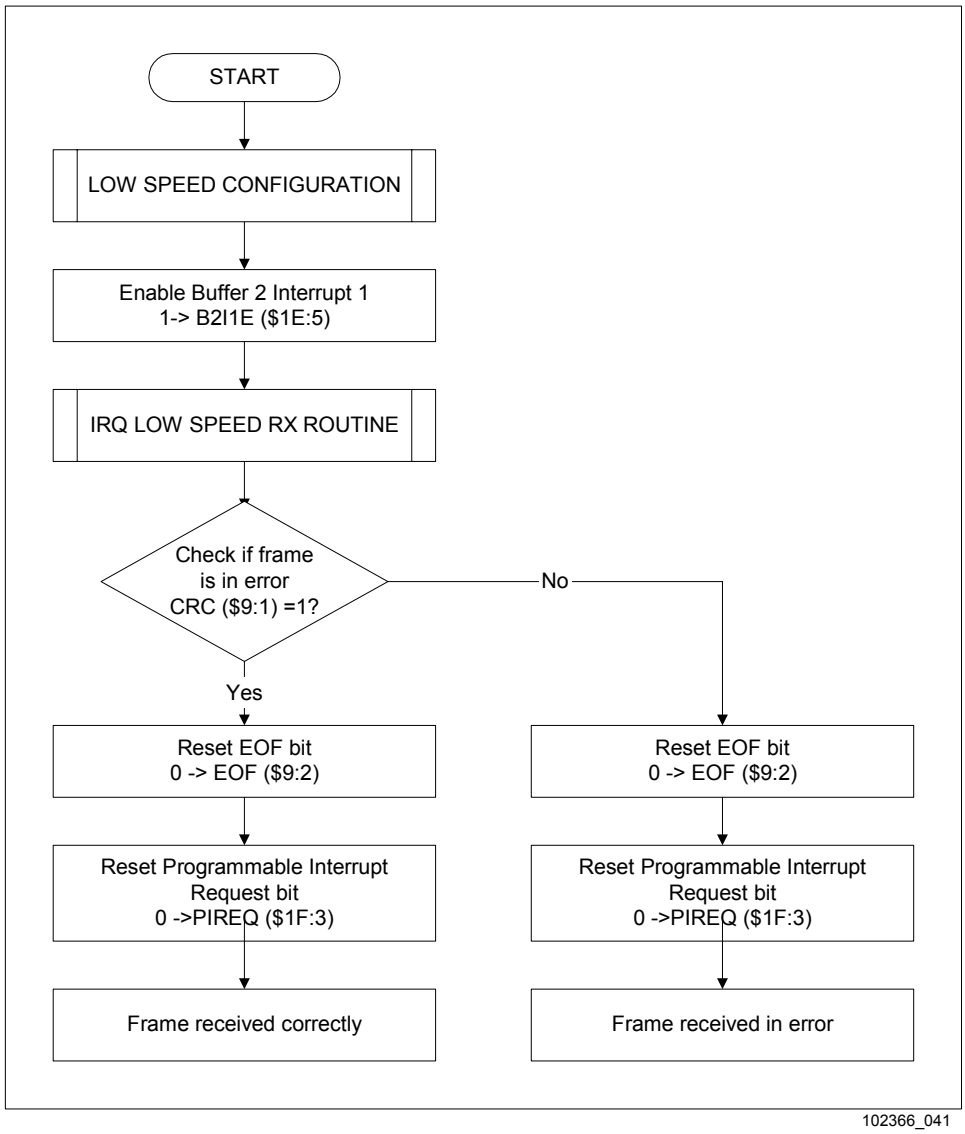


Figure 8-15. Low Speed Interrupt-Driven Receive

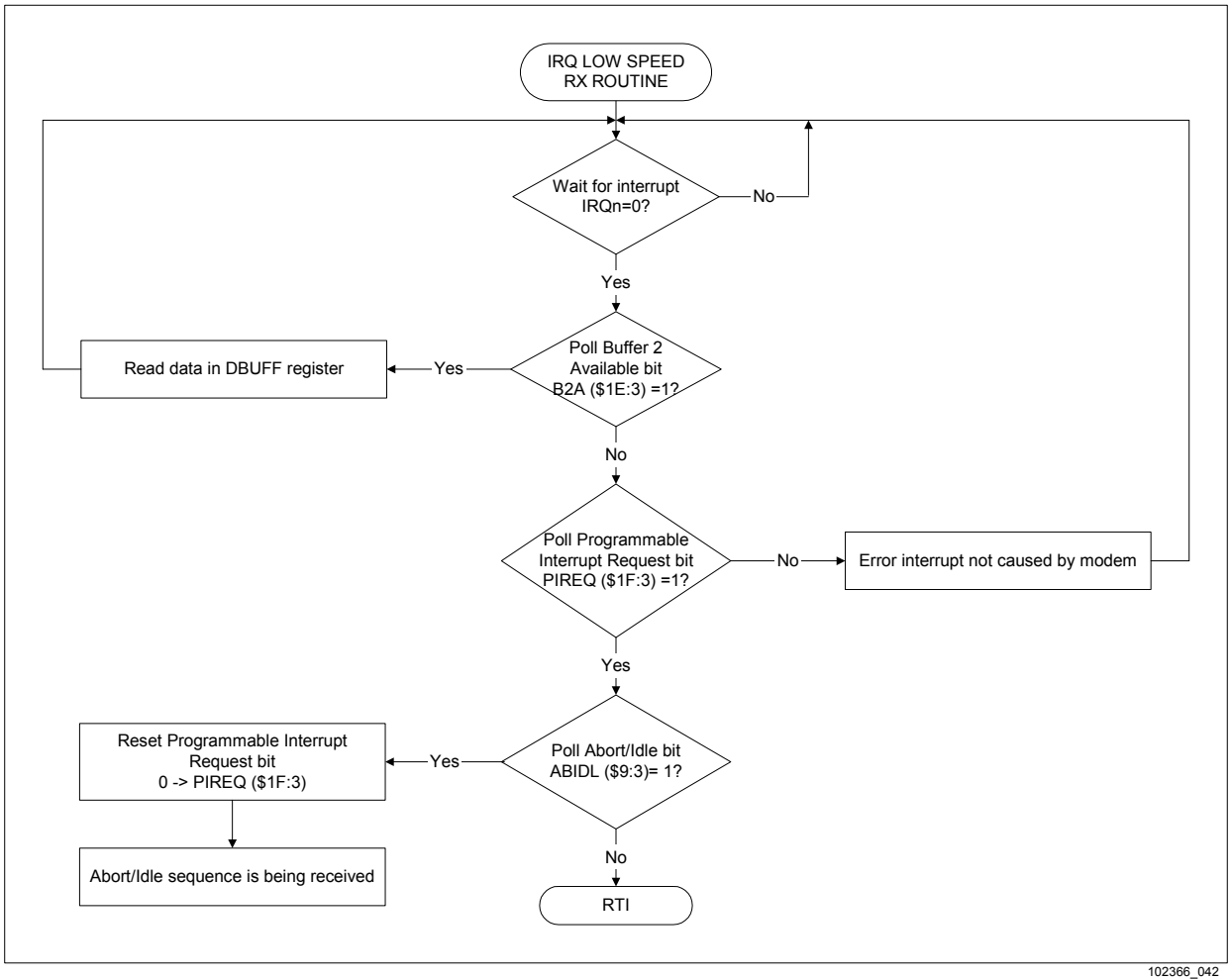


Figure 8-16. High Speed Configuration Setup

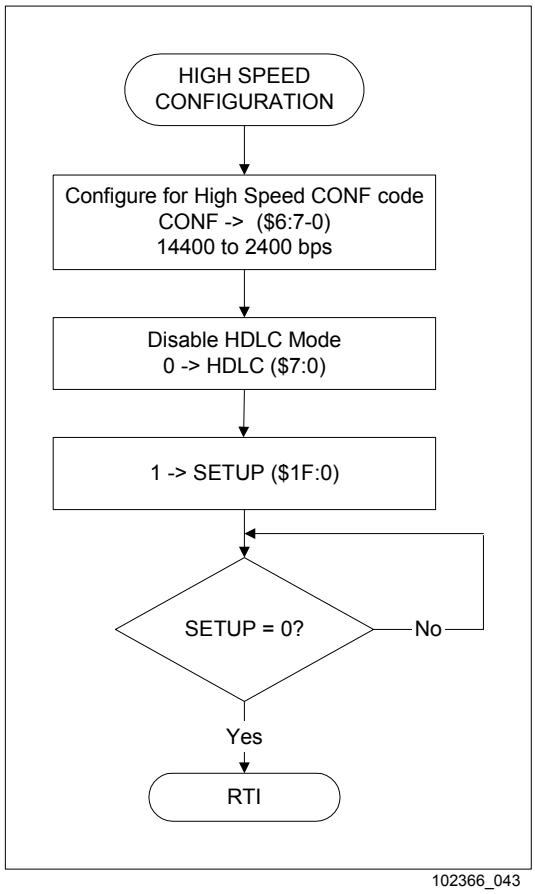


Figure 8-17. Transmitting TCF

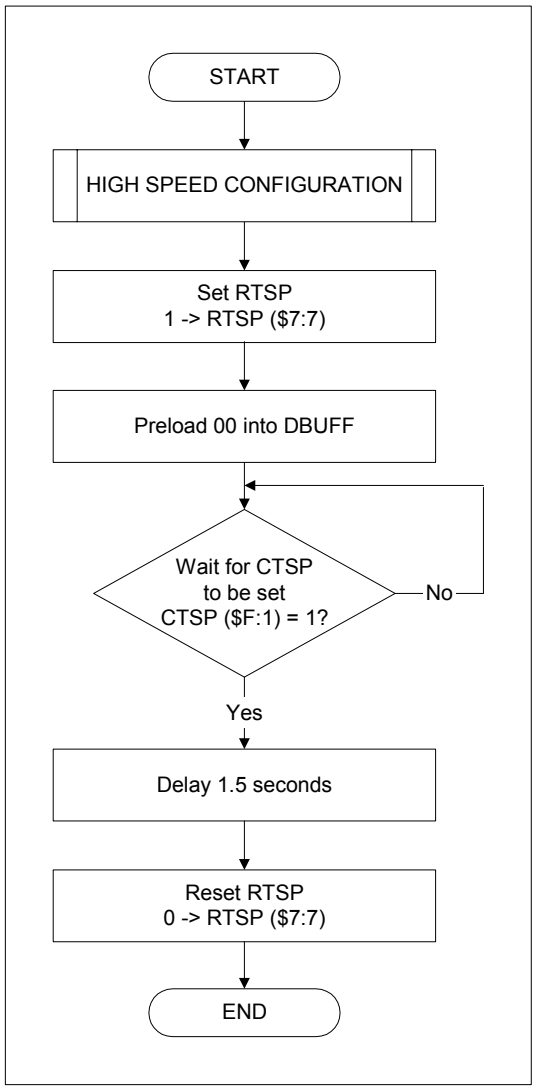


Figure 8-18. High Speed Message Transmission

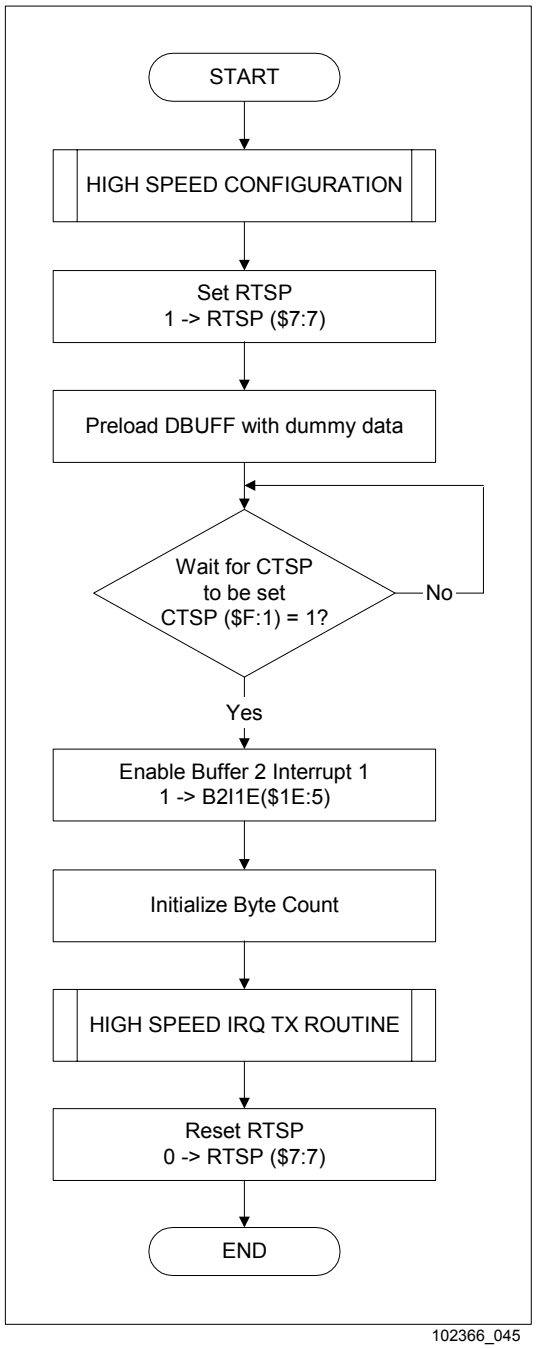


Figure 8-19. High Speed Interrupt-Driven Transmit

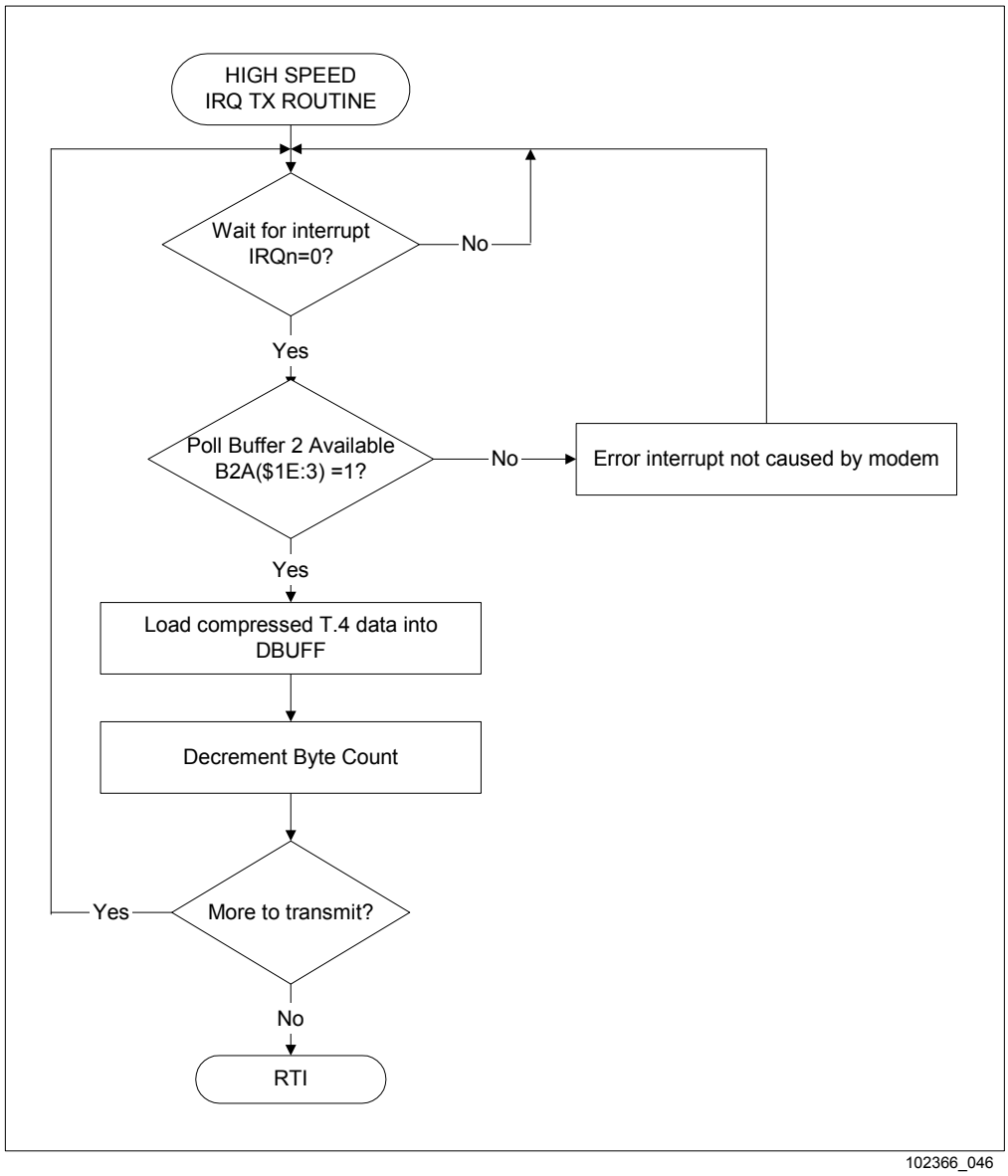


Figure 8-20. High Speed Reception Setup

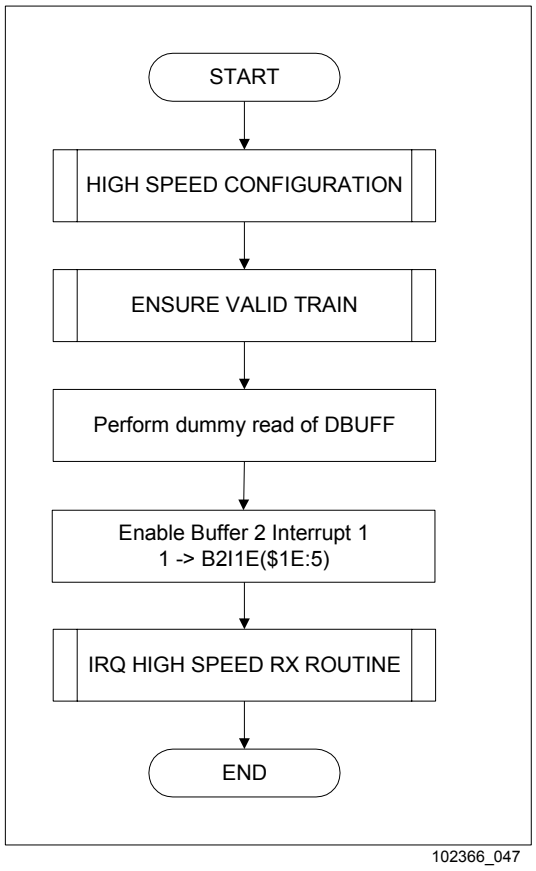


Figure 8-21. High Speed Interrupt Driven Receive

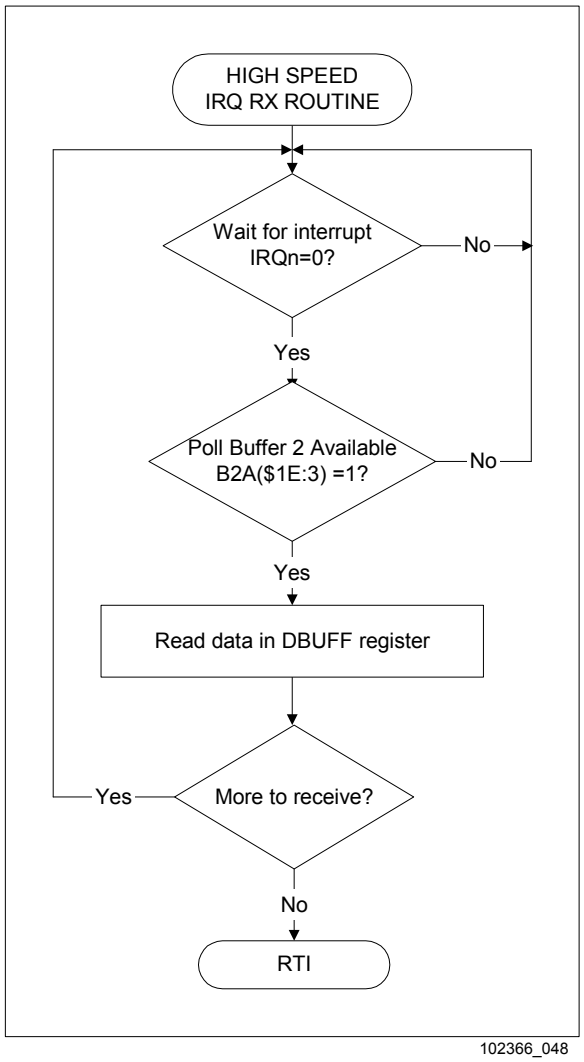
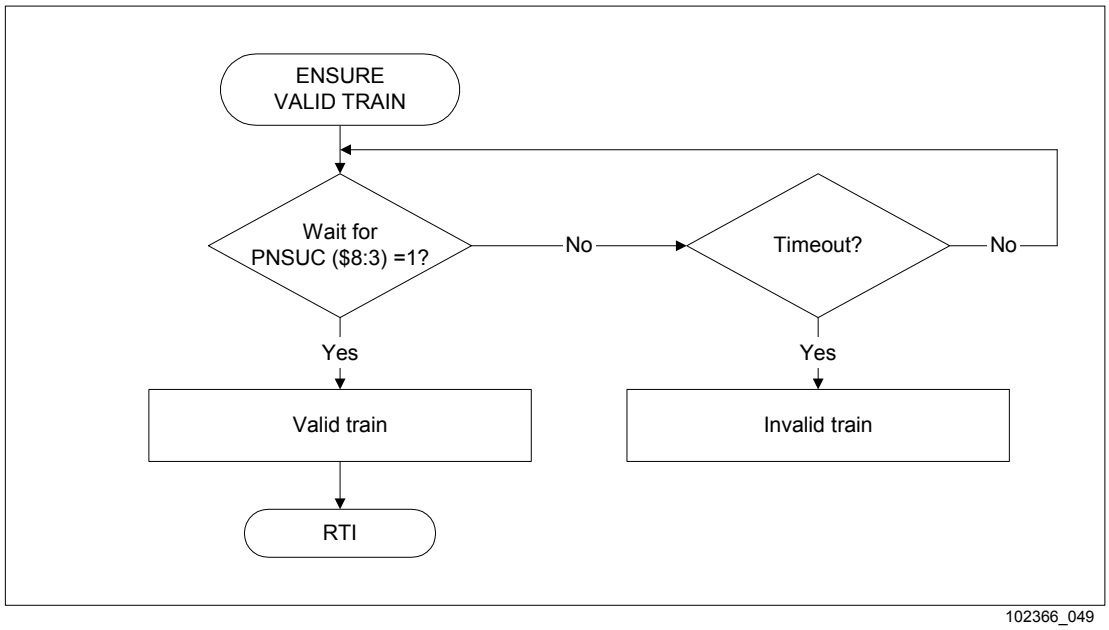


Figure 8-22. Valid Training Sequence Check



8.2 Error Correction Mode

8.2.1 General

The revised T.30 contains an Error Correction Mode (ECM) option. The ECM allows the phase C portion of the facsimile transmission to be encoded in a HDLC framing format using a specified number of bits in the information field. The transmitted high speed message is broken up into a number of frames identified by frame numbers. If an error is detected during reception of the message, the called station records the frame number. After all the frames in the message has been received, the called station transmits the frame numbers that were received in error. The calling station then re-transmits only those frames in error. This continues until the entire message is received error free or the calling station decides not to transmit any more frames.

The error detection is performed by comparing the CRC or FCS. Using ECM, the data rate can be as fast as 14,400 bps, therefore, the host microprocessor cannot keep up implementing HDLC without the use of a serial I/O device. The modem provides HDLC features at speeds up to 14,400 bps.

8.2.2 ECM Frame Structure

In Error Correction Mode, one frame of facsimile data consists of 256 or 64 octets of data. Each page may contain 1 to 256 frames. Also, 1 to 256 pages may be transmitted. The ECM frame structure is illustrated in Figure 8-23. Following the high speed training sequence, the flag, address field, and control field is transmitted. In ECM, Flag = 7E, Address = FF, and Control = B0. The Facsimile Control Field for the Facsimile Coded Data block (FCD) is 60. The frame number follows the FCF for FCD, followed by the facsimile data. Pad bits such as EOL, Tag, and Align bits follow the facsimile data. Finally, the FCS check and the ending flag is transmitted.

After 256 frames, a Return Control for Partial page (RCP) block is transmitted three times. The RCP block consists of the same Flag, Address Field, and Control field followed by the FCF for RCP. The FCS immediately follows with the ending flag. After the third RCP, a maximum of 50 ms of flags are transmitted.

An ECM message protocol example is shown in Figure 8-24. The bold arrows are high speed transmissions and the other arrows are FSK transmissions. The example is self-explanatory. If more information is needed, refer to the T.30 ECM specification.

In this paragraph the Q refers to the NULL, EOP, MPS, or EOM Facsimile Control Field commands. The Partial Page Signals (PPS-Q) and Partial Page Request (PPR) frame structures are shown in Figure 8-25. The PPS-Q frame begins with the same Flag, Address field, and Control field. Two FCF commands follow. The first FCF transmitted is to indicate PPS. The second FCF is either NULL, EOP, MPS, or EOM. The page count followed by the block count, followed by the total number of frames in the block are transmitted next. The FCS and ending flag are finally transmitted.

The PPR frame structure also begins with the same Flag, Address, and Control field. The FCF for PPR is the next octet. The FIF consists of 256 or 64-bits depending on how many frames were transmitted. The contents of FIF is either a 0 or a 1. The bit number corresponds to the frame number and a 0 indicates the frames was received correctly and a 1 indicates an incorrect frame was received.

Figure 8-23. ECM Frame Structure

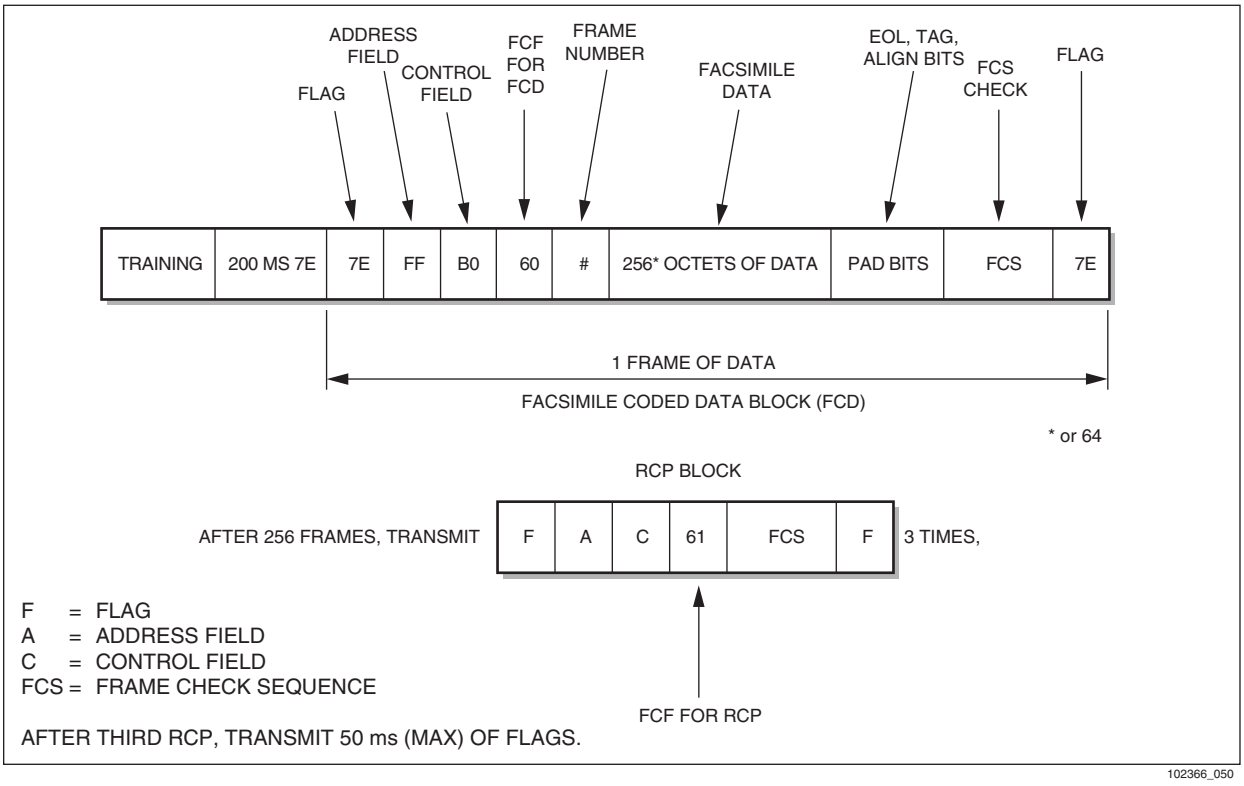


Figure 8-24. ECM Message Protocol Example

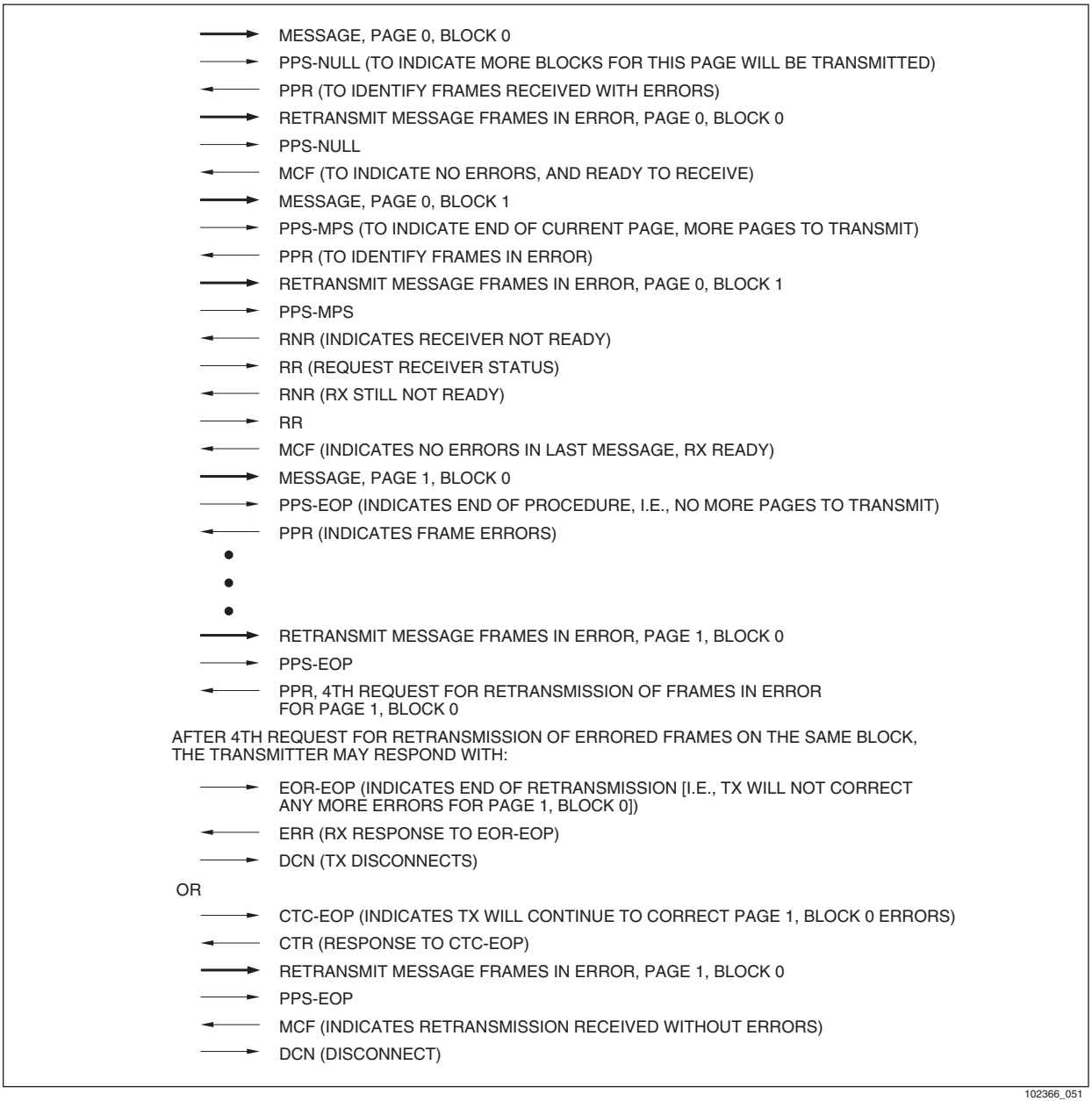
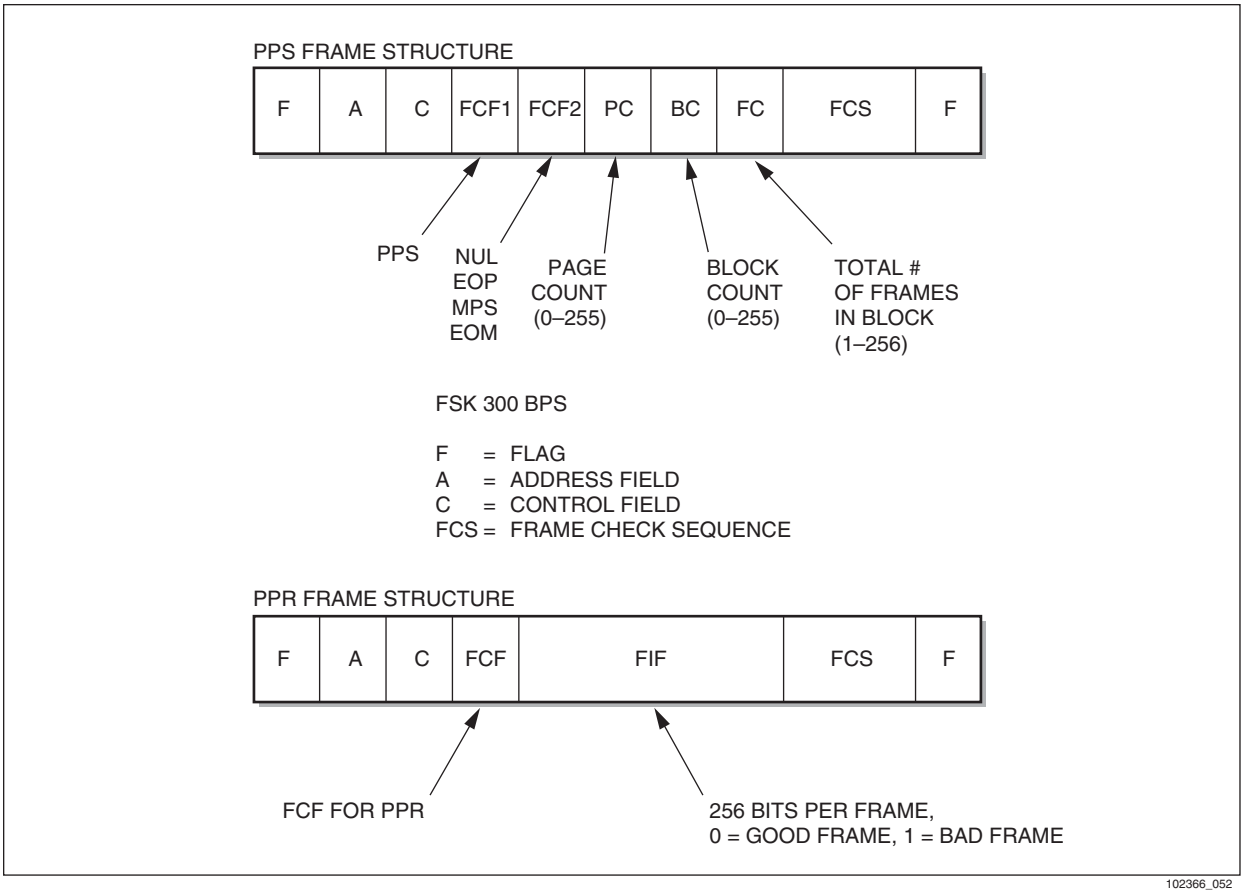


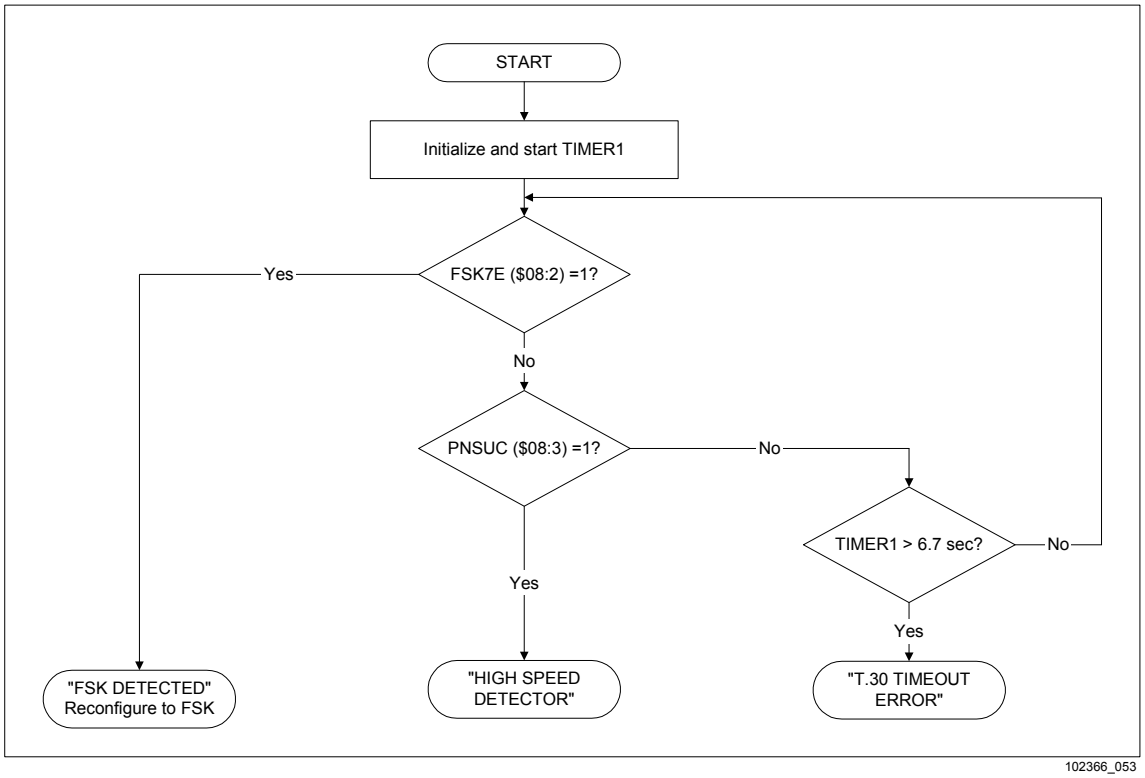
Figure 8-25. PPS and PPR Frame Structure



8.3 Signal Recognition Algorithm

A method of determining whether a high speed message or V.21 Channel 2 FSK handshaking is being received by the modem is necessary when implementing the T.30 recommendation. When the calling unit transmitter and called unit receiver configure for V.17, V.29, or V.27 ter, sometimes the high speed message may not be received (typically due to a noisy line). In this case, the calling unit transmitter will try to send the message up to three times before re-negotiating in FSK signaling. The called unit receiver must, therefore, be able to distinguish between a high speed message and FSK handshaking. This algorithm is shown in Figure 8-26.

Figure 8-26. Signal Recognition Algorithm in High Speed Mode



9. Caller ID

Calling Number Delivery (CND), known as Caller ID, is a telephone service intended for residential and small business customers. It allows the called Customer Premises Equipment (CPE) to receive a calling party's directory number and the date and time of the call during the first silent interval in the ringing cycle. The customer must contact a Bellcore Client Company to initiate CND service.

All of this CND information, according to Bellcore, is sent between the first and the second ring and starts as early as 300 ms after the first ring burst and ends at least 475 ms before the second ring burst.

The following information summarizes the CND information provided by Bellcore.

9.1 Parameters

The data signaling interface has the following characteristics:

Link Type:	2-wire, simplex
Transmission Scheme:	Analog, phase-coherent FSK
Logical 1 (mark):	1200 ±12 Hz
Logical 0 (space):	2200 ±22 Hz
Transmission Rate:	1200 bps
Transmission Level:	-13.5 ±1 dBm into 600 Ω load

9.2 Protocol

The protocol uses 8-bit data words (bytes), each bounded by a start bit and a stop bit. The CND message uses the Single Data Message format shown below.

Channel Seizure Signal	Carrier Signal	Message Type Word	Message Length Word	Data Word(s)	Checksum Word

9.2.1 Channel Seizure Signal

The channel seizure signal is 30 continuous bytes of 55h (01010101). This provides a detectable alternating function to the modem.

9.2.2 Carrier Signal

The carrier signal consists of 130±25 ms of mark (1200 Hz) to condition the receiver for data.

9.2.3 Message Type Word

The message type word indicates the service and capability associated with the data message. The message type word for CND service is 04h (00000100).

9.2.4 Message Length Word

The message length word specifies the total number of data words to follow.

9.2.5 Data Words

The data words are encoded in ASCII and represent the following information:

The first two words represent the month.

The next two words represent the day of the month.

The next two words represent the hour in local military time.

The next two words represent the minute after the hour.

The calling party's directory number is represented by the remaining words in the data word field. If the calling party's directory number is not available to the terminating central office, the data word field contains an ASCII "O". If the calling party invokes the privacy capability, the data word field contains an ASCII "P".

9.2.6 Checksum Word

The Checksum word contains the twos complement of the modulo 256 sum of the other words in the data message (message type, message length, and data words). The receiving equipment may calculate the modulo 256 sum of the received words and add this sum to the received checksum word. A result of zero generally indicates that the message was correctly received. Message retransmission is not supported.

9.2.7 Example CND Single Data Message

An example of a received CND message, beginning with the message type word is as follows:

04 12 30 39 33 30 31 32 32 34 36 30 39 35 35 35 31 32 31 32 51

04h = Calling number delivery information code (message type word)

12h = 18 decimal; Number of data words (date, time, and directory number words)

ASCII 30, 39 =09; September

ASCII 33, 30 = 30; 30th day

ASCII 31, 32 = 12; 12:00 PM

ASCII 32, 34 = 24; 24 minutes (12:24 PM)

ASCII 36 30 39 35 35 35 31 32 31 32 = 609-555-1212; calling party's directory number.

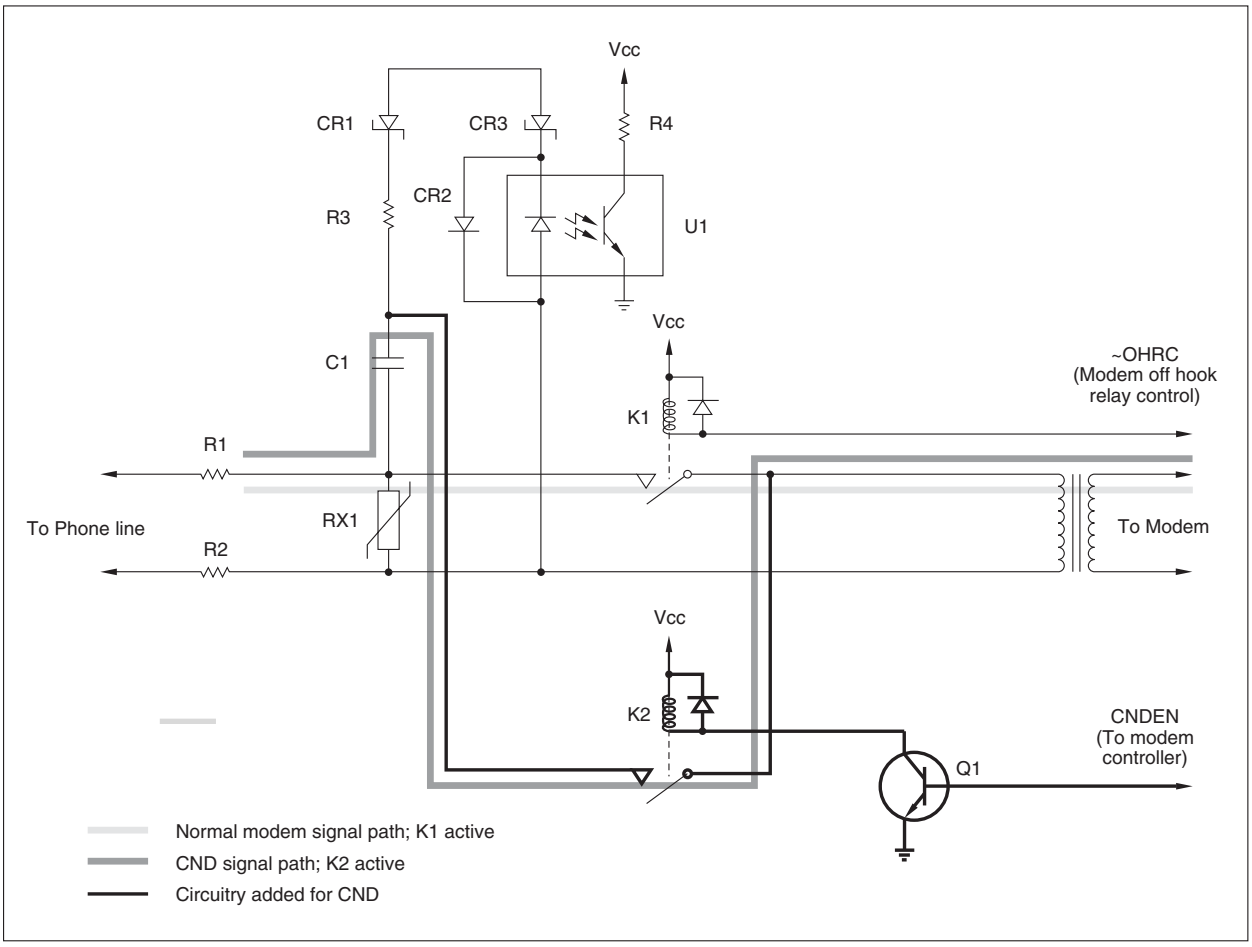
51h = Checksum Word.

9.3 DAA Requirements

To receive CND information, the modem monitors the phone line between the first and second ring bursts without causing the DAA to go off hook in the conventional sense, which would inhibit the transmission of CND information by the local central office. A simple modification to an existing DAA circuit (Figure 9-1) easily accomplishes the task.

With the addition of Q1 and K2, the DAA is AC-coupled to the phone line through the ring detect capacitor, C1, allowing the CND signal to pass to the modem while blocking DC loop current that would place the line off hook.

Figure 9-1. DAA Circuit Supporting CND



9.4 Modem Requirements

Although the data signaling interface parameters match those of a Bell 202 modem, the receiving CPE need not be a Bell 202 modem. A V.23 1200 bps modem receiver may be used to demodulate the Bell 202 signal.

The ring detection circuit, combined with a "Ring Detection" firmware routine done by the host, allows the host to activate and deactivate the CNDEN relay to monitor the telephone line for receiving the CND information.

After a valid ring is detected, the RI bit is set to indicate occurrence of the first ring burst to the host. The host waits for 250 ms of silence then activates the CNDEN line (see Figure 9-1) and configures the modem for CND reception as follows:

CONF = 22h

SETUP = 1 and wait until SETUP = 0

Wait until CDET = 1

The received data is now available via DBUFF ($10:7-0).

CNDEN must be deactivated by the host prior to the reception of the second ring burst.

9.5 Applications

Flowcharts corresponding to the above process are shown in Figure 9-2.

Once CND information is received, the user may process the information in a number of ways.

1. The date, time, and calling party's directory number can be displayed.
2. Using a look-up table, the calling party's directory number can be correlated with his or her name and the name displayed.
3. CND information can also be used in additional ways such as for:
   - **a)** Bulletin board applications,
   - **b)** Black-listing applications,
   - **c)** Keeping logs of system user calls, or
   - **d)** Implementing a telemarketing data base.

9.6 References

For more information on Calling Number Delivery (CND), refer to Bellcore publications TR-TSY-000030 and TR-TSY-000031.

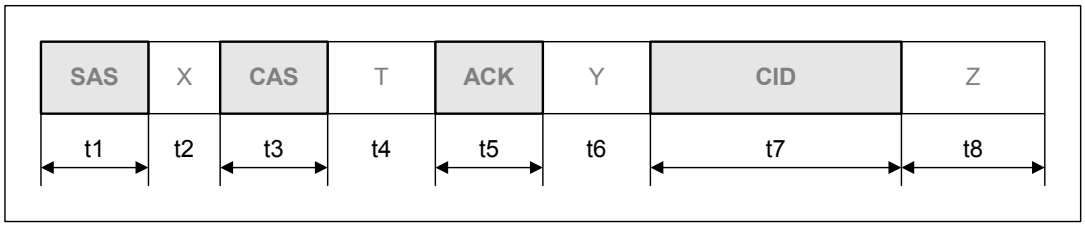
To obtain Bellcore documents, contact:

Bellcore Customer Service
60 New England Avenue, Room 1B252
Piscataway, NJ 08834-4196
(201) 699-5800

9.7 Type II Caller ID

Type II Caller ID CAS detection operates concurrently with three tone detectors. Status bit CASD ($08:3) is set by the modem when the CAS dual-tone Type II Caller ID signal is detected and configured to CAS Detection Mode (90h). After CASD is set and CAS signal detected, the host must reset status bit CASD to allow subsequent Type II Caller ID CAS signals to be detected.

Type II Caller ID provides the calling party's identity delivery when a call is waiting. This service is combined with the Call Waiting service. The following shows a typical example of Type II Caller ID signal.



SAS : Subscriber Alerting Signal

t1: 440 Hz 300 ms typical (250 – 1000 ms)

t2: 0-50 ms

CAS: CPE Alerting Signal 2130 Hz/2750 Hz dual tone at -15 dBm

t3: 80-85 ms Rx is expected at -32 to -14 dBm with 75 to 80 ms duration up to 6 dB twist

ACK: DTMF D (or DTMF A)

t4+t5: 155- 165 ms

t4: t4 should be less than 100 ms

t5: 55 - 65 ms

t6: 0- 500 ms

CID: Caller ID Signal

t7: varies depending upon service type.

t8: 0-50 ms

The host is responsible for sending the acknowledge signal for the CAS tone back to the phone company for Type II Caller ID reception.

Figure 9-2. Caller ID Example Flowchart

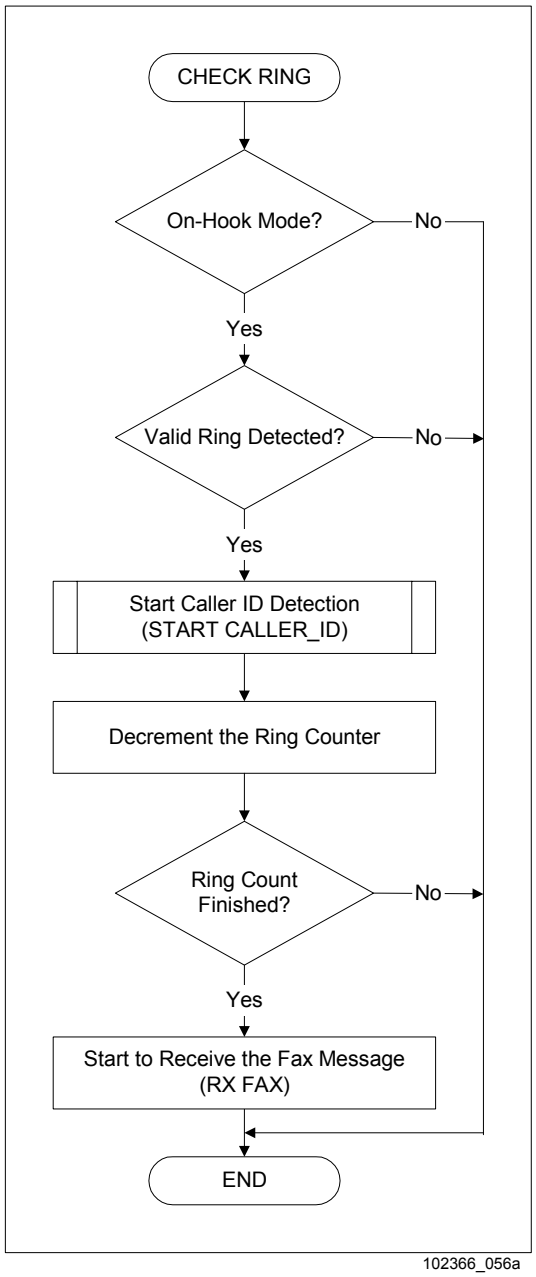


Figure 9-2. Caller ID Example Flowchart (Continued)

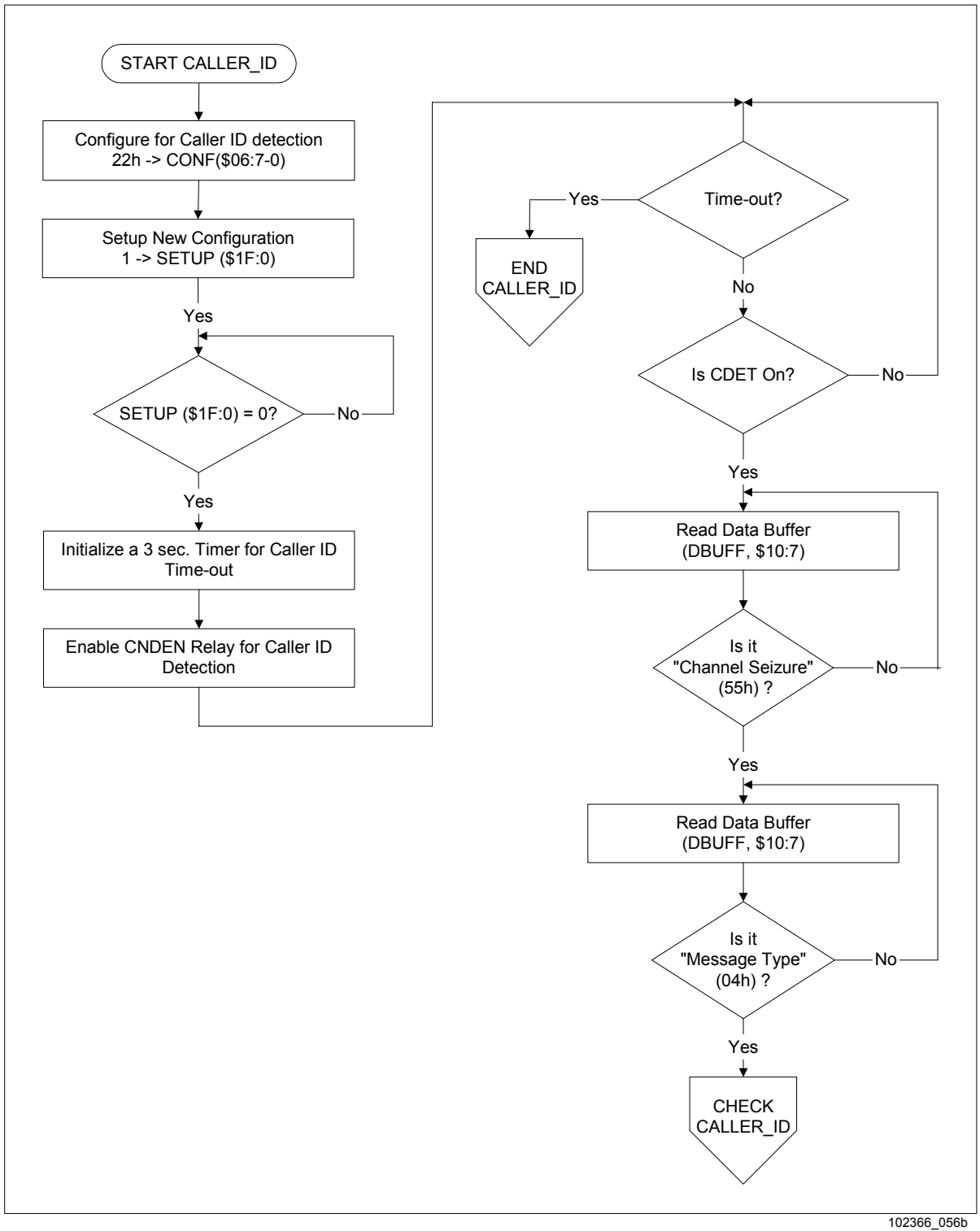
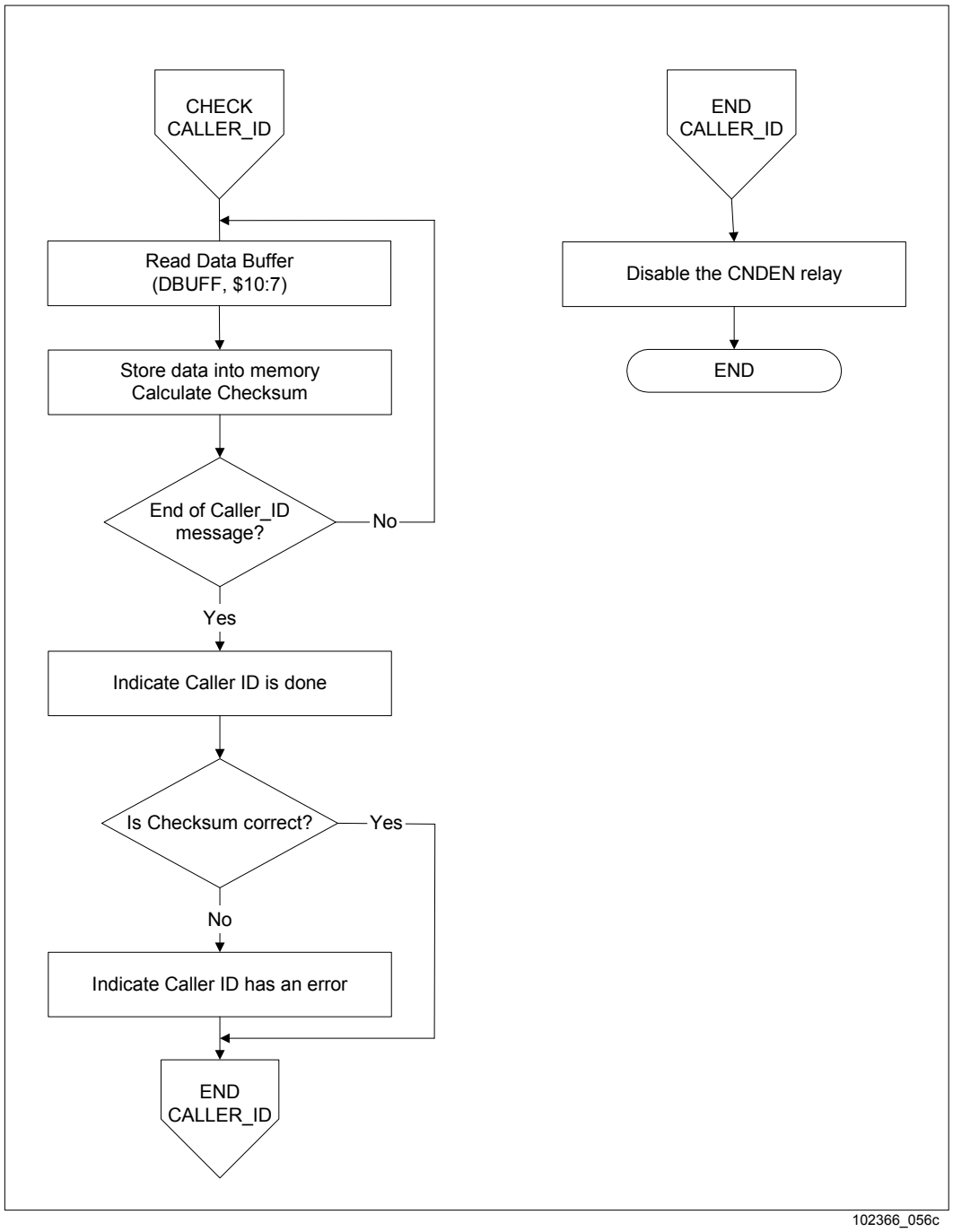


Figure 9-2. Caller ID Example Flowchart (Continued)



9.8 Russian CID

Russian Caller ID (RCID) detection is supported in Tone Detect configuration (80h). Three tone detectors are also available in this mode. RCID is disabled/enabled by the host setting/resetting control bit RCIDDIS before setting new configuration request bit SETUP.

Upon request, a PBX transmits the calling party number to the requesting device. Data is transmitted within a packet consisting of 9 codes placed in the following order:

1. Start code (S)
2. Category of subscriber code (CS)
3. Seven digit codes.

Start	CS	7th digit	6th digit	5th digit	4th digit	3rd digit	2nd digit	1st digit

Information is transmitted cyclically and usually repeated several times. For example, number 1234567, with CS 8 can be transmitted as "S87654321S87654321". Consecutive, identical digits are transmitted using the "Repeat" code R. For example number 2256789 can be transmitted as "S898765R2".

The RCID detector detects and reports all valid codes in the order they are received.

9.8.1 RCID Detector Status Bits

Figure 9-3. RCID Detector Example

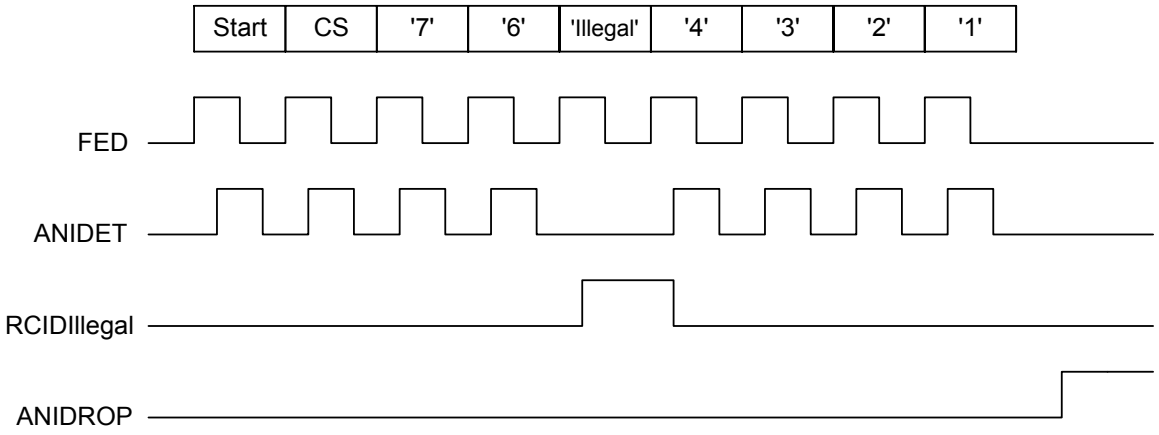


Table 9-1. Modem DSP RAM Access Codes

No.1, 2	Function	BR	CR	IO	AREX	ADD	Read Reg. No.
9:1	RCID Inter-Tone Silence Counter	0	1	0	1	0C	2,3
9:2	RCID Rejection Threshold	0	1	0	1	23	2,3
9:3	RCID Frequency Deviation	0	1	0	1	17	2,3
		0	1	0	1	2B	2,3
		0	1	0	1	3F	2,3
		0	1	0	1	53	2,3
		0	1	0	1	67	2,3
9:4	RCID 3rd Tone Rejection	0	1	0	1	18	2,3
		0	1	0	1	2C	2,3
		0	1	0	1	40	2,3
		0	1	0	1	54	2,3
		0	1	0	1	68	2,3
9:5	RCID Free Running Sample Counter	0	1	0	1	8C	0,1
9:6	RCID Code 0 Positive Twist	0	1	0	1	00	2,3
9:7	RCID Code 0 Negative Twist	0	1	0	1	80	0,1
9:8	RCID Code 1 Positive Twist	0	1	0	1	01	2,3
9:9	RCID Code 1 Negative Twist	0	1	0	1	81	0,1
9:10	RCID Code 2 Positive Twist	0	1	0	1	02	2,3
9:11	RCID Code 2 Negative Twist	0	1	0	1	82	0,1
9:12	RCID Code 3 Positive Twist	0	1	0	1	03	2,3
9:13	RCID Code 3 Negative Twist	0	1	0	1	83	0,1
9:14	RCID Code 4 Positive Twist	0	1	0	1	04	2,3
9:15	RCID Code 4 Negative Twist	0	1	0	1	84	0,1
9:16	RCID Code 5 Positive Twist	0	1	0	1	05	2,3
9:17	RCID Code 5 Negative Twist	0	1	0	1	85	0,1
9:18	RCID Code 6 Positive Twist	0	1	0	1	06	2,3
9:19	RCID Code 6 Negative Twist	0	1	0	1	86	0,1
9:20	RCID Code 7 Positive Twist	0	1	0	1	07	2,3
9:21	RCID Code 7 Negative Twist	0	1	0	1	87	0,1
9:22	RCID Code 8 Positive Twist	0	1	0	1	08	2,3
9:23	RCID Code 8 Negative Twist	0	1	0	1	88	0,1
9:24	RCID Code 9 Positive Twist	0	1	0	1	09	2,3
9:25	RCID Code 9 Negative Twist	0	1	0	1	89	0,1
9:26	RCID Code A (Start) Positive Twist	0	1	0	1	0A	2,3
9:27	RCID Code A (Start) Negative Twist	0	1	0	1	8A	0,1
9:28	RCID Code B (Repeat) Positive Twist	0	1	0	1	0B	2,3
9:29	RCID Code B (Repeat) Negative Twist	0	1	0	1	8B	0,1

Notes:

1. Parameter numbers refer to corresponding numbers in Section 4.

Function 9:1 Inter-Tone Silence Counter (RCID)

The modem sets status bit ANIDROP when the inter-tone silence counter expires.

Format: 16-bits, positive, twos complement

Equation: T * 9600

Where: T is inter-tone silence counter value in ms.

Range: 0 to 7FFFh

Default Value: 0120h, T = 30 ms

Function 9:2 Rejection Threshold (RCID)

RCID received signal energy rejection threshold.

Format: 16-bits, positive, twos complement

Equation : Rejection Threshold = [1+(Rejection Threshold(dBm)/50)]*32768

Range: 0 to 7FFFh, -50 dBm ≤ Rejection Threshold(dBm) ≤ 0

Default Value: 0FC0h, Rejection Threshold(dBm) = -43.8 dBm

Function 9:3 Frequency Deviation (RCID)

This parameter controls the acceptable frequency range for RCID tones. Increasing the value of this parameter increases the frequency range. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the current value. The same parameter value must be written to all 5 parameter addresses.

Format: 16-bits, positive, twos complement

Equation: Frequency Deviation ±(Increase/Decrease)h

Range: 0 to 7FFFh

Default Value: 1100h

Function 9:4 3rd Tone Rejection (RCID)

The 3rd Tone Rejection parameter prevents RCID signal detection in the presence of a 3rd tone detected within 15 dB of the RCID dualtone signal's lowest energy tone. Increasing this parameter reduces the rejection threshold below 15 dB. Decreasing this parameter increases the rejection threshold above 15 dB. The same parameter value must be written to all 5 parameter addresses.

Format: 16-bits, positive, twos complement

Equation: 3rd Tone Rejection ±(Increase/Decrease)h

Range: 0 to 7FFFh

Default Value: 169Ch

Function 9:5 Free Running Sample Counter (RCID)

The Free Running Sample Counter is a counter-timer initialized to zero upon completion of configuration set-up. The modem continuously increments the counter-timer every sample period. The host can monitor RCID detection timing by setting the counter-timer to zero then reading the counter-timer when RCID status bits change state.

Format: 16-bits, unsigned

Equation: Time = (counter-timer)(3.41)

Range: 0 to FFFFh

Function 9:6 – 9:29 Positive and Negative Twist (RCID)

These parameters control acceptable negative and positive twist for the RCID signals. Decreasing this parameter increases the acceptable twist level. The twist will vary from one RCID symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the default value.

Format: 16-bits, positive, twos complement

Equation: Twist ±(Increase/Decrease)h

Range: 0 to 7FFFh

Default Value:

RCID Code	Positive	Negative
0	1330h	1330h
1	1330h	1330h
2	0C30h	0C30h
3	1330h	1330h
4	0630h	0630h
5	0C30h	0C30h
6	1330h	1330h
7	0300h	0300h
8	1630h	1630h
9	0C30h	0C30h
Start	0630h	0630h
Repeat	0C30h	0C30h

This page is intentionally blank.

10. Digital Equalization/High Pass Filter

A programmable digital equalizer (PDE) is provided in both the receiver and transmitter. The programmable digital equalizer consists of four cascaded biquads. This is similar to the tone detectors when cascaded by enabling bit 12TH. The programmable digital equalizer is enabled by setting bit PDEQZ. The block diagram is shown in Figure 10-1.

10.1 PDE Frequency Response

The programmable digital equalizer defaults to a Japanese two link delay equalizer, with 1.1 dB gain at 2700 Hz. The frequency response curves are shown in Figure 10-2.

10.1.1 PDE Coefficients

The equation to calculate the hex coefficients is:

$Coefficient_{16}$ = Coefficient * 32768

The format is 16 bits, signed, twos complement. The coefficient range is from -1 (8000h) to +1 minus 1 least significant bit (7FFFh).

The poles and zeros are shown in Table 10-1.

The programmable digital equalizer RAM access codes are shown in Table 10-2.

Note: *The default filter coefficients are written by the modem at power-on.*

10.2 Fixed Digital Cable Compromise Equalizer

An optional fixed cable compromise equalizer (in the receiver/transmitter) is enabled by setting bit DCABLE. The digital cable equalizer frequency response is shown in Figure 10-3.

10.3 High Pass Filter

An optional receiver digital high pass filter (HPF) is enabled by setting bit HPFEN. Figure 10-4 and Figure 10-5 show the modem response with and without the high pass filter enabled, respectively.

Note: *The filter response will be shifted such that the notch is at 72 Hz.*

Figure 10-1. PDE Block Diagram

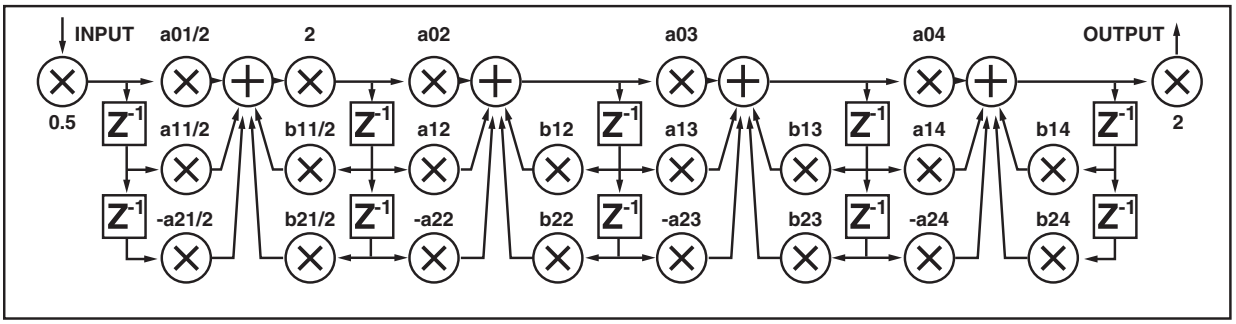


Figure 10-2. PDE Response

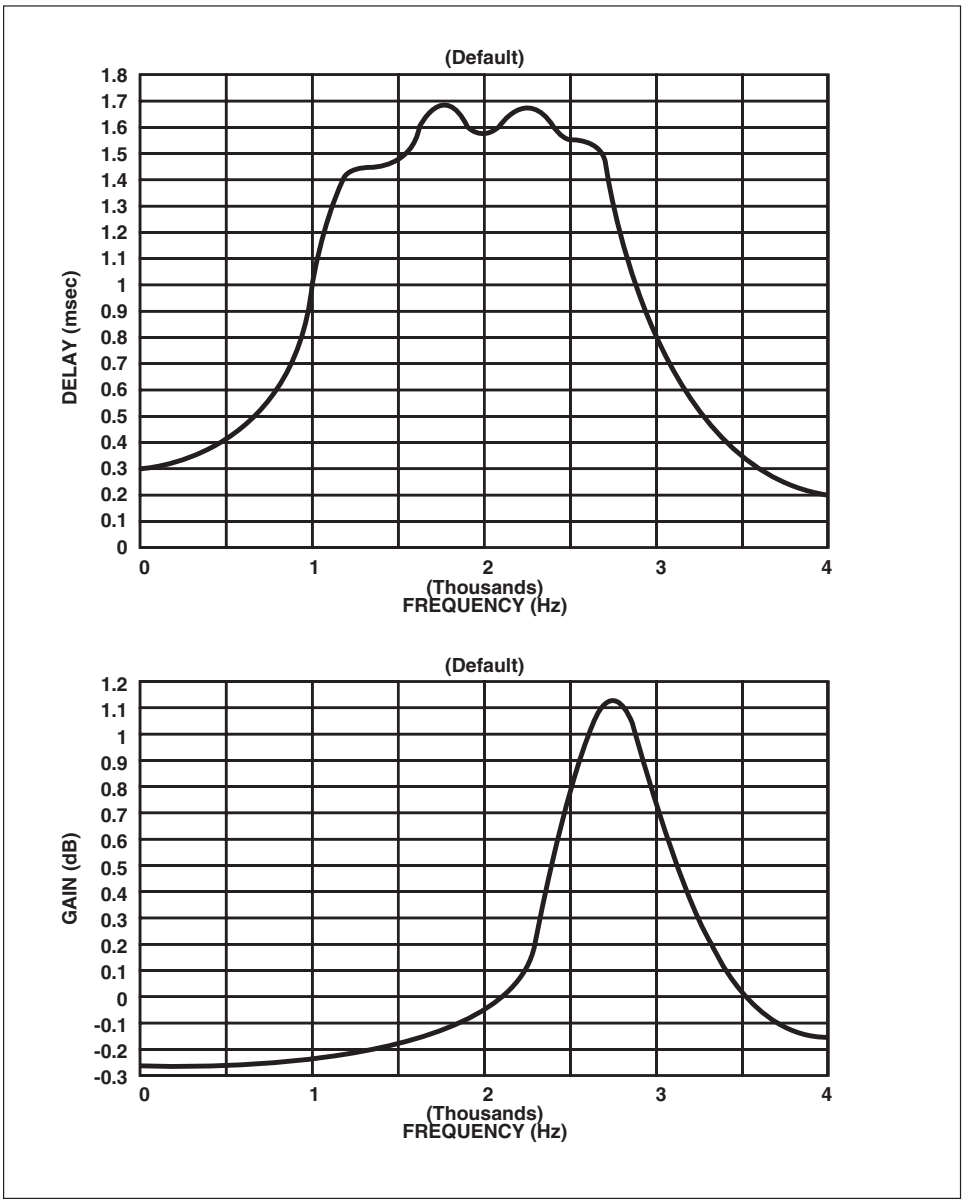


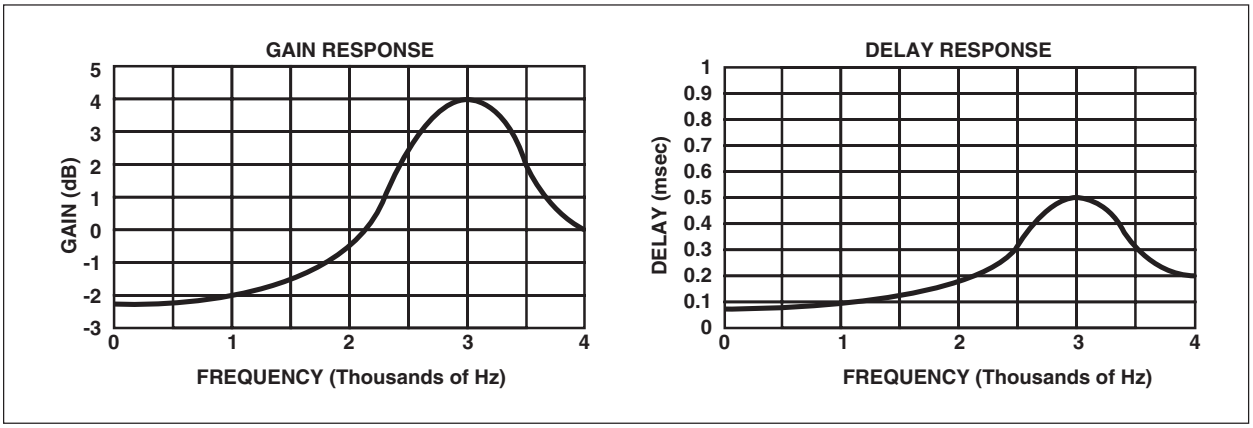
Table 10-1. PDE Poles and Zeros

Section Number	Poles	Zeros
1	0.794 @ 1215 Hz	1.26 @ 1215 Hz
2	0.798 @ 1728 Hz	1.25 @ 1728 Hz
3	0.793 @ 2241 Hz	1.26 @ 2241 Hz
4	0.830 @ 2713 Hz	1.27 @ 2713 Hz

Table 10-2. PDE RAM Access Codes

Parameter	AREX	BR	CR	IO	ADD	Read Reg. No.	Default Value (Hex.)	Default Value (Dec.)
a01/2	0	0	0	0	C6	0, 1	285C	0.31531771
a02	0	0	0	0	C8	0, 1	516C	0.63611724
a03	0	0	0	0	CA	0, 1	50A5	0.63002045
a04	0	0	0	0	CC	0, 1	4FB4	0.62269083
a11/2	0	0	1	0	46	2, 3	B8D1	-0.55611875
a21/2	0	0	1	0	47	2, 3	C000	-0.50000000
a12	0	0	1	0	48	2, 3	A8FF	-0.67972752
a22	0	0	1	0	49	2, 3	8000	-1.00000000
a13	0	0	1	0	4A	2, 3	EAD7	-0.16531356
a23	0	0	1	0	4B	2, 3	8000	-1.00000000
a14	0	0	1	0	4C	2, 3	291D	0.32118352
a24	0	0	1	0	4D	2, 3	8000	-1.00000000
b11/2	0	0	1	0	C8	0, 1	472F	0.55611875
b21/2	0	0	1	0	C9	0, 1	D7A4	-0.31531771
b12	0	0	1	0	CA	0, 1	5701	0.67972752
b22	0	0	1	0	CB	0, 1	AE94	-0.63611724
b13	0	0	1	0	CC	0, 1	1529	0.16531356
b23	0	0	1	0	CD	0, 1	AF5B	-0.63002045
b14	0	0	1	0	CE	0, 1	D4EA	-0.33660000
b24	0	0	1	0	CF	0, 1	AA61	-0.66890000

Figure 10-3. Digital Cable Equalizer Frequency Response



102366_059

Figure 10-4. Receive Path Frequency Response without HPF

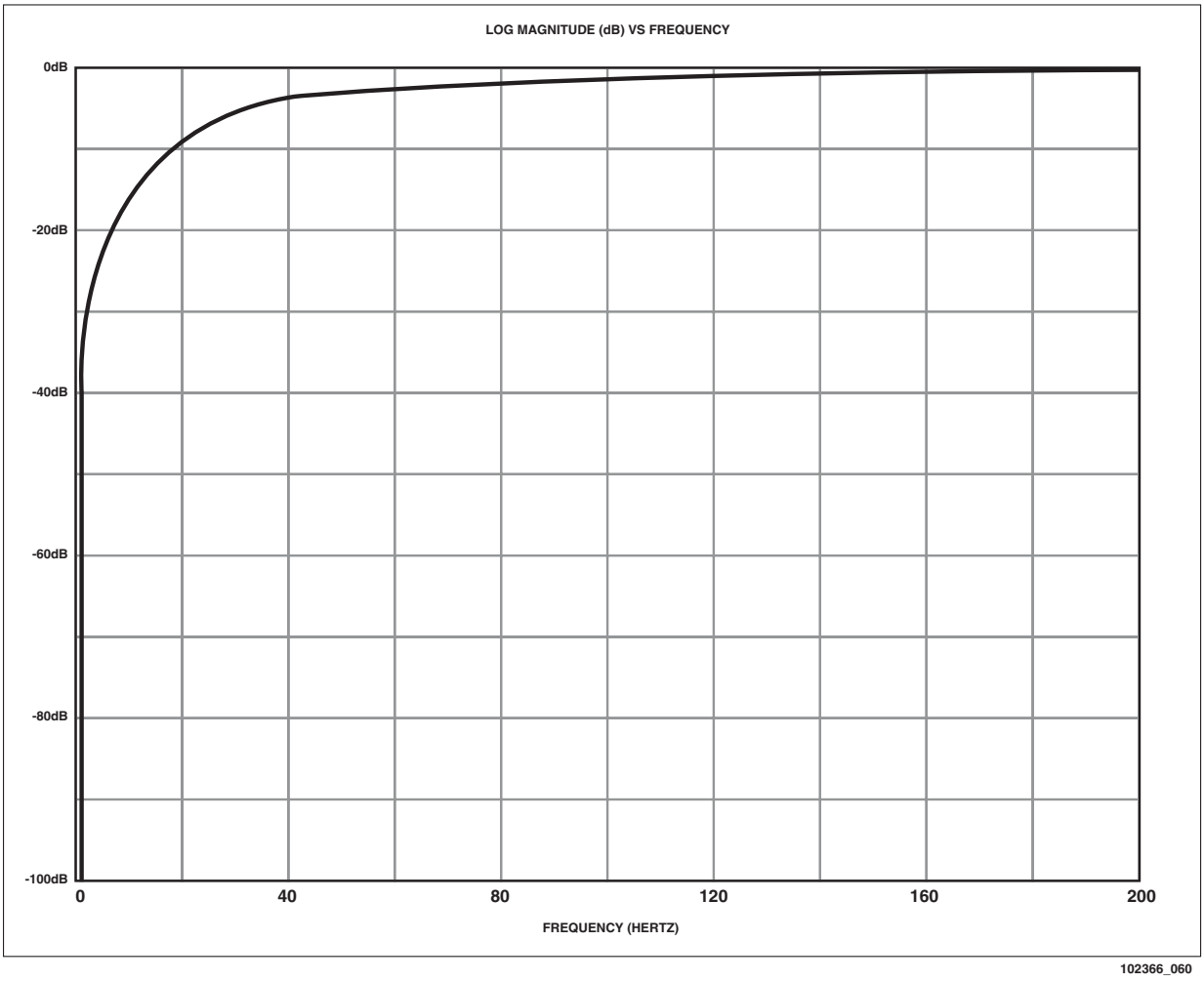
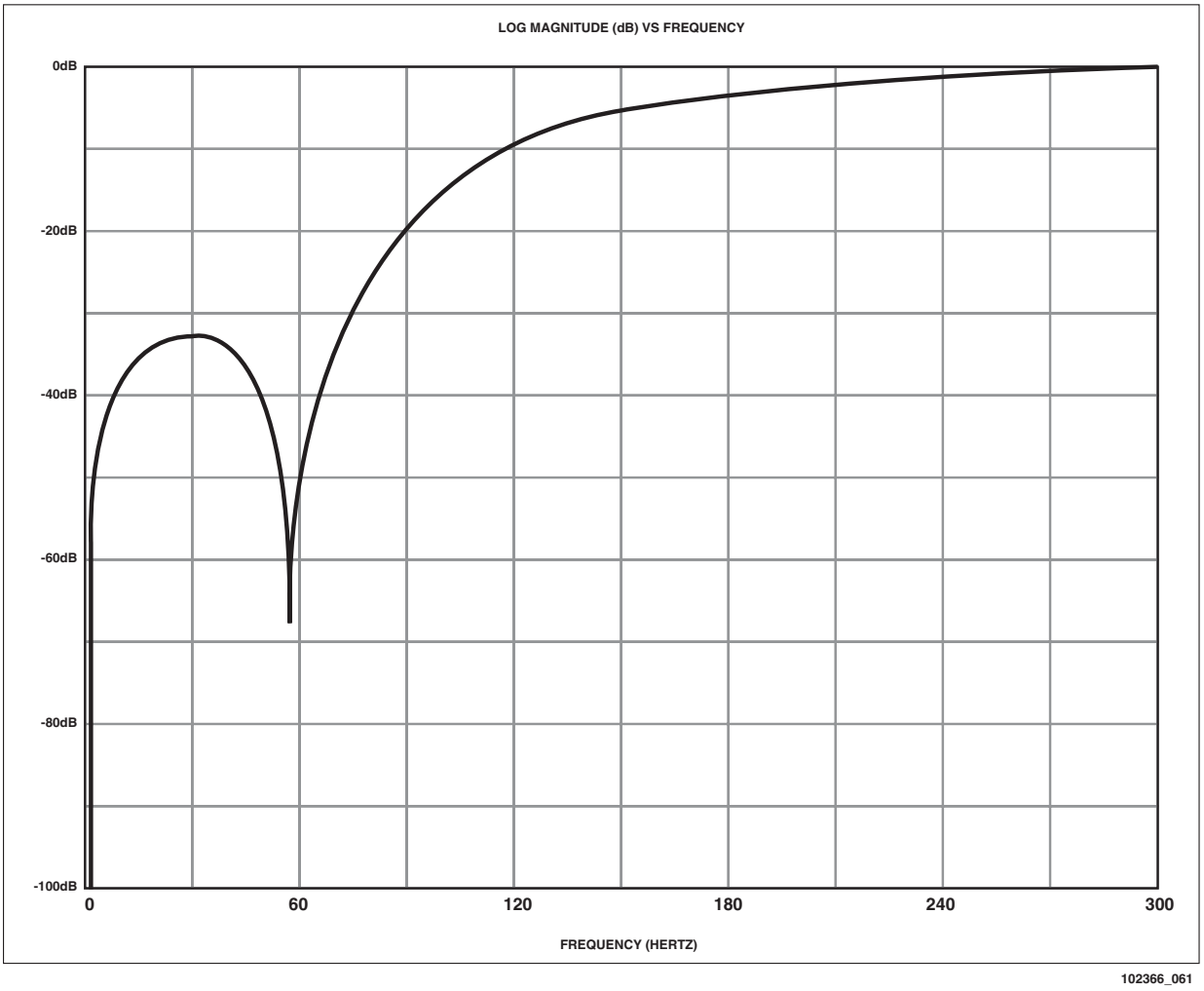


Figure 10-5. Receive Path Frequency Response with HPF



This page is intentionally blank.

11. Performance

DTMF performance is described in Table 11-1.

Performance is specified for a test configuration conforming to that specified in ITU-T Recommendation V.56. Bit error rates are measured for a flat line at a received line signal level of –20 dBm.

- At 2400 bps (V.27 ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-noise phase jitter at 120 Hz.
- At 4800 bps (V.27 ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.
- At 7200 bps (V.29), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 25 dB in the presence of 12° peak-to-peak phase jitter at 300 Hz.
- At 9600 bps (V.29), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 20° peak-to-peak phase jitter at 30 Hz.

Table 11-1. DTMF Receiver Performance Characteristics

Characteristic	Minimum[10]	Maximum[10]	Units	Programmable?	Notes
Acceptable Twist	–8.2 ±0.2	+4.3 ±0.2	dB	Yes	1, 2, 4, 5, 6, 7, 9
Acceptable Positive Frequency Deviation		+1.5 to +3.2	%	Yes	1, 3, 4, 5, 6, 7, 9
Acceptable Negative Frequency Deviation	–2.1 to –2.8		%	Yes	1, 3, 4, 5, 6, 7, 9
Required On-Time	40.0 ±1.0		ms	Yes	2, 3, 4, 5, 6, 7, 9
Required Off-Time	40.0 ±1.0		ms	Yes	2, 3, 4, 5, 6, 7, 9
Required Cycle-Time	93.0 ±1.0		ms	Yes	2, 3, 4, 5, 6, 7, 9
Dynamic Range	-43.0	0.0	dBm	Yes	1, 2, 3, 5, 6, 7, 9
Signal-to-Noise Ratio	12.0		dB	-	1, 2, 3, 4, 5, 6, 7, 9
Talk Off	2	3	Hits	-	8, 9

Notes:

1. On-time = 50 ms, off-time = 50 ms, and cycle-time = 100 ms.
2. Nominal DTMF frequencies.
3. Both tones of DTMF symbol have equal amplitude—0 dB twist.
4. Received signal level = –35.0 dBm.
5. All 16 DTMF symbols transmitted.
6. Error rate of 1/10,000 or less.
7. TAS Telephone Network Simulator Model #112, flat line transmission path.
8. Mitel CM7291 DTMF Receiver Test Cassette.
9. All DTMF receiver parameters are equal to their default values.
10. Values shown are for DTMF Receiver (configuration code 21h).

This page is intentionally blank.

12. Modem Interface Circuit

The modem is supplied in a 100-pin LQFP for design into OEM circuit boards. The Fax interface schematic in Figure 12-1 illustrates the connections and components required to configure the modem to OEM electronics.

A typical line interface using an external hybrid is shown in Figure 12-2.

Figure 12-3 shows a typical speaker circuit.

Table 12-1 specifies parameters for crystals or oscillators identified in these schematics.

Figure 12-1. Fax Interface Circuit

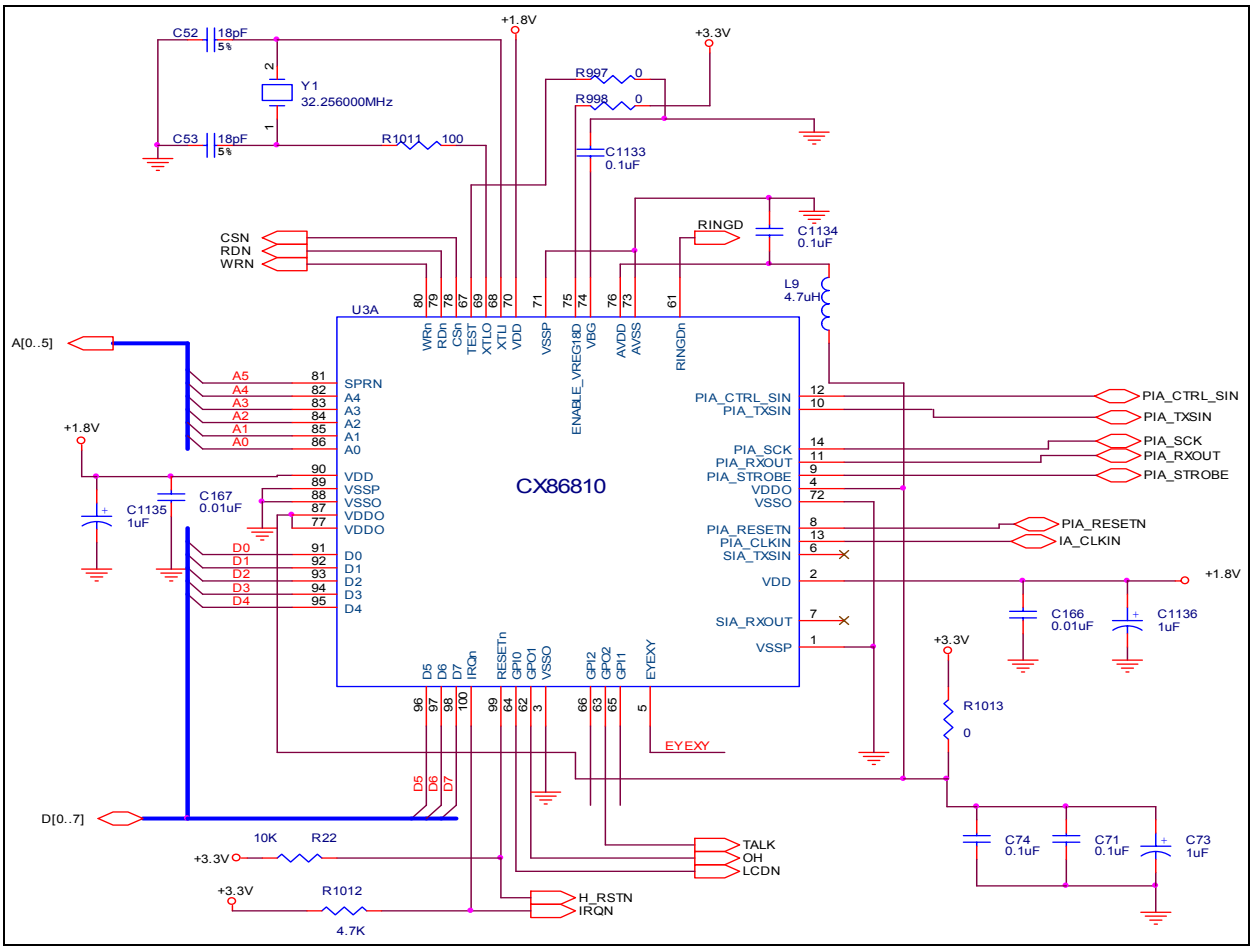


Figure 12-2. Typical Interface to External Hybrid

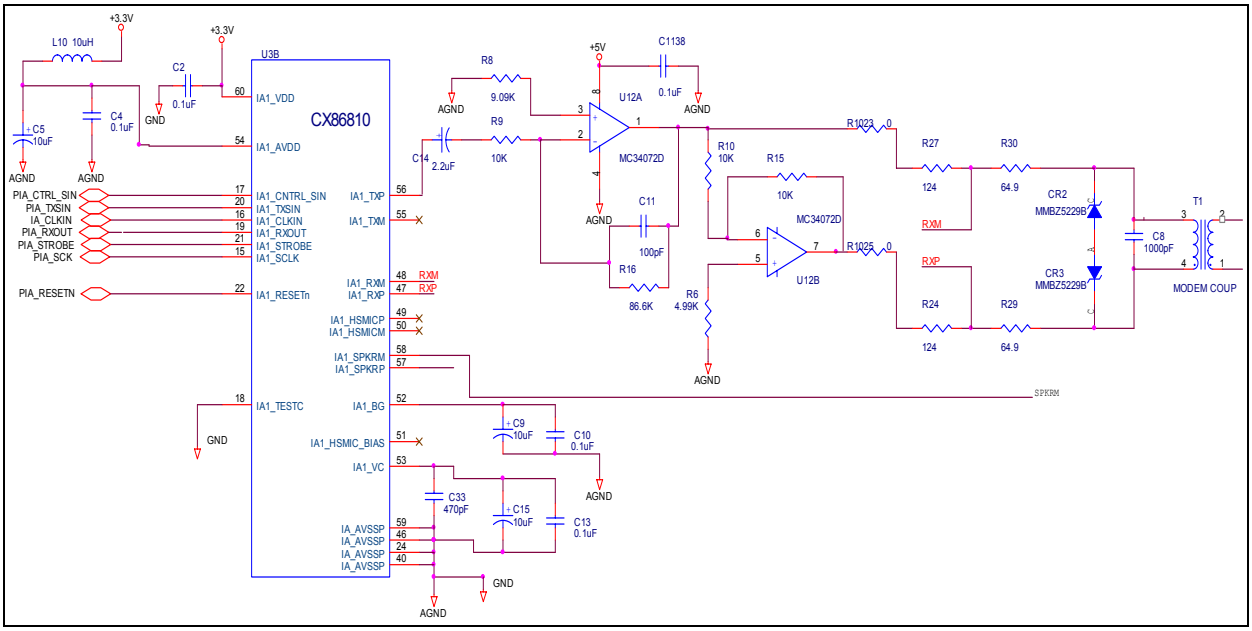


Figure 12-3. Typical Speaker Circuit

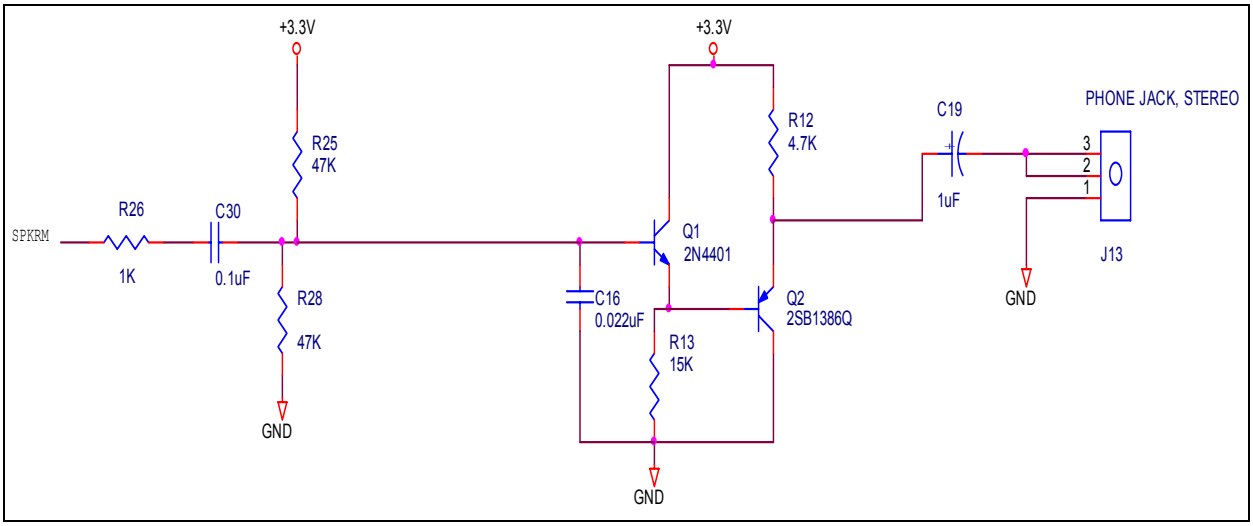


Table 12-1. Crystal Specifications - 32.256 Functional Mode

Characteristic	HC49U-32.256-FL	HC49U-32.256-L
Conexant Part No.		
Electrical		
Frequency	32.256 MHz nominal	32.256 MHz nominal
Frequency Tolerance	±50 ppm (C_L = 18 pF)	±50 ppm (C_L = 18 pF)
Frequency Stability		
vs. Temperature	±35 ppm (-20°C to 70°C)	±35 ppm (-20°C to 70°C)
vs. Aging	±15 ppm/5 years	±15 ppm/5 years
Oscillation Mode	Fundamental	Third Overtone
Calibration Mode	Parallel resonant	Parallel resonant
Load Capacitance, C_L	18 pF nom.	18 pF nom.
Shunt Capacitance, C_O	7 pF max.	7 pF max.
Series Resistance, R_1	35 Ω max. @100 nW drive level	40 Ω max. @100 nW drive level
Drive Level	100 µW correlation;	100 µW correlation;
	500 µW max.	1.0 mW max.
Operating Temperature	0°C to 70°C	-20°C to 70°C
Storage Temperature	–40°C to 85°C	–40°C to 85°C
Mechanical		
Holder Type	SMT	Through Hole
Third Lead	Required	Required

Notes:

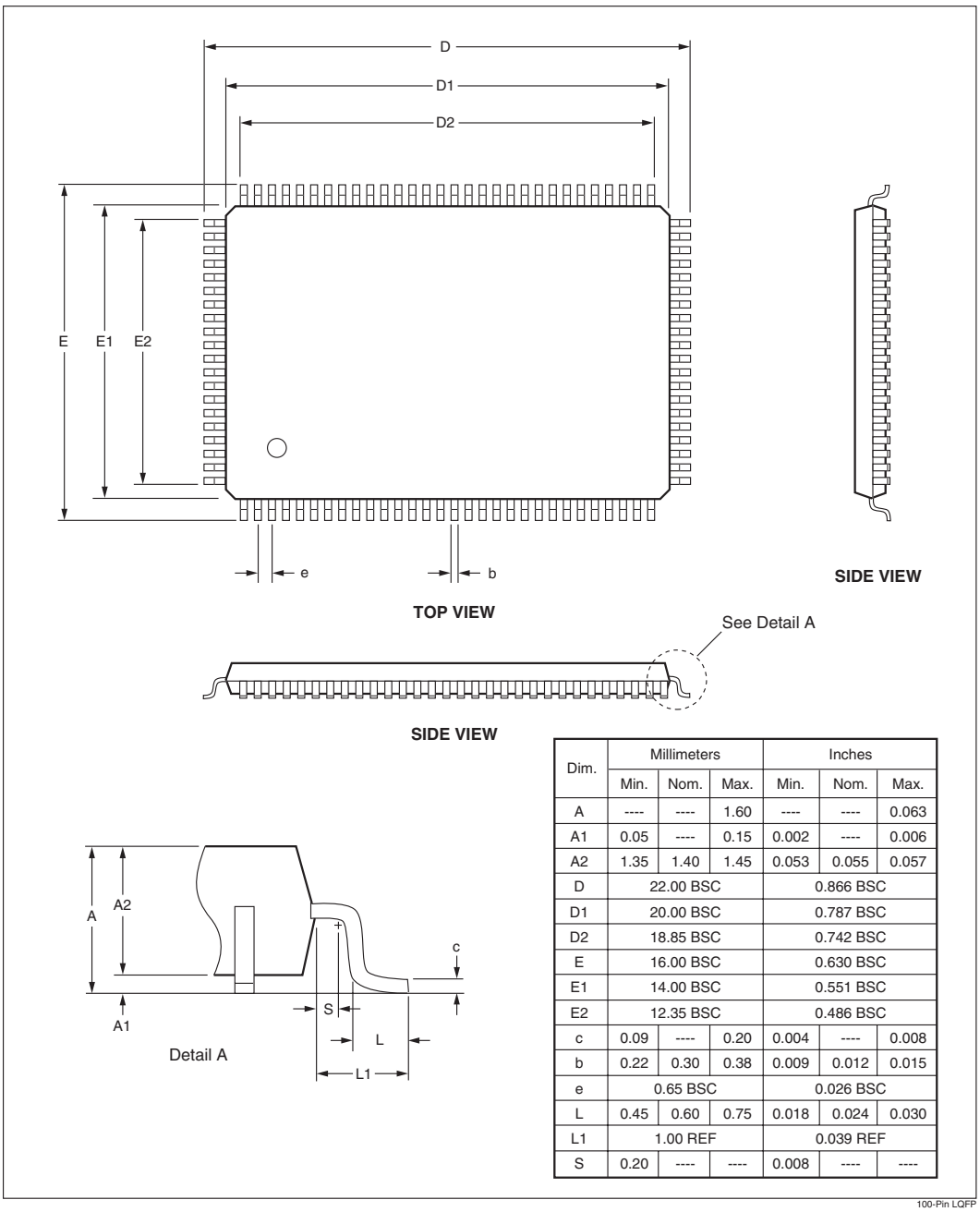
1. Characteristics @ 25°C unless otherwise noted.
2. Suggested supplier:
   ILSI America
   5458 Louie Lane
   Reno, NV 89511
   USA
   (702) 851-8880

This page is intentionally blank.

13. Package Dimensions

Package dimensions are shown in Figure 13-1 (100-pin LQFP).

Figure 13-1. 100-Pin LQFP Dimensions



Dim.	Millimeters			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	----	----	1.60	----	----	0.063
A1	0.05	----	0.15	0.002	----	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	22.00 BSC			0.866 BSC		
D1	20.00 BSC			0.787 BSC		
D2	18.85 BSC			0.742 BSC		
E	16.00 BSC			0.630 BSC		
E1	14.00 BSC			0.551 BSC		
E2	12.35 BSC			0.486 BSC		
c	0.09	----	0.20	0.004	----	0.008
b	0.22	0.30	0.38	0.009	0.012	0.015
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	----	----	0.008	----	----

This page is intentionally blank.

NOTES

www.conexant.com
General Information:
U.S. and Canada: (888) 855-4562
International: (732) 345-7500
Headquarters – Red Bank
100 Schultz Drive
Red Bank, NJ 07701