

3-Phase Standalone Pulse Width Modulation Engine

Advance Information

Supersedes January 1997 version, DS3755-3.5

DS3755 - 4.7 April 1999

The SA868 Motor Control IC has been designed for Pulse-Width Modulation (PWM) control of 3-phase induction motors used in appliances such as washing machines, HVAC equipment and light industrial machinery.

The SA868 allows selection of 16 factory programmed rotational speeds with option of either internal or external direction control. Selection of a particular frequency is made via 4 debounced digital inputs, allowing easy interfacing to mechanical timer sequencers, push buttons or microcontroller ports.

Smooth acceleration and deceleration rates are defined using two external resistor/capacitor pairs and controlled automatically by a patented algorithm to prevent damage to power electronics or load.

The SA868 controls both voltage and frequency via its PWM engine ensuring that the motor flux is accurately controlled over the full speed range. Comprehensive protection circuitry is provided to ensure reliable operation. All PWM outputs have high current drive capability to allow direct drive of opto coupler or pulse transformer isolator stages.

All parameters including the preselectable speeds, carrier frequency, power waveform type, minimum pulse width, pulse underlap and voltage/frequency characteristics can be specified by the customer and are mask programmed into the SA868 during manufacture.

The SA868 may be used in a variety of cost-sensitive applications. Since the PWM outputs are capable of generating signals that exceed the normal line frequency, this device can also be used for high speed machine tools such as cutting and polishing equipment.

Note - For prototyping and low volume applications, the Mitel SA866DE device can be used. Instead of an on-chip mask programmed ROM, an external serial EEPROM stores the programmable parameters. When production rises to high volumes the SA866DE can be replaced with the SA868.

Features

- Designed for Stand Alone Operation - No Micro Required.
- 16 Selectable Preset Speeds and Direction.
- All Programmable Parameters Held in Factory Mask Programmed ROM.
- Three Programmable Power Waveforms including Deadbanded Triplen for Reduced Switching Losses.
- Acceleration and Deceleration Times Controlled by Two External RC pairs.
- High Current Output Drivers.
- Carrier Frequency Selectable up to 24kHz for Silent Operation.

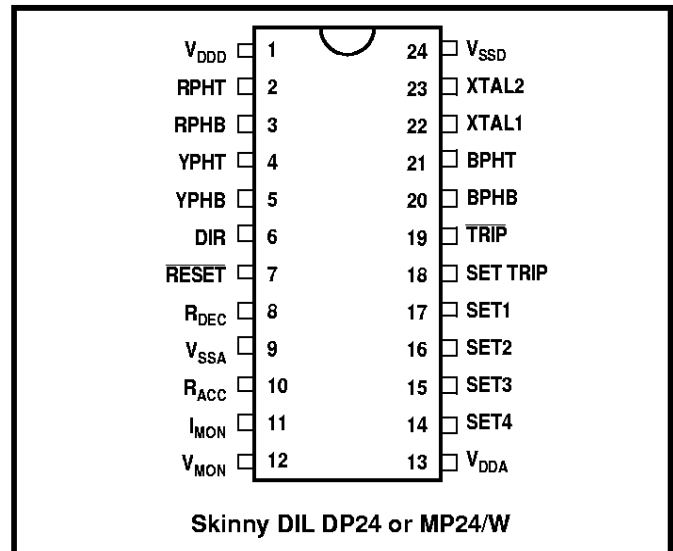


Fig.1 Pin connections - top view

- Wide Power Frequency Range 0 to 4kHz.
- Mask Programmed Minimum Pulse Width and Underlap Times.
- Double Edged Regular Sampling.
- Bootstrap Driver Precharge.
- Designed for Control of Domestic Appliances, HVAC and Light Industrial Equipment.

Ordering Information

SA868XXX/IG/DP1S - 24 Lead Skinny DIL
SA868XXX/IG/MP1S - 24 Lead Wide Body SOIC

(Note XXX = Customer specific variant number)

Demonstrator Variants

Deadbanding Waveform

SA868001/PR/DP1S - 24 Lead Skinny DIL
SA868001/PR/MP1S - 24 Lead Wide Body SOIC

Sine Waveform

SA868010/PR/DP1S - 24 Lead Skinny DIL
SA868010/PR/MP1S - 24 Lead Wide Body SOIC

SA868

Absolute Maximum Ratings

Supply voltage, V_{DD}	7V
Voltage on any pin	$V_{SS} - 0.5V$ to $V_{DD} + 0.5V$
Storage temperature	$-55^{\circ}C$ to $+150^{\circ}C$
Operating temperature	$-40^{\circ}C$ to $+85^{\circ}C$

The temperature ranges quoted apply to all package types. Alternative package types may be available. Further informat-

ion is available on request.

Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the devices at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.

Electrical Characteristics

Test conditions $V_{DD}, V_{DDA} = 5V \pm 10\%$ and $T_{amb} = 25^{\circ}C$ unless otherwise stated.

Characteristic	Symbol	Min.	Typ.	Max.	Units	Conditions
Input high voltage	V_{IH}	2	-	-	V	-
Input low voltage	V_{IL}	-	-	0.8	V	-
Input low current	I_{IL}					$V_{IN} = V_{SS}$
SET TRIP input		-1.0	-	1.0	μA	$V_{DD} = 5V$
All other input		-	-	10	μA	
Input high current	I_{IH}					
SET TRIP inputs		22	-	66	μA	$V_{IN} = V_{DD} = 5.5V$
All other inputs		-	-	10	μA	
Output high voltage	V_{OH}	4.0	>4.5	-	V	$I_{OH} = -12mA$ Phase outputs and \overline{TRIP}
Output low voltage	V_{OL}	-	<0.2	0.4	V	$I_{OL} = 12mA$ Phase outputs and \overline{TRIP}
Supply current (static)	$I_{DD(static)}$	-	-	1.0	mA	All outputs open circuit
Supply current (dynamic)	$I_{DD(dynamic)}$	-	5	25	mA	XTAL = 25MHz
Supply voltage	V_{DD}, V_{DDA}	4.5	5.0	5.5	V	V_{DD} and V_{DDA} must be connected together
$V_{MONITOR} / I_{MONITOR}$ threshold $(V_{thr} + V_{thf})/2$		2.44	$V_{DD}/2$	2.56	V	$V_{DD} = 5.0V$ -
$V_{thr} - V_{thf}$		140	200	320	mV	
Clock frequency	f_{CLK}	15	-	25	MHz	-
External clock duty cycle	D_{CLK}	40	-	60	%	-
SET TRIP = 1 → outputs tripped → $\overline{TRIP} = 0$	t_{TRIP}	$3/f_{CLK}$	-	$4/f_{CLK}$	s	-
Minimum Reset Period at power on	t_{RST}	-	2RC	-	s	Where 'RC' are the components on the R_{ACC} pin
R_{ACC}, R_{DEC} frequency range	f_{AD}	0.5	-	100	kHz	-
R_{ACC}, R_{DEC} Defeat threshold	V_{DFT}	-	$0.125 V_{DDA}$	-	V	-
SET [1:4], DIR Debounce Period	t_{DBNCE}	$256/f_{CARR}$	-	$384/f_{CARR}$	s	-

Pin Descriptions

Pin No.	Name	Type	Function
1	V _{DDD}	P	Positive Supply - Digital.
2	RPHT	O	Red Phase Top.
3	RPHB	O	Red Phase Bottom.
4	YPHT	O	Yellow Phase Top.
5	YPHB	O	Yellow Phase Bottom.
6	DIR	I	External Direction.
7	RESET	I	External Reset - Active Low.
8	R _{DEC}	I	Sets Deceleration Rate.
9	V _{SSA}	P	Ground - Analog
10	R _{ACC}	I	Sets Acceleration Rate.
11	I _{MON}	I	Overcurrent - Forces deceleration. Active High.
12	V _{MON}	I	Overvoltage - Inhibits Accel / Decel. Active High.
13	V _{DDA}	P	Positive Supply - Analog.
14	SET4	I	Setpoint Speed Select Bit (3).
15	SET3	I	Setpoint Speed Select Bit (2).
16	SET2	I	Setpoint Speed Select Bit (1).
17	SET1	I	Setpoint Speed Select Bit (0).
18	TRIP	O	Trip Latch Status - Active Low.
19	BPHB	O	Blue Phase Bottom.
20	BPHT	O	Blue Phase Top.
21	SET TRIP	I	Set Output Trip. Active High. Internal Pulldown.
22	XTAL1	I	Clock Crystal Connection.
23	XTAL2	I/O	Clock Crystal Connection.
24	V _{SSD}	P	Ground - Digital

Note: V_{DDD} and V_{DDA} must be connected together externally, as must V_{SSA} and V_{SSD}.

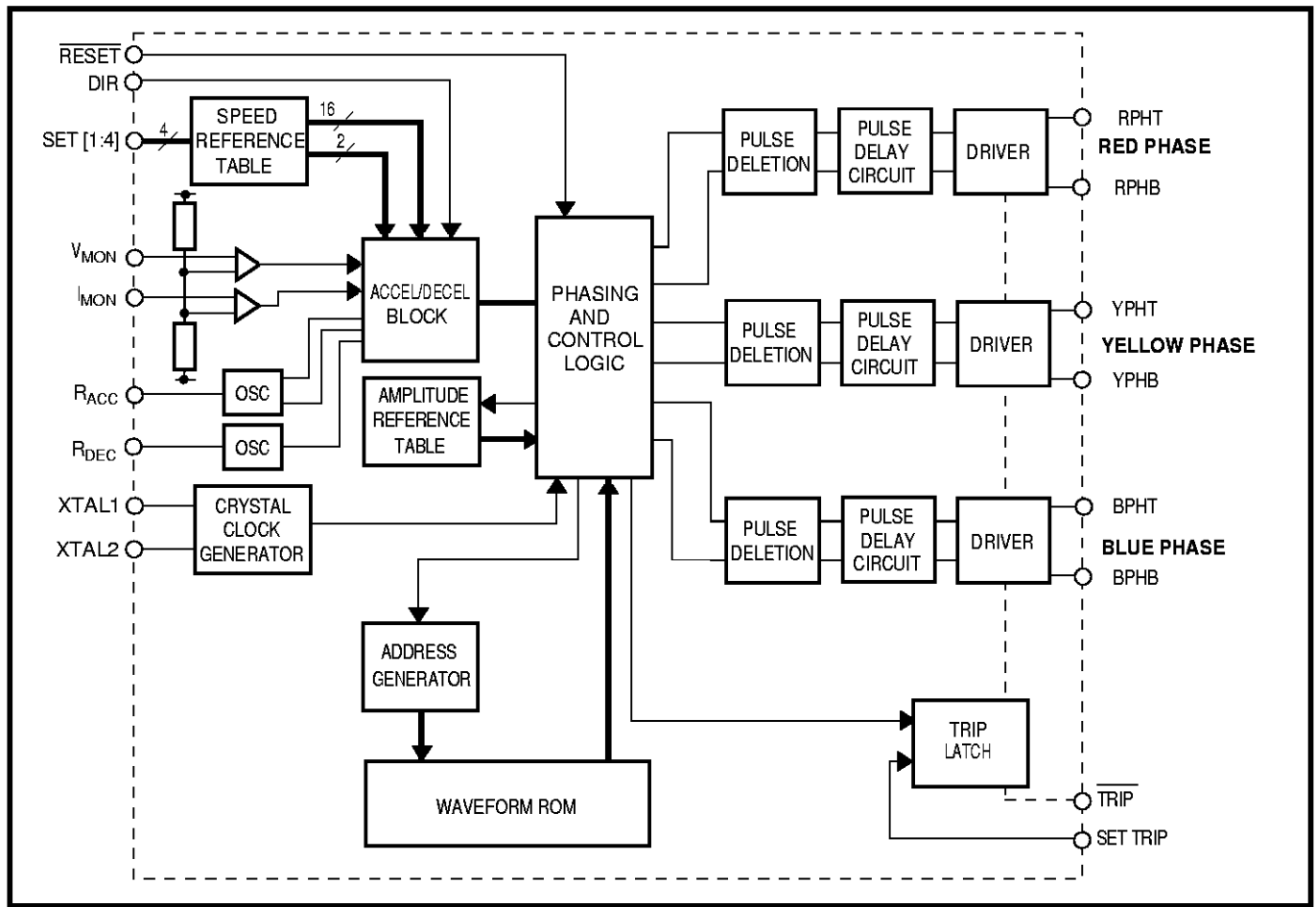


Fig.2 SA868 Block diagram

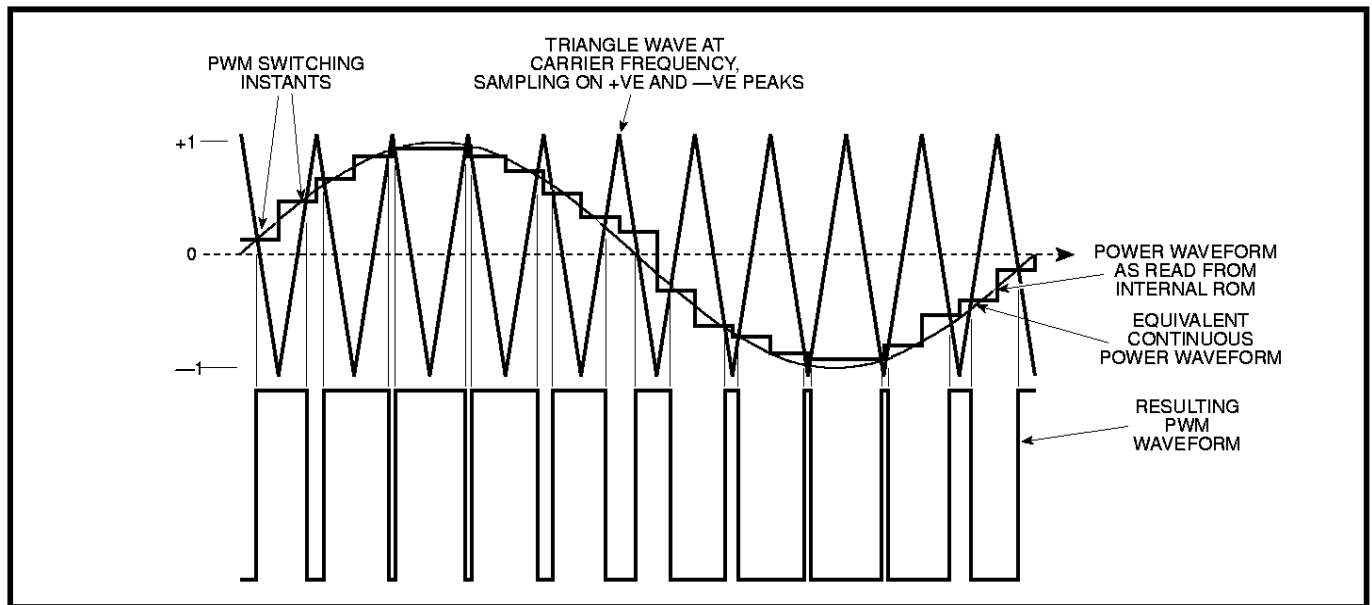


Fig.3 Asynchronous PWM generation with 'double-edged' regular sampling as used by the SA868

Functional Description

The block diagram in Fig.2 shows the internal architecture of the SA868.

Power Frequency is controlled by a 4 bit binary input applied to the SET[1:4] inputs. These select 1 of 16 Setpoint frequencies from the Speed Reference Table. The 18-bit speed value together with the external direction signal, DIR, is fed to the Acceleration / Deceleration block. This block controls the rate of change of Power Frequency when the frequency demand signal changes. The rate of change is defined by two external RC pairs which control the frequency of the on-chip acceleration/deceleration oscillators. Two protection inputs also connect to this block, V_{MON} and I_{MON} . These can be used to provide overvoltage and overcurrent protection for the external drive circuit.

All Initialisation Parameters, in addition to the 16 Setpoint frequencies, can be defined by the customer and are stored in a factory mask programmed ROM during manufacture. These Initialisation Parameters are:

CARRIER FREQUENCY
POWER FREQUENCY RANGE
PULSE DELAY (UNDERLAP)
PULSE DELETION
WAVEFORM TYPE
V/f GRADIENT
V/f PEDESTAL

The Phasing and Control Logic block provides all the necessary logic to produce the PWM signals. This uses a digital representation of the power waveform which is stored in the Waveform ROM and contains the three selectable Power Waveforms: Sinusoid, Triplen and Deadbanded Triplen. The output Voltage/Frequency characteristic can be set to follow a Linear (Constant Torque) curve defined by the two initialisation parameters: GRAD (Gradient) and PED (Pedestal).

The three pairs of PWM outputs from the Phasing and Control Logic each drive into a Pulse Control circuit that defines minimum pulse width and underlap times. Fast, high current Output Drivers are provided, suitable for direct drive of Opto-Isolators and industry standard Gate Driver IC's. To facilitate the use of boot-strap driver circuits for the power switches, whenever the phase outputs are restarted after they have all been shut down, the bottom phase outputs are all pulsed high for a whole carrier cycle before normal operation is resumed. This gives a time during which boot-strap capacitors may be charged before any top switch is driven. An external SET TRIP input is provided for rapid shutdown of the PWM outputs. The on-chip Clock Generator allows use of an external crystal or ceramic resonator to provide a stable, accurate clock source.

Phasing And Control Logic

The main Phasing and Control Logic block contains the PWM generation logic. An asynchronous method of PWM generation is used with uniform or 'double-edged' regular sampling of the waveform stored in the internal ROM as illustrated in Fig.3.

In general, a pulse width modulation signal is derived by comparing a signal waveform, (in this case the power waveform), with a saw-tooth or triangular carrier waveform of significantly higher frequency. The intersections between the waveforms, in the time domain, define the locations of transitions in the digital output train, and hence the width of the output pulses. The width of the pulses are directly proportional to 'the magnitude of the power waveform, thus the larger the magnitude, the

longer the 'ON' pulse.

The SA868 uses a digital implementation of this technique which avoids drift problems associated with the use of analog circuitry. A triangular waveform is synthesised using an up/down counter and a digital comparator is used to compare this with the power waveform. The power waveform is sampled regularly at every peak and trough of the carrier waveform allowing both edges of the PWM output pulse to move in time, hence the term 'double-edged' regular sampling. (A saw-tooth carrier waveform would result in one fixed edge and one moving edge for each PWM pulse.)

The power waveform is stored digitally in on-chip ROM. (1536 samples per 360°) The power frequency is controlled by the rate at which the ROM is addressed - a rate which is not related to the carrier frequency on the SA868, hence the term 'asynchronous method of PWM generation'.

Fig.3 shows the triangular carrier waveform together with the stepped waveform which results from sampling the outputs of the ROM at the peaks and troughs of the carrier. (A continuous power waveform is also shown for reference.) It can be seen that the PWM edges of the waveform are obtained at the points where the carrier and the sampled power waveform intersect. The carrier frequency is selectable to over 24kHz (assuming the maximum clock frequency of 25MHz is used), enabling ultrasonic operation for noise critical applications. With a 25MHz clock, power frequency ranges to over 4kHz are possible, with the actual output frequency defined to 16-bit accuracy within the chosen range. The output phase sequence of the PWM outputs can also be changed to allow both forward and reverse motor operation. This can be controlled with either the external Direction input or internally, using data from the mask programmed ROM.

PWM output pulses can be 'tailored' to the inverter characteristics by defining the minimum allowable pulse width, (the SA868 will delete all shorter pulse from the 'pure' PWM pulse train), and the underlap time, without the need for external circuitry.

Speed Reference Table

The Speed Reference Table consists of a 16x18-bit mask programmed ROM containing user-specific data. Each 18-bit field dictates a particular Setpoint speed to the rest of the IC. The least significant 16 bits dictate the scalar value of the frequency of the PWM output according to the SET [1:4] inputs. The remaining 2 bits, in conjunction with the DIR pin are dedicated to the direction of rotation, as shown in Table 1:-

BIT16	BIT17	DIR PIN	Actual Direction
Enable DIR	Internal Sign		(SETPOINT)
0	0	X	0 (REVERSE)
0	1	X	1 (FORWARD)
1	X	0	0 (REVERSE)
1	X	1	1 (FORWARD)

Table 1 External/internal direction decoder

This allows the external state of DIR to be "locked-out" for any entry in the look-up table and the direction forced internally. Note that these are direction demands and do not indicate an instantaneous change to a particular direction. The actual change of direction will only occur after the appropriate deceleration and re-acceleration period.

In the event that direction is entirely controlled from the Speed Reference Table, DIR must be tied high or low to prevent ex-

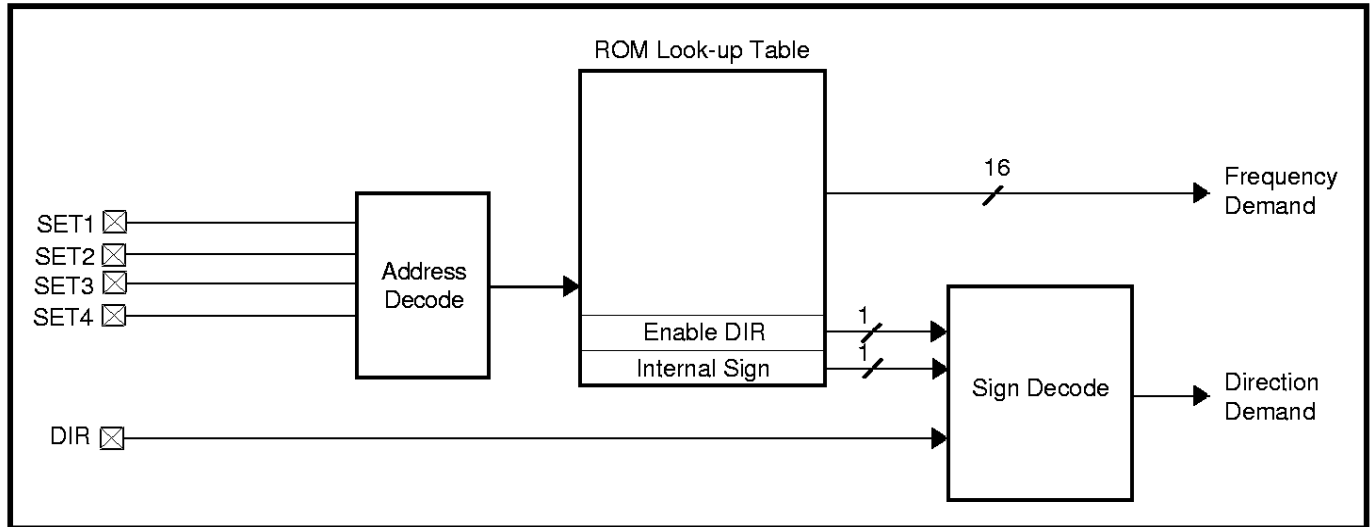


Fig. 4 Speed selection block diagram

cessive current consumption.

The frequency represented by the 16-bit word is calculated as follows:-

$$f_{POWER} = \frac{f_{RANGE}}{65536} \times p$$

where p = decimal value of 16 least significant bits in speed look-up table and f_{RANGE} = power frequency range (see later).

Location 0 in the look-up table always dictates “decelerate to rest and shut down PWM outputs”. This location is not available for customer specific values.

Whenever a new value of SET [1:4] is selected after SET[1:4] = 0, the bottom phase outputs are pulsed high (the top phase remaining low), before normal operation is commenced. This provides an opportunity to charge bootstrap capacitors in a drive circuit before any high side switch input is driven.

Zero speed is always represented as +0 (i.e. sign bit high) to ensure correct acceleration/deceleration. A speed of -0 is illegal and cannot be programmed into the look-up table.

Speeds need not be programmed into the Speed Reference Table in any particular frequency order, and zero frequency may be programmed at any location (always with sign bit high). However, when zero frequency demand is selected from a location other than SET [1:4] = 0, the phase of the power waveform freezes, but the phase outputs of the SA868 are **NOT** shut down, i.e. an unchanging PWM stream will be output. The bootstrap capacitor charging sequence is not invoked on the phase outputs, when a new frequency demand is selected following this state.

Note that SET [1:4] and DIR inputs are debounced since they may be fed by mechanical switches. Please refer to Electrical Characteristics on page 2 for details.

Acceleration/Deceleration Block

The Acceleration/Deceleration block consists of a 16-bit magnitude comparator and a 17-bit up/down counter clocked by the output from the Accel or Decel oscillators. The acceleration and deceleration rates are separately selectable using external resistors and capacitors.

Separate resistors (R) are connected from the R_{ACC} pin and the R_{DEC} pin to V_{DDA} . Similarly separate capacitors (C) are connected from the R_{ACC} pin and the R_{DEC} pin to V_{SSA} . The values of R's and C's may be the same or different, to produce equal or

different acceleration and deceleration times.

The time taken to accelerate from rest to the maximum value of the Power Frequency range f_{RANGE} (or to decelerate from f_{RANGE} to rest) is given by:

$$t_{acc/dec} = 65536 \times R.C. \times \ln 3$$

$$\approx 72 \times R.C. \times 10^3$$

where $5k\Omega \leq R \leq 100k\Omega$, $1nF \leq C \leq 25nF$

If R_{ACC} pin is connected to V_{SS} , all acceleration and deceleration will be instantaneous (irrespective of the state of the R_{DEC} pin). This makes the device suitable for waveform generation applications. In this mode of operation it is not necessary to connect a resistor and capacitor to R_{DEC} , although the R_{DEC} pin must be tied low.

It is possible to drive the R_{ACC} and R_{DEC} inputs directly with external clock signals, instead of using the RC oscillators. Typical input levels are $V_{IL} = 0.3V_{DD}$ and $V_{IH} = 0.6V_{DD}$, but care must be taken to ensure the lower level does not go below $0.125V_{DD}$ or the higher level above $0.75V_{DD}$.

The 16-bit magnitude comparator compares the scalar frequency demand from the Speed Reference Table with the instantaneous scalar frequency output from the up/down counter. The result is a 2-bit output as shown in Table 2.

UP	DOWN	Result
0	0	Same, No ACCEL or DECEL
0	1	LOWER
1	0	HIGHER
1	1	ILLEGAL STATE

Table 2 Acceleration/deceleration decoder

These 2 bits Up and DOWN are used in conjunction with the V_{MON} and I_{MON} pins and the sign bits to obtain an absolute indication of the required acceleration/deceleration, according to the following rules:-

- 1) If the V_{MON} condition is invoked ($V_{MON} > V_{thr}$), any acceleration/deceleration will be prevented until V_{MON} falls to $< V_{thr}$. This condition has highest priority. Normal acceleration/deceleration will continue when V_{MON} falls to $< V_{thr}$ as dictated by the rest of the

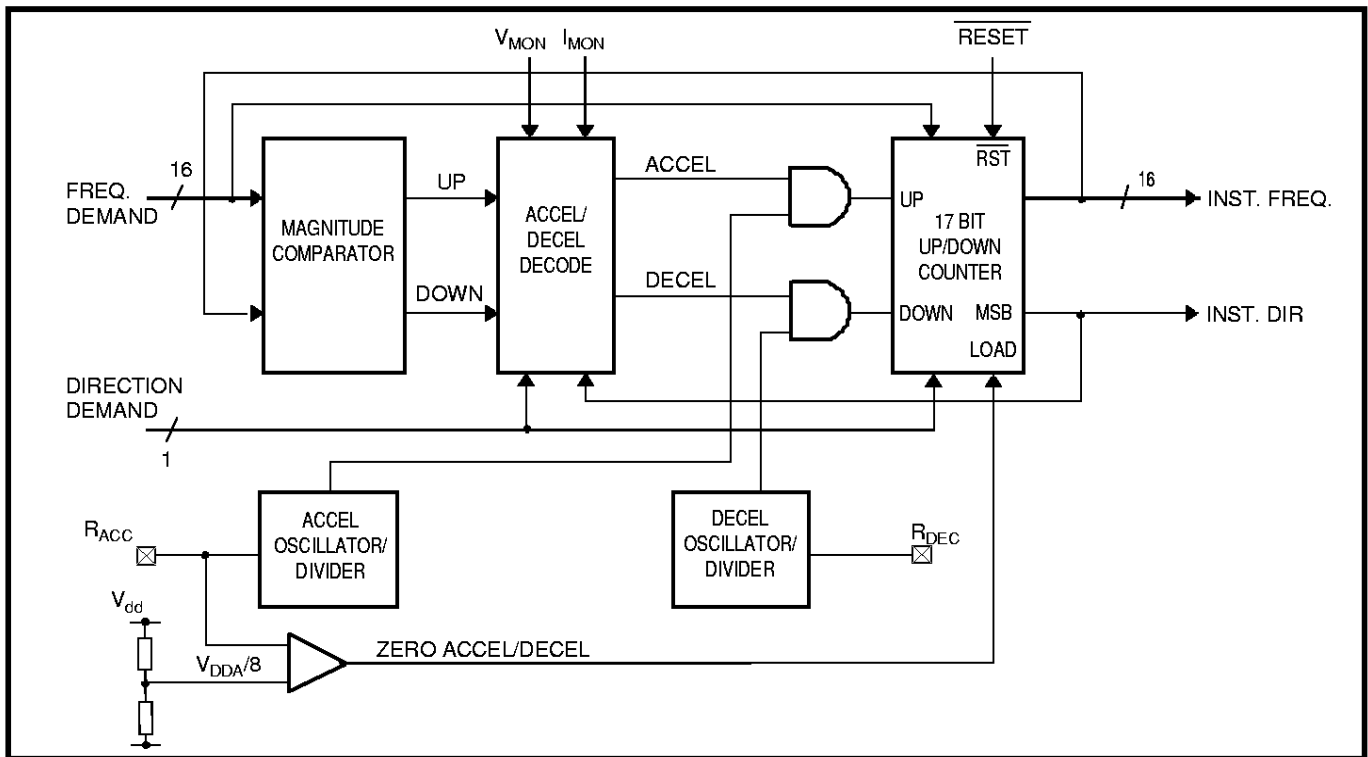


Fig. 5 Acceleration/deceleration block diagram

algorithm. This input is used to prevent excessive deceleration rates regenerating too much power into the dc link capacitor and causing an overvoltage condition.

2) If I_{MON} is invoked ($I_{MON} > V_{thr}$) the scalar value of the instantaneous frequency is reduced at the predetermined deceleration rate irrespective of the states of UP and DOWN. If the instantaneous frequency attains the value zero while I_{MON} is $> V_{thr}$ the PWM outputs are turned off (logic 0) for the duration of this condition (this prevents undue motor heating while at rest). No acceleration or deceleration is allowed once the frequency has attained the value zero. When I_{MON} is released normal acceleration/deceleration resumes as required by the prevailing conditions. In addition, the PWM outputs are re-enabled.

This condition has lower priority than V_{MON} since the act of decelerating due to I_{MON} being taken high may itself invoke the V_{MON} condition.

This input is intended to prevent too high an acceleration rate from causing an overcurrent/overtemperature situation at the switching devices.

Note: V_{thr} and V_{thr} are the rising and falling input voltage thresholds on the V_{MON} and I_{MON} pins.

3) If I_{MON} and V_{MON} are inactive, the algorithm takes the UP and DOWN outputs from the magnitude comparator, together with the direction demand and the instantaneous direction from the up/down counter to compute whether acceleration or deceleration is required:-

(a) If the required and instantaneous directions are different, the first requirement is to decelerate to rest since no change of direction is possible until this has occurred. Therefore, so long as this condition holds, decelerate (see 1 and 2 in Table 3).

(b) If the directions are the same and UP and DOWN are both zero then the required and instantaneous speeds are matched both in terms of direction and magnitude, therefore neither acceleration or deceleration is required (see 3 and 4 in Table 3).

(c) If the directions are the same but either UP or DOWN is high then the direction of rotation does not need to change, but the magnitude does. Therefore, if UP is high, accelerate or if DOWN is high, decelerate (see 5,6,7 and 8 in Table 3).

(d) UP and DOWN both high is an illegal state since both conditions cannot exist concurrently.

Condition	UP	DOWN	Required Direction	Instantaneous Direction	ACCEL	DECEL
					Active High	
1	X	X	0	1	0	1
2	X	X	1	0	0	1
3	0	0	0	0	0	0
4	0	0	1	1	0	0
5	0	1	0	0	0	1
6	0	1	1	1	0	1
7	1	0	0	0	1	0
8	1	0	1	1	1	0
9	1	1	X	X	ILLEGAL STATE	

Table 3 Acceleration/deceleration block conditions

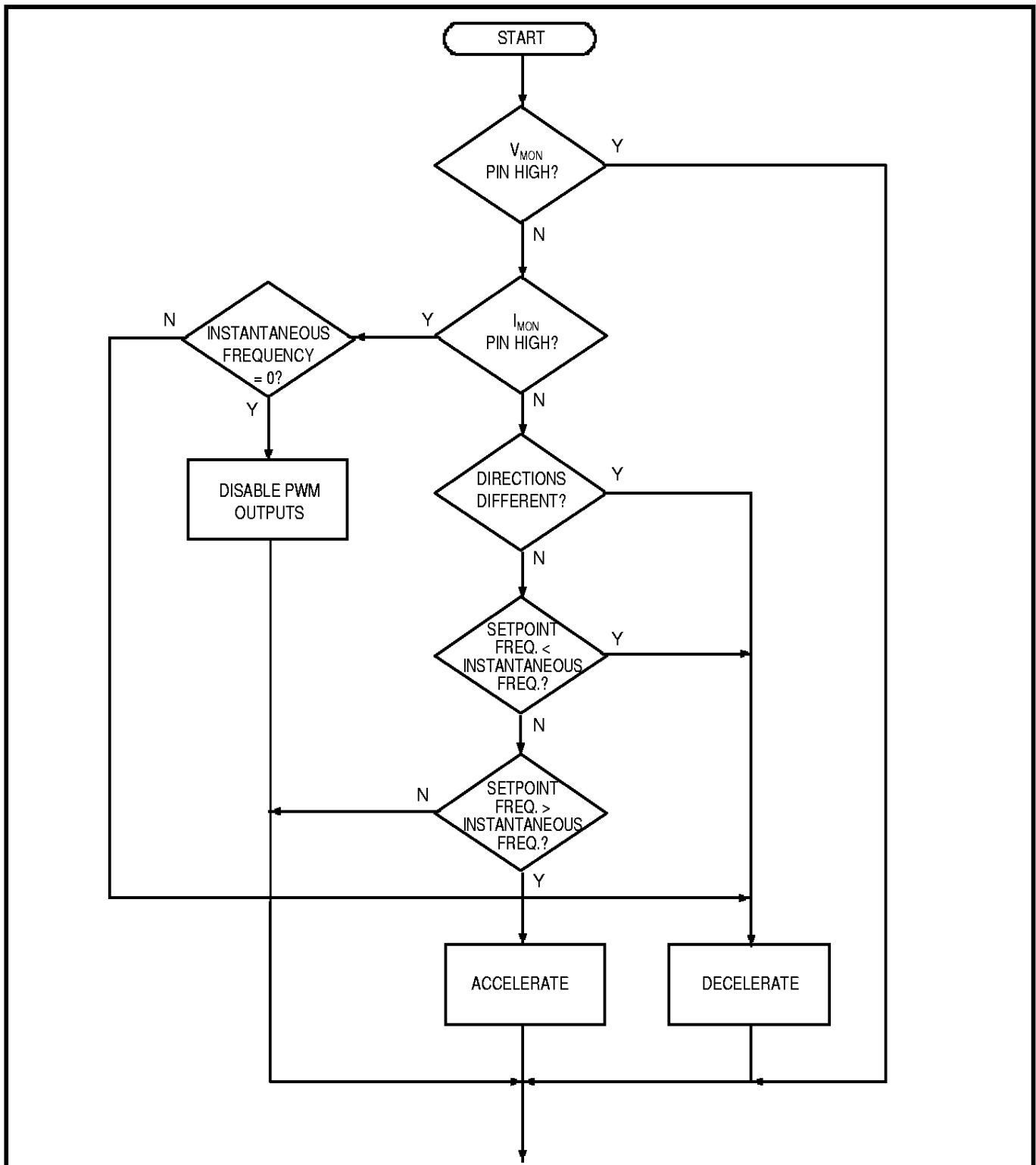


Fig.6 Acceleration/deceleration block flow diagram

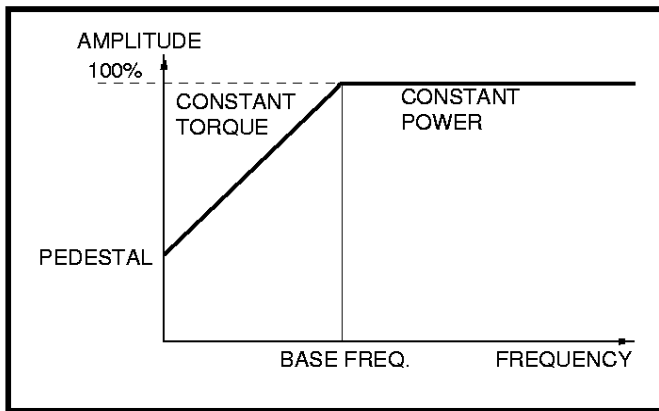


Fig.7 General form of the voltage/frequency curve

The ACCEL and DECEL signals are gated with the accel or decel oscillator to increment or decrement the speed.

This algorithm is clarified in the flow diagram of Fig.6.

The counter is a 17-bit synchronous up/down counter, the most significant bit being the instantaneous direction. The reset condition of this block is a logic 1 on the direction bit (MSB) and zeros on all other bits, being representative of zero speed and a forward direction. Zero speed is always represented in this way to prevent confusion between +/- 0. (-0 is not a valid state).

Amplitude Control Block

In order to ensure adequate control of motor flux, the SA868 controls the motor voltage at all frequencies. The general form of the voltage/frequency curve is shown in Fig.7.

At zero frequency a variable 'Pedestal' voltage is applied to the motor to overcome copper losses. The voltage then increases in proportion to the frequency up to the selectable 'Base Frequency'. This is generally 50Hz or 60Hz but may be selected to be anywhere in the frequency range. Frequencies up to the Base Frequency are said to be in the Constant Torque region.

Beyond the Base Frequency the amplitude is held at its maximum value. This inevitably leads to a fall in the generated torque with increasing frequency. Hence this is termed the Constant Power region.

The SA868 incorporates an Amplitude Control Block as shown in Fig.8.

The instantaneous frequency word is multiplied by the mask-programmed Gradient word. The result is added to the 8-bit Pedestal value and the result is rounded to 8 bits by the Overflow

Detection/Correction circuit before being passed to the PWM generator blocks.

Factory Masked Initialisation Parameters

The following section defines parameters that can be specified by the user, and are programmed in the factory mask programmed ROM during manufacture. A special Order Form is available for this purpose - please contact your local Customer Service Centre for details.

Carrier frequency selection

The carrier frequency is a function of the externally applied clock frequency and a division ratio *n*, determined by the 3-bit CFS word. The values of *n* are selected as shown in Table 4. The carrier frequency, *f_{CARR}* is then given by:

CFS word	111	110	101	100	011	010	001	000
Value of <i>n</i>	7	6	5	4	3	2	1	0

Table 4 Values of clock division ratio *n*

$$f_{CARR} = \frac{f_{CLK}}{512 \times 2^{n+1}}$$

where *f_{CLK}* = clock input frequency.

Power frequency range selection

The power frequency range defines the maximum limit of the power frequency. The operating power frequency is controlled by the 16-bit instantaneous frequency from the Accel/Decel block.

The power frequency range is a function of the carrier waveform frequency (*f_{CARR}*) and a multiplication factor *m*, determined by the 3-bit FRS word. The value of *m* is determined as shown in Table 5.

The power frequency range, *f_{RANGE}* is then given by:

FRS word	110	101	100	011	010	001	000
Value of <i>m</i>	6	5	4	3	2	1	0

Table 5 Values of carrier frequency multiplication factor

$$f_{RANGE} = \frac{f_{CARR} \times 2^m}{384}$$

where *f_{CARR}* = carrier frequency.

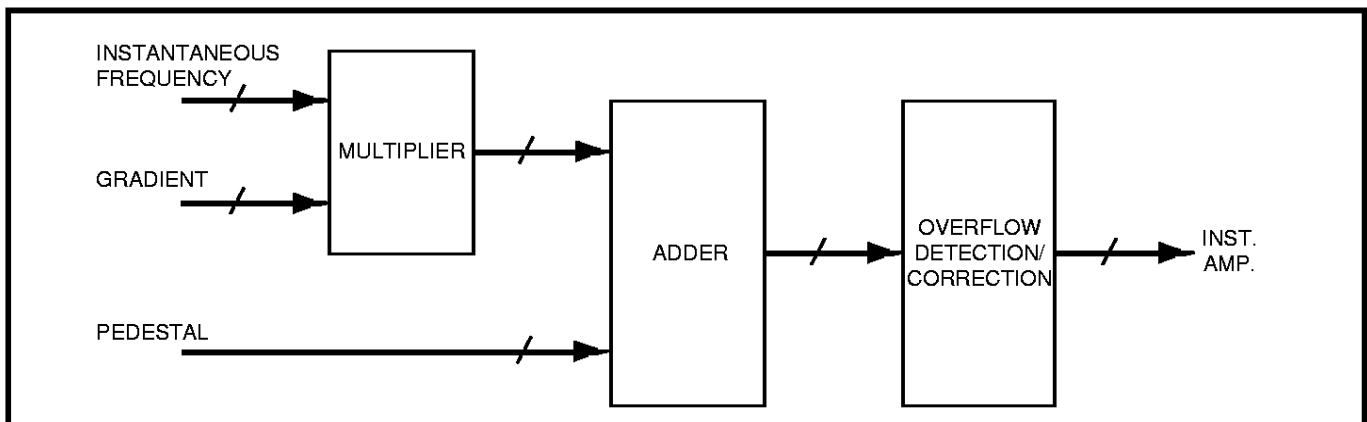


Fig. 8 Amplitude Control block diagram

Pulse delay time

The pulse delay time affects all six PWM outputs by delaying the rising edges of each of the outputs by an equal amount. The pulse delay time, t_{pdy} , is a function of the carrier waveform frequency and PDY, defined by the 6-bit pulse delay time select word. The value of PDY is selected as shown in Table 6.

PDY word	111111	111110	...etc...	000000
Value of PDY	63	62	...etc...	0

Table 6 Values of PDY

The pulse delay time, t_{pdy} , is then given by:

$$t_{pdy} = \frac{63 - PDY}{f_{CARR} \times 512}$$

where f_{CARR} = carrier frequency.

Fig.9 shows the effect of pulse delay on a pure PWM waveform.

It should be noted that as the pulse delay circuit follows the pulse deletion circuit (see Fig. 2), the minimum pulse width seen at the PWM outputs will be shorter than the pulse deletion time set in the initialisation register. The actual shortest pulse generated is given by $t_{pd} - t_{pdy}$.

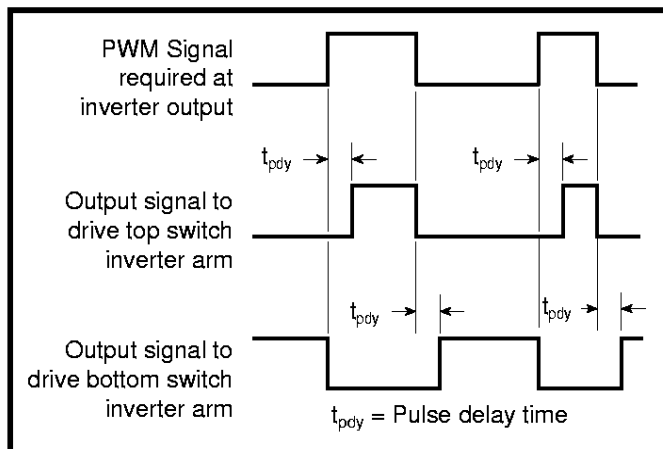


Fig.9 Effect of pulse delay on PWM pulse train

Pulse deletion time

To eliminate short pulses the true PWM pulse train is passed through a pulse deletion circuit. The pulse deletion circuit compares pulse widths with the pulse deletion time set in the Initialisation Register. If a pulse (either positive or negative) is greater in duration than the pulse deletion time, it is passed through unaltered, otherwise the pulse is deleted.

The pulse deletion time, t_{pd} , is a function of the carrier wave frequency and PDT, defined by the 7-bit pulse deletion time word. The value of PDT is selected as shown in Table 7.

PDT word	1111111	1111110	...etc...	0000000
Value of PDT	127	126	...etc...	0

Table 7 Values of PDT

The pulse deletion time, t_{pd} , is then given by:

$$t_{pd} = \frac{127 - PDT}{f_{CARR} \times 512}$$

where f_{CARR} = carrier frequency.

Fig.10 shows the effect of pulse deletion on a pure PWM waveform.

Waveform Selection

Two bits, WS0 and WS1, are used to define the power waveform, according to Table 8:

WS1	WS0	Waveform
0	0	Sinusoid (default)
0	1	Triplen (harmonic injection)
1	0	Deadbanded Triplen (switching loss reduction)
1	1	Reserved

Table 8 Waveform selection

The waveforms may be described by the following mathematical relationships and are shown graphically in Fig. 11:

Sinusoid:

$$f(t) = A \sin(\omega t) \quad \text{where } A = \text{amplitude,} \\ \omega = \text{angular displacement}$$

Triplen:

$f(t)$	Valid
$f(t) = A(2. \sin(\omega t + 30^\circ) - 1)$	$0^\circ \leq \omega t < 60^\circ$
$f(t) = A$	$60^\circ \leq \omega t \leq 120^\circ$
$f(t) = A(2. \sin(\omega t - 30^\circ) - 1)$	$120^\circ \leq \omega t < 180^\circ$
$f(t) = A(2. \sin(\omega t + 30^\circ) + 1)$	$180^\circ \leq \omega t < 240^\circ$
$f(t) = -A$	$240^\circ \leq \omega t \leq 300^\circ$
$f(t) = A(2. \sin(\omega t - 30^\circ) + 1)$	$300^\circ \leq \omega t < 360^\circ$

Deadbanding:

Below are the modulating functions for the Deadbanded Triplen waveform. These have been normalised and scaled to give a peak line voltage (phase to phase) of 2A. All the 3 phases are shown for clarity, $f(t)$, $g(t)$ and $h(t)$.

Function	Valid
$f(t) = 2A. \sin(\omega t + 30^\circ) - 1$	$0^\circ < \omega t \leq 60^\circ$
$g(t) = -1$	
$h(t) = 2A. \sin(\omega t + 90^\circ) - 1$	
$f(t) = 1$	$0^\circ < \omega t \leq 120^\circ$
$g(t) = 1 + 2A. \sin(\omega t - 150^\circ)$	
$h(t) = 1 + 2A. \sin(\omega t + 150^\circ)$	
$f(t) = 2A. \sin(\omega t - 30^\circ) - 1$	$120^\circ < \omega t \leq 180^\circ$
$g(t) = 2A. \sin(\omega t - 90^\circ) - 1$	
$h(t) = -1$	
$f(t) = 1 + 2A. \sin(\omega t + 30^\circ)$	$180^\circ < \omega t \leq 240^\circ$
$g(t) = 1$	
$h(t) = 1 + 2A. \sin(\omega t + 90^\circ)$	
$f(t) = -1$	$240^\circ < \omega t \leq 300^\circ$
$g(t) = 2A. \sin(\omega t - 150^\circ) - 1$	
$h(t) = 2A. \sin(\omega t + 150^\circ) - 1$	
$f(t) = 1 + 2A. \sin(\omega t - 30^\circ) - 1$	$300^\circ < \omega t \leq 360^\circ$
$g(t) = 1 + 2A. \sin(\omega t - 90^\circ) - 1$	
$h(t) = 1$	

Line output voltages appearing across the load are:

$$V_{fg} = f(t) - g(t) \\ V_{gh} = g(t) - h(t) \\ V_{hf} = h(t) - f(t)$$

The line voltage waveforms are sinusoidal.

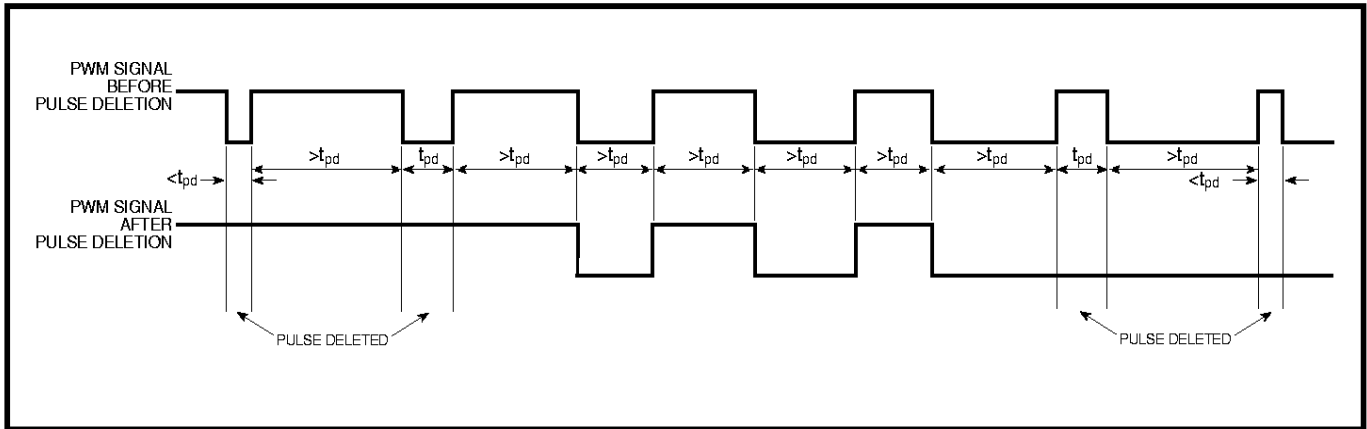


Fig.10 The effect of the pulse deletion circuit

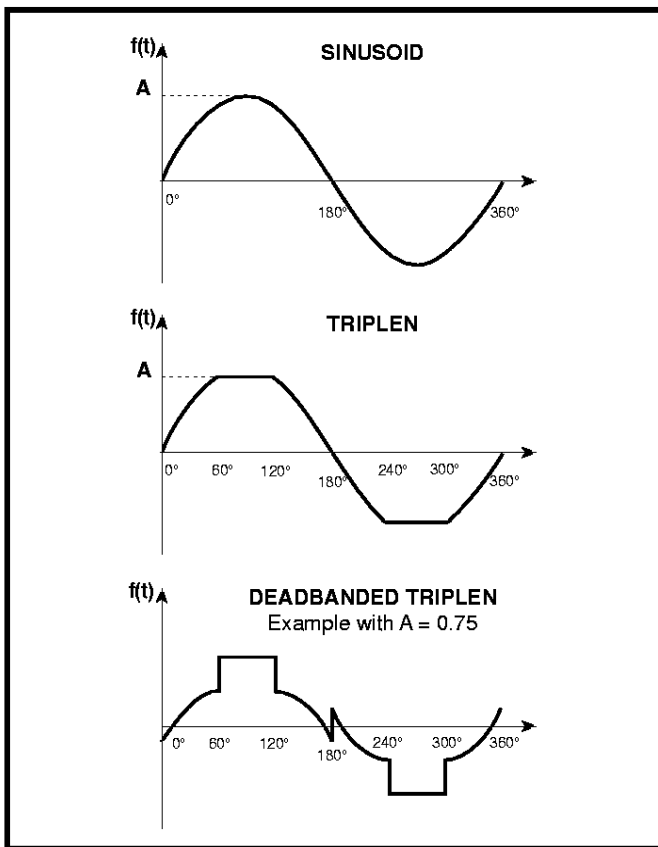


Fig.11 Power waveforms

Voltage/Frequency Gradient Selection

GRAD7	GRAD6	GRAD5	GRAD4	GRAD3	GRAD2	GRAD1	GRAD0
MSB				LSB			

Table 9 Voltage/frequency gradient

This parameter is used to define the Voltage/Frequency gradient in the Constant Torque region of motor operation - as shown in Fig.7. Its value is dependent upon the Pedestal value and the Base Frequency, f_{base} , according to the following equation:

$$GRAD = \frac{(255 - PED) f_{RANGE}}{f_{base} \times 16}$$

where $0 \leq GRAD \leq 255$.

Pedestal Selection

PED7	PED6	PED5	PED4	PED3	PED2	PED1	PED0
MSB				LSB			

Table 10 Pedestal values

This Pedestal value defines the voltage present on the motor at zero frequency and is used to counteract the effect of winding resistance which tends to dominate the overall losses at low speeds. The specific value should be chosen carefully to ensure that the power dissipation in the motor is not excessive.

$$\text{Pedestal value (\%)} = \frac{PED \times 100}{255}$$

where $0 \leq PED \leq 255$.

If GRAD = 0 then voltage is set independently of the power frequency and is given by the Pedestal value calculated above. PED = 255 gives 100% output voltage across the power frequency range irrespective of the value of GRAD.

Hardware Input/Output Functions

SET TRIP Input

The SET TRIP input allows an external, active high event to provide a rapid shutdown of the PWM signals. When the SET TRIP input remains high for a period of 3-4 crystal clock cycles, then the PWM outputs will be shut down and the TRIP acknowledge output will become active.

This condition can only be cleared by applying a RESET cycle.

The SET TRIP input has an internal pull-down resistor. However, it is recommended that this input is tied low if it is not used.

TRIP Output

The TRIP output indicates the status of the trip latch and is active low. It does not become active until the end of the SET TRIP delay time (assuming that the SET TRIP input stays high for this period).

This output is capable of directly driving an LED through a current limiting resistor for display purposes.

RESET Input

The RESET input is active low and performs the following functions:-

- i) All PWM outputs are forced low.
 - ii) All internal counters are reset to zero.
 - iii) The instantaneous frequency word is set to zero and the direction bit to 1 (forward).
 - iv) When released, the rising edge reactivates the PWM outputs and sets the trip latch to inactive, provided that the SET TRIP input is inactive and SET [1:4] $\neq 0$.
- The removal of RESET forces the phase bottom outputs to be driven high for a whole carrier cycle before the phase top outputs are enabled if SET [1:4] $\neq 0$.

As a consequence of (iii) and (iv) the device will be re-enabled and will re-accelerate when reset after a TRIP event.

XTAL1/XTAL2

These pins are for the crystal or ceramic resonator, if used. Alternatively, XTAL1 may be used as an input for an externally generated clock signal. Any external input is constrained to having a mark/space ratio between 40% and 60% to ensure correct device operation.

A small capacitor should be connected from each of these pins to the negative supply rail when using a crystal or ceramic resonator. Capacitor values are dependant on the crystal characteristics. Typical values are in the range 22-56pF.

V_{MON} Input

Analog input which, when $>V_{thr}$ suspends acceleration and deceleration. This input has higher priority than the I_{MON} pin and the V_{MON} condition therefore prevails if both V_{MON} and I_{MON} are active simultaneously.

DIR Input

Logic input which, in combination with Enable DIR and Internal Sign bits, allows the direction of rotation of PWM outputs to be reversed. A high input (when allowed by Enable DIR bit) causes forward rotation (R-Y-B) and low causes reverse rotation (R-B-Y).

I_{MON} Input

Analog input which causes the instantaneous output frequency to reduce at the predetermined deceleration rate when $>V_{thr}$. If the frequency is reduced to zero while this input is $>V_{thr}$ the PWM outputs are temporarily shut down and the deceleration inhibited.

Note that I_{MON} is an override condition which does not affect the frequency and direction demand values selected from the Speed Reference Table. Once I_{MON} has fallen below V_{thr}, the frequency and direction demands selected according to the value of SET [1:4] are re-imposed immediately and appropriate acceleration/deceleration takes place.

If the outputs had been shutdown as the result of an I_{MON} condition, the removal of this condition will cause the outputs to go through the bootstrap-capacitor charging sequence providing SET [1:4] $\neq 0$. All the bottom phase outputs are asserted high for a whole carrier cycle before normal PWM operation is resumed.

Programming Example (SA868001)

The following example illustrates how the Initialisation Parameters are calculated to provide the data required for the Factory mask programmed ROM. A special order form is available on which information must be submitted. Please contact your local Customer Service Centre for details.

Note that the values shown in this example are actually the same as used in the SA868001 Demonstrator IC.

1. Crystal frequency

Chosen as 20MHz since such crystals are low cost and readily available.

2. Carrier frequency

Set to maximum so that switching is ultrasonic- i.e. out of the audible range.

$$f_{CARR} = \frac{f_{CLK}}{512 \times 2^{n+1}}$$

With $f_{CLK} = 20 \times 10^6$ and $n = 0$ this gives $f_{CARR} = 19531.25\text{Hz}$, i.e. inaudible

Therefore **CFS** = 000b.

3. Power frequency range

We want 400Hz as the highest of the 16 frequencies set up in the speed ROM, so select the next highest range.

$$f_{RANGE} = \frac{f_{CARR} \times 2^m}{384}$$

With $f_{CARR} = 19531.25\text{Hz}$ and $m = 3$ this gives $f_{RANGE} = 406.90\text{Hz}$.

Therefore **FRS** = 011b.

4. Pulse delay time

Choose a 'safe' figure which will be okay even with slow IGBT's- say 2.4 μs .

$$t_{pd} = \frac{(63 - PDY)}{f_{CARR} \times 512}$$

Therefore: PDY = 39d = **27h**.

5. Pulse deletion

Choose a figure close to pulse delay time- say 2 μs . Since the pulse delay logic follows the pulse deletion logic, and given that the pulse delay logic alters the length of pulses, the actual minimum pulse length is equal to the difference between the two delays. In other words, we must compensate for the pulse delay time by adding its value to pulse deletion.

Therefore, required pulse deletion time is 4.4 μs .

$$t_{pd} = \frac{(127 - PDT)}{f_{CARR} \times 512}$$

Therefore: PDT = 83d = **53h**.

6. Waveform

For maximum efficiency driving a 3-phase motor set the waveform to Deadbanded Triplen.

i.e. WS1 = 1 and WS0 = 0

Therefore **WS** = 10b.

7. Pedestal

Choose Pedestal = 10%. This is suitable for smaller motors (required pedestal falls with increasing motor size).

$$\text{Pedestal} = \frac{\text{PED} \times 100}{255}$$

This gives 25.5. Use PED = 25d so that pedestal does not exceed 10%. In fact this gives **Pedestal = 9.8%**.

Therefore **PED = 19h**.

8. Gradient

A choice is usually necessary here between selecting 50Hz or 60Hz base frequency. Since 50Hz Base Frequency gives better torque when running at 50Hz, we will select this value.

$$\text{GRAD} = \frac{(255 - \text{PED}) \times f_{\text{RANGE}}}{f_{\text{base}} \times 16}$$

This gives GRAD = 116.98

Therefore use GRAD = 117d = **75h**.

Actual **Base Freq.** is then **49.99Hz**.

9. Speed Reference Table

Table 11 shows the speeds programmed into the SA868001 Demonstrator IC. These include the most common motor base-plate frequencies - 50Hz, 60Hz and 400Hz. Most allow the use of the external DIR pin for maximum user flexibility. A sample speed calculation for SPD3:

$$f_{\text{POWER}} = \frac{\text{SPD3}}{65536} \times f_{\text{RANGE}}$$

For a desired speed (power frequency) of 30Hz and a frequency range of 406.90Hz, SPD3 = 4831.85d. Rounding to 4832 (=12E0h) gives an actual power frequency of 30.001Hz.

Programming Example (SA868010)

All parameters as previous example except waveform is Sine (required for single phase applications). Therefore **WS = 00b**.

The Speed Reference Table for this variant is also slightly different, see table 12.

Speed ROM Location	Frequency (Hz)	Direction	INT_SIGN (Bit-17)	EXT_SIGN (Bit-16)	18-Bit Speed Word (HEX)
SPD0	0	INT+	1 (Fixed)	0 (Fixed)	20000 (fixed)
SPD1	10	EXT	X	1	1064B
SPD2	20	EXT	X	1	10C95
SPD3	30	EXT	X	1	112E0
SPD4	40	EXT	X	1	1192A
SPD5	50	INT+	1	0	21F75
SPD6	50	INT-	0	0	01F75
SPD7	50	EXT	X	1	11F75
SPD8	60	EXT	X	1	125C0
SPD9	70	EXT	X	1	12C0A
SPD10	80	EXT	X	1	13255
SPD11	90	EXT	X	1	138A0
SPD12	100	EXT	X	1	13EEA
SPD13	150	EXT	X	1	15E5F
SPD14	200	EXT	X	1	17DD4
SPD15	400	EXT	X	1	1FBA9

Table 11 SA868001 Speed reference table (Note: X = Don't care, set to 0)

Speed ROM Location	Frequency (Hz)	Direction	INT_SIGN (Bit-17)	EXT_SIGN (Bit-16)	18-Bit Speed Word (HEX)
SPD0	0	INT+	1 (Fixed)	0 (Fixed)	20000 (fixed)
SPD1	10	INT+	1	X	2064B
SPD2	20	INT+	1	X	20C95
SPD3	30	INT+	1	X	212E0
SPD4	40	INT+	1	X	2192A
SPD5	49	INT+	1	X	21ED4
SPD6	50	INT+	1	X	21F75
SPD7	51	INT+	1	X	22016
SPD8	60	INT+	1	X	225C0
SPD9	70	INT+	1	X	22C0A
SPD10	80	INT+	1	X	23255
SPD11	90	INT+	1	X	238A0
SPD12	100	INT+	1	X	23EEA
SPD13	150	INT+	1	X	25E5F
SPD14	200	INT+	1	X	27DD4
SPD15	400	INT+	1	X	2FBA9

Table 12 SA868010 Speed reference table (Note: X = Don't care, set to 0)

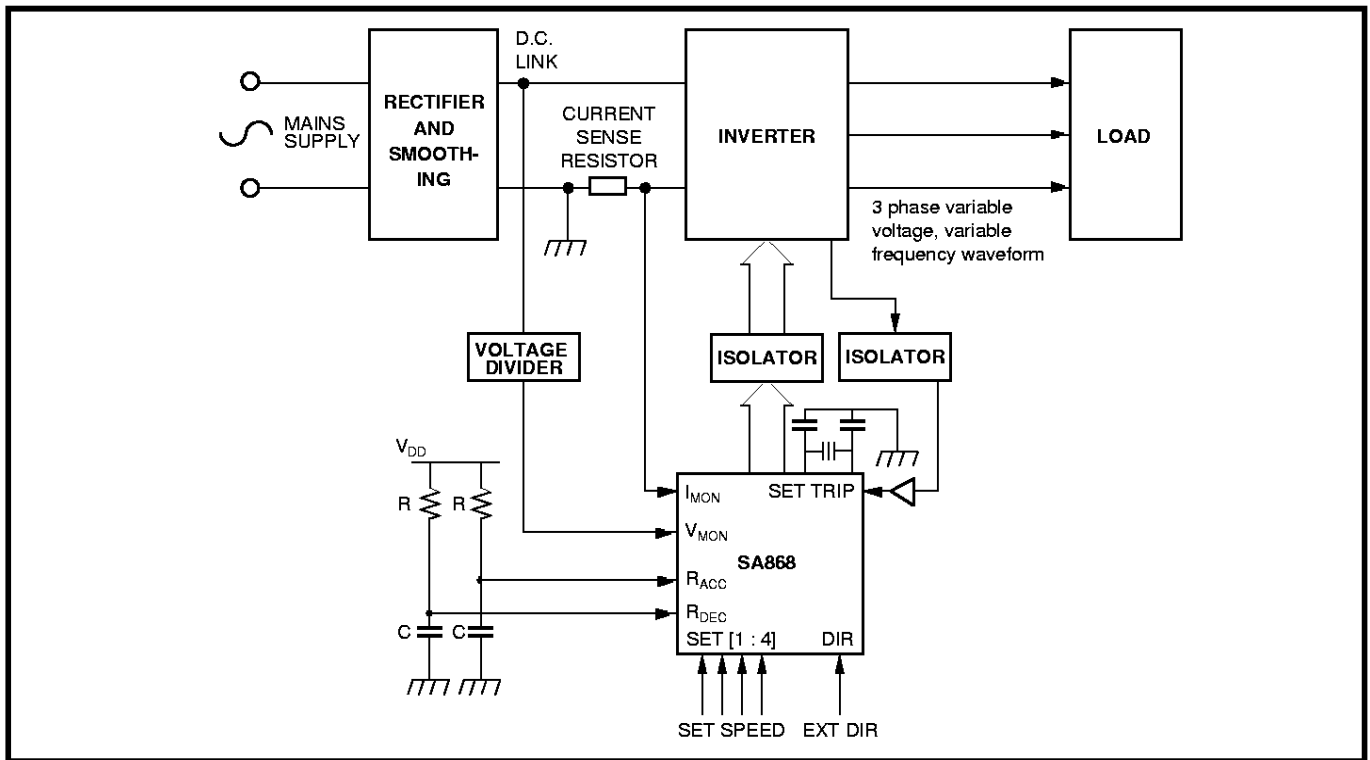
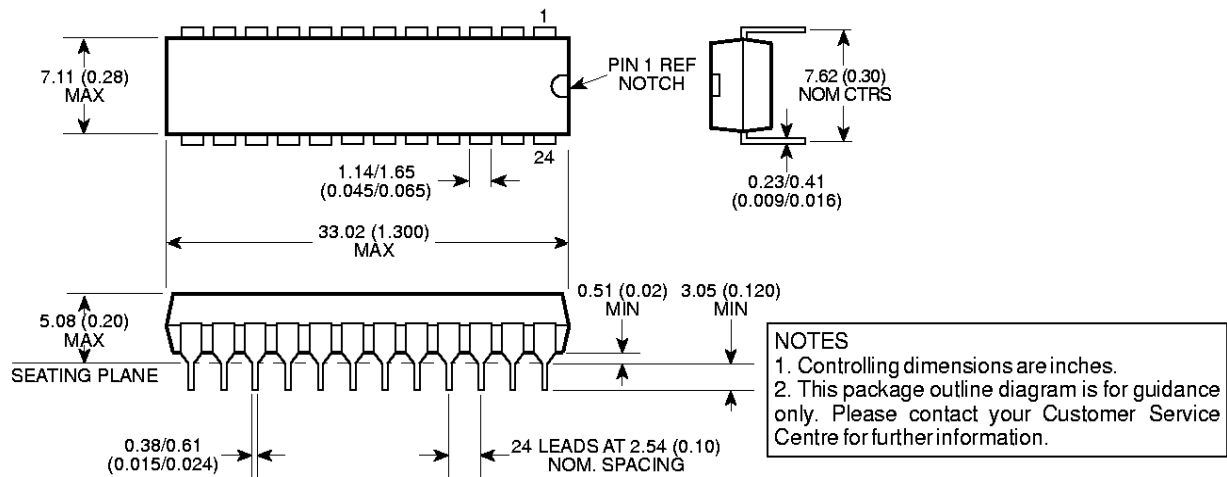


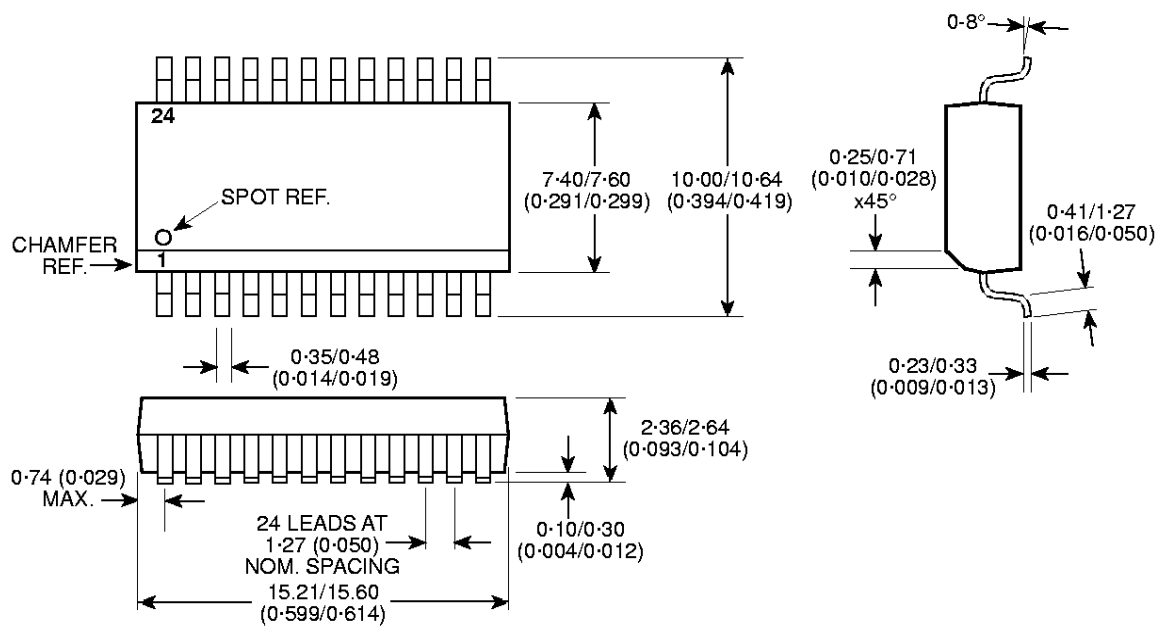
Fig.12 Typical applications circuit

Package Details

Dimensions are shown thus: mm (in). For further package information, please contact your nearest representative or Customer Service Centre.



24-LEAD PLASTIC SKINNY DIL - DP24



24-LEAD MINIATURE PLASTIC DIL - MP24



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