Voltage Detector (Reset) IC Series for Automotive Application

Free Time Delay Setting CMOS Voltage Detector (Reset) IC

BD52xxNVX-2C Series BD5320NVX-2C

General Description

ROHM's Free Time Delay Setting CMOS Voltage Detector ICs are highly accurate, with ultra-low current consumption feature that uses CMOS process. Delay time setting can be control by an external capacitor. The lineup includes N-channel open drain output (BD52xx NVX-2C) and CMOS output (BD5320NVX-2C). The devices are available for specific detection voltage is 1.4 V, 1.6 V, 2.0 V, 2.6 V to 3.1 V (0.1 V step).
The time delay has ±50 % accuracy in the overall operating temperature range of -40 °C to 125 °C.

Features

- AEC-Q100 Qualified *(Note 1)*
- Nano Energy™
- Delay Time Setting Controlled by External Capacitor
- Two output types (Nch open drain and CMOS output)
- Miniature Surface-mount Package

(Note 1) Grade 1

Key Specifications

- Detection Voltage: 1.4 V, 1.6 V, 2.0 V, 2.6 V, 2.7 V 2.8 V, 2.9 V, 3.0 V, 3.1 V(Typ)
- Ultra-Low Current Consumption: 270 nA (Typ)
- Time Delay Accuracy: ±50 % (-40 °C to +125 °C, CT pin capacitor ≥ 1 nF)

Special Characteristics

- Detection Voltage Accuracy:
  ±3.0 %±12 mV (V_{DET}=1.4 V, 1.6 V)
  ±2.5 %(V_{DET}=2.0 V, 2.6 V to 3.1 V)

Package

W(Typ) x D(Typ) x H(Max)

SSON004R1010: 1.00 mm x 1.00 mm x 0.60 mm

Application

All automotive devices that requires voltage detection

Typical Application Circuit

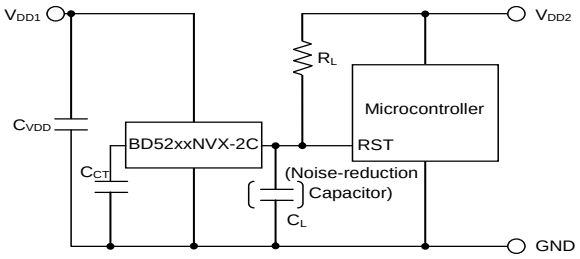


Figure 1. Open Drain Output Type
BD52xxNVX-2C Series

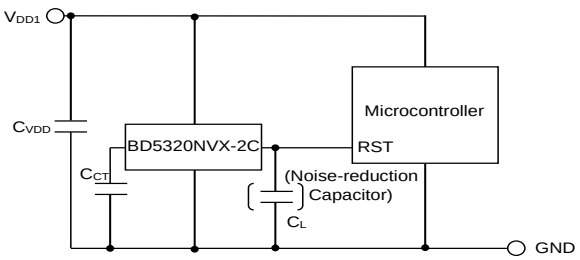
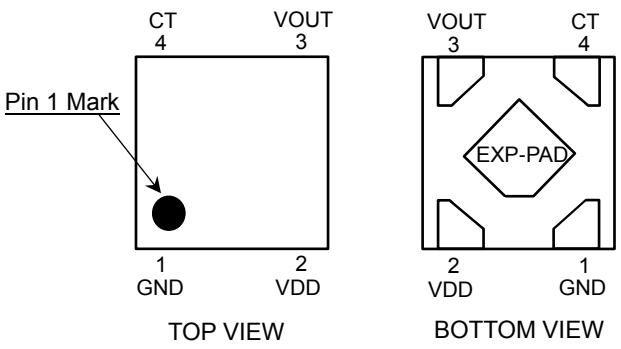


Figure 2. CMOS Output Type
BD5320NVX-2C

Pin Configuration

SSON004R1010



Pin Description

SSON004R1010		
PIN No.	PIN NAME	Function
1	GND	GND
2	VDD	Power supply voltage
3	VOUT	Output pin
4	CT	Capacitor connection pin for output delay time setting
-	EXP-PAD	Same potential with substrate voltage (V_{DD}), it is recommended to connect to V_{DD} or can be left open

Block Diagram

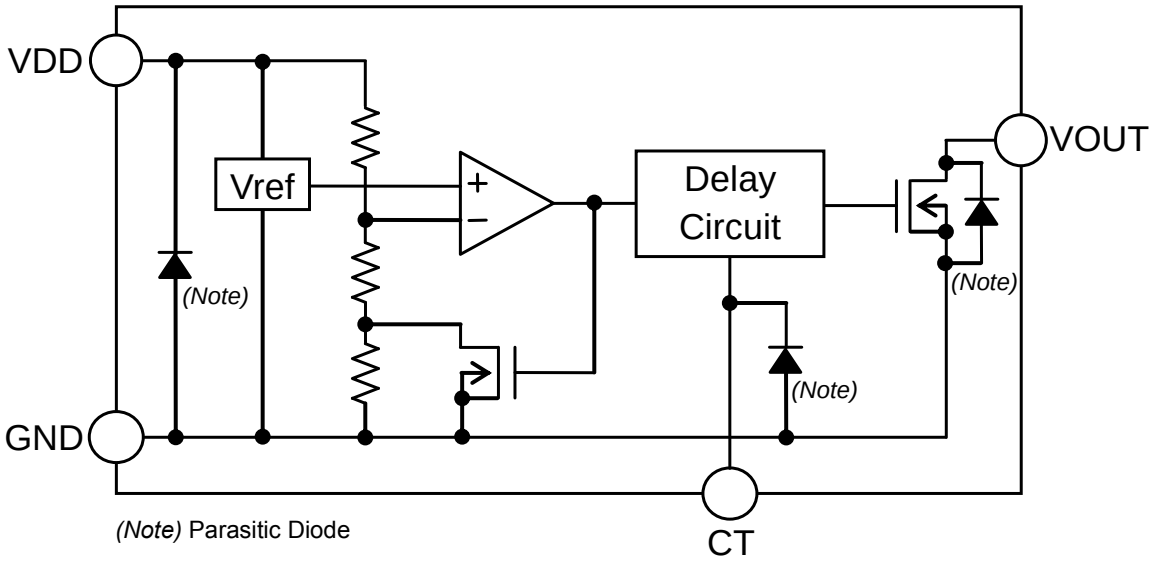


Figure 3. BD52xxNVX-2C Series

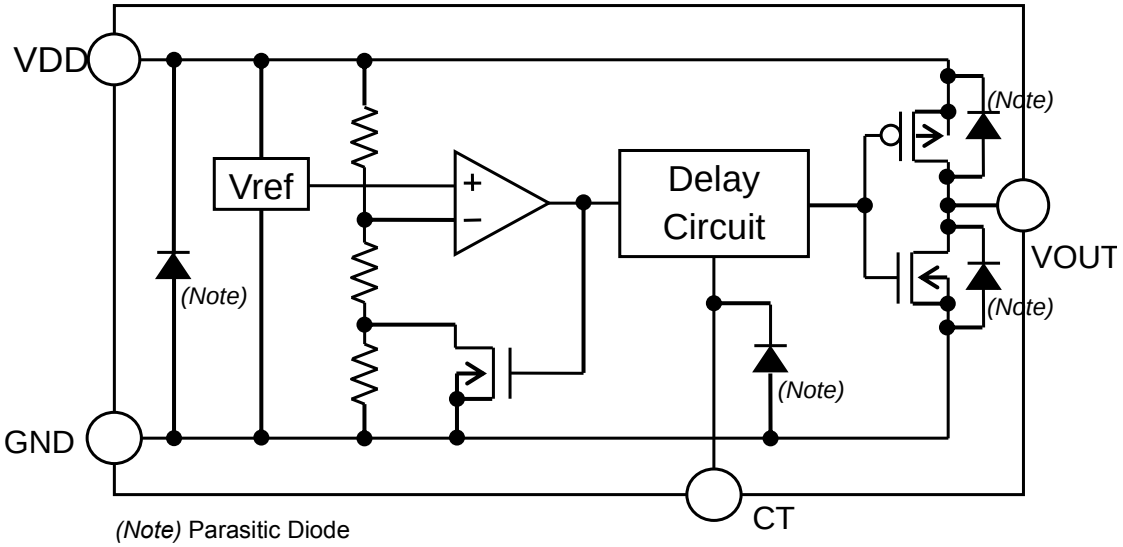


Figure 4. BD5320NVX-2C

Ordering Information

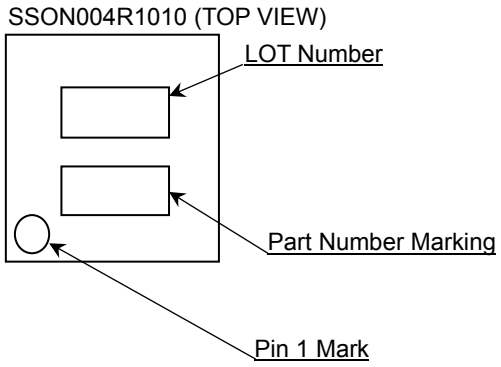
B D x x x x N V X - 2 C T L

- Output Type: 52 : Open Drain; 53 : CMOS
- Detection Voltage: 14 : 1.4 V; 16 : 1.6 V; 20 : 2.0 V; 26 : 2.6 V; ↓ 0.1 V step; 31 : 3.1 V
- Package: NVX : SSON004R1010
- Product Rank: C : for Automotive
- Packing and Forming Specification: TL : Embossed tape and reel

Lineup

Output Type	Open Drain		CMOS	
Detection Voltage	Marking	Part Number	Marking	Part Number
3.1 V	6l	BD5231NVX	-	-
3.0 V	5l	BD5230NVX	-	-
2.9 V	4l	BD5229NVX	-	-
2.8 V	3l	BD5228NVX	-	-
2.7 V	2l	BD5227NVX	-	-
2.6 V	1l	BD5226NVX	-	-
2.0 V	-	-	nl	BD5320NVX
1.6 V	g	BD5216NVX	-	-
1.4 V	e	BD5214NVX	-	-

Marking Diagram



Absolute Maximum Ratings (Ta=25 °C)

Parameter		Symbol	Limit	Unit
Power Supply Voltage		V_{DD} - GND	-0.3 to +7	V
Output Voltage	Nch Open Drain Output	V_{OUT}	GND-0.3 to +7	V
	CMOS Output		GND-0.3 to V_{DD}+0.3	
Output Current		I_O	70	mA
Maximum Junction Temperature		Tjmax	+150	°C
Storage Temperature Range		Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
SSON004R1010				
Junction to Ambient	θ_{JA}	450.2	97.1	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	99	22	°C/W

(Note 1) Based on JESD51-2A(Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connects with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Function Explanation

1. Nano Energy™
   Nano Energy™ is a combination of technologies which realizes ultra low quiescent current operation.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature	Topr	-40	+25	+125	°C

Electrical Characteristics (Unless otherwise specified Ta=-40 °C to +125 °C, VDD=0.8 V to 6.0 V)

Parameter	Symbol	Condition	Limit			Unit
			Min	Typ	Max	
Detection Voltage	V_{DET}	V_{DET}=1.4 V, 1.6 V, V_{DD}=H→L, R_L=100 kΩ *(Note 2)*	$V_{DET}(T)$ ×0.97 -0.012	$V_{DET}(T)$ *(Note 1)*	$V_{DET}(T)$ ×1.03 +0.012	V
		V_{DET}=2.0 V~3.1 V, V_{DD}=H→L, R_L=100 kΩ *(Note 2)*	$V_{DET}(T)$ ×0.975	$V_{DET}(T)$ *(Note 1)*	$V_{DET}(T)$ ×1.025	
Hysteresis Voltage	Δ V_{DET}	V_{DD}=L→H→L, R_L=100 kΩ	V_{DET} ×0.035	V_{DET} ×0.05	V_{DET} ×0.065	V
Circuit Current when ON	I_{DD1}	V_{DD}=V_{DET}-0.2 V	-	0.23	1.50	μA
Circuit Current when OFF	I_{DD2}	V_{DD}=V_{DET}+0.5 V	-	0.27	1.60	μA
Minimum Operating Voltage	V_{OPL}	V_{OL}≤0.4 V, R_L=100 kΩ *(Note 2)*	0.80	-	-	V
"Low" Output Voltage(Nch)	V_{OL}	V_{DD}=0.8 V, I_{SINK}=0.17 mA, V_{DET}=1.4 V, 1.6 V	-	-	0.4	V
		V_{DD}=1.2 V, I_{SINK}=1.0 mA, V_{DET}=2.0 V to 3.1 V	-	-	0.4	
		V_{DD}=2.4 V, I_{SINK}=2.0 mA, V_{DET}=2.6 V to 3.1 V	-	-	0.4	
"High" Output Voltage(Pch)	V_{OH}	V_{DD}=4.8 V, I_{SOURCE}=2.0 mA, V_{DET}=2.0 V	V_{DD}-0.4	-	-	V
		V_{DD}=6.0 V, I_{SOURCE}=2.5 mA, V_{DET}=2.0 V	V_{DD}-0.4	-	-	
Output Leak Current	Ileak	V_{DD}=V_{DS}=6 V	-	-	1.0	μA
Delay Time(L→H)	t_{PLH}	V_{OUT}=GND→50 %, C_{CT}=0.01 μF *(Note 3) (Note 4)*	27.7	55.5	83.2	ms

(Note 1) $V_{DET}(T)$: Standard Detection Voltage (1.4 V, 1.6 V, 2.0 V, 2.6 V, 2.7 V, 2.8 V, 2.9 V, 3.0 V, 3.1 V)
(Note 2) R_L: Pull-up resistor connected between V_{OUT} and power supply
(Note 3) t_{PLH}: V_{DD}=($V_{DET}(T)$–0.5 V) → ($V_{DET}(T)$+0.5 V) for V_{DET}=1.4 V, 1.6 V, 2.0 V, 2.6 V, 2.7 V, 2.8 V, 2.9 V, 3.0 V, 3.1 V
(Note 4) CT delay capacitor range: open to 4.7 μF

Typical Performance Curves

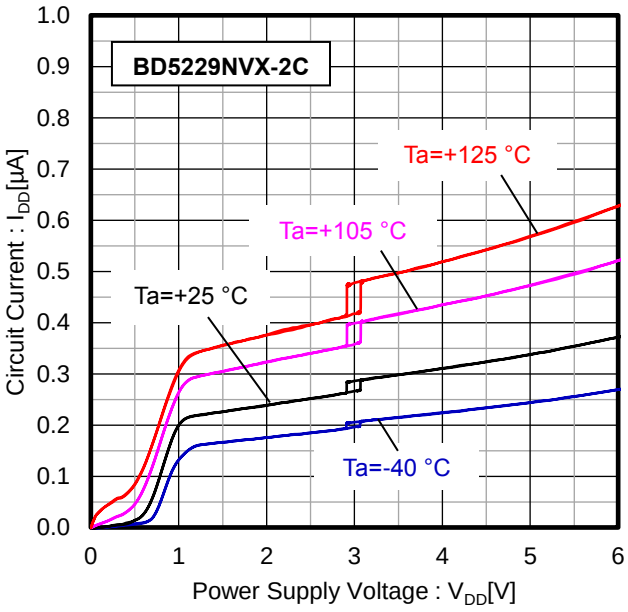


Figure 5. Circuit Current vs Power Supply Voltage

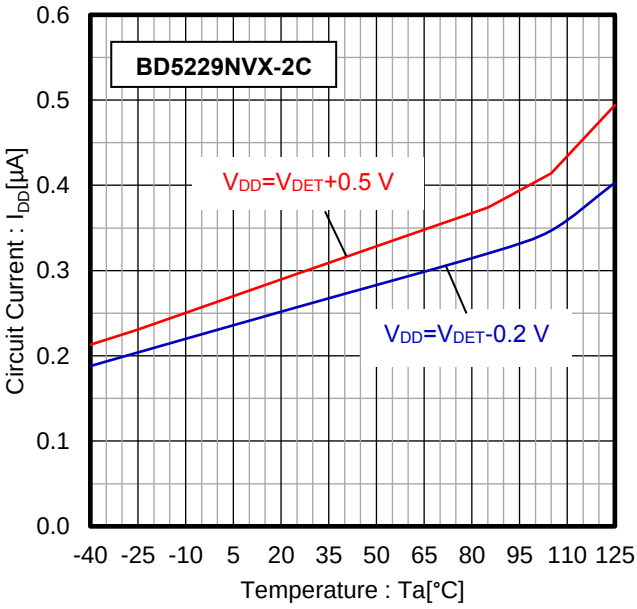


Figure 6. Circuit Current vs Temperature

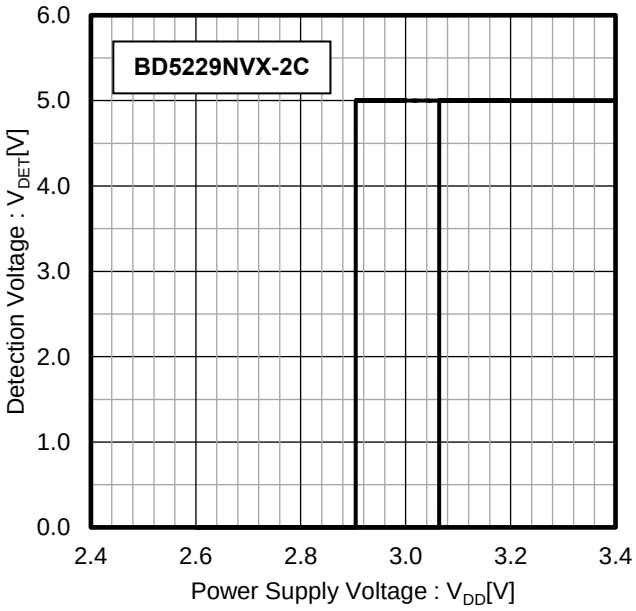


Figure 7. Detection Voltage vs Power Supply Voltage

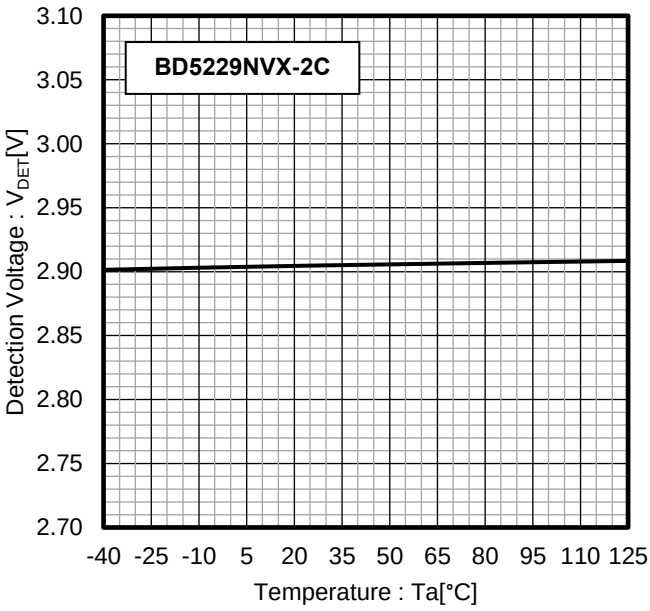


Figure 8. Detection Voltage vs Temperature

Typical Performance Curves - continued

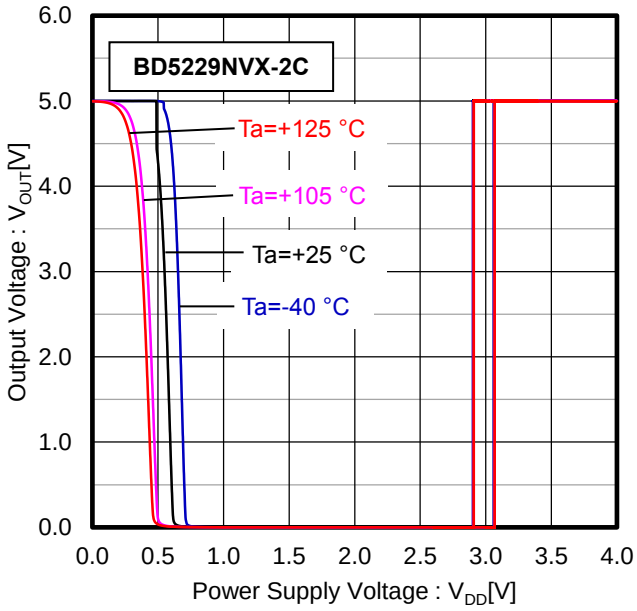


Figure 9. I/O Characteristics
(VOUT Pull-up to 5 V, R_L=100 kΩ)

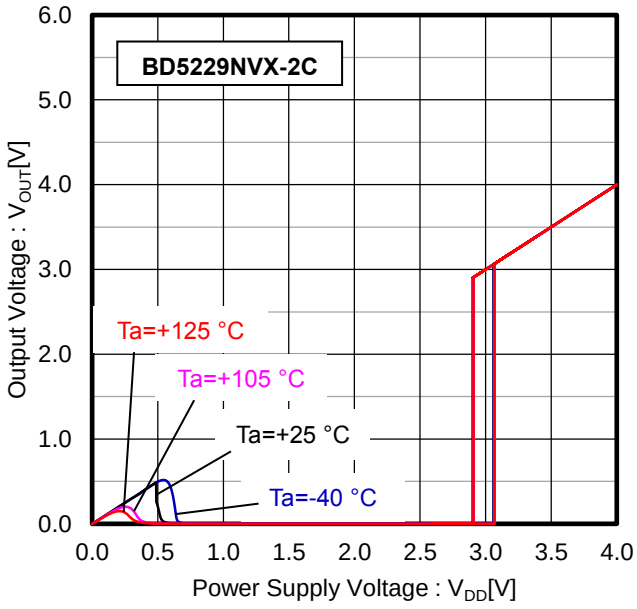


Figure 10. I/O Characteristics
(VOUT Pull-up to V_{DD}, R_L=100 kΩ)

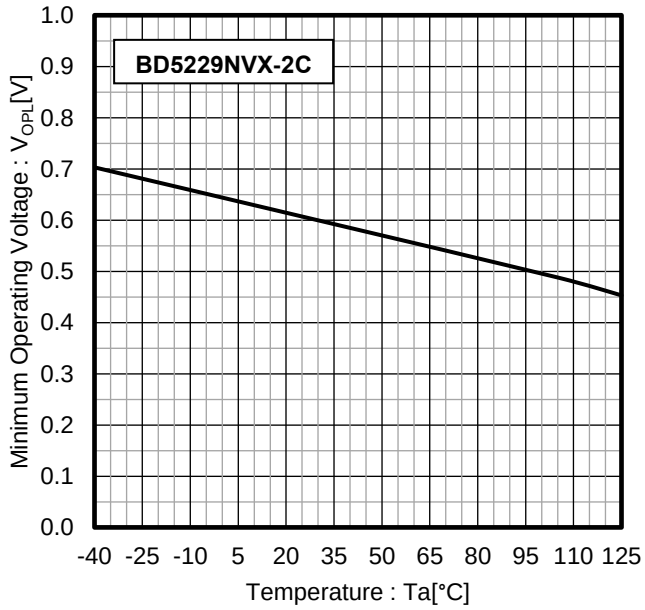


Figure 11. Minimum Operating Voltage vs Temperature
(VOUT Pull-up to 5 V, R_L=100 kΩ)

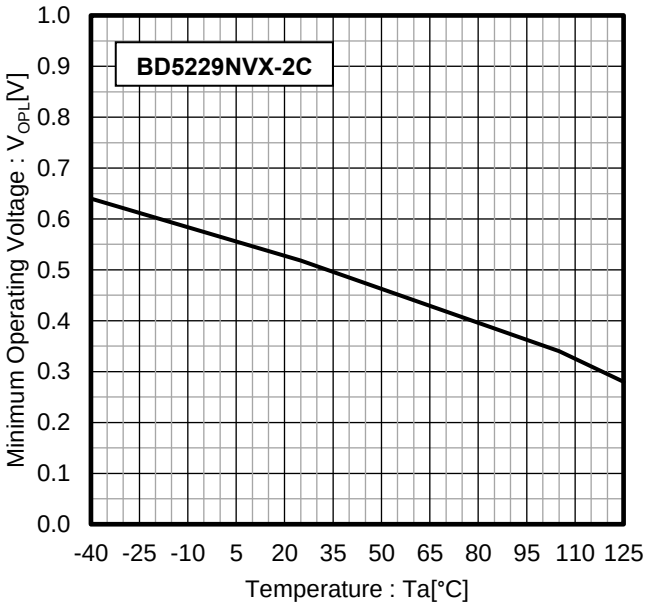


Figure 12. Minimum Operating Voltage vs Temperature
(VOUT Pull-up to V_{DD}, R_L=100 kΩ)

Typical Performance Curves - continued

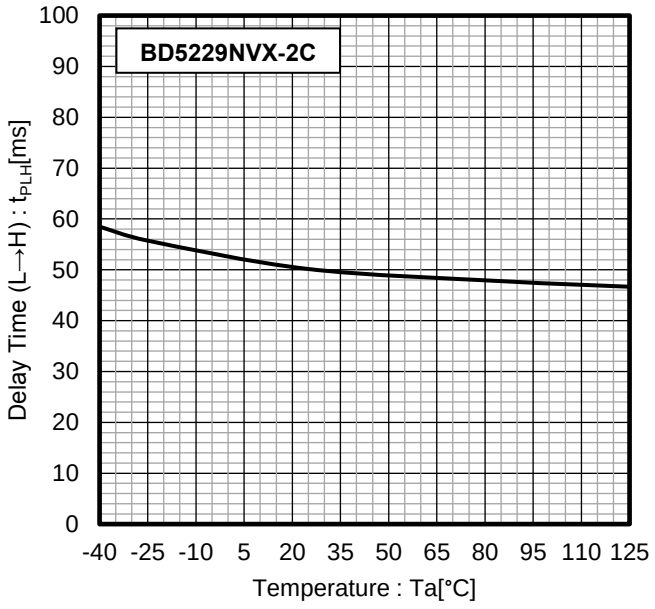


Figure 13. Output Delay Time (L→H) vs Temperature (C_{CT}=10 nF)

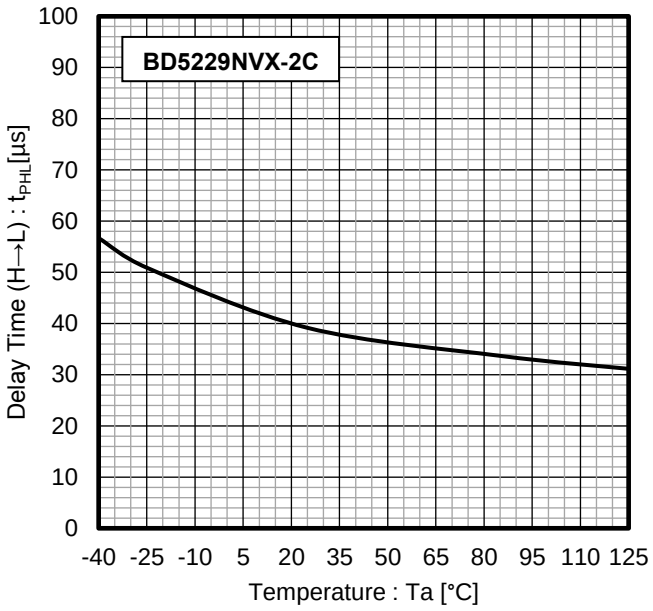


Figure 14. Output Delay Time (H→L) vs Temperature

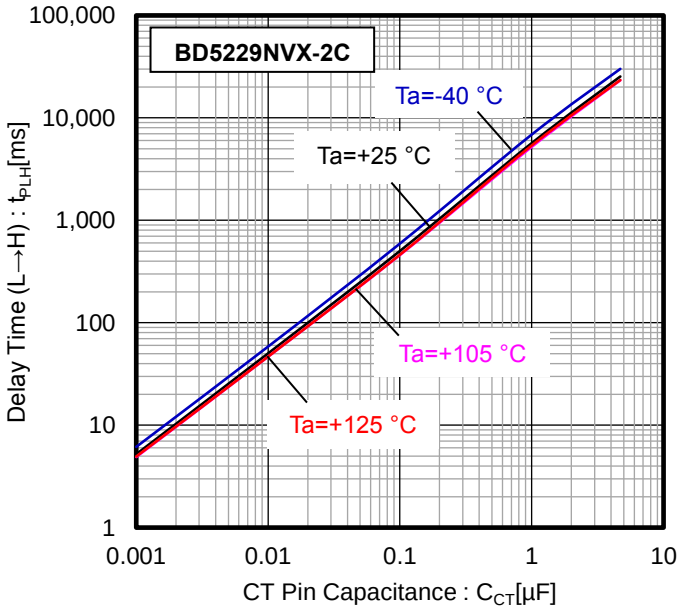


Figure 15. Output Delay Time (L→H) vs CT Pin Capacitance

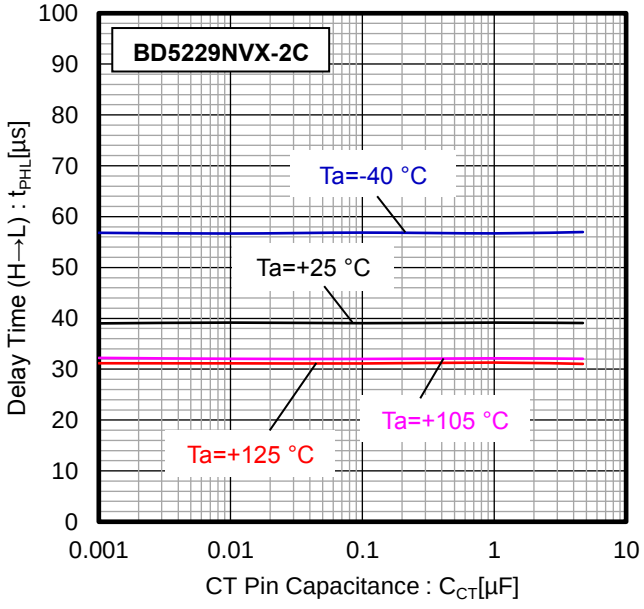


Figure 16. Output Delay Time (H→L) vs CT Pin Capacitance

Typical Performance Curves - continued

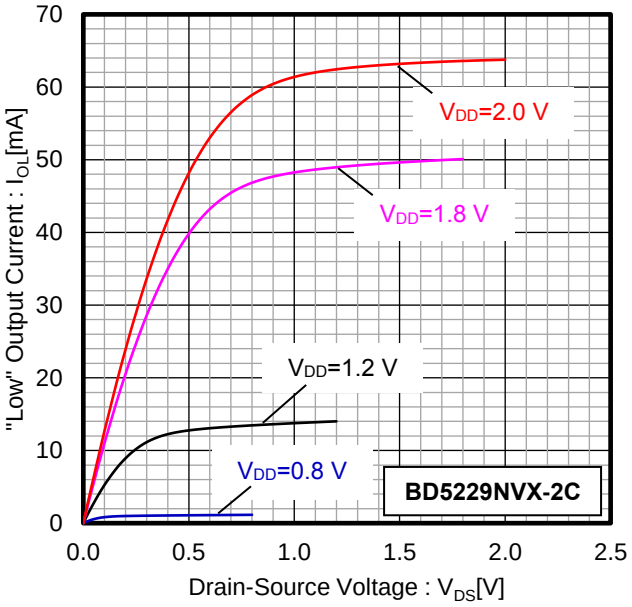


Figure 17. “Low” Output Current vs Drain-Source Voltage

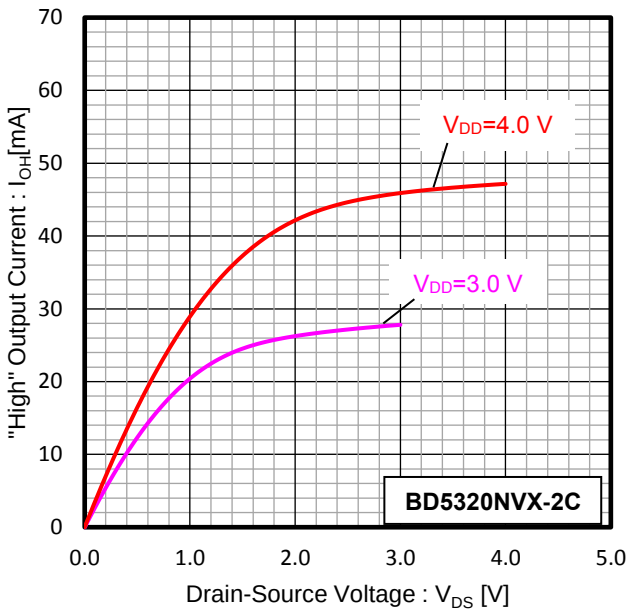


Figure 18. “High” Output Current vs Drain-Source Voltage

Application Information

Operation Description

The detection and release voltage are used as threshold voltages. When the voltage applied to the V_{DD} reaches the applicable threshold voltage, the V_{OUT} level switches from either “H”→“L” or from “L”→“H”. BD52xxNVX-2C series and BD5320NVX-2C have delay time function, which set t_{PLH} (output “L”→”H”) using an external capacitor connected in CT pin (C_{CT}).

Because the BD52xxNVX-2C series uses an open drain output type, it is necessary to connect a pull up resistor to V_{DD} or another power supply. [In this case, the output (V_{OUT}) “H” voltage becomes V_{DD} or the voltage of the other power supply].

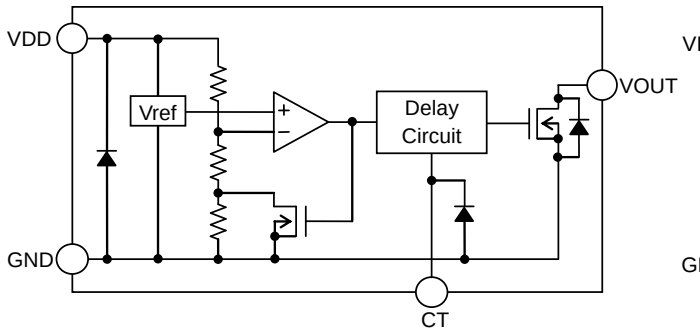


Figure 19. (BD52xxNVX-2C type internal block diagram)

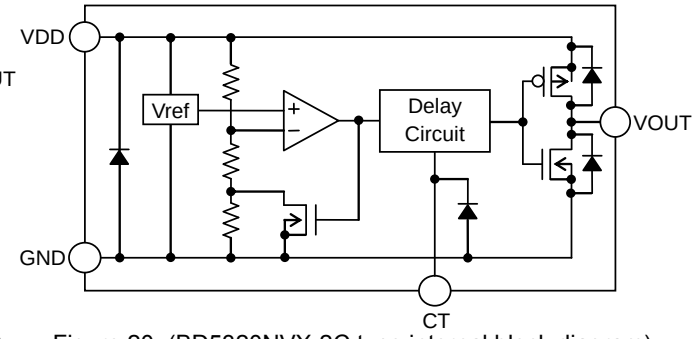


Figure 20. (BD5320NVX-2C type internal block diagram)

Setting of Detector Delay Time

Delay time L→H (t_{PLH}) is the time when V_{OUT} rises to 1/2 of V_{DD} after V_{DD} rises up and beyond the release voltage ($V_{DET}+\Delta V_{DET}$).

Delay time L→H (t_{PLH}) is determined by CT capacitor and can be calculated from the following formula. When CT capacitor ≥ 1nF, t_{CTO} has less effect and t_{PLH} computation is shown on Example No.2. The result has ±50 % tolerance within the operating temperature range of -40 °C to +125 °C.

Formula: (Ta=25 °C)

$$t_{PLH} = C_{CT} \times Delay\ Coefficient + t_{CTO} \quad [s]$$

where:

C_{CT} is the CT pin external capacitor

Delay Coefficient is equal to 5.55 x 10^6

t_{CTO} is the delay time when CT=open *(Note 1)*

Temperature	Delay Time (t_{CTO})		
	Min	Typ	Max
Ta = -40 °C to +125 °C	15 µs	50 µs	150 µs

(Note 1) t_{CTO} is design guarantee only

Example No.1:

CT capacitor = 100 pF

$$t_{PLH\_min} = (100 \times 10^{-12} \times 5.55 \times 10^{6}) \times 0.5 + 15 \times 10^{-6} = 292\ \mu s$$

$$t_{PLH\_typ} = (100 \times 10^{-12} \times 5.55 \times 10^{6}) \times 1.0 + 50 \times 10^{-6} = 605\ \mu s$$

$$t_{PLH\_max} = (100 \times 10^{-12} \times 5.55 \times 10^{6}) \times 1.5 + 150 \times 10^{-6} = 983\ \mu s$$

Example No.2:

CT capacitor = 1 nF

$$t_{PLH\_typ} = 1 \times 10^{-9} \times 5.55 \times 10^{6} = 5.55\ ms$$

Application Information - continued

Timing Waveform

The following shows the relationship between the input voltage V_{DD} and the output voltage V_{OUT} when the power supply voltage V_{DD} is sweep up and sweep down.

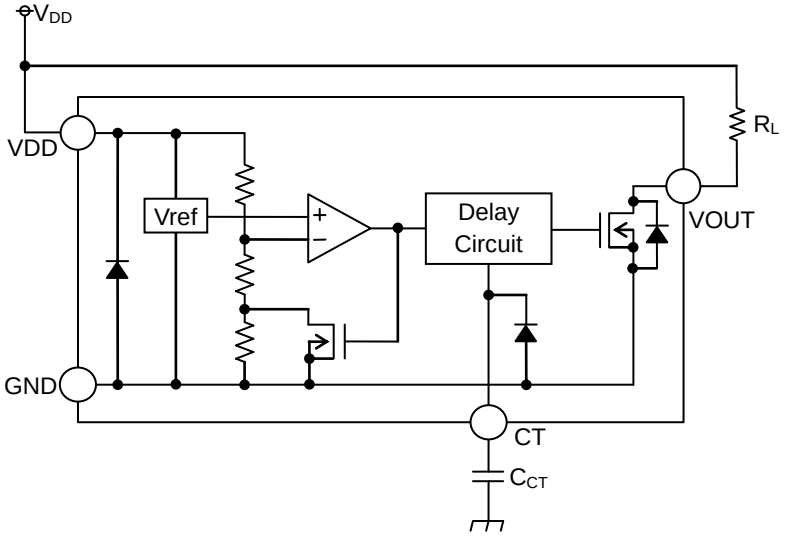


Figure 21. BD52xxNVX-2C Set-up

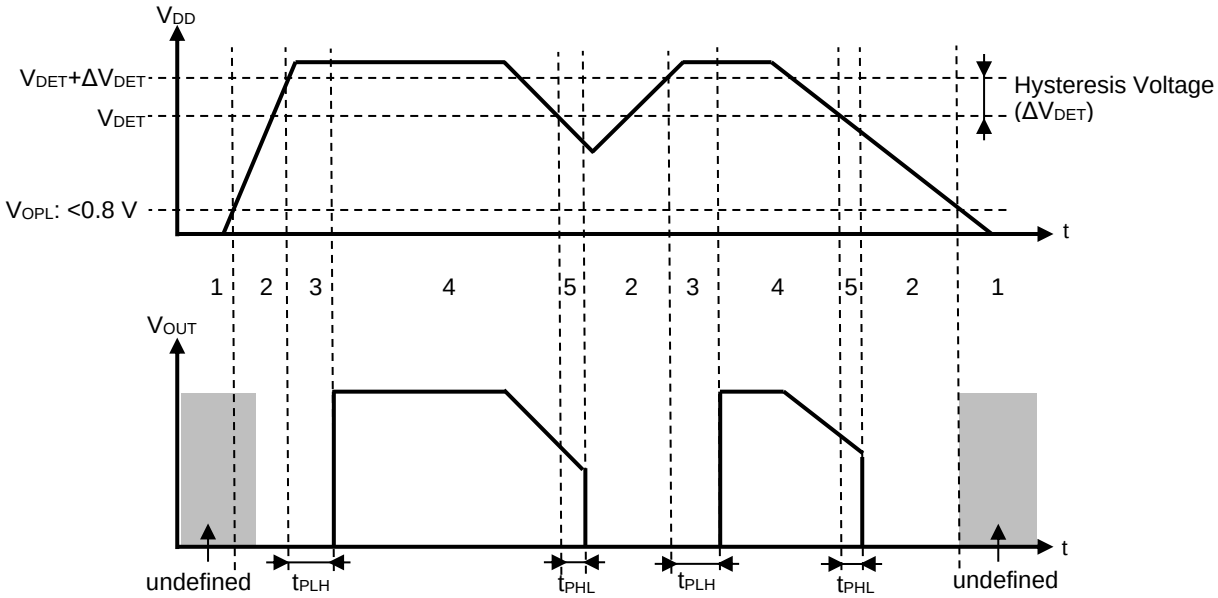


Figure 22. Timing Diagram

Operating Conditions Explanation

1 When the power supply turns on, the Output Voltage (V_{OUT}) becomes unstable until V_{DD} exceeds the Minimum Operating Voltage (V_{OPL}).
2 V_{OUT} changes to “L”. However, this change depends on the V_{OUT} rise time when the power supply starts up, so thorough confirmation is required.
3 When V_{DD} exceeds the release voltage ($V_{DET}+\Delta V_{DET}$), delay time (t_{PLH}) set by the capacitor at CT pin (C_{CT}) happens, then V_{OUT} switches from “L” to “H”.
4 V_{OUT} remains “H”.
5 When V_{DD} drops below Detection Voltage (V_{DET}), delay time (t_{PHL}) happens, then V_{OUT} switches from “H” to “L”.

The potential difference between the detection voltage and the release voltage is known as the Hysteresis Voltage width (ΔV_{DET}). The system is designed such that the output will not toggle with power supply fluctuations within this hysteresis width, preventing malfunctions due to noise.

Application Information – continued

Bypass Capacitor for Noise Rejection
To help reject noise, put more than 0.1 µF capacitor between VDD and GND pin and connect it closer to the pin as possible. Be careful when using extremely big capacitor as transient response will be affected.

External Parameters
The recommended value of CT capacitor is from open to 4.7 µF and pull-up resistance value is 50 kΩ to 1 MΩ. There are many factors (board layout, etc.) that can affect characteristics. Operating beyond the recommended values does not guarantee correct operation. Please verify and confirm using practical applications.
In addition, this IC has extremely high impedance pins. Small leak current due to the uncleanness of PCB surface might cause unexpected operations. Application values in these conditions should be selected carefully. For example, if a 10 MΩ leakage is assumed between VOUT and GND pin, consider to set the value of pull up resistor lower than 1/10 of the impedance of assumed leakage route.

Behavior when below the Operating Voltage Limit
When V_{DD} falls below the minimum operating voltage, output will be open. When output is connected to pull-up voltage, output will be equivalent to pull-up voltage.

CT Pin Discharge
Due to the capabilities of the CT pin discharge transistor, the CT pin may not completely discharge when a short input pulse is applied, and in this case the delay time may not be controlled. Please verify the actual operation.

Application Circuits

(1) Examples of common application circuits

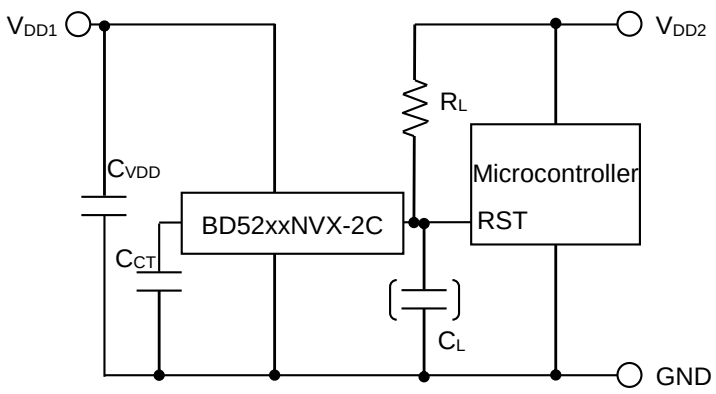


Figure 23. Open Drain Output Type

Application examples of BD52xxNVX-2C series (Open drain output type) and BD5320NVX-2C (CMOS output type) are shown below.

If the power supply of the microcontroller (V_{DD2}) differs from the power supply of the detection (V_{DD1}), use the load resistance R_L connected to V_{DD2} in the output of open drain output type (BD52xxNVX-2C series) as shown in Figure 23.

Power supply of the microcontroller (V_{DD1}) is the same as the power supply of the reset detection (V_{DD1}):
Use a CMOS output type (BD5320NVC-2C) device as shown in Figure 24, or an open-drain output type (BD52xxNVX-2C series) device with a pull-up resistor between the output and V_{DD1}.

When connecting a capacitor C_L for noise elimination and for output time delay setting to VOUT pin (reset signal input pin of micro-controller), the waveform is dull during rising and falling of the output so use after confirmation that there is no problem.

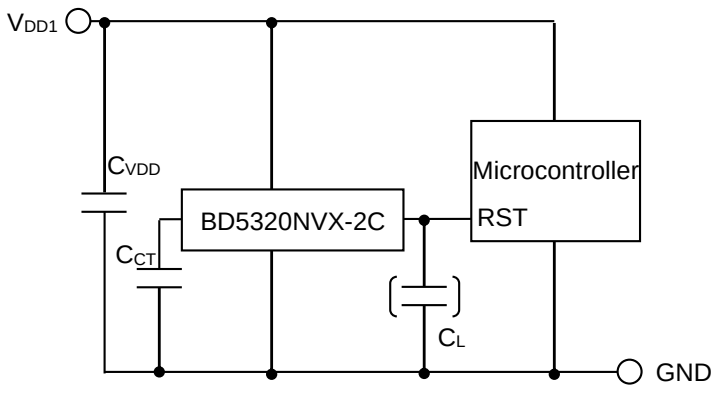


Figure 24. CMOS Output Type

Application Circuits – continued

(2) The following is an example of an OR connection between two types of detection voltage resets the microcontroller.

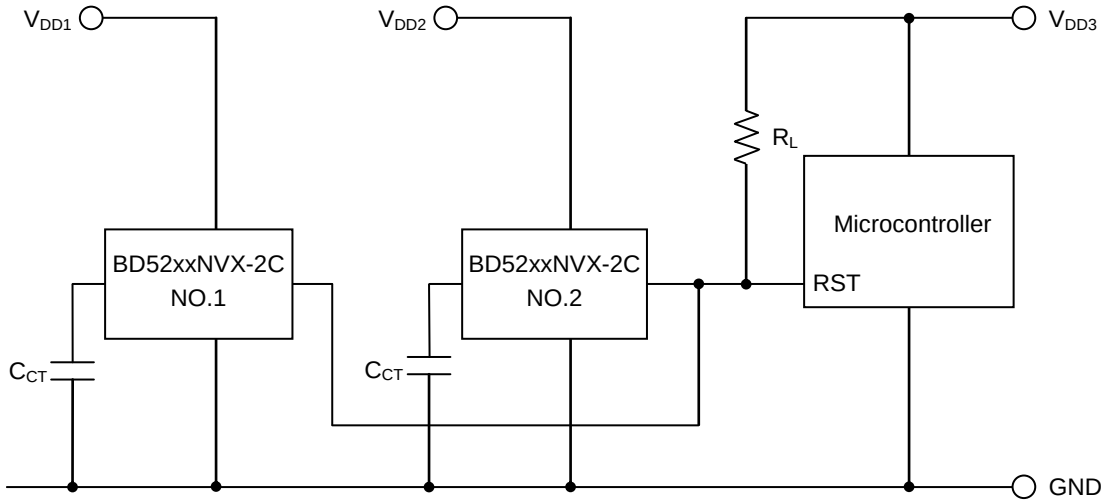


Figure 25. OR Circuit Connection Application

There are multiple power supply in the system, and in case monitoring for each independent power supply V_{DD1} and V_{DD2} and reset of micro-controller is required, an application where output "H" voltage is aligned to the microcontroller power supply V_{DD3} is possible by connecting OR application and pull-up at random voltage (V_{DD3}) such as shown in Figure 25.

(3) Examples of the power supply with resistor dividers

In applications wherein the power supply voltage of an IC comes from a resistor divider circuit, an inrush current will flow into the circuit when the output level switches from "Low" to "High" or vice versa. Inrush current is a sudden surge of current that flows from the power supply (V_{DD}) to ground (GND) as the output logic changes its state. This current flow may cause malfunction in the systems operation such as output oscillations, etc.

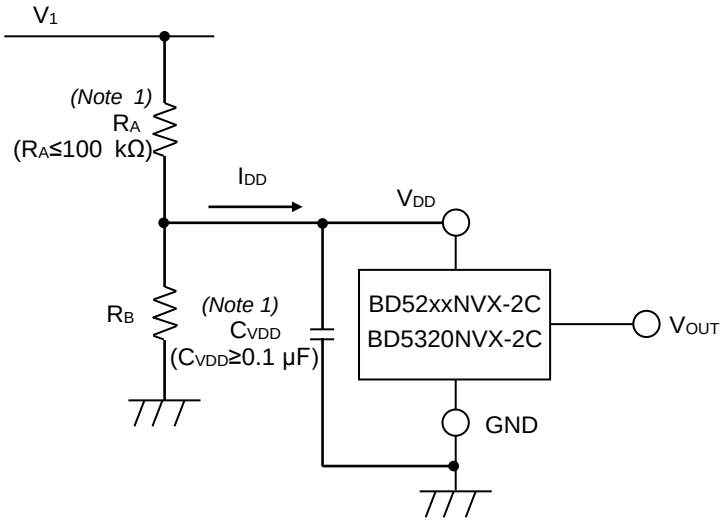


Figure 26. Resistor Divider Connection Application

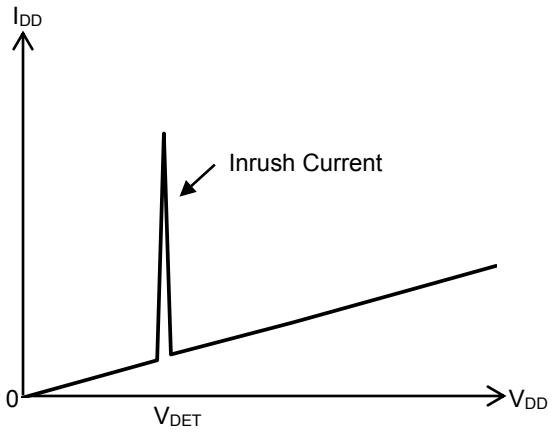


Figure 27. Current Consumption vs V_{DD} Voltage

A voltage drop [Inrush current (I_1)] x [input resistor (R_A)] is caused by the inrush current, and causes the input voltage to drop when the output switches from "L"→"H". When the input voltage drops and falls below the detection voltage, the output will switch from "H"→"L". At this time, the inrush current stops flowing through output "L", and the voltage drop disappears. As a result, the output switches from "L"→"H", which again causes the inrush current to flow and the voltage to drop. This operation repeats and leads to oscillation.
In case resistor divider is not use and only use R_A, same response will happen.

(Note 1) The circuit connection mentioned above does not guarantee successful operation.
Perform thorough evaluation using the actual application and set countermeasures.

Application Circuits - continued

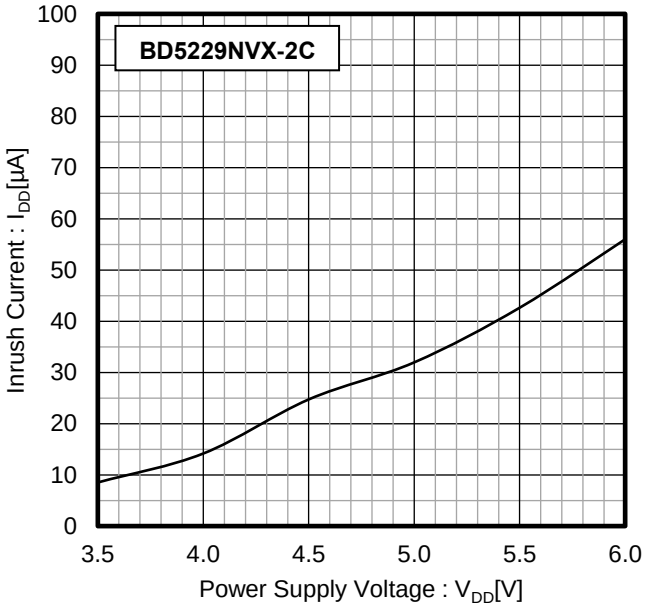


Figure 28. I_{DD} Inrush Current vs Power Supply Voltage (Ta=25 °C)

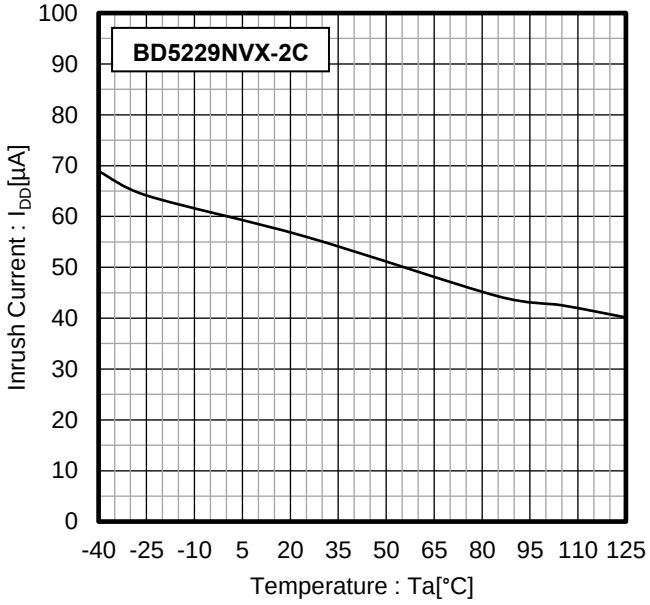


Figure 29. I_{DD} Inrush Current vs Temperature (V_{DD}=6 V)

Depending on the application set-up, there are times that V_{DD} voltage is always below the Release Voltage ($V_{DET}+\Delta V_{DET}$) because of the effect of inrush current as shown in Figure 30.

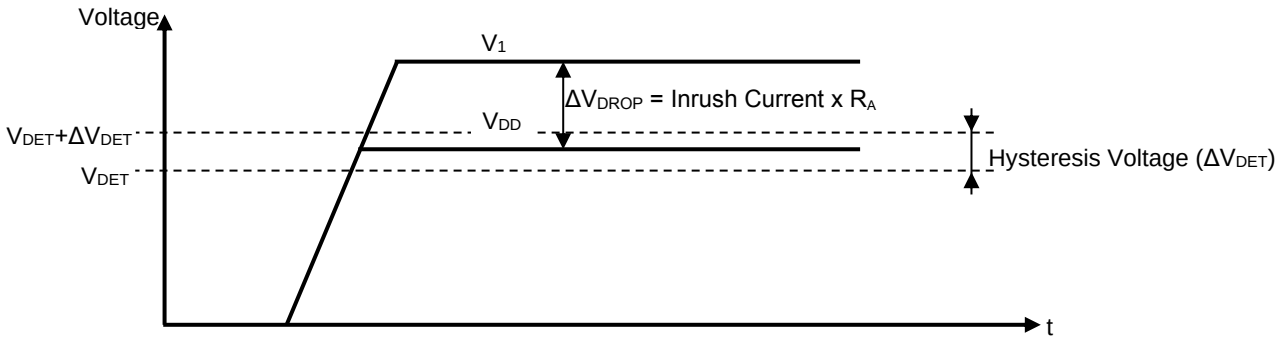


Figure 30. V_{DD} Drop Caused by Inrush Current

Considerations on Input and Output Capacitor

It is suggested to use input and output capacitors which is positioned as near as possible to the pins. The capacitor between the input pin and GND is effective when the power supply impedance increases or when the wiring is long. A large capacitor at the output improves stability and output load characteristics. Before implementation, check the state of mounting. In addition, the ceramic capacitor deviates in general and has temperature characteristics and AC bias characteristics. Furthermore, depending on the usage, the capacitance value decreases over time. It is recommended that ceramic capacitor to use is decided after gathering detailed data information by consulting brand manufacturers.

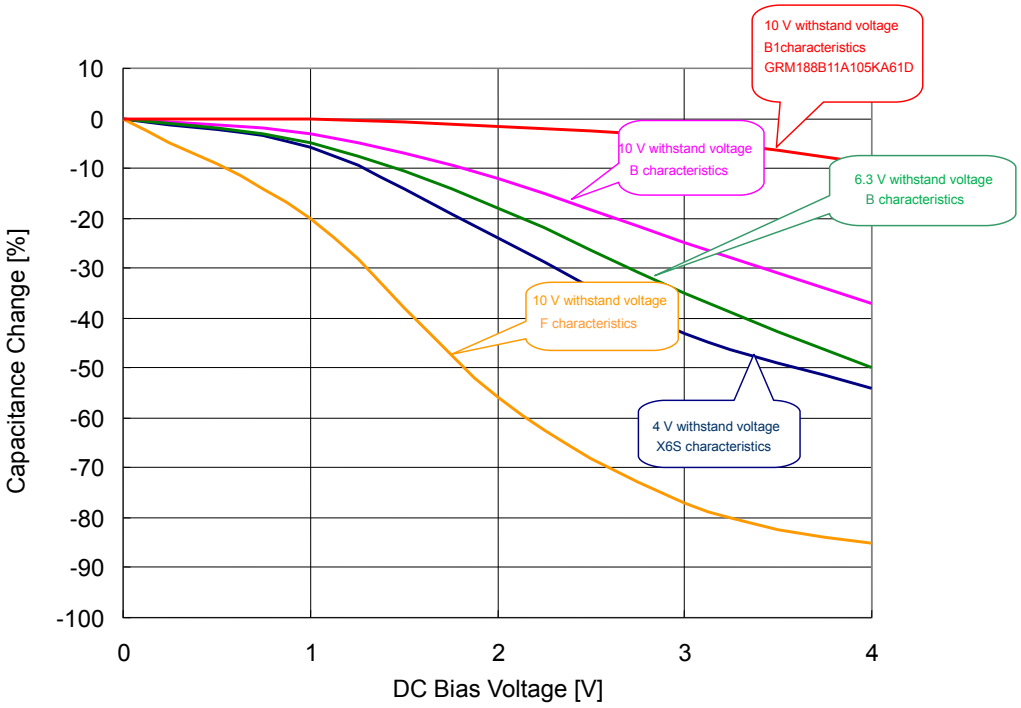


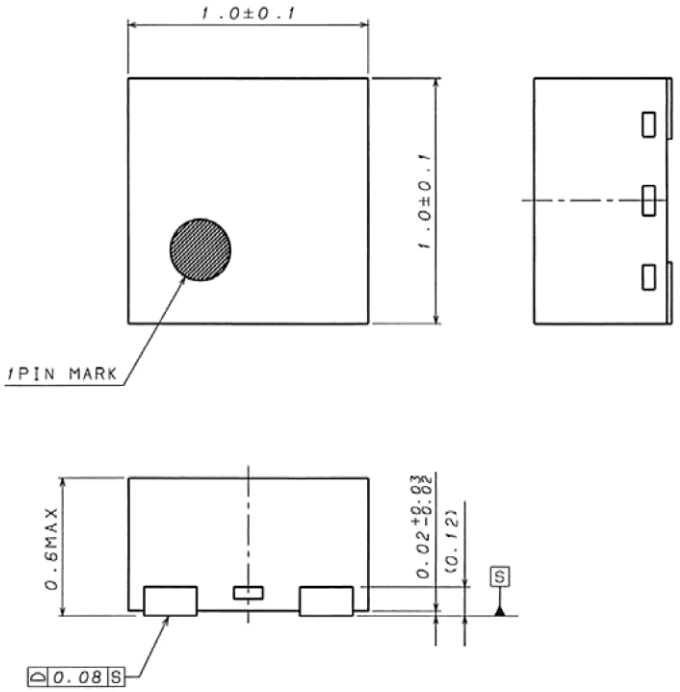
Figure 31. Ceramic Capacitance Change - DC Bias Properties (Characteristic example)

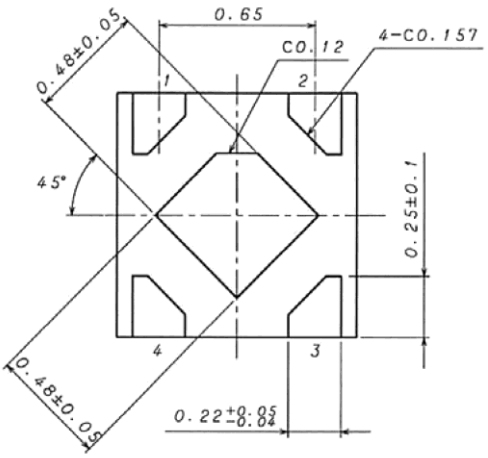
Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.
2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.
3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.
4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.
5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.
6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.
7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.
8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.
9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.
10. **Regarding the Input Pin of the IC**
    In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.
11. **Ceramic Capacitor**
    When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Physical Dimension and Packing Information

Package Name	SSON004R1010



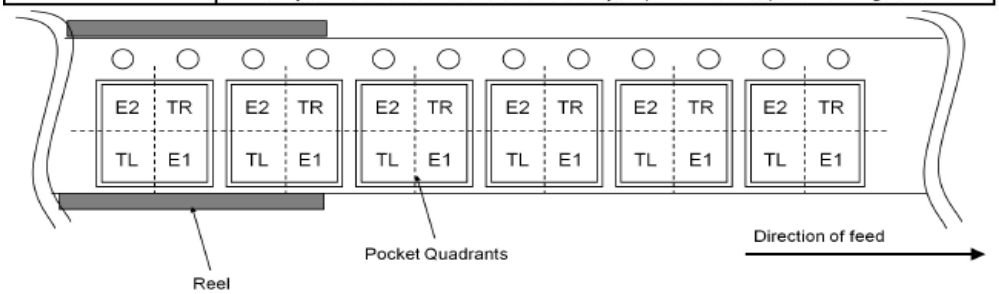


(UNIT:mm)

PKG:SSON004R1010
Drawing No. EX077-5001

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	5000pcs
Direction of feed	TL The direction is the pin 1 of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
23.Jan.2018	001	New Release
31.Jul.2018	002	Format Change Add Notation of “Nano Energy”
09.Sep.2021	003	Add lineup (BD5214NVX-2C, BD5216NVX-2C, BD5320NVX-2C)

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
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   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

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5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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