4K MEMORY CARD

DESCRIPTION

The 2650 PC2000 is a 4K Memory Card designed to be compatible with the 2650 microprocessor. It is composed of 32, 21L02 NMOS, 1K by 1 bit static RAM's, and organized in four groups of one kilobyte each. Decoding is provided to select one of the four groups and also distinguish the card in multi-card configurations. In a system application utilizing up to 8 cards (32K), each card is uniquely identified by hardwired jumpers. No external decoding is required.

The decoding logic is sectioned into two blocks. The first block determines if the address identifies that card as being part of the 8K page address. (The 2650 memory scheme is organized into 4 pages of 8K each.) The second block uniquely locates 1K bytes of memory on the board in the 8K bytes of memory of the selected page. Each 1K bank is individually selected by hardwired jumpers to the decoder.

FEATURES

- **Requires only single +5V supply**
- **Industry standard 21L02 memories**
- **Fully decoded for 32K memory organization**
- **Data bus buffered with tri-state drivers/receivers**
- **Accessable from microprocessor or DMA controller**
- **TTL compatible**
- **Dimensions are 8" X 6.875" with a 50 pin edge connector along the 8" dimension**
- **Typical power consumption of 4.5 watts**

SIGNAL DEFINITION

Memory control signals and address lines between the 2650 microprocessor and the 2650 PC2000 are indicated in the block diagram. The $\overline{\text{OPEX}}$ control line is reserved for use with DMA controllers. Its function is similar to that of the OPREQ line from the 2650. When either of these lines are true and a memory operation is specified ($M/\overline{IO}$ = High) the memory card is enabled to decode address lines AO through A14. When a bank is selected, the selected card control logic block allows the read-write line ($\overline{R}/W$) and write pulse (WRP) to pass to the memory array and also enable the external data bus drivers. When the operation is complete the memory card responds with a true condition on $\overline{\text{OPACK}}$.

JUMPER ADDRESS DECODING

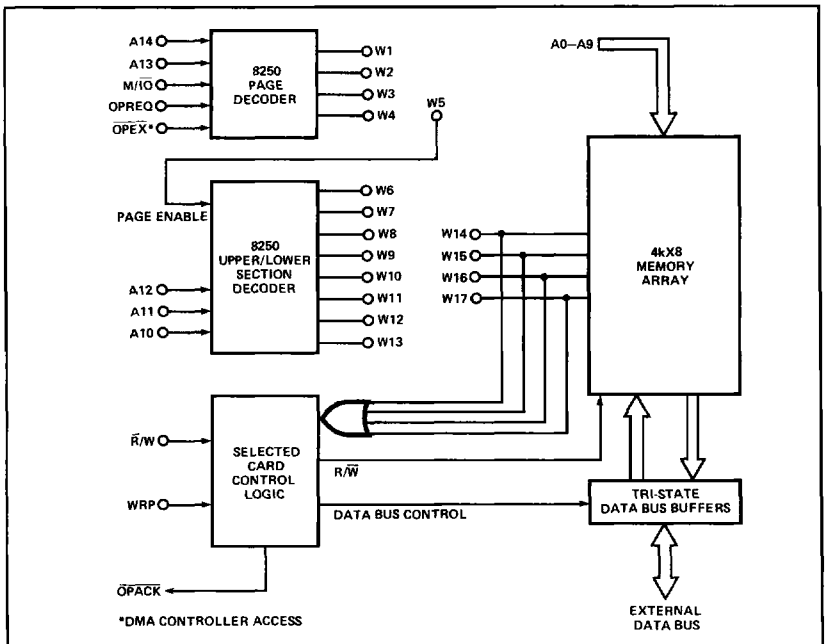
Jumpers are applied to designated plated-through holes identified by a 'Wn' mnemonic. To identify the card to be part of a particular page, jumper point W5 to one of the following:

WI for page 0
W2 for page 1
W3 for page 2
W4 for page 4

To locate each of the 1K bytes of the memory card in the selected memory page, four bank jumpers are required. The outputs of the decoder used to select one of eight 1K byte memory segments (W6-W13) must be connected to the selected 1K bytes of memory on the 2650 PC2000 (W14-W17).

Factory installed jumpers allow for immediate hook-up to a Demo System (DS1000/2000) which has 2K of memory. These jumpers have been hooked-up as follows:

W1 to W5 (page 0)
W8 to W14
W9 to W15
W10 to W16
W11 to W17



2650 PC2000 BLOCK DIAGRAM

2650 PC 2000 EDGE CONNECTOR

PIN	NAME	PIN	NAME
1,2,A,B	GROUND	34	ABUS13
4	$\overline{\text{DBUS0}}$	35	ABUS12
5	$\overline{\text{DBUS1}}$	36	ABUS14
6	$\overline{\text{DBUS2}}$	37	ABUS9
7	$\overline{\text{DBUS3}}$	38	ABUS10
8	$\overline{\text{DBUS4}}$	39	ABUS8
9	$\overline{\text{DBUS5}}$	40	ABUS7
10	$\overline{\text{DBUS6}}$	41	ABUS6
11	$\overline{\text{DBUS7}}$	42	ABUS5
17	$\overline{R}/W$	43	ABUS3
18	WRP	44	ABUS0
20	OPREQ	45	ABUS1
21	$M/\overline{IO}$	46	ABUS4
22	$\overline{\text{OPACK}}$	47	ABUS2
24	$\overline{\text{OPEX}}$	50,f	VCC +5V
33	ABUS11		