FAIRCHILD
A Schlumberger Company

Bipolar Division

93475
1024 x 4-Bit Static Random Access Memory

TTL Bipolar Memory

Description

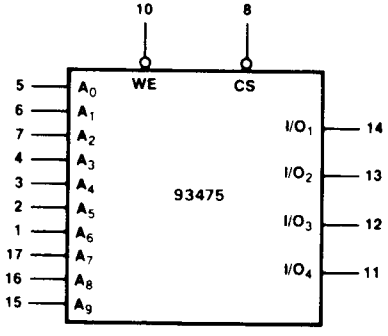
The 93475 is a 4096-bit read/write Random Access Memory (RAM), organized 1024 words by four bits per word. It is designed for high speed cache, control and buffer torage applications. The military version of the 93475 is available in two speeds, "standard" speed and an "A" grade. The device includes full on-chip decoding and an active LOW Chip Select line.

- **Address Access Time — 45 ns Max**
- **Chip Select Access Time — 35 ns Max**
- **Features Three State Outputs**
- **Common Data I/O's**
- **Industry Standard 2114 Pinout**
- **Power Dissipation — 0.16 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

A_0-A_9	Address Inputs
$\overline{CS}$	Chip Select Input (Active LOW)
$\overline{WE}$	Write Enable Input (Active LOW)
I/O_1-I/O_4	Data Input/Data Outputs

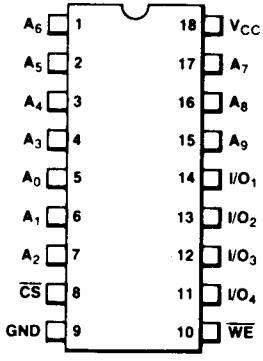
Logic Symbol



V_{CC} = Pin 18
GND = Pin 9

Connection Diagram

18-Pin DIP (Top View)



Note:
The 18-pin Flatpak version has the same pinout connections as the Dual In-line package.

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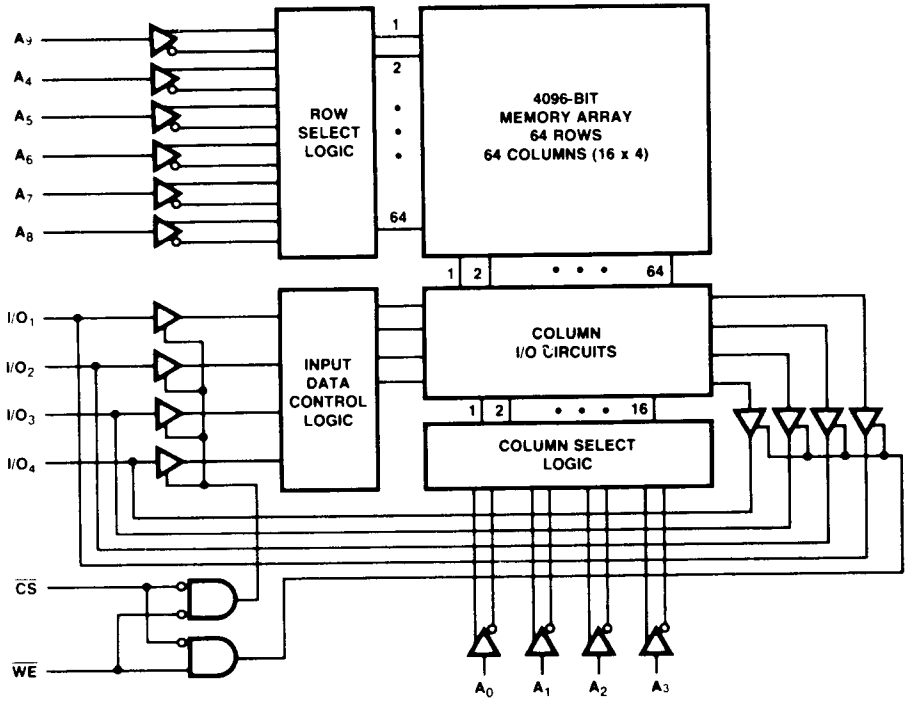
Logic Diagram



Functional Description

The 93475 is a fully decoded 4096-bit read/write Random Access Memory organized 1024 words by four bits per word. Word selection is achieved by means of a 10-bit address, A_0 through A_9.

One Chip Select input is provided for logic flexibility or for memory array expansion of up to 8196 bits without the need for external decoding. For larger memories, the fast chip select access time permits the decoding of Chip Select, ($\overline{CS}$) from the address without affecting system performance.

The read and write functions of the 93475 are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. When $\overline{WE}$ is held LOW and the chip is selected, the data at I/O_1 through I/O_4 is written into the addressed locations. Since the write function is level triggered, data must be held stable at the data input for at least $t_{WSD(min)}$ plus $t_{W(min)}$ to insure a valid write.

When $\overline{WE}$ is held HIGH and the chip selected, data is read from the addressed location and presented at the outputs (I/O_1-I/O_4).

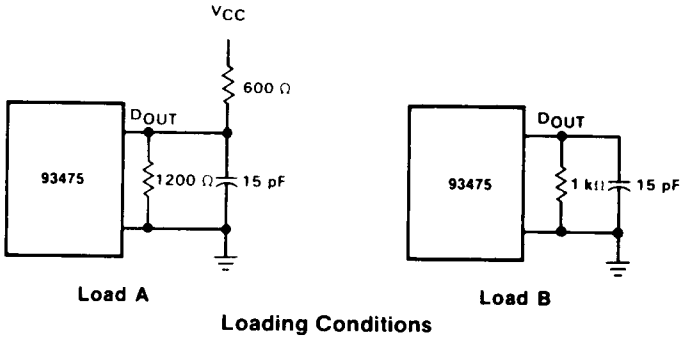
The 93475 has three-state outputs for use in bus organized systems.

Truth Table

Inputs			
$\overline{CS}$	$\overline{WE}$	I/O_1-I/O_4	Mode
H	X	HIGH Z	Not Selected
L	H	D_{OUT}	Read
L	L	D_{IN} HIGH Z	Write

H = HIGH Voltage Level (2.4 V)
L = LOW Voltage Level (.5 V)
X = Don't Care (HIGH or LOW)

Fig. 1 AC Test Load Output Load



Loading Conditions

Fig. 2 Input Levels