

M5M442256AJ,L,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

DESCRIPTION

M5M442256AJ, L, TP, RT is a high speed 1048576-bit Dual Port Dynamic Memory equipped with a 256K x 4 Dynamic RAM Port and a 512 x 4 Serial Read/Write Port. High performance CMOS process using triple-layer polysilicon and silicide technology provide both high circuit density and low power dissipation.

The Serial Read/Write Ports are connected to an internal 2048 bit Data Register through a 512 x 4 Serial Input/Output Control circuit and can be serially readout or written in with a clock rate of up to 33MHz.

All reads and writes are done relative to the RAM array, thus data transfer from the RAM array to the Data Register is referred to as a Read Transfer, while Data Transfer from the Data Register to the RAM array is referred to as a Write Transfer.

FEATURES

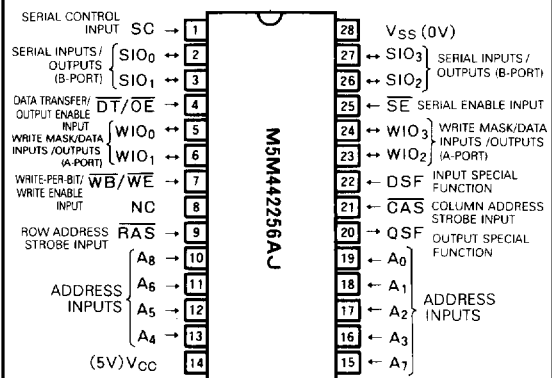
Type name	RAS Access Time (ns)	Random Read/Write Cycle Time (ns)	Serial Read Cycle Time (ns)	Random Read V _{CC} Supply Current (mA)	Serial Read/Write V _{CC} Supply Current (mA)
M5M442256AJ, L, TP, RT-7	70	130	30	85	40
M5M442256AJ, L, TP, RT-8	80	150	30	75	40
M5M442256AJ, L, TP, RT-10	100	180	30	65	40

- Dual Port Architecture
 - RAM Port: 256K word x 4 bit
 - Serial Port: 512 word x 4 bit
- Bidirectional Data Transfer function between the RAM array and the Data Register
- Fully Asynchronous Dual Port Accessibility (Split SAM)
- Addressable Start of Serial Read/Write (Pointer Control Function)
- Write per Bit Function
- Real Time Data Transfer from the RAM Array to the Data Register
- Fast Page Mode, Hidden Refresh and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh
- 512 cycle/8ms Refresh
- Flash write operation
- Block write operation

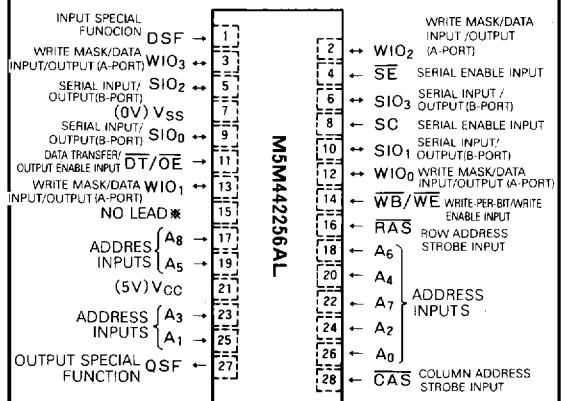
APPLICATION

Display equipment for personal computer/work station, Frame memory for digital TV/VCR, Videotex, Teletext, Video printer, High Speed data transmission systems

PIN CONFIGURATION (TOP VIEW)



Outline 28P0K (400 mil 28 pin SOJ)



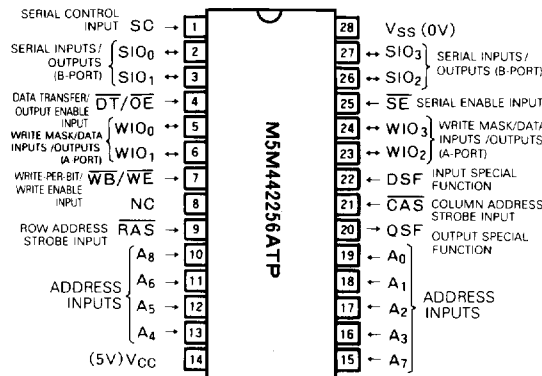
Outline 28P5L (400 mil 28 pin ZIP)

NC: NO CONNECTION

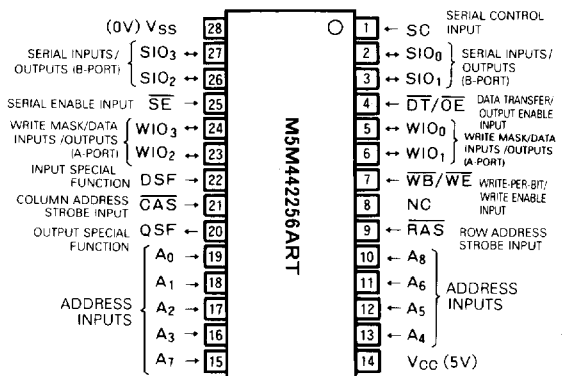
M5M442256AJ,L,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

PIN CONFIGURATION (TOP VIEW)



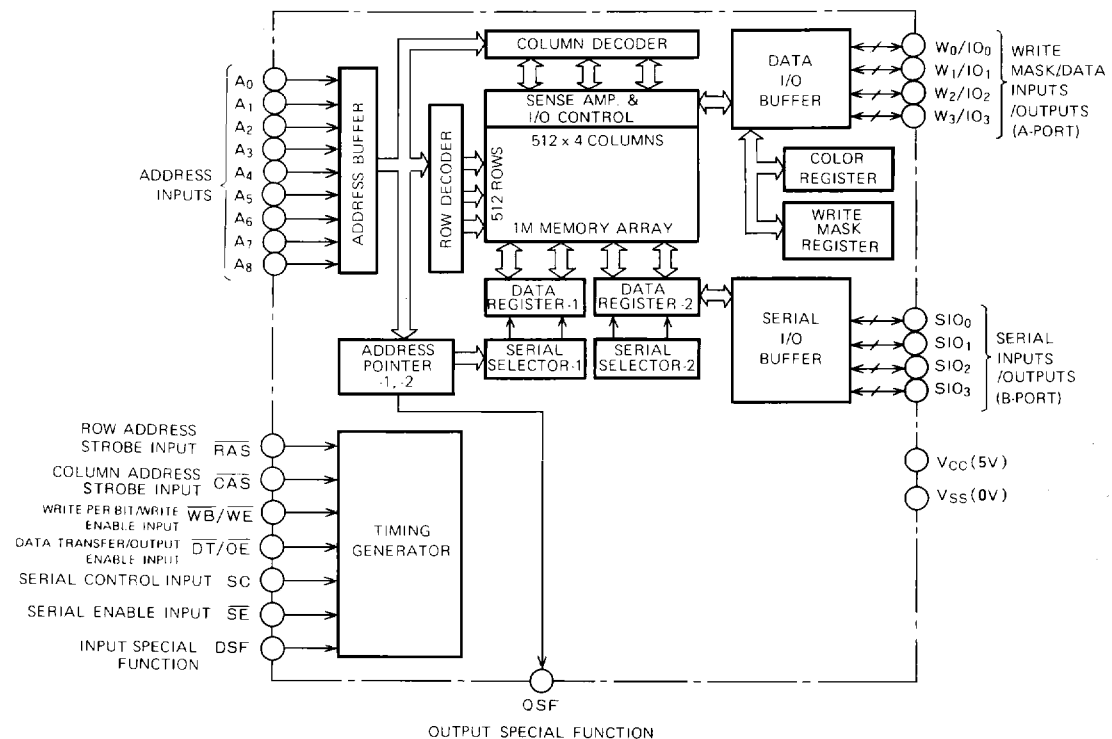
Outline 28P3Y-H (400mil 28 pin TSOP)
(Normal Bend Type)



Outline 28P3Y-J (400 mil 28 pin TSOP)
(Reverse Bend Type)

NC: NO CONNECTION

BLOCK DIAGRAM



FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

PIN DESCRIPTION

Pin	Name	Function
$\overline{RAS}$	ROW ADDRESS STROBE INPUT	It is used as a clock which latches the row address ($A_0 \sim A_8$) and selects the word line. It also latches the mask data for write-per-bit, flash write, write transfer and split write transfer function when the $\overline{WB}$ level is low. $\overline{CAS}$ before $\overline{RAS}$ refresh mode is available by preceding $\overline{CAS}$ low.
$\overline{CAS}$	COLUMN ADDRESS STROBE INPUT	It is used as a clock which latches the column address ($A_0 \sim A_8$) and initiates the reading or writing of the selected words. In the data transfer cycle this latches the SAM Top Address Point. (TAP)
$A_0 \sim A_8$	ADDRESS INPUT	The M5M442256 utilizes an address multiplex method for selecting one word among the 256K-word memory cells. 9 row addresses and 9 column addresses are latched by the $\overline{RAS}$ and $\overline{CAS}$ falling edge. In the data transfer cycle, this RAM address input is also combined with the serial access start address. (TAP)
$\overline{WB}/\overline{WE}$	WRITE-PER-BIT / WRITE ENABLE INPUT	When the $\overline{WB}/\overline{WE}$ level is low at the $\overline{RAS}$ falling edge, Write-per-bit (RAM write with Mask) or Write transfer with MASK or Flash write with MASK cycle is selected. When it is high, normal read/write or Read transfer or Load color register cycle is selected. This clock also controls early/late write mode at the $\overline{CAS}$ falling edge.
$\overline{DT}/\overline{OE}$	DATA TRANSFER / OUTPUT ENABLE INPUT	In RAM read cycle, it makes the data output (RAM port) enable. Also when the $\overline{DT}/\overline{OE}$ level is low at the $\overline{RAS}$ falling edge, the data transfer cycle is selected and when it is high, RAM read/write cycle or Load color register cycle or Flash write cycle is activated according to the $\overline{WB}/\overline{WE}$ and the DSF combination.
WIO_n^*	WRITE MASK / DATA INPUT / OUTPUT	These are the data input/output pins to the RAM. During RAM write-per-bit cycle/split write transfer cycle/flash write cycle, the high data pin at the $\overline{RAS}$ falling edge enables the selected-bit (row) write operation. In Write cycle, the data is latched at the late falling edge of the $\overline{CAS}$ or the $\overline{WB}/\overline{WE}$ input, whichever is the later.
SC	SERIAL CONTROL INPUT	The serial access is initiated from the SC clock rising edge. In the serial read cycle, the output data is held until the next clock rise. Also in the serial write cycle, the data is latched at the SC clock rising edge.
SIO_n^*	SERIAL INPUT / OUTPUT	512 x 4 word serial data input/output pins
$\overline{SE}$	SERIAL ENABLE INPUT	This enables the serial input/output. In the write transfer cycle, when $\overline{SE}$ is high at the $\overline{RAS}$ falling edge, Pseudo transfer cycle is selected, and when it is low, Write transfer cycle is selected.
DSF	INPUT SPECIAL FUNCTION	This input defines special functions such as Split read/write transfer, Flash write, Block write and Load color register. When it is low grounded, the device works as a basic dual-port memory except for the Normal write transfer cycle masking mode.
QSF	OUTPUT SPECIAL FUNCTION	Output indicating the serial data selector status.

Note *: $n = 0 \sim 3$

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

256Kx4 Truth Table

Code mnemo nic	RAS falling edge							CAS falling edge				Write mask op.	Raster op.	Register			
	CAS	DT OE	WB WE	DSF	SE	Addr	WIO _n	WB/WE	DSF	Addr	WIO _n			Write mask temporary	Write mask persistent	Color	
CBR	0	0/1	0/1	0/1	—	—	—	—	—	—	—	—	—	—	—	—	C.B.R
MWT/ PWT	1	0	0	0	0/1	Row/ Ref	WM1	—	0	TAP	—	Yes per row	—	Load use	—	—	Wr. transfer (SE=0) Pseudo write transfer (SE=1)
SWT	1	0	0	1	—	Row	WM1	—	0	TAP	—	Yes per row	—	Load use	—	—	Split write transfer with new mask
	1	0	0	1	—	Row	WM1	—	1	TAP	—						
RT	1	0	1	0	—	Row	—	—	0	TAP	—	—	—	—	—	—	Read transfer
	1	0	1	0	—	Row	—	—	1	TAP	—						
SRT	1	0	1	1	—	Row	—	—	0	TAP	—	—	—	—	—	—	Split read transfer
	1	0	1	1	—	Row	—	—	1	TAP	—						
RWNM	1	1	0	0	—	Row	WM1	*E/L	0	Col.	DQ _{in}	Yes	—	Load use	—	—	RAM write with new mask
BWNM	1	1	0	0	—	Row	WM1	—	1	Col.	Sel.	Yes	—	Load use	—	Use	Block write with new mask
FWT	1	1	0	1	—	Row	WM1	—	0	—	—	Yes per row	—	Load use	—	—	Flash write with new mask
	1	1	0	1	—	Row	WM1	—	1	—	—						
RW	1	1	1	0	—	Row	—	*E/L	0	Col.	DQ _{in}	—	—	—	—	—	R/W
BW	1	1	1	0	—	Row	—	—	1	Col.	Sel.	—	—	—	—	Use	Block write with no mask
LCR	1	1	1	1	—	Ref	—	*E/L	0	—	CLR.	—	—	—	—	Load	Load color reg.
	1	1	1	1	—	Ref	—	*E/L	1	—	CLR.						

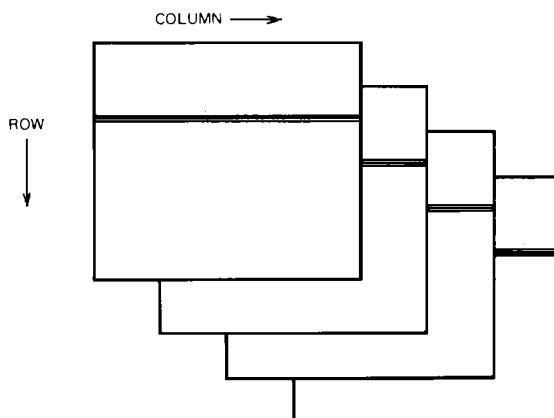
*E/L: Early write/Late write

**Ref: Refresh Address

FUNCTION

1. Flash Write

Utility: A high speed clear can be performed with flash write cycle.

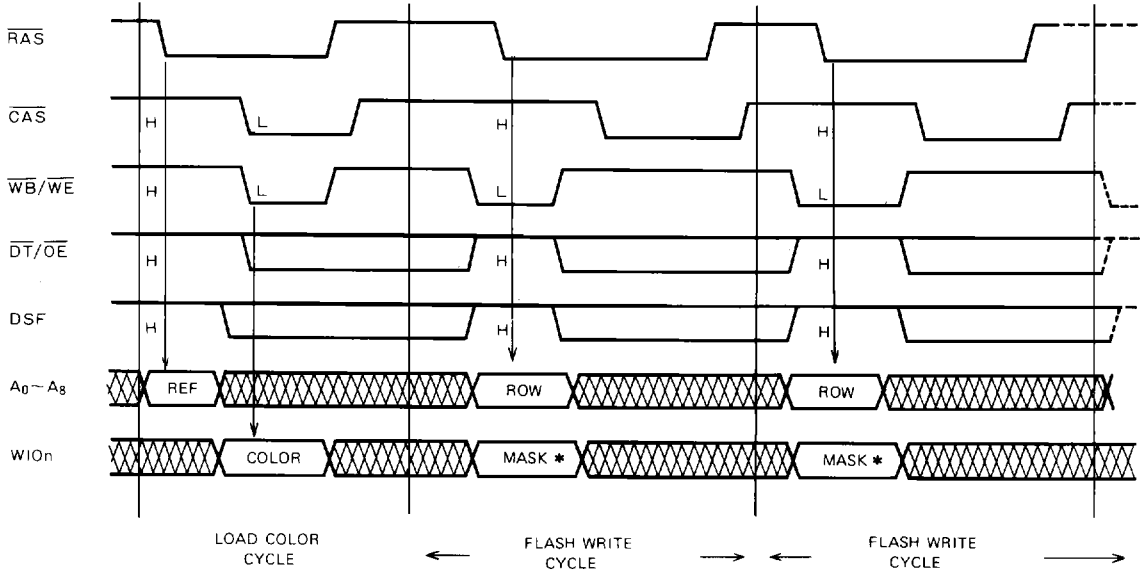


* Write a color (0 or 1) to an entire row in one RAM cycle.

* Before flash write cycle, the color data must be set into an internal color register at least once.

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

Flash Write Timing Description

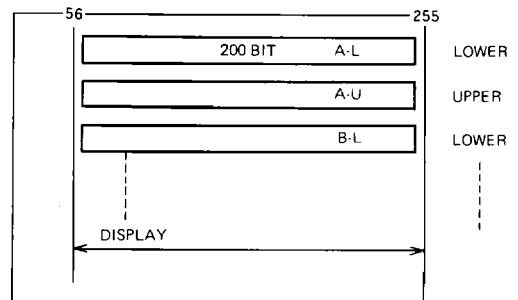
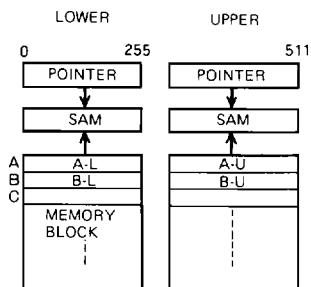


* The mask must be asserted on each flash write cycle.

2. Split Register

Utility

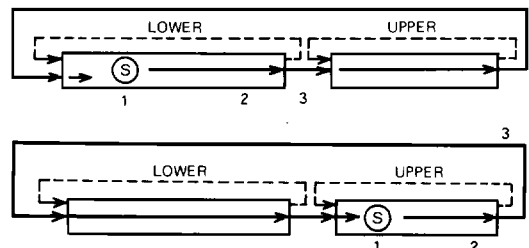
- a. To simplify real time transfer timing (Fully asynchronous Serial Access)
- b. Split Serial Register into two halves – To optimize the memory size to CRT.



Pointer Path

At Normal read transfer cycle

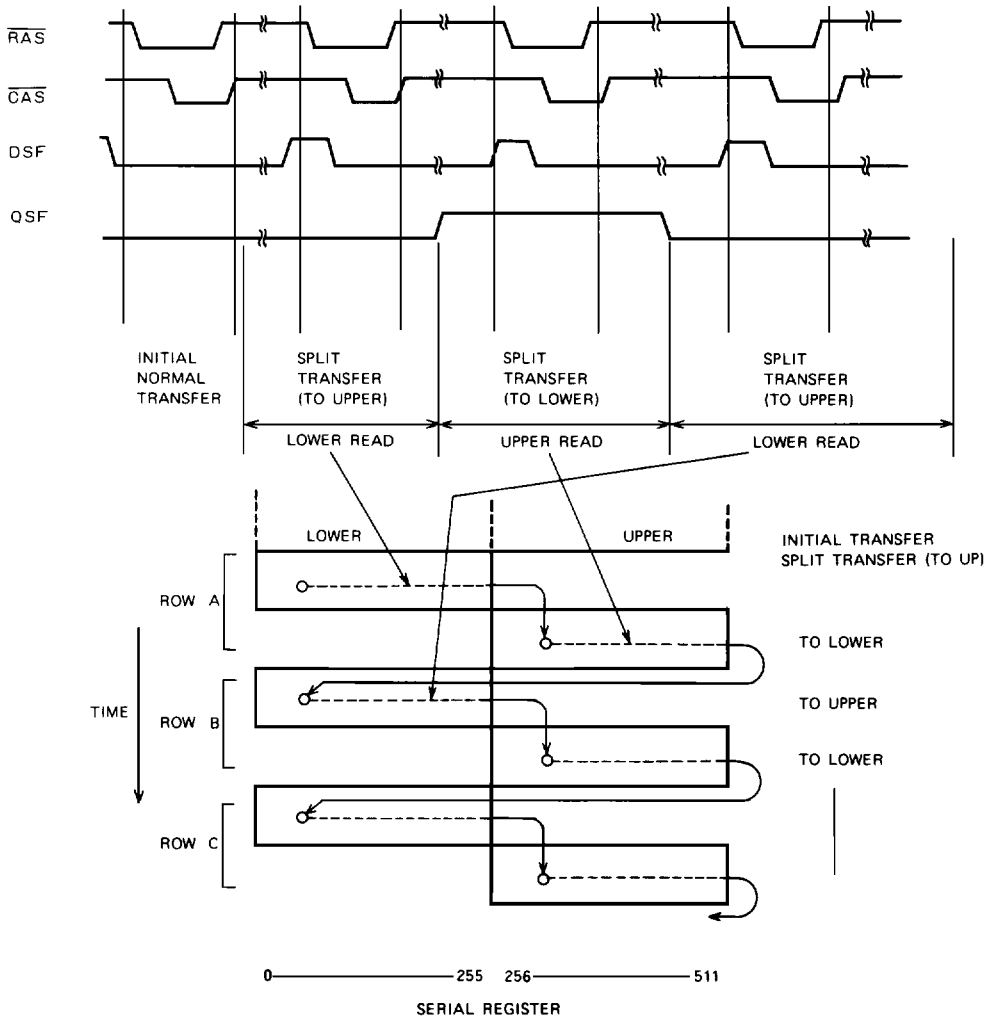
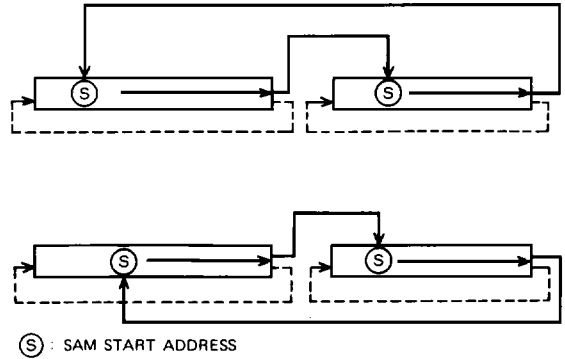
1. Transfer the data from RAM to SAM, and set the SAM start address among 512.
2. Start the Serial Read cycle.
3. Serial Read from Lower to Upper/Upper to Lower.
(The pointer of the Lower/Upper SAM will be automatically cleared to address 0/256 after over-carried)



FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

At Split read transfer cycle

1. Normal transfer cycle must be performed prior to the split transfer cycle.
2. The data is transferred between idle half of the SAM and the selected Row. At the same time the idle SAM's start address is set to give the next start address after the end of the busy SAM.
3. At the split transfer mode, data are transferred to the idle half of the SAM automatically. (Column A_8 is ignored.)
4. QSF indicates the busy SAM.
(Lower Half SAM is busy: 0)
(Upper Half SAM is busy: 1)
5. Serial Read can be performed asynchronously during RAM cycle and Split transfer cycle.

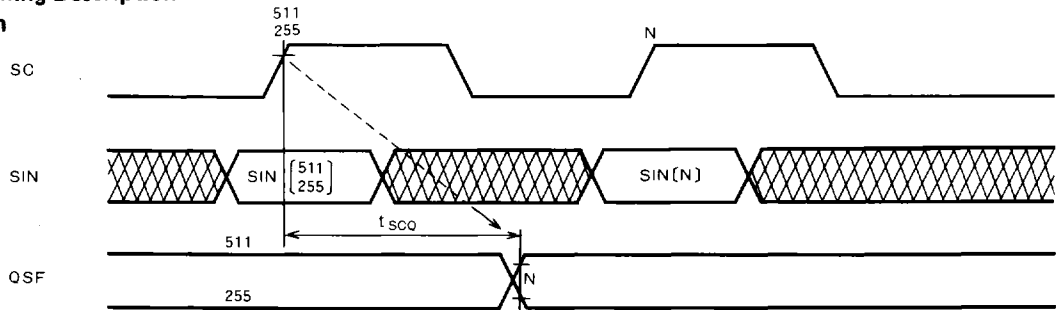


M5M442256AJ,L,TP,RT-7,-8,-10

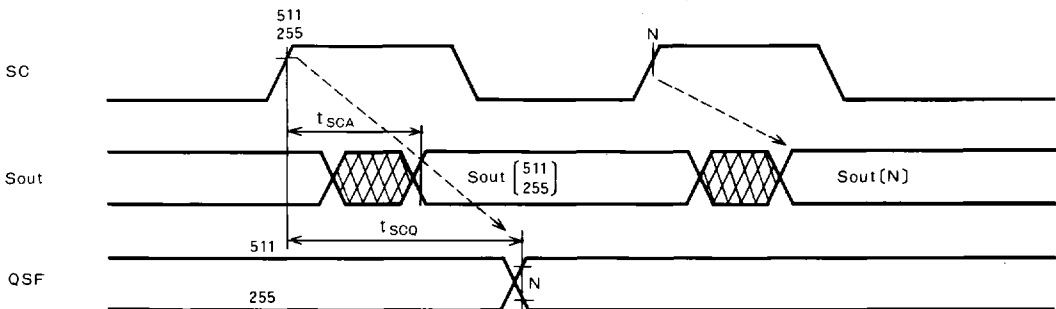
FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

QSF Timing Description

Serial-In



Serial-Out



Data transfer mode	SIO mode	SAM TAP	Data transfer	QSF set
Normal read transfer	Output	Col. (A ₀ ~A ₈)	RAM→SAM	A ₈
Normal write transfer	Input	Col. (A ₀ ~A ₈)	SAM→RAM	A ₈
Pseudo write transfer	Input	Col. (A ₀ ~A ₈)	—	A ₈
Split read transfer	Not effect	Col. (A ₀ ~A ₇)	RAM→SAM *1	—
Split write transfer	Not effect	Col. (A ₀ ~A ₇)	SAM→RAM *1	—

*1: If QSF=0 then the upper half data (256~511) is transferred.
If QSF=1 then the lower half data (0~255) is transferred.

3. Block Write

In the Block Write cycle, Data from the Color Register can be written into 4 bit-columns (which Blocks are selected with column address CA₂~CA₈) at one time. The DQ_{0~3} the input at CAS falling edge enables a selective column write operation of the selected 4 bit-columns.

When $\overline{WB/WE}$ is low at RAS falling edge Write-per-bit operation applies to the writing of color data.

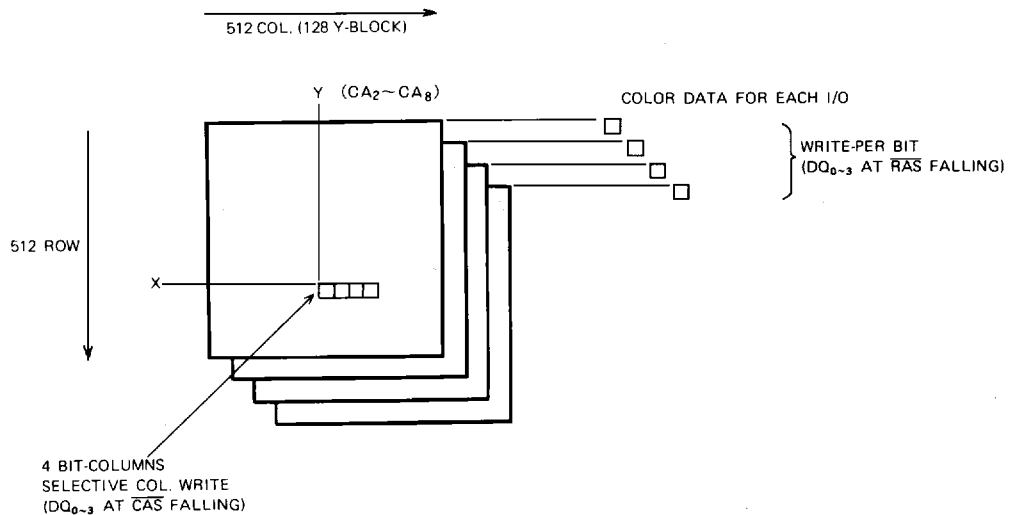
The Color Register must be loaded prior to the Block Write cycle.

Application

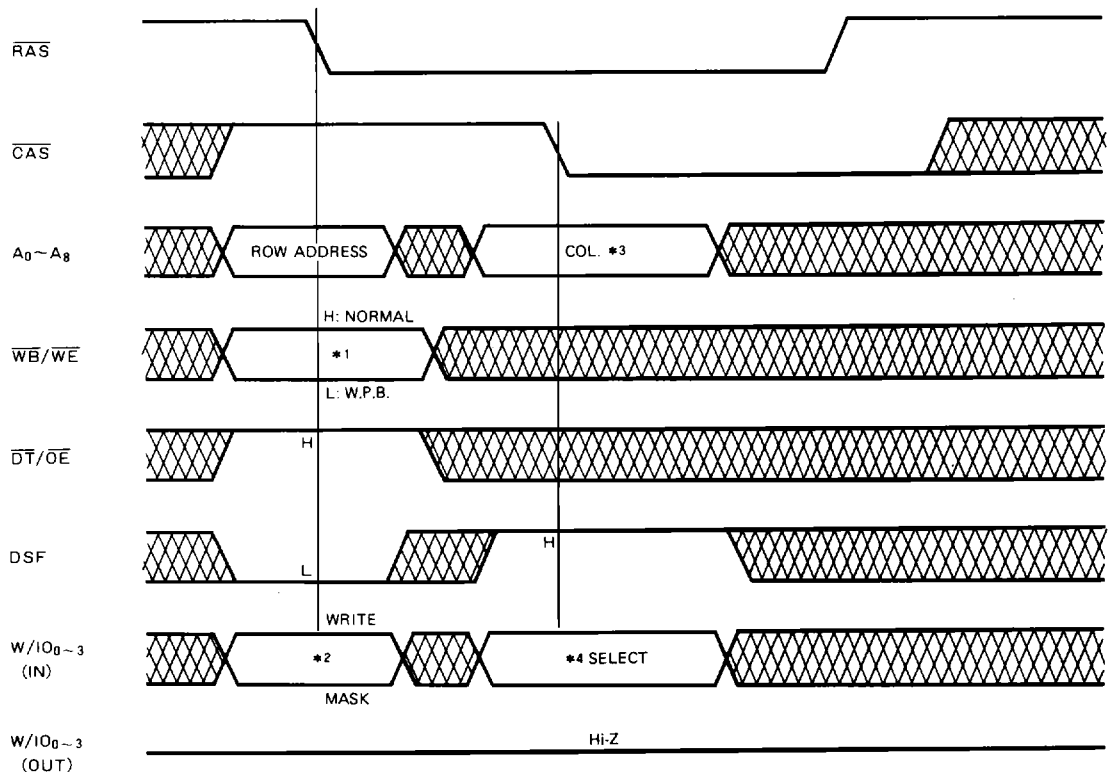
Block Write operation is useful for the partial-clearing or partial-painting of a bit-map display with same color data. With the selective-column writing of data, any of the 4 bit-columns can be masked, so allowing the boundary treatment in the same cycle.

M5M442256AJ,L,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM



Block Write Timing Description



*1: H: No mask

L: Write per bit operation

*2: H: Write enable (No mask)

L: Disable (mask)

Only when WB/WE is low at RAS falling edge

*3: Column address CA₂ ~ CA₈; CA₀, CA₁ = Don't care (H/L fixed)

*4: Select W/IO₀: CA₀=0, CA₁=0

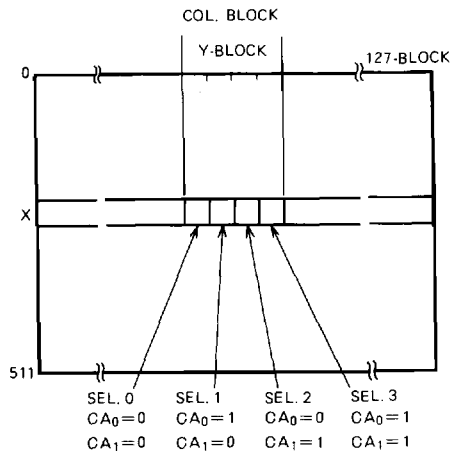
W/IO₁: CA₀=1, CA₁=0

W/IO₂: CA₀=0, CA₁=1

W/IO₃: CA₀=1, CA₁=1

H: Write enable (no mask)

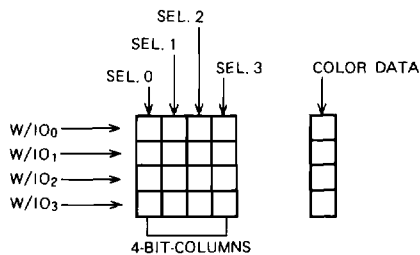
L: Disable (mask)

M5M442256AJ,L,TP,RT-7,-8,-10**FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM**

A₀, A₁ at $\overline{\text{CAS}}$ falling edge are "don't care", but must be set H or L state.

Example of Block Write Operation

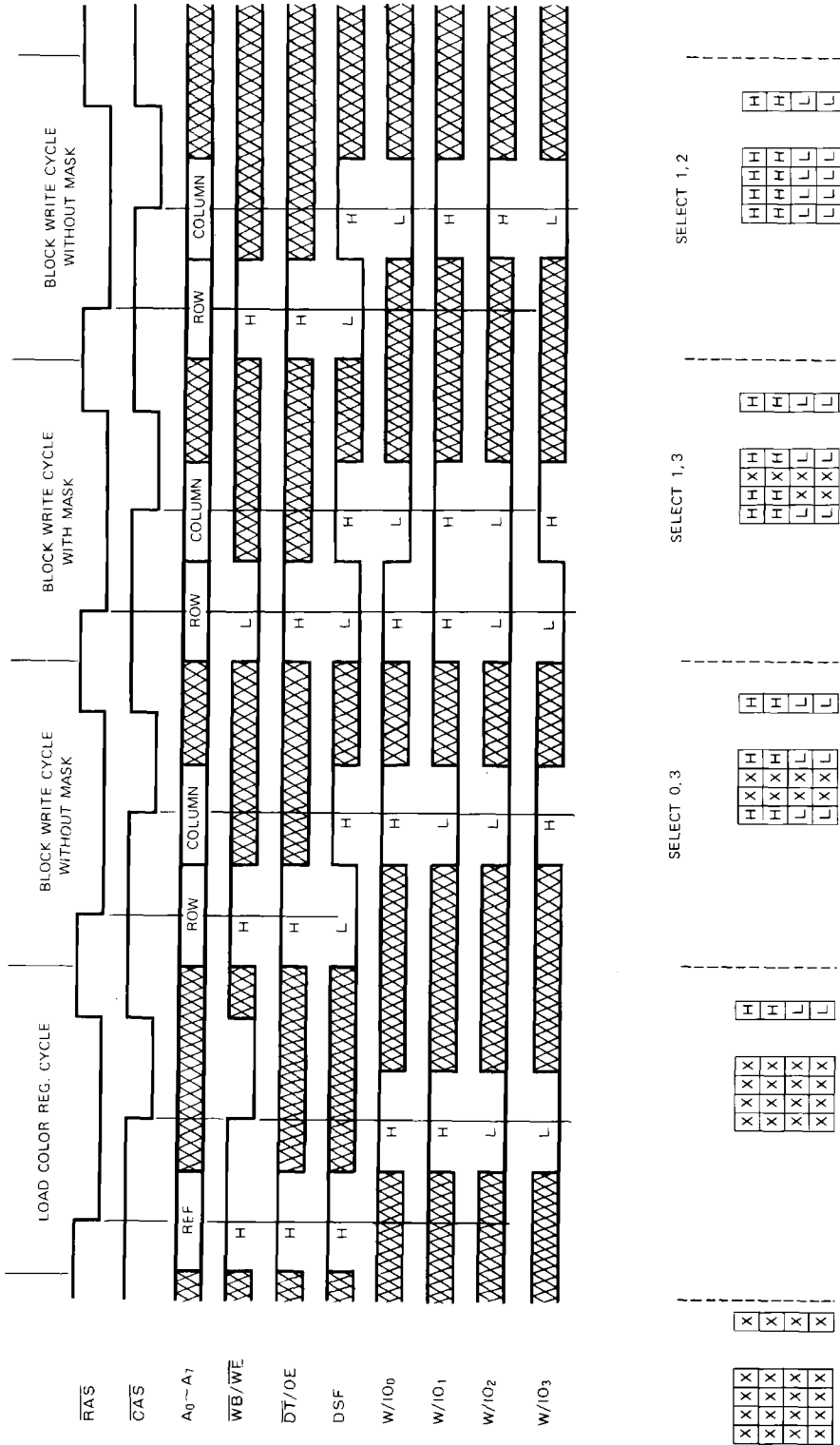
'X' indicates pre-state, 'H'; high level (1), 'L'; low level (0).



M5M442256AJ,L,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

Example



M5M442256AJ,L,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS}	-1 ~ 7	V
V _I	Input voltage		-1 ~ 7	V
V _O	Output voltage		-1 ~ 7	V
I _O	Output current		50	mA
P _d	Power dissipation	T _a = 25°C	1000	mW
T _{opr}	Operating temperature		0 ~ 70	°C
T _{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Norm	Max	
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	High-level input	2.4		6.5	V
V _{IL}	Low-level input	-1.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{OH(R)}	High level output (RAM port)	I _{OH(R)} = -2 mA	2.4		V _{CC}	V
V _{OL(R)}	Low level output (RAM port)	I _{OL(R)} = 4.2 mA	0		0.4	V
V _{OH(S)}	High level output (Serial I _O port)	I _{OH(S)} = -2 mA	2.4		V _{CC}	V
V _{OL(S)}	Low level output (Serial I _O port)	I _{OL(S)} = 4.2 mA	0		0.4	V
I _{OZ}	Off-state output current	Q Floating 0 < V _{out} < V _{CC}	-10		10	μA
I _I	Input current	0 < V _{in} < V _{CC}	-10		10	μA

Note 2: Current flowing into an IC is positive, out is negative.

CAPACITANCE (T_a = 25°C, f = 1MHz, V_I = 25mVrms)

Symbol	Pin name	Test conditions	Limits			Unit
			Min	Typ	Max	
C _{IN0}	RAS, CAS, WB/WE, SC, SE, DT/OE, DSF	V _I = V _{SS} , f = 1MHz, V _I = 25mVrms			7	pF
C _{IN1}	A ₀ ~ A ₈				7	pF
C _O	WIO ₀ ~ WIO ₇ , SIO ₀ ~ SIO ₇ , QSF				9	pF

MITSUBISHI LSIs

M5M442256AJ,L,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			M5M442256A-7	M5M442256A-8	M5M442256A-10	
	RAM port	SAM port	Max	Max	Max	
ICC1	Random R/W cycle, $\overline{RAS}/\overline{CAS}$ cycling, $t_{RC} = \min$ (Note 3, 4)	Standby ($SC = V_{IL}$)	85	75	65	mA
ICC2	Standby, $\overline{RAS} = V_{IH}$, $\overline{CAS} = V_{IH}$, $D_{OUT} = Hi-Z$		5	5	5	mA
ICC3	$\overline{RAS}$ only refresh cycle, $\overline{RAS} = \text{cycling}$, $\overline{CAS} = V_{IH}$, $t_{RC} = \min$ (Note 3, 4)		85	75	65	mA
ICC4	Page mode cycle, $\overline{RAS} = V_{IL}$, $\overline{CAS} = \text{cycling}$, $t_{PC} = \min$ (Note 3, 4)		75	65	55	mA
ICC5	$\overline{CAS}$ before $\overline{RAS}$ refresh, $t_{RC} = \min$ before (Note 3, 4)		85	75	65	mA
ICC6	Data transfer cycle, $t_{RC} = \min$ (Note 3, 4)		85	75	65	mA
ICC7	Random R/W cycle, $\overline{RAS}/\overline{CAS}$ cycling, $t_{RC} = \min$ (Note 3, 4)	Active ($t_{SCQ} = \min$)	115	105	95	mA
ICC8	Standby, $\overline{RAS} = V_{IH}$, $\overline{CAS} = V_{IH}$, $D_{OUT} = Hi-Z$ (Note 3, 4)		40	40	40	mA
ICC9	$\overline{RAS}$ only refresh cycle, $\overline{RAS} = \text{cycling}$, $\overline{CAS} = V_{IH}$, $t_{RC} = \min$ (Note 3, 4)		115	105	95	mA
ICC10	Page mode cycle, $\overline{RAS} = V_{IL}$, $\overline{CAS} = \text{cycling}$, $t_{PC} = \min$ (Note 3, 4)		105	95	85	mA
ICC11	$\overline{CAS}$ before $\overline{RAS}$ refresh, $t_{RC} = \min$ (Note 3, 4)		115	105	95	mA
ICC12	Data transfer cycle, $t_{RC} = \min$ (Note 3, 4)		115	105	95	mA

Note 3: ICC1, ICC3 ~ ICC12 are dependent on output loading. Specific values are obtained with the output open.
 4: ICC1, ICC3 ~ ICC12 are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

SWITCH CHARACTERISTICS (Ta = 0 ~ 70°C, VCC = 5V ± 12%, VSS = 0V, unless otherwise noted) (Note 5)

Symbol	Parameter	Limits						Unit
		M5M442256A-7		M5M442256A-8		M5M442256A-10		
		Min	Max	Min	Max	Min	Max	
t _{CAG}	Access time from $\overline{CAS}$ (Note 6, 8)		20		20		25	ns
t _{RAC}	Access time from $\overline{RAS}$ (Note 6, 9)		70		80		100	ns
t _{CAA}	Column address access time (Note 6, 10)		35		40		50	ns
t _{CPA}	Access time from $\overline{CAS}$ precharge (Note 6, 11)		40		45		55	ns
t _{OEA}	Access time from $\overline{OE}$ (Note 6)		20		20		25	ns
t _{CLZ}	Output low impedance from $\overline{CAS}$ low	5		5		5		ns
t _{OFF}	Output disable time after $\overline{CAS}$ high (Note 12)	0	20	0	20	0	20	ns
t _{OEZ}	Output disable time after $\overline{OE}$ high (Note 12)	0	20	0	20	0	20	ns
t _{SCA}	Access time from $\overline{SC}$ high (Note 7)		25		25		25	ns
t _{SOA}	Access time from $\overline{SE}$ low (Note 7)	0	20	0	20	0	25	ns
t _{SOZ}	Output disable time after $\overline{SE}$ high (Note 12)	0	20	0	20	0	20	ns
t _{SOH}	Serial output hold time after $\overline{SC}$ high	5		5		5		ns

Note 5: An initial pause of 500 μ s is required after power up followed by eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock, such as $\overline{RAS}$ only refresh)

Note that $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 8 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

6: Measured with a load circuit equivalent to 1TTL loads and 100pF.

7: Measured with a load circuit equivalent to 1TTL loads and 30pF.

8: Assume that $t_{ACD} \geq t_{RCD}(\max)$ and $t_{RAD} \leq t_{RAD}(\max)$.

9: Assume that $t_{ACD} \leq t_{RCD}(\max)$ and $t_{RAD} \geq t_{RAD}(\max)$.

10: Assume that $t_{ACD} - t_{RAD} \leq t_{CAA}(\max) - t_{CAC}(\min)$ and $t_{RCD} \geq t_{RCD}(\max)$.

11: Assume that $t_{CP} \leq t_{CP}(\max)$.

12: $t_{OFF}(\max)$, $t_{SOZ}(\max)$ and $t_{OEZ}(\max)$ define the time at which output achieves high impedance state.

M5M442256AJ,L,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

TIMING REQUIREMENTS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted) (Note 13, 14)

(1) Read, Write, Refresh, Load Color Register, Block Write, Flash Write

Read/Write Transfer and Page Mode Cycles

Symbol	Parameter	Limits						Unit
		M5M442256A-7		M5M442256A-8		M5M442256A-10		
		Min	Max	Min	Max	Min	Max	
t _{RC}	Read, write cycle time	130		150		180		ns
t _{RAS}	RAS low pulse width	70	10000	80	10000	100	10000	ns
t _{CAS}	CAS low pulse width	20	10000	20	10000	25	10000	ns
t _{CSH}	CAS hold time after RAS	70		80		100		ns
t _{RSH}	RAS hold time after CAS	25		25		30		ns
t _{REF}	Refresh cycle time		8		8		8	ms
t _{RP}	RAS high pulse width	50		60		70		ns
t _{RCD}	Delay time RAS low to CAS low (Note 15)	20	50	25	60	25	75	ns
t _{CRP}	Delay time CAS high to RAS low (Note 16)	10		10		10		ns
t _{CPN}	CAS high pulse width	10		10		10		ns
t _{ASR}	Row address setup time before RAS	0		0		0		ns
t _{RAH}	Row address hold time after RAS	10		15		15		ns
t _{RAD}	Column address delay time from RAS (Note 17)	15	35	20	40	20	50	ns
t _{ASC}	Column address setup time before CAS	0		0		0		ns
t _{CAH}	Column address hold time after CAS	15		20		20		ns
t _{WSR}	WB/WE setup time before RAS	0		0		0		ns
t _{RWH}	WB/WE hold time after RAS	10		15		15		ns
t _{DTRS}	DT/OE setup time before RAS	0		0		0		ns
t _{DTRH}	DT/OE high hold time after RAS	10		15		15		ns
t _{FSR}	DSF setup time before RAS	0		0		0		ns
t _{RFH}	DSF hold time after RAS	10		15		15		ns
t _{FSC}	DSF setup time before CAS	0		0		0		ns
t _{CFH}	DSF hold time after CAS	15		20		20		ns
t _{WS}	Write mask setup time before RAS	0		0		0		ns
t _{WH}	Write mask hold time after RAS	10		15		15		ns
t _T	Transition time (Note 18)	3	35	3	35	3	35	ns

Note 13: Timing requirements are assumed $t_T = 5\text{ns}$.

14: $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals.

15: $t_{RCD}(\text{max})$ limit ensures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than $t_{RCD}(\text{max})$, access time is controlled by t_{CAC} or t_{CAA} as shown in notes 7 or 9.

16: t_{CRP} requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.

17: $t_{RAD}(\text{max})$ limit ensures that $t_{RAC}(\text{max})$ can be met. $t_{RAD}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than $t_{RAD}(\text{max})$, access time is controlled by t_{CAC} or t_{CAA} as shown in notes 7 or 9.

18: t_T is measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$.

M5M442256AJ,L,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

(2) Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M442256A-7		M5M442256A-8		M5M442256A-10		
		Min	Max	Min	Max	Min	Max	
t _{RCS}	Read setup time before $\overline{\text{CAS}}$ low	0		0		0		ns
t _{RCH}	Read hold time after $\overline{\text{CAS}}$ high (Note 19)	0		0		0		ns
t _{RRH}	Read hold time after $\overline{\text{RAS}}$ high (Note 19)	0		0		0		ns
t _{RAL}	Column address to $\overline{\text{RAS}}$ setup time	35		40		50		ns
t _{RPC}	Precharge to $\overline{\text{CAS}}$ active time	0		0		0		ns
t _{h(CLOE)}	$\overline{\text{OE}}$ hold time after $\overline{\text{CAS}}$ low	20		25		25		ns
t _{h(RLOE)}	$\overline{\text{OE}}$ hold time after $\overline{\text{RAS}}$ low	70		80		100		ns
t _{DOEL}	Delay time data to $\overline{\text{OE}}$ low	0		0		0		ns
t _{OEHD}	Delay time $\overline{\text{OE}}$ high to Data	15		15		20		ns
t _{h(OECH)}	$\overline{\text{CAS}}$ hold time after $\overline{\text{OE}}$ low	20		20		25		ns
t _{h(OERH)}	$\overline{\text{RAS}}$ hold time after $\overline{\text{OE}}$ low	20		20		25		ns

Note 19: Either t_{RCH} or t_{RRH} must be satisfied.

(3) Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M442256A-7		M5M442256A-8		M5M442256A-10		
		Min	Max	Min	Max	Min	Max	
t _{WCS}	Write setup time before $\overline{\text{CAS}}$ (Note 20)	0		0		0		ns
t _{WCH}	Write hold time after $\overline{\text{CAS}}$	15		15		15		ns
t _{CWL}	$\overline{\text{CAS}}$ hold time after write	20		20		25		ns
t _{RWL}	$\overline{\text{RAS}}$ hold time after write	20		20		25		ns
t _{WP}	Write pulse width	15		15		15		ns
t _{DSC}	Data setup time before $\overline{\text{CAS}}$	0		0		0		ns
t _{DHC}	Data hold time after $\overline{\text{CAS}}$	15		15		20		ns
t _{DSW}	Data setup time before write	0		0		0		ns
t _{DHW}	Data hold time after write	15		15		20		ns
t _{OEHD}	Delay time $\overline{\text{OE}}$ high to data	15		15		20		ns
t _{h(WOE)}	$\overline{\text{OE}}$ hold time after write	15		15		20		ns

Note 20: t_{WCS} , t_{RWL} , t_{CWL} and t_{DHW} do not define the limits of operation, but are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$, early write cycle is performed with data outputs keeping high impedance state. If $t_{RWL} \geq t_{RWL}(\min)$, $t_{CWL} \geq t_{CWL}(\min)$ and $t_{DHW} \geq t_{DHW}(\min)$, read-write cycle is performed with the data of the selected address being out from the data output. If neither of the above condition is satisfied, the condition of data out (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indetermined.

MITSUBISHI LSIs

M5M442256AJ,L,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

(4) Read-Write and Read-Modify-Write Cycle

Symbol	Parameter	Limits						Unit
		M5M442256A-7		M5M442256A-8		M5M442256A-10		
		Min	Max	Min	Max	Min	Max	
t _{RWC}	Read-write, read-modify-write cycle time	185		205		245		ns
t _{RAS}	$\overline{\text{RAS}}$ low pulse width	115	10000	125	10000	155	10000	ns
t _{CAS}	$\overline{\text{CAS}}$ low pulse width	70	10000	70	10000	85	10000	ns
t _{CSH}	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$	115		125		155		ns
t _{RSH}	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$	70		70		85		ns
t _{RCS}	Read setup time before $\overline{\text{CAS}}$	0		0		0		ns
t _{CWD}	Delay time $\overline{\text{CAS}}$ to write (Note 20)	40		40		50		ns
t _{RWD}	Delay time $\overline{\text{RAS}}$ to write (Note 20)	90		100		125		ns
t _{CWL}	$\overline{\text{CAS}}$ hold time after write	20		20		25		ns
t _{RWL}	$\overline{\text{RAS}}$ hold time after write	20		20		25		ns
t _{WP}	Write pulse width	15		15		15		ns
t _{DSW}	Data setup time before write	0		0		0		ns
t _{DHW}	Data hold time after write	15		15		20		ns
t _{AWD}	Delay time address to write (Note 20)	55		60		75		ns
t _{h(OLOE)}	$\overline{\text{OE}}$ hold time after $\overline{\text{CAS}}$	20		20		25		ns
t _{h(ROLE)}	$\overline{\text{OE}}$ hold time after $\overline{\text{RAS}}$	70		80		100		ns
t _{DOEL}	Delay time data to $\overline{\text{OE}}$ low	0		0		0		ns
t _{OEHD}	Delay time $\overline{\text{OE}}$ high to data	15		15		20		ns
t _{h(WOE)}	$\overline{\text{OE}}$ hold time after write	15		15		20		ns

(5) Fast-Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle)

Symbol	Parameter	Limits						Unit
		M5M442256A-7		M5M442256A-8		M5M442256A-10		
		Min	Max	Min	Max	Min	Max	
t _{PC}	Read, write cycle time	45		50		60		ns
t _{RWPC}	Read-write, read modify write cycle time	95		100		115		ns
t _{RASP}	RAS low pulse width	115	100000	135	100000	160	100000	ns
t _{CAS}	CAS low pulse width	20	10000	20	10000	25	10000	ns
t _{CP}	CAS high pulse width (Note 21)	10	15	10	20	10	25	ns
t _{RSH}	RAS hold time after CAS	25		25		30		ns

Note 21: t_{CP}(max) is specified as a reference point only. If t_{CP}(max) ≤ t_{CP}, access time is determined by t_{CAC}.

(6) $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle (Note 22)

Symbol	Parameter	Limits						Unit
		M5M442256A-7		M5M442256A-8		M5M442256A-10		
		Min	Max	Min	Max	Min	Max	
t _{CSR}	$\overline{\text{CAS}}$ setup time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	10		10		10		ns
t _{CHR}	$\overline{\text{CAS}}$ hold time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	15		15		20		ns
t _{RPC}	Precharge to $\overline{\text{CAS}}$ active time	0		0		0		ns

Note 22: Eight or more $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles are necessary for proper operation of $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh mode.

M5M442256AJ,L,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

(7) Normal-Read/Normal-Write/Pseudo-Write Transfer Cycle

Symbol	Parameter	Limits						Unit
		M5M442256A-7		M5M442256A-8		M5M442256A-10		
		Min	Max	Min	Max	Min	Max	
t _{RDH}	$\overline{DT}/\overline{OE}$ low hold time after $\overline{RAS}$	10	10000	15	10000	15	10000	ns
t _{RSD}	Delay time $\overline{RAS}$ to SC	80		80		100		ns
t _{ASD}	Delay time address to SC	40		40		50		ns
t _{CSD}	Delay time $\overline{CAS}$ to SC	30		30		30		ns
t _{SDH}	SC hold time after $\overline{DT}$	15		15		15		ns
t _{RQ}	Delay time $\overline{RAS}$ to QSF		85		85		85	ns
t _{AQ}	Delay time address to QSF		40		40		40	ns
t _{CQ}	Delay time $\overline{CAS}$ to QSF		35		35		35	ns
t _{DTQ}	Delay time $\overline{DT}$ to QSF		25		25		25	ns
t _{TRP}	$\overline{DT}$ to $\overline{RAS}$ precharge time	70		80		90		ns
t _{DTW}	$\overline{DT}$ high pulse width	30		30		30		ns
t _{ES}	$\overline{SE}$ setup time before $\overline{RAS}$ low	0		0		0		ns
t _{EH}	$\overline{SE}$ hold time after $\overline{RAS}$ low	15		15		15		ns
t _{SRS}	Last SC to $\overline{RAS}$ setup time (serial input)	30		30		30		ns
t _{SRH}	$\overline{RAS}$ to first SC delay time (serial input)	20		20		20		ns
t _{SZS}	Serial input to first SC delay time (serial in → serial out)	0		0		0		ns
t _{SDZ}	Serial output turn-off delay from $\overline{RAS}$ (serial out → serial in)	10	50	10	50	10	50	ns
t _{SDP}	$\overline{RAS}$ to serial input delay time (serial out → serial in)	50		50		50		ns

(8) Real Time Read Transfer Cycle

Symbol	Parameter	Limits						Unit
		M5M442256A-7		M5M442256A-8		M5M442256A-10		
		Min	Max	Min	Max	Min	Max	
t _{RDH}	$\overline{DT}$ hold time after $\overline{RAS}$	55	10000	65	10000	80	10000	ns
t _{CDH}	$\overline{DT}$ hold time after $\overline{CAS}$	30		30		30		ns
t _{ADH}	$\overline{DT}$ hold time after address	30		30		30		ns
t _{SDD}	Delay time SC to $\overline{DT}$	5		5		5		ns
t _{SDH}	SC hold time after $\overline{DT}$	15		15		15		ns
t _{DTQ}	Delay time $\overline{DT}$ to QSF		25		25		25	ns

M5M442256AJ,L,TP,RT-7,-8,-10

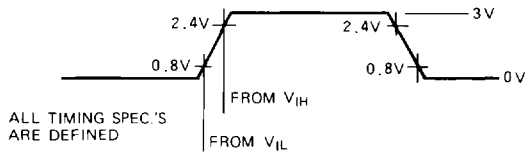
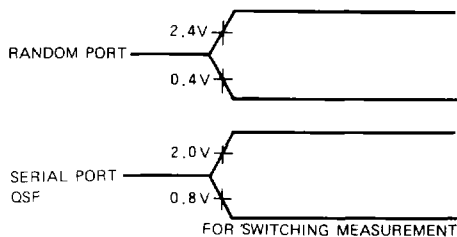
FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

(9) Split Read/Write Transfer Cycle

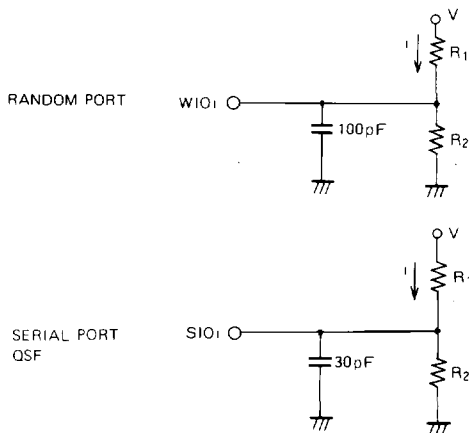
Symbol	Parameter	Limits						Unit
		M5M442256A-7		M5M442256A-8		M5M442256A-10		
		Min	Max	Min	Max	Min	Max	
t _{SCSR}	Split transfer setup time	30		30		30		ns
t _{SCHR}	Split transfer hold time	30		30		30		ns

(10) Serial Read/Serial Write Cycle

Symbol	Parameter	Limits						Unit
		M5M442256A-7		M5M442256A-8		M5M442256A-10		
		Min	Max	Min	Max	Min	Max	
t _{SCC}	SC clock cycle time	30		30		30		ns
t _{SGH}	SC high pulse width	10		10		10		ns
t _{SCL}	SC low pulse width	10		10		10		ns
t _{SOP}	$\overline{SE}$ high pulse width	25		25		25		ns
t _{SOE}	$\overline{SE}$ low pulse width	25		25		25		ns
t _{SIS}	Serial input data setup time before SC high	0		0		0		ns
t _{SIH}	Serial input data hold time after SC high	15		15		15		ns
t _{SWIS}	$\overline{SE}$ disable setup time before SC high	5		5		5		ns
t _{SWIH}	$\overline{SE}$ disable hold time after SC high	15		15		15		ns
t _{SWS}	$\overline{SE}$ enable setup time before SC high	5		5		5		ns
t _{SWH}	$\overline{SE}$ enable hold time after SC high	15		15		15		ns
t _{SZE}	Serial input to $\overline{SE}$ delay time	0		0		0		ns
t _{SCQ}	Delay time SC to QSF		25		25		25	ns

M5M442256AJ,L,TP,RT-7,-8,-10**FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM****Switching Measurement Condition****1. Input reference point****2. Output reference point**

DC LEVEL OF OUTPUT IS $V_{OH} = 2.4V$, $V_{OL} = 0.4V$

3. Load condition

$$\begin{bmatrix} V = V_{OH} + R_1 \cdot I_H & V = V_{OL} + R_1 \cdot I_L \\ V_{OH} = (I_H - I_{OH}) \cdot R_2 & V_{OL} = (I_L - I_{OL}) \cdot R_2 \end{bmatrix}$$

When $V = 5V$, $R_1 = 919 \Omega$, $R_2 = 497 \Omega$

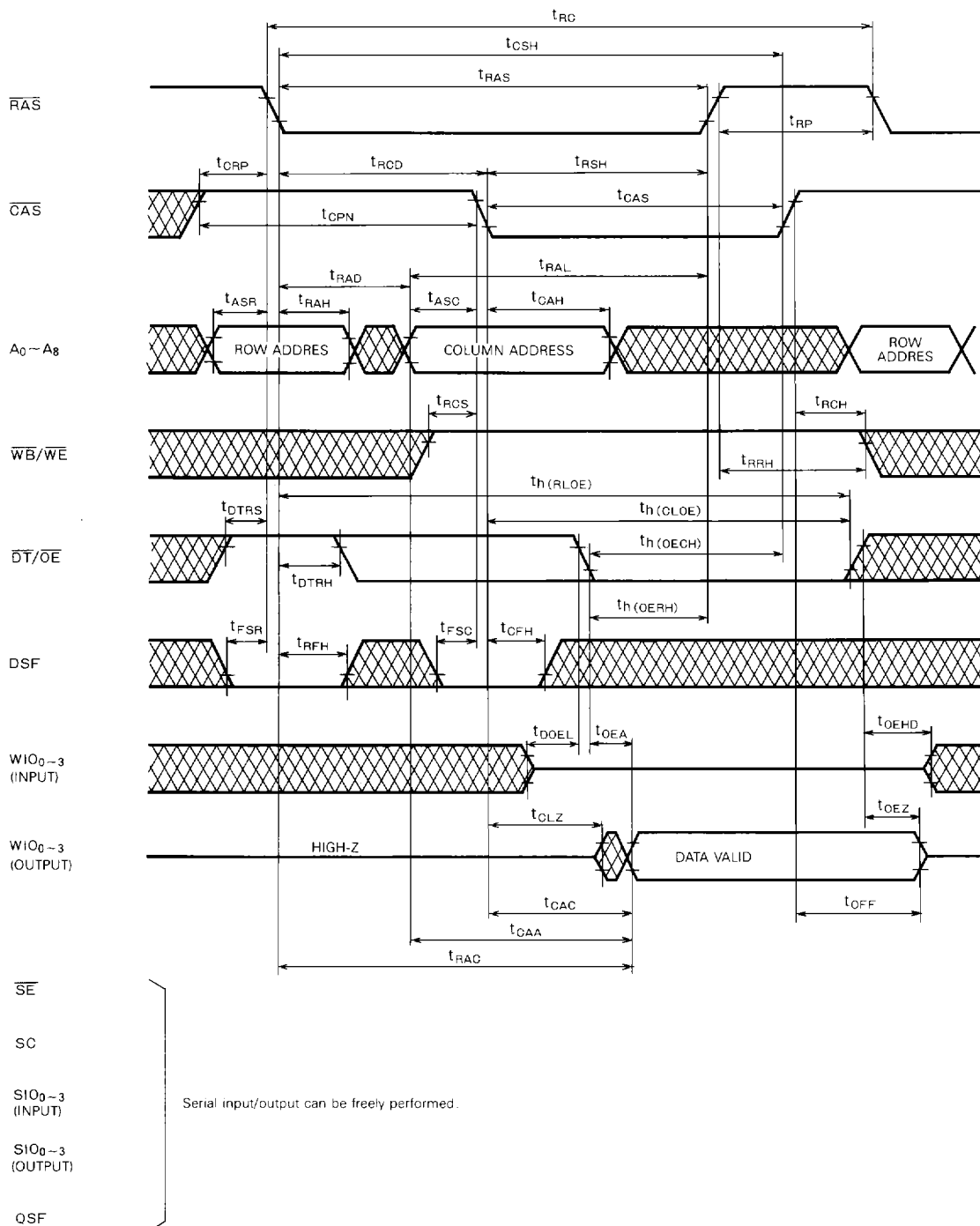
$$\begin{bmatrix} R_1 = \frac{V_{OH}(V - V_{OL}) - V_{OL}(V - V_{OH})}{V_{OH} \cdot I_{OL} - V_{OL} \cdot I_{OH}} \\ R_2 = \frac{V_{OH} \cdot R_1}{(V - V_{OH}) - I_{OH} \cdot R_1} \end{bmatrix}$$

M5M442256AJ,L,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

TIMING DIAGRAMS

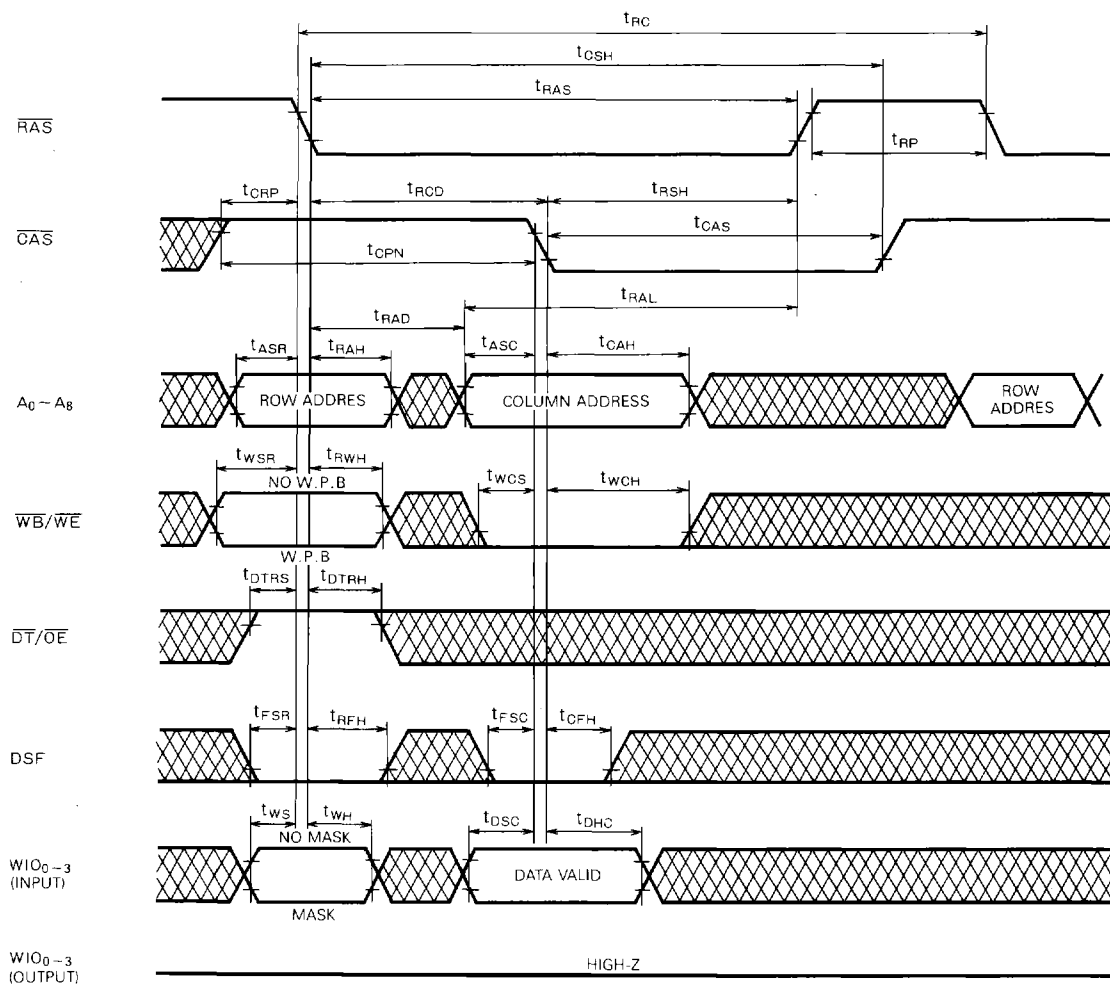
Read Cycle



M5M442256AJ,L,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

Write Cycle (Early Write)



SE

SC

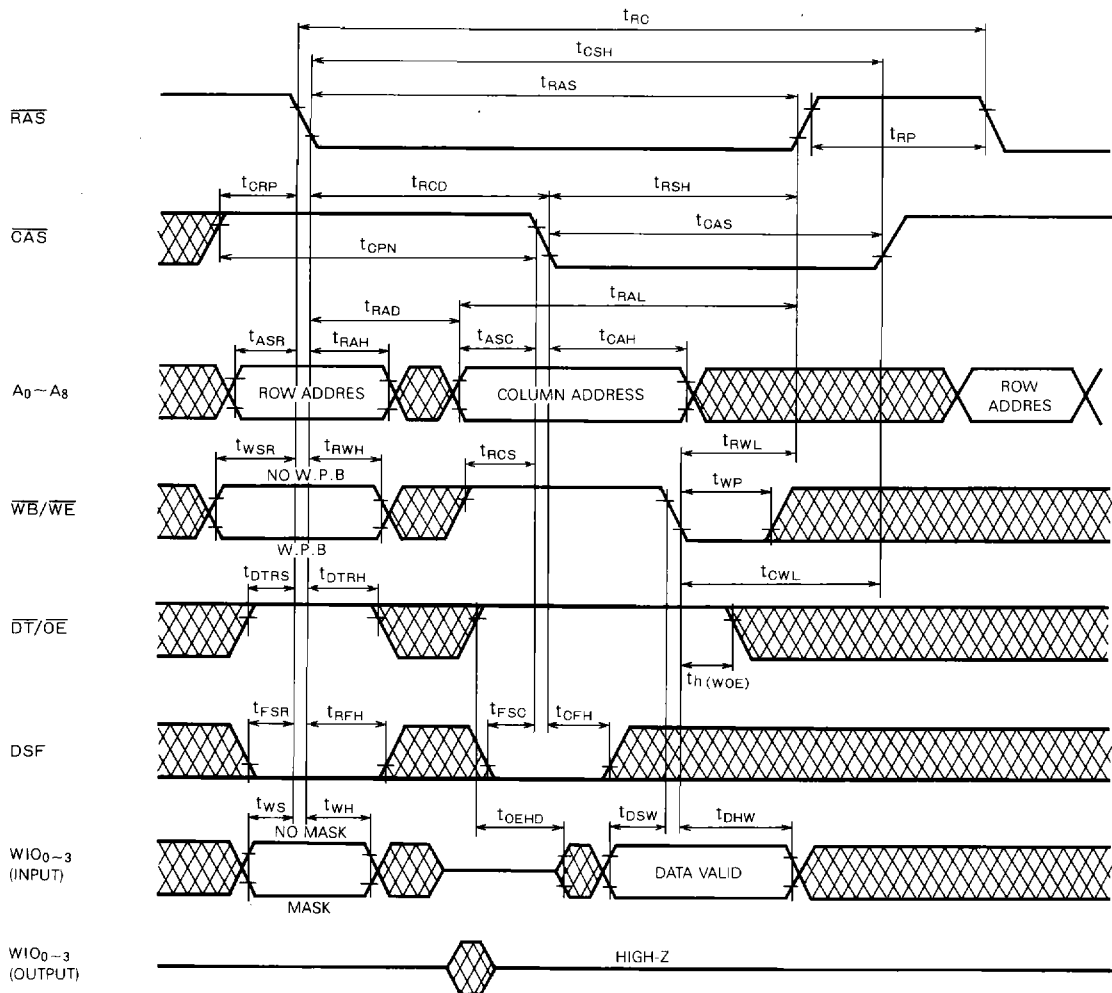
SIO₀-3
(INPUT)

SIO₀-3
(OUTPUT)

QSF

Serial input/output can be freely performed.

Write Cycle (Late Write)



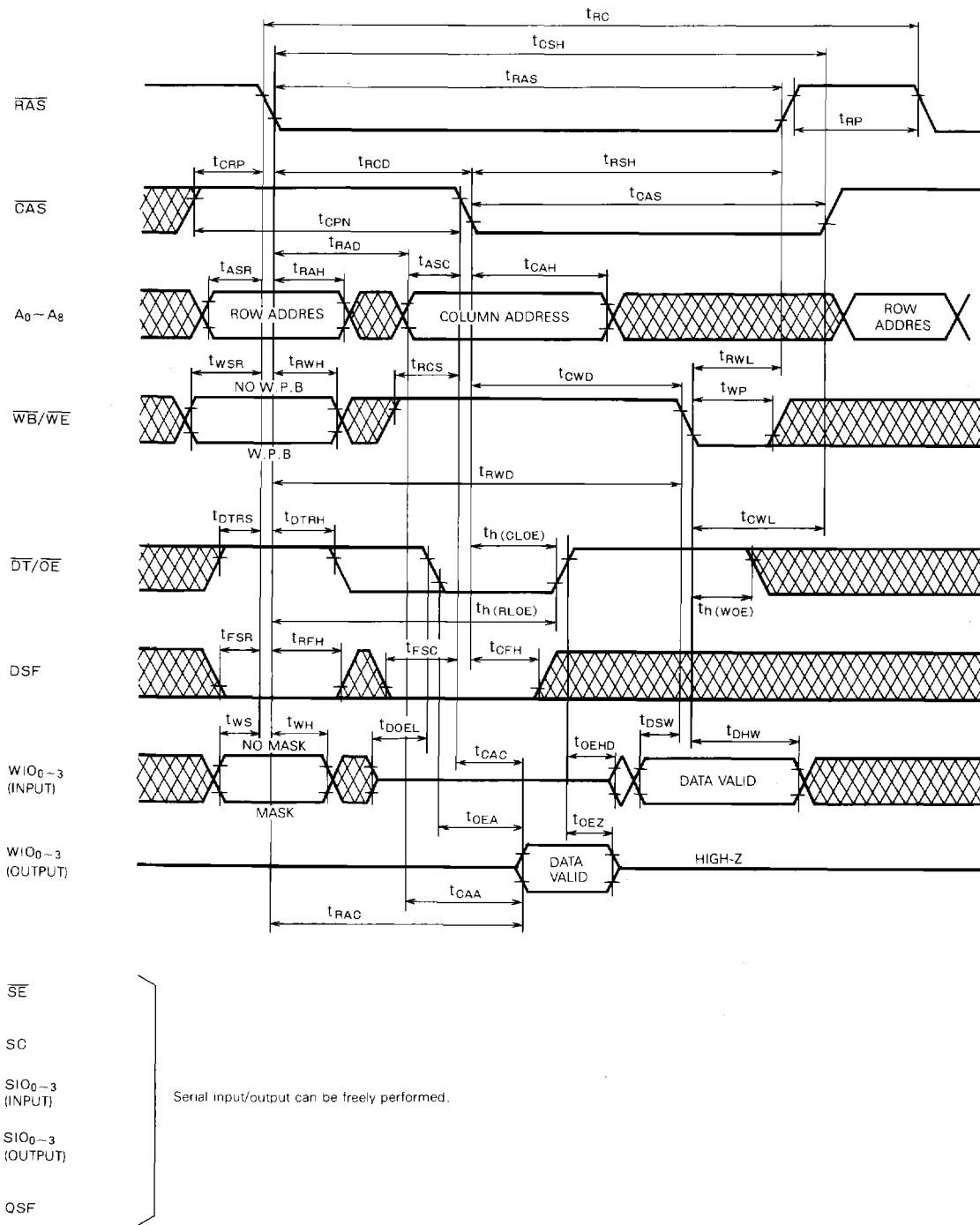
QSF

Serial input/output can be freely performed.

M5M442256AJ,L,TP,RT-7,-8,-10

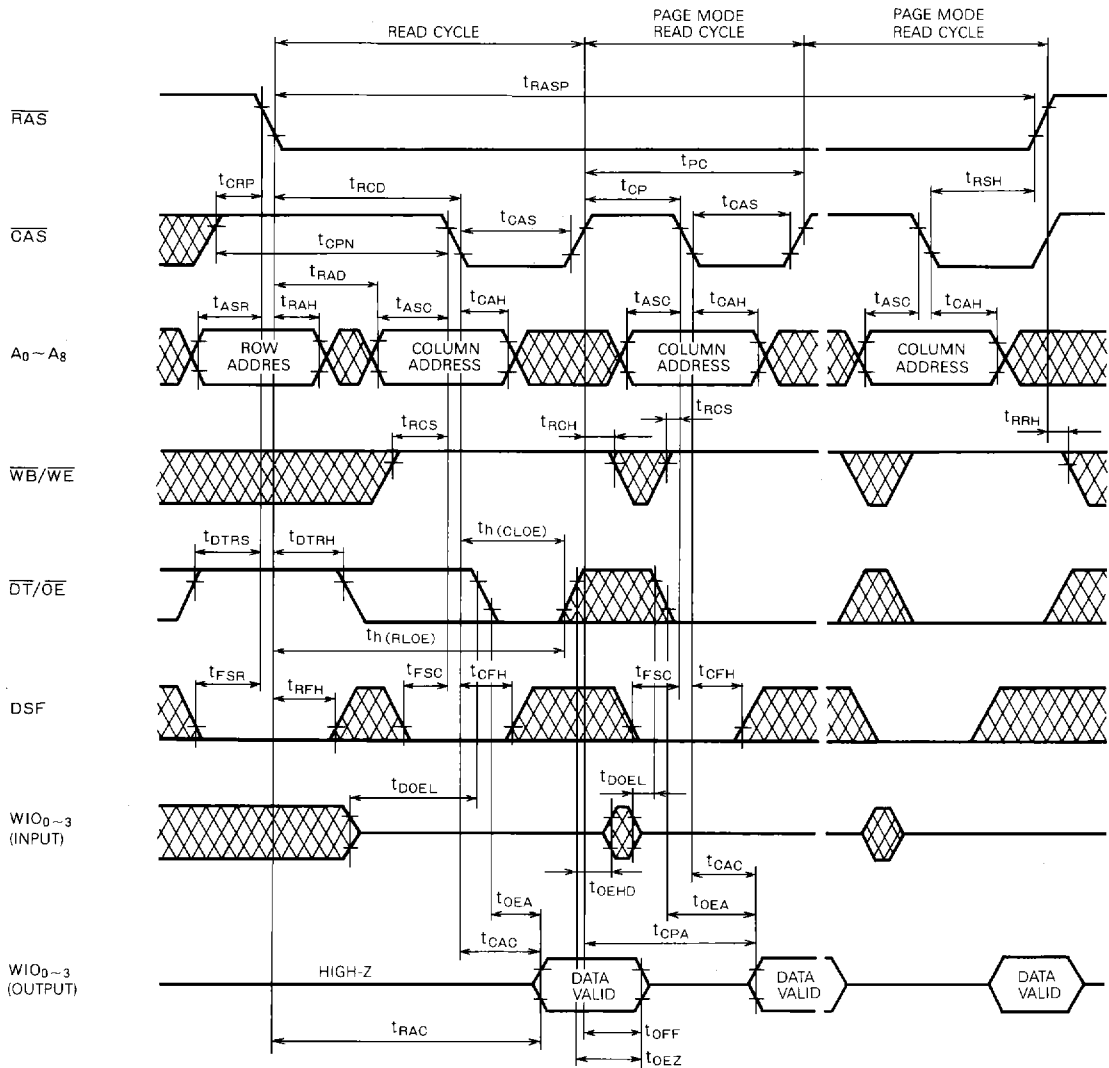
FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

Read Modify Write Cycle



FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

Page Mode Read Cycle



SE

SC

SIO0~3
(INPUT)

SIO0~3
(OUTPUT)

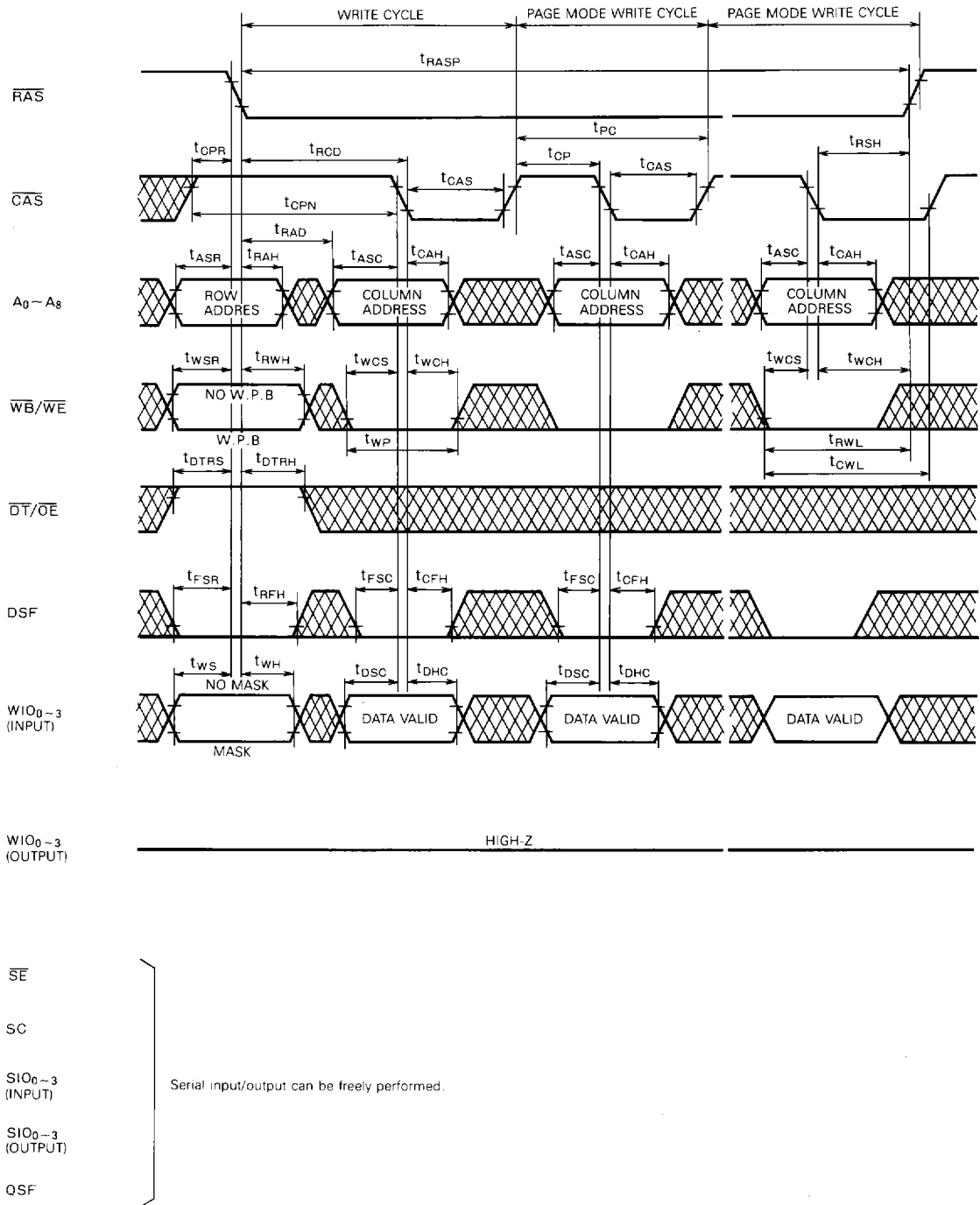
QSF

Serial input/output can be freely performed.

M5M44256AJ,L,TP,RT-7,-8,-10

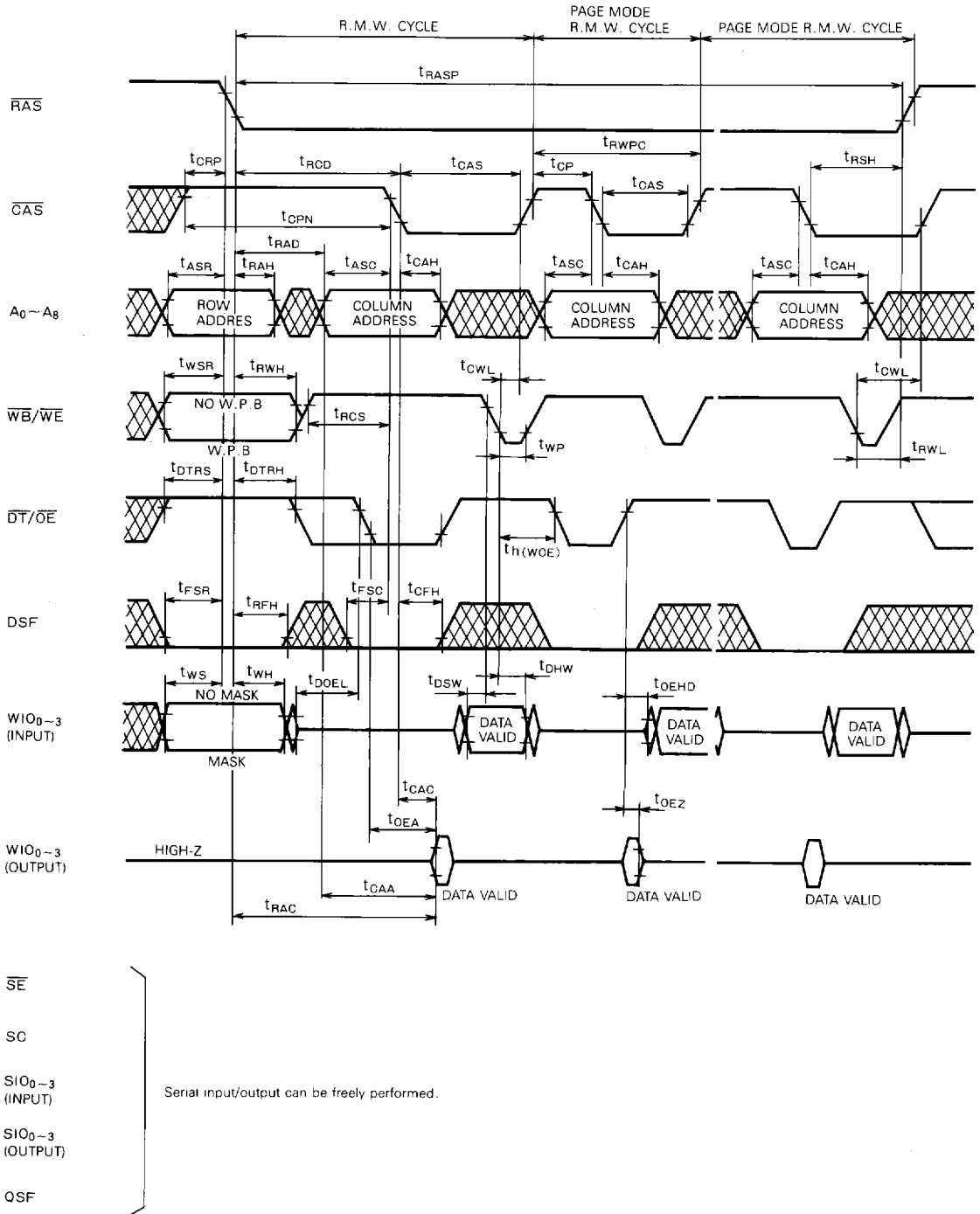
FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

Page Mode Write Cycle (Early Write)



FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

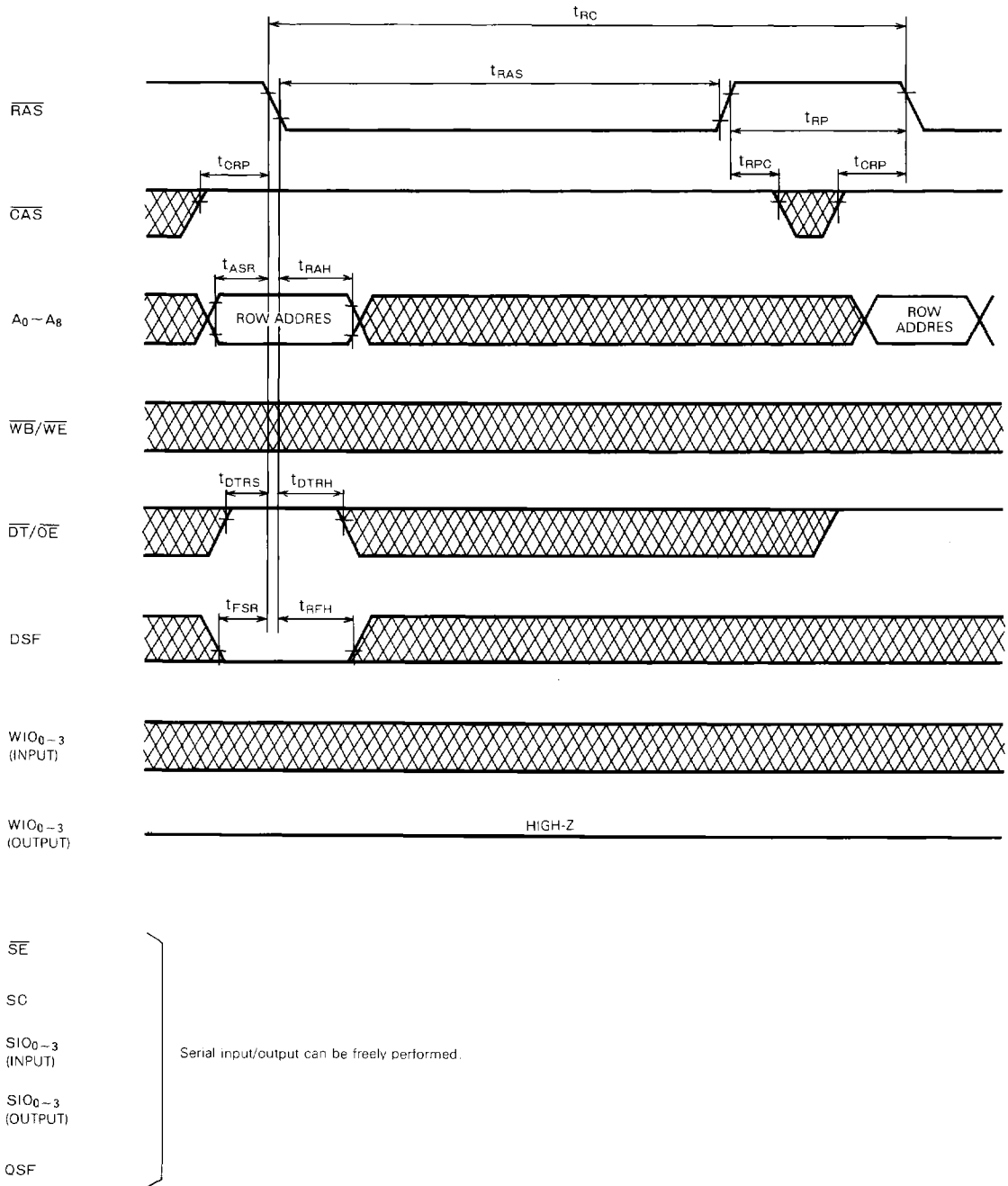
Page Mode Write Cycle (Read-Modify-Write)



M5M442256AJ,L,TP,RT-7,-8,-10

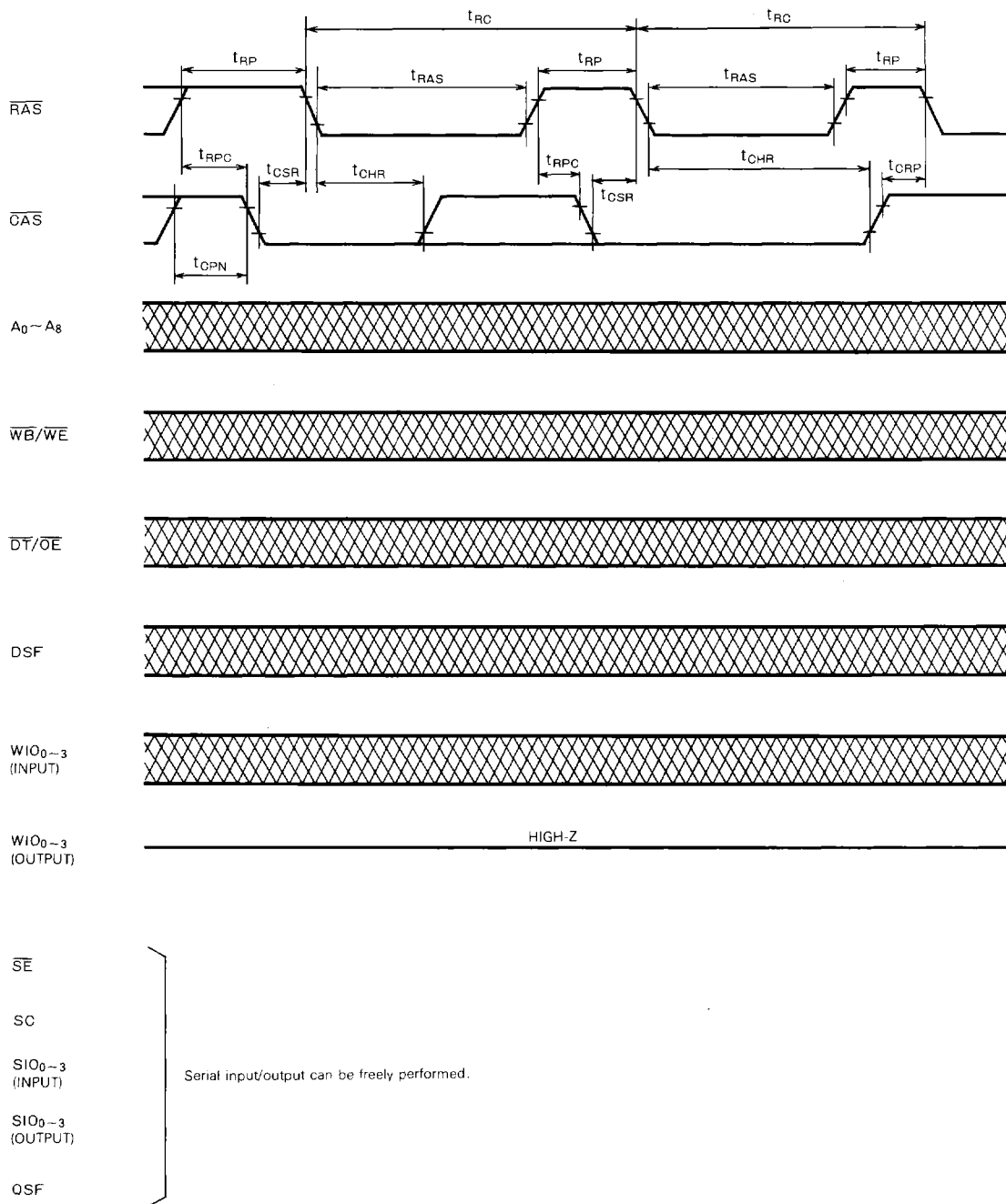
FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

RAS Only Refresh Cycle



FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

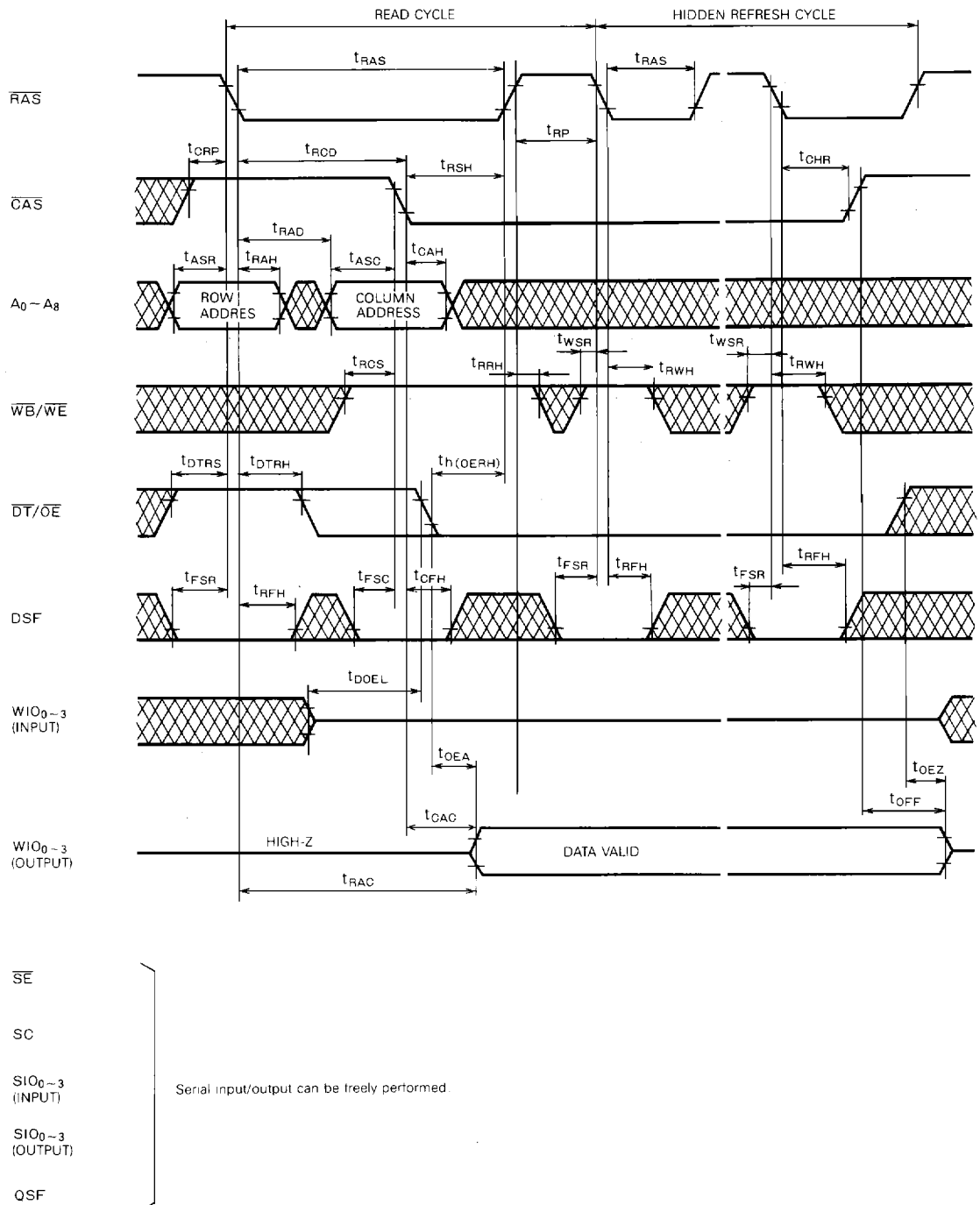
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle



M5M442256AJ,L,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

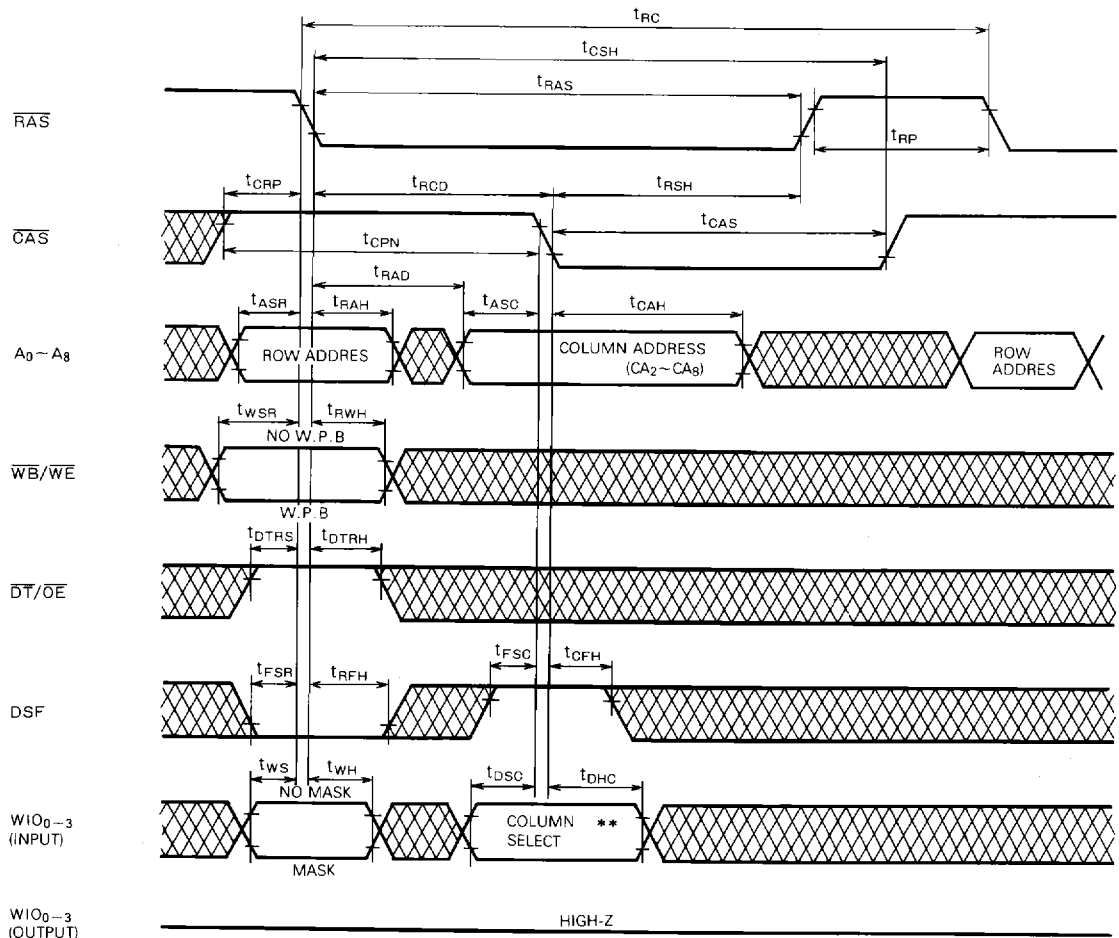
Hidden Refresh Cycle



M5M442256AJ,L,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

Block Write Cycle



SE
SC
SIO₀~3 (INPUT)
SIO₀~3 (OUTPUT)
QSF

Serial input/output can be freely performed.

Column select **

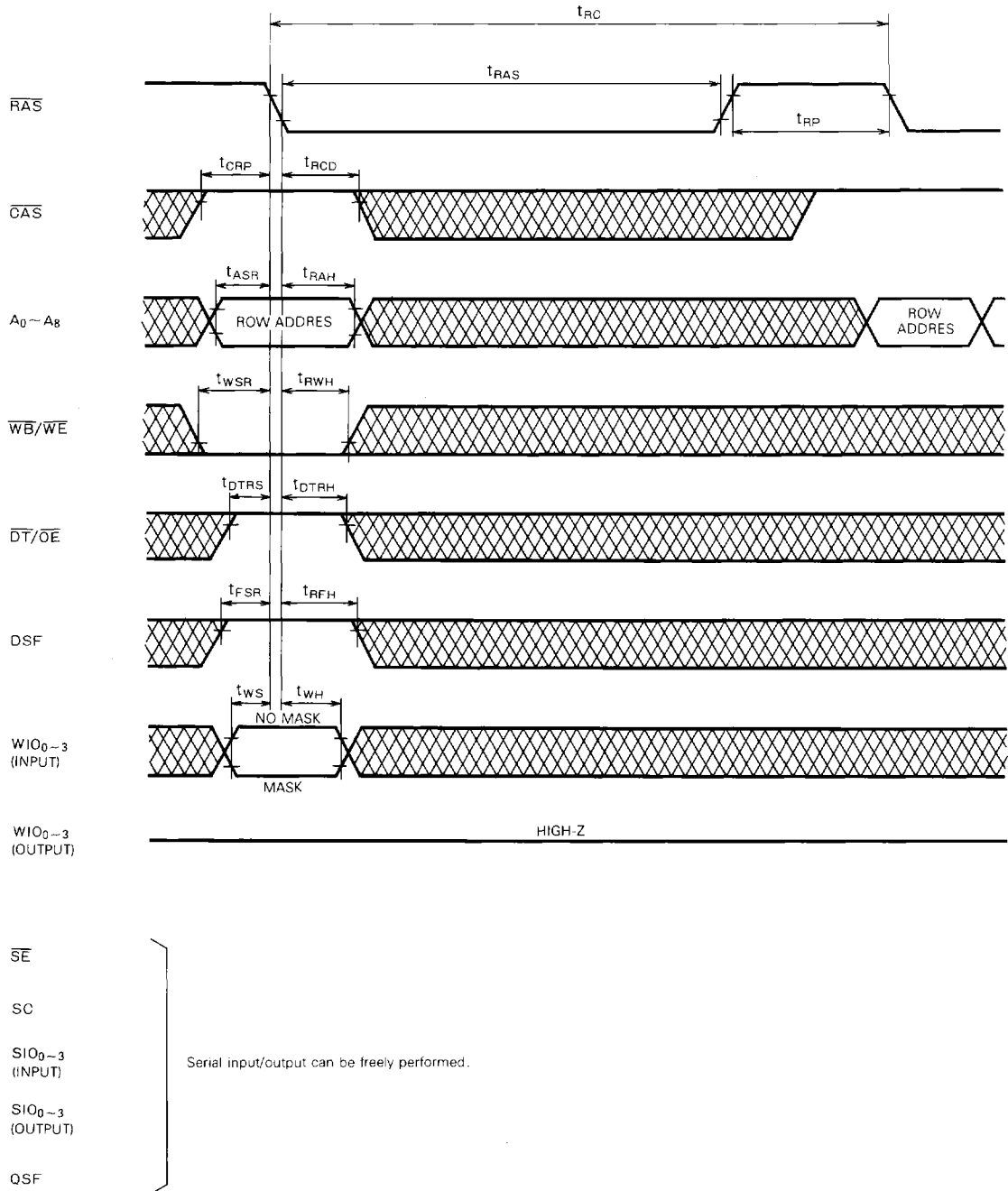
WIO 0	Col-0	CA ₀ =0, CA ₁ =0
WIO 1	Col-1	CA ₀ =1, CA ₁ =0
WIO 2	Col-2	CA ₀ =0, CA ₁ =1
WIO 3	Col-3	CA ₀ =1, CA ₁ =1

WIO 0	Col-0	$CA_0=0, CA_1=0$
WIO 1	Col-1	$CA_0=1, CA_1=0$
WIO 2	Col-2	$CA_0=0, CA_1=1$
WIO 3	Col-3	$CA_0=1, CA_1=1$

M5M442256AJ,L,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

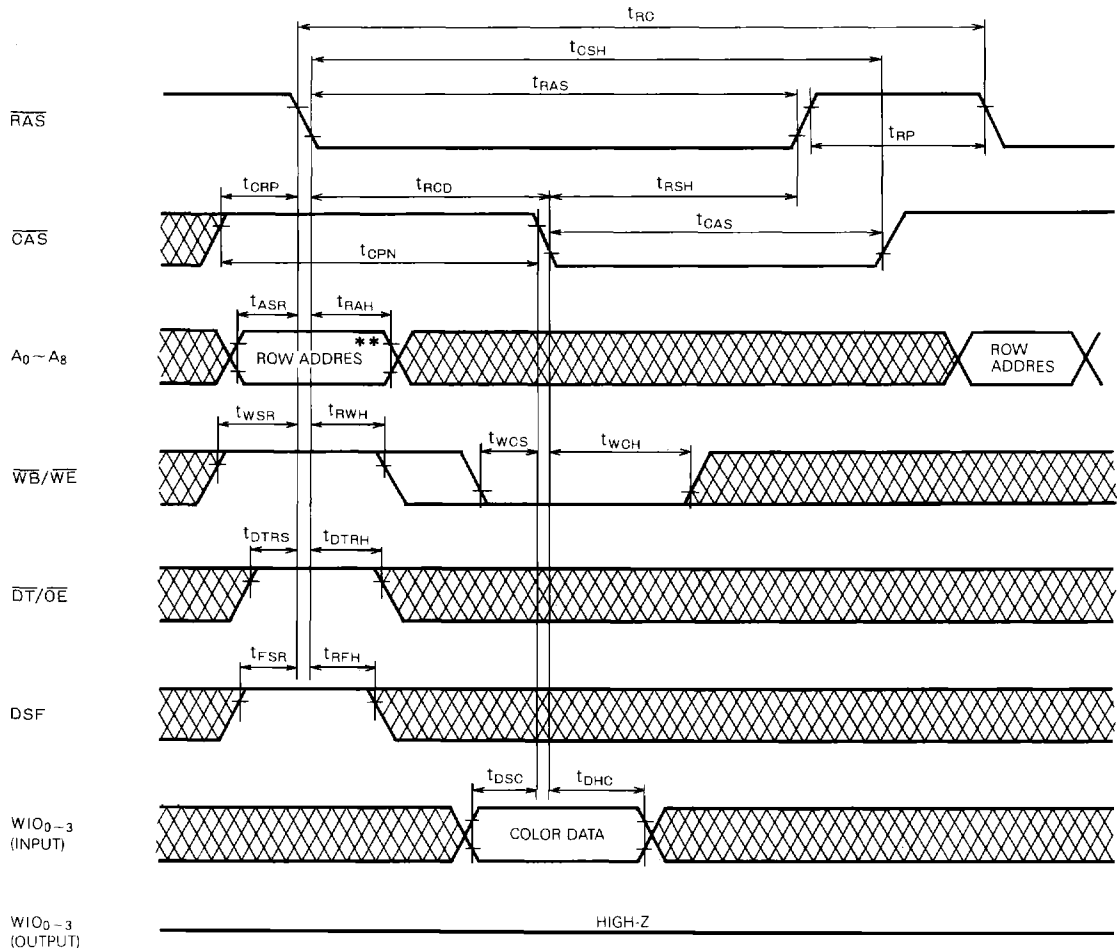
Flash Write Cycle



M5M442256AJ,L,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

Load Color Register Cycle



$\overline{SE}$

$\overline{SC}$

$SIO_0 \sim 3$
(INPUT)

$SIO_0 \sim 3$
(OUTPUT)

$\overline{QSF}$

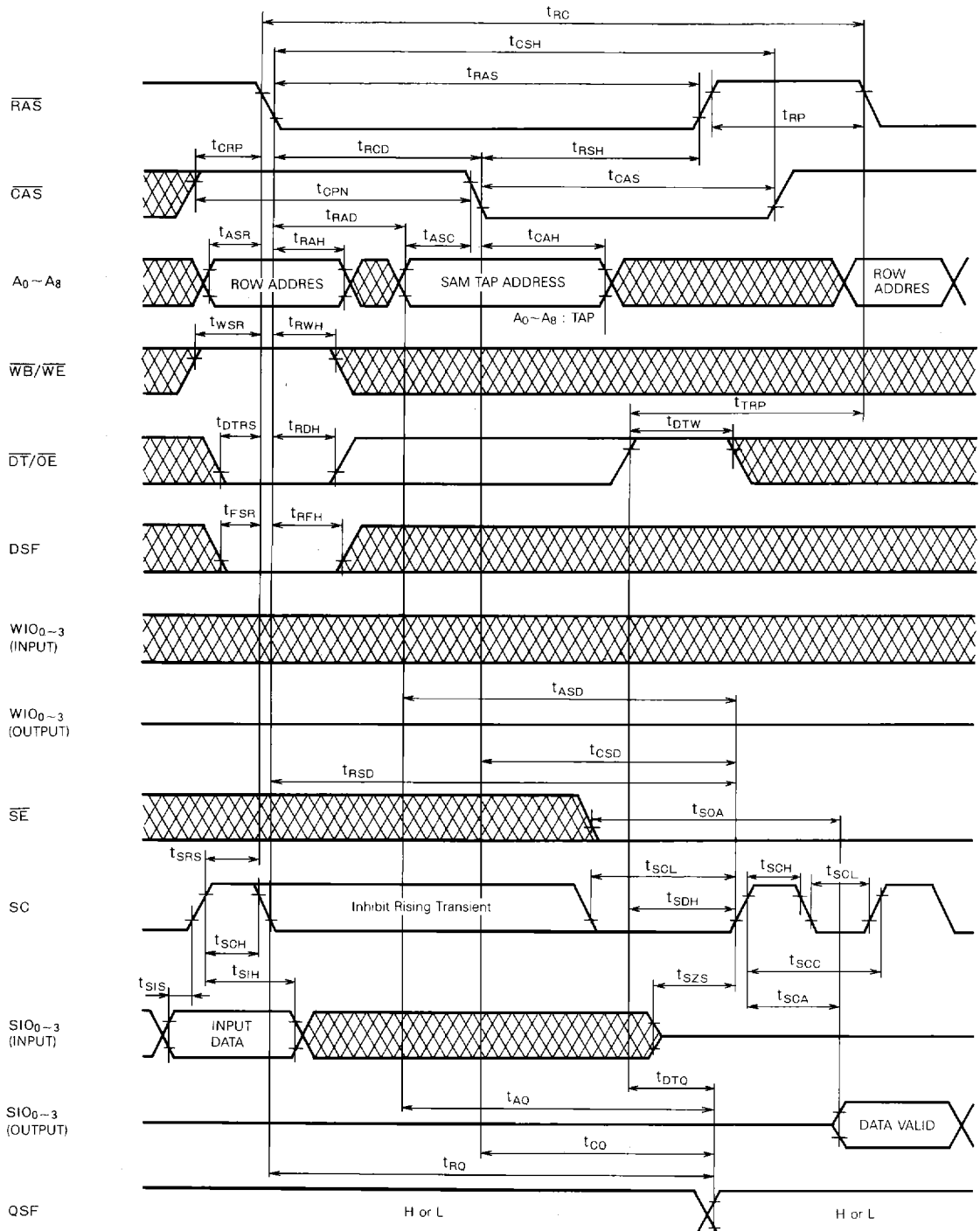
Serial input/output can be freely performed.

** ROW ADDRESS: For refresh address

M5M442256AJ,L,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

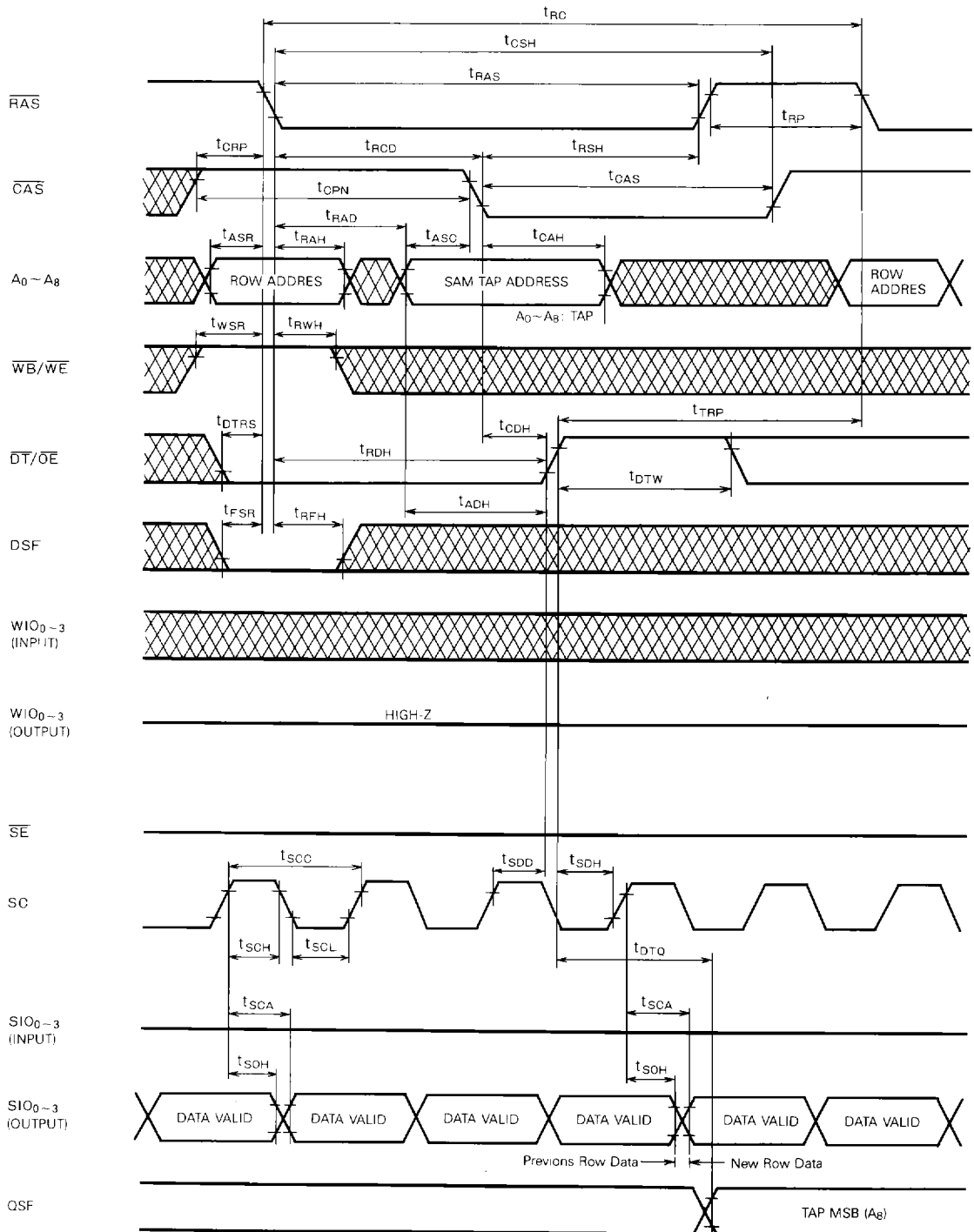
Read Transfer Cycle (Previous Transfer=Write Transfer)



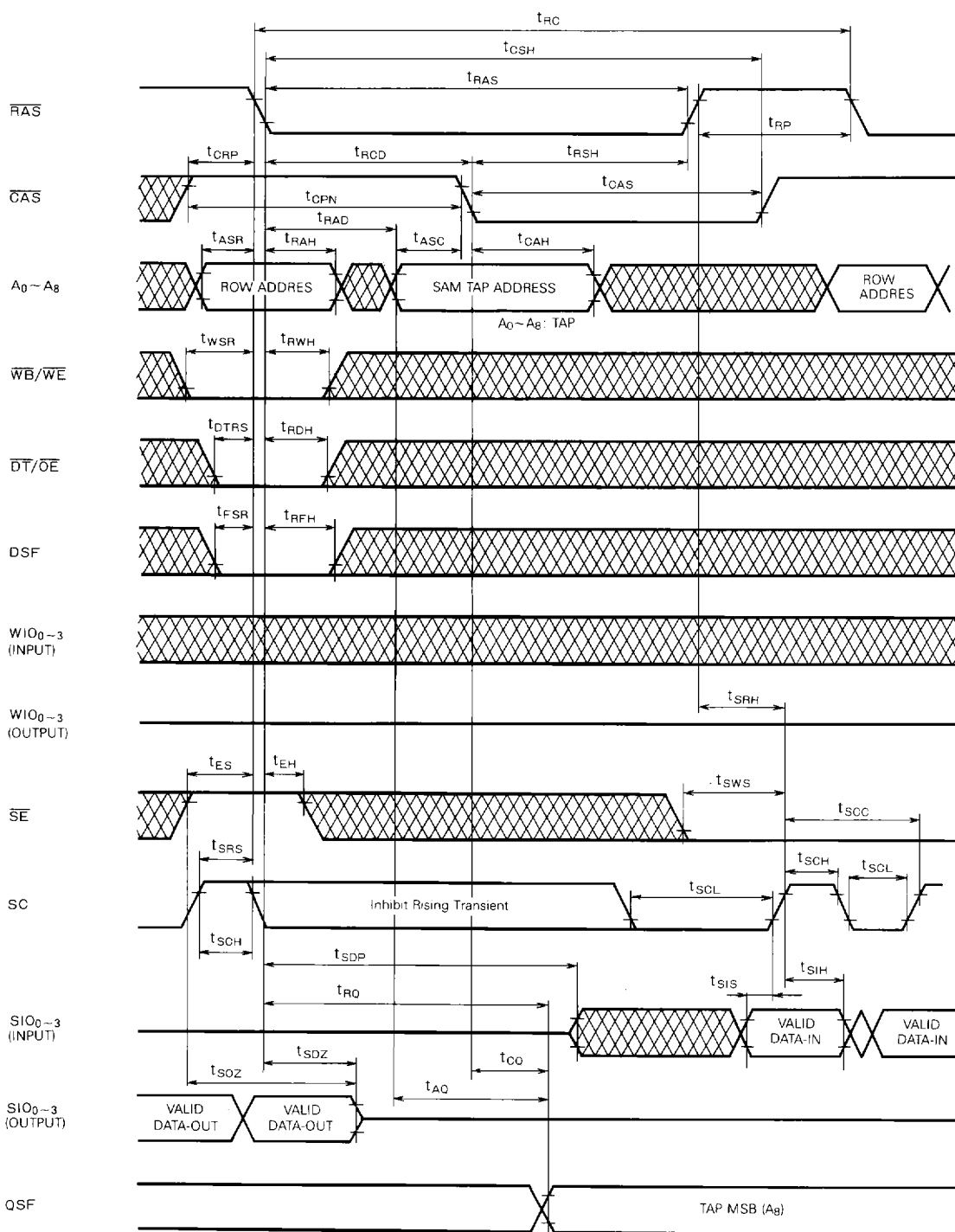
M5M442256AJ,L,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

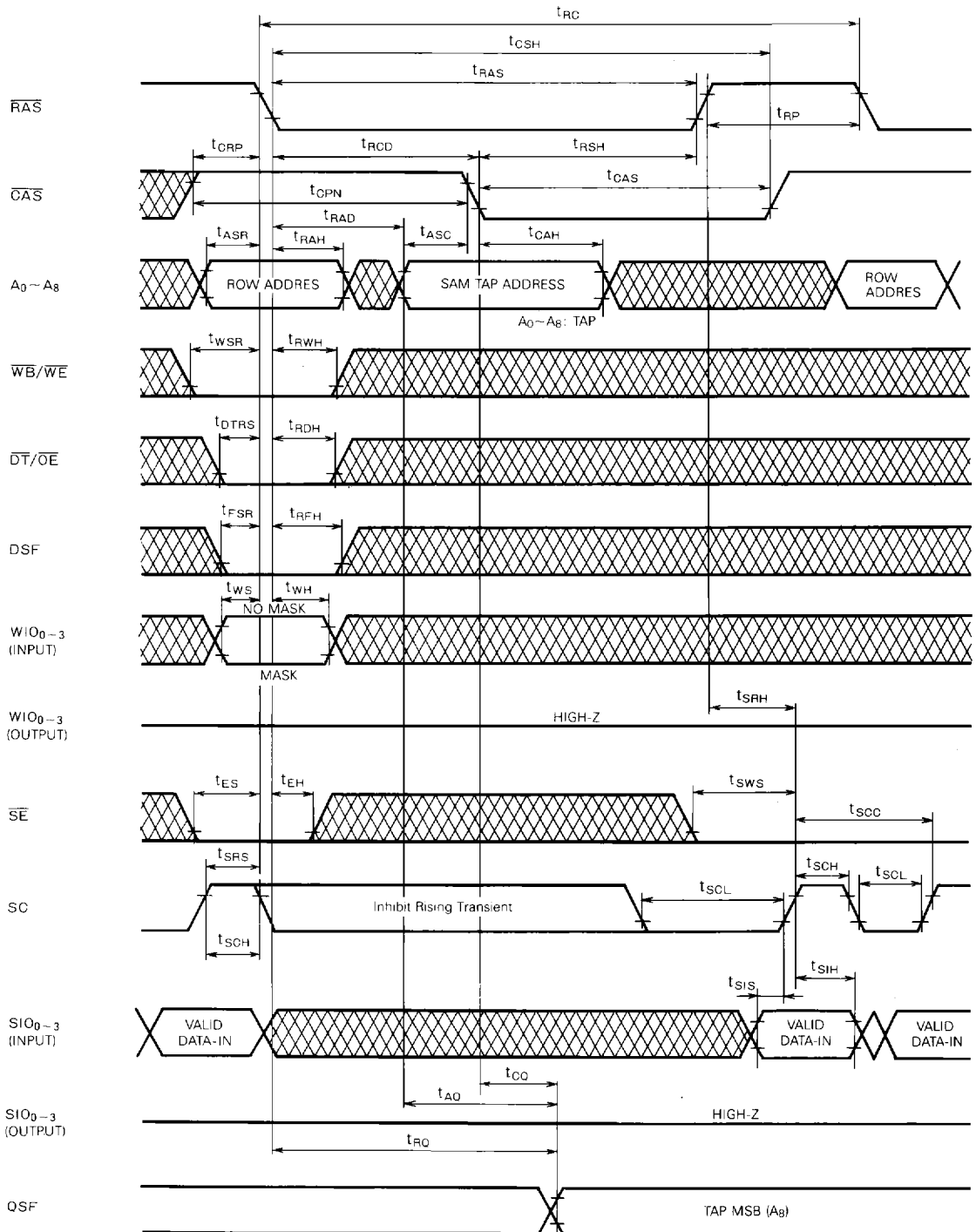
Real Time Read Transfer



Pseudo Write Transfer Cycle



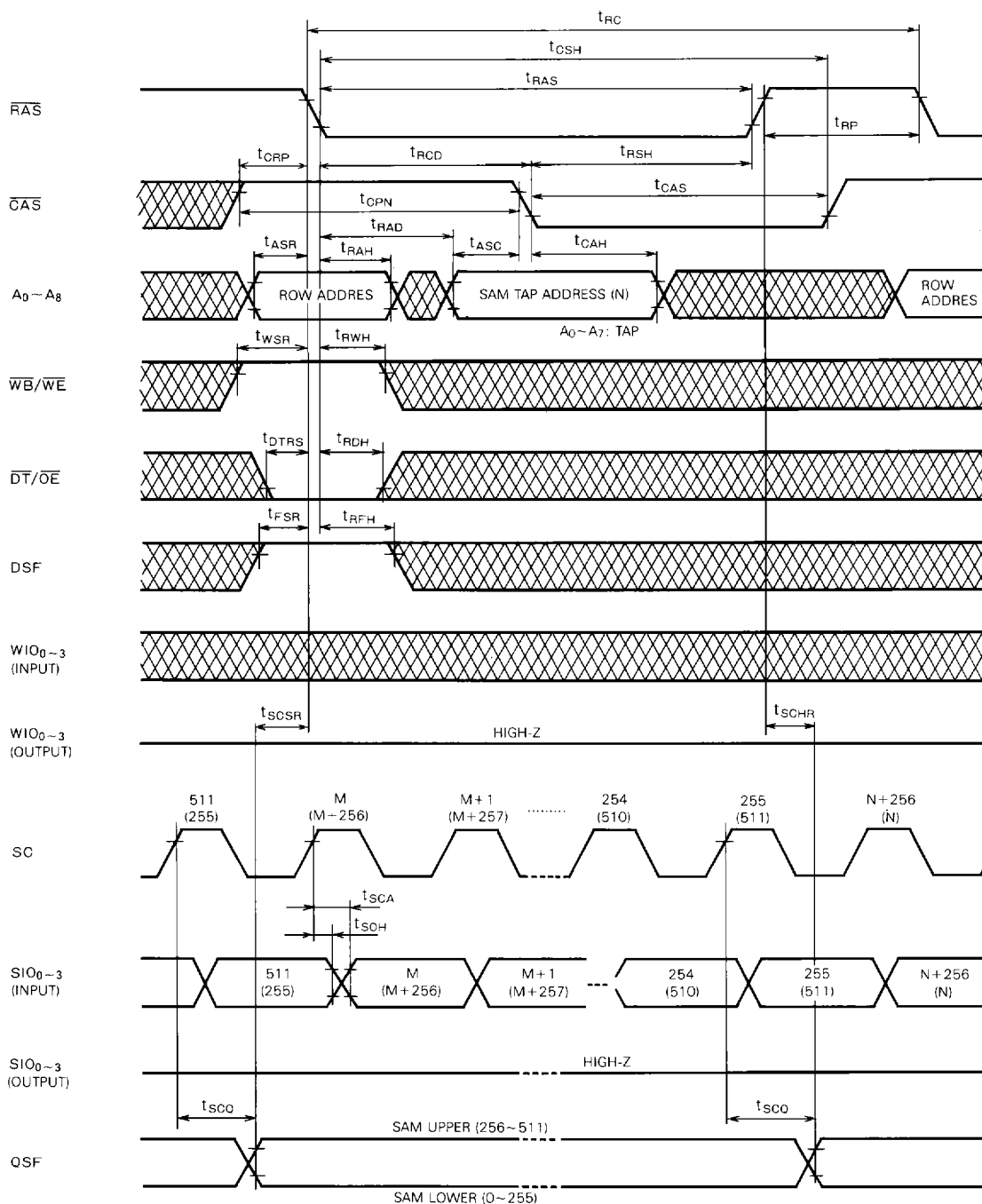
Write Transfer Cycle



M5M442256AJ,L,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

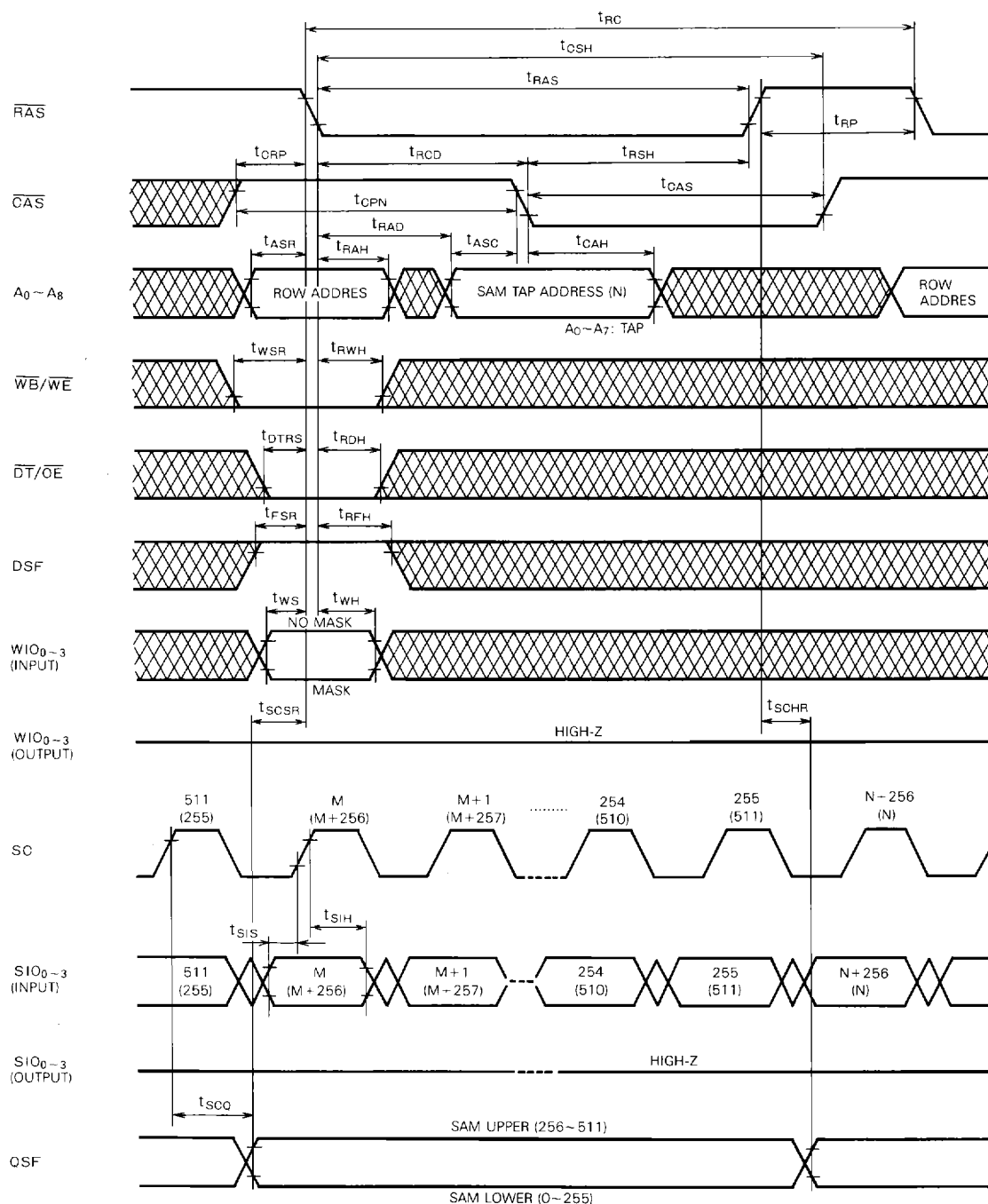
Split Read Transfer Cycle



M5M442256AJ,L,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

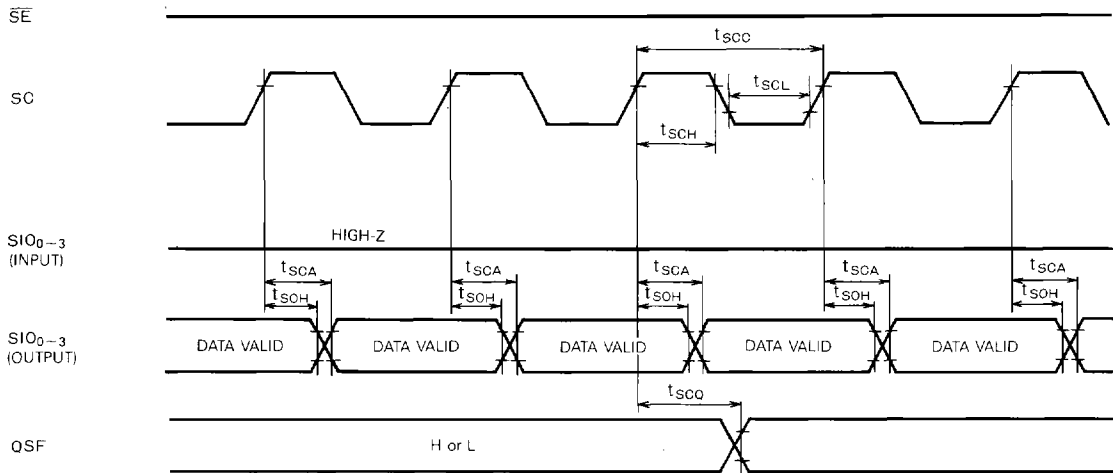
Split Write Transfer Cycle



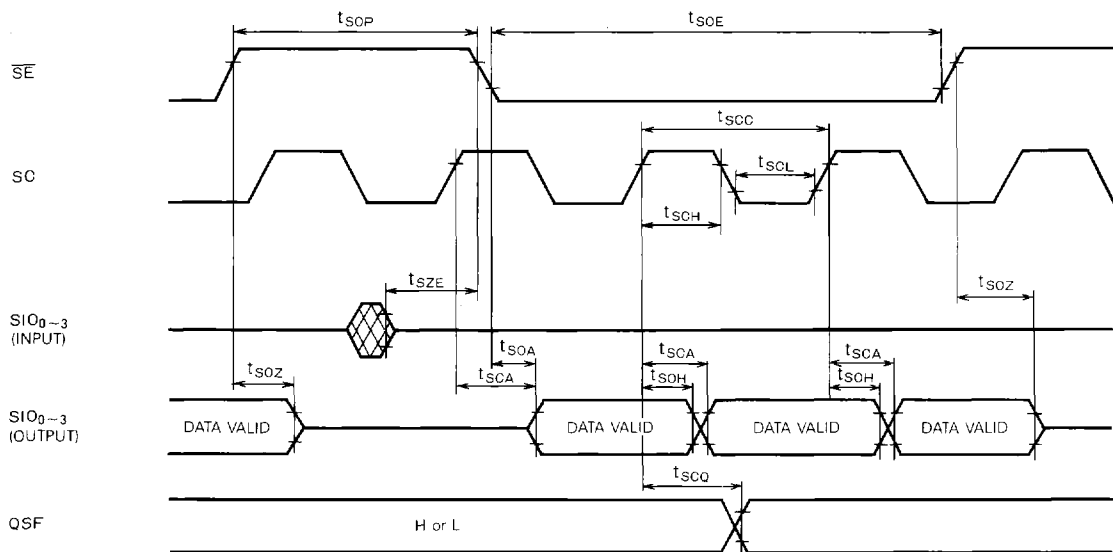
M5M442256AJ,L,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

Serial Read Cycle ($\overline{SE}=L$)



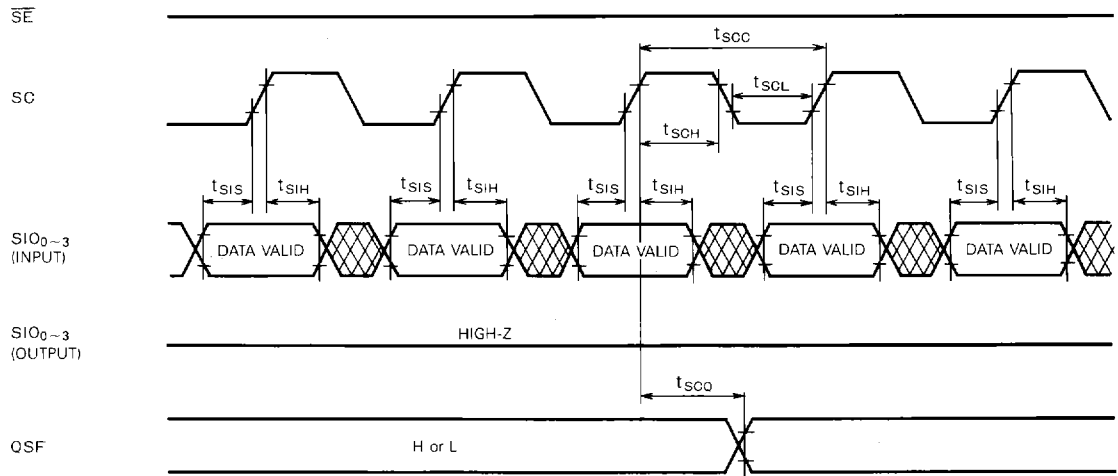
Serial Read Cycle ($\overline{SE}$ Control)



M5M44256AJ,L,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

Serial Write Cycle ($\overline{SE}=L$)



Serial Write Cycle ($\overline{SE}$ Control)

