IS25C128-2/3
IS25C256-2/3

131,072/262,144-BIT SPI SERIAL ELECTRICALLY ERASABLE PROM

PRELIMINARY INFORMATION
NOVEMBER 2001

FEATURES

- 2.1 MHz Clock Rate
- Low power CMOS
  - — Active current less than 3.0 mA (5.5V)
  - — Standby current less than 10 µA (5.5V)
- Low-voltage Operation
  - — IS25C256-3 & IS25C128-3 (Vcc = 2.5V to 5.5V)
  - — IS25C256-2 & IS25C128-2 (Vcc = 1.8V to 5.5V)
- Block Write Protection
  - — Protect 1/4, 1/2, or Entire Array
- 64 byte page write mode
- Serial Peripheral Interface (SPI) Compatible
  - — Supports SPI Modes 0 (0,0) and 3 (1,1)
- Self timed write cycles (5 ms Typical)
- High-reliability
  - — Endurance: 1 million cycles per byte
  - — Data retention: 100 years
  - — ESD protection >4000V
- Industrial temperature available
- 8-pin PDIP or SOIC, and 14-pin TSSOP Packages

DESCRIPTION

The IS25C128 2 is a 1.8V (1.8V 5.5V) 128K bit (16364x8) electrically Erasable PROM, IS25C128 3 is a 2.5V (2.5V 5.5V) 128K bit (16364x8) electrically Erasable PROM, IS25C256 2 is a 1.8V (1.8V 5.5V) 256K bit (32768x8) electrically Erasable PROM, IS25C256 3 is a 2.5V (2.5V 5.5V) 256K bit (32768x8) electrically Erasable PROM.

This IS25Cxxx family is a low cost and low voltage/low power SPI Serial EEPROM. It is fabricated using ISSI's advanced CMOS EEPROM technology and provides for low power industrial and commercial applications. The IS25Cxxx family is available in 8 pin PDIP, 8 pin SOIC, and 14 pin TSSOP packages.

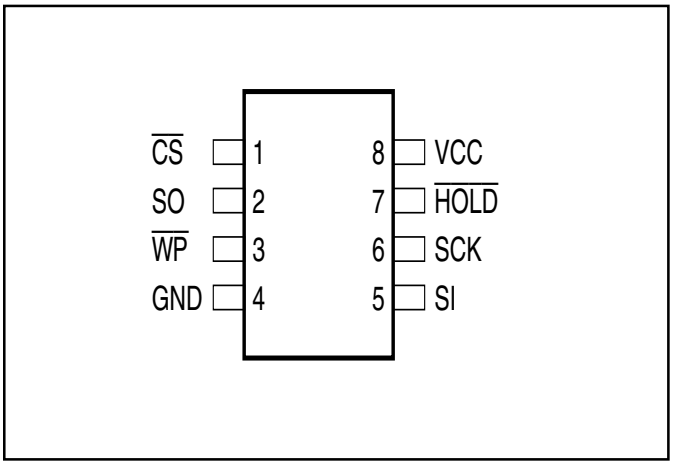
Each device in this family is enabled through the Chip Select ($\overline{CS}$) and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All programming cycles are completely self-timed, and no separate ERASE cycle is required before WRITE. BLOCK WRITE protection is enabled by programming the status register with one of four configurations of write protection. Separate program enable and program disable instructions are provided for additional data protection. Hardware data protection is provided via the #WP pin to protect against inadvertent write attempts to the status register. The $\overline{HOLD}$ pin can suspend communications without re-initializing the serial sequence.

PRODUCT OFFERING OVERVIEW

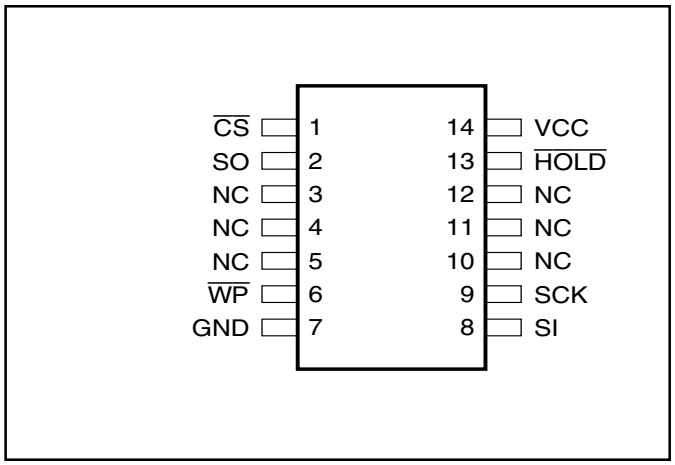
Part No	Voltage	Speed	Standby ICC	Read ICC	Write ICC	Temperature
IS25C256-2	1.8V-5.5V	500 KHz	< 5 µA	1 mA	3 mA	C,I
IS25C256-3	2.5V-5.5V	2.1MHz	< 10 µA	1 mA	3 mA	C,I
IS25C128-2	1.8V-5.5V	500 KHz	< 5 µA	1 mA	3 mA	C,I
IS25C128-3	2.5V-5.5V	2.1MHz	< 10 µA	1 mA	3 mA	C,I

PIN CONFIGURATION

8-Pin DIP and SOIC



14-pin TSSOP



PIN DESCRIPTIONS

$\overline{CS}$	Chip Select
SCK	Serial Data Clock
SO	Serial Data Input
SI	Serial Data Output
GND	Ground
Vcc	Power
$\overline{WP}$	Write Protect
$\overline{HOLD}$	Suspends Serial Input
NC	No Connect

PIN DESCRIPTIONS

Serial Clock (SCK) - This pin is used to synchronize the communication between the microcontroller and the IS25C256, IS25C128. Op-codes, byte addresses, or data present on the SI pin and latched on the rising edge of the SCK. Data on the SO pin is updated on the falling edge of the SCK for SPI modes (0,0 & 1,1).

Serial Data Input (SI) - The SI pin is used to input all op-codes, byte addresses, and data to be written to the device. Input data is latched on the rising edge of the serial clock for SPI modes (0,0 & 1,1).

Serial Data Output (SO) - The SO pin is used to transfer data out of the device. During a read cycle, data is shifted out on the falling edge of the serial clock for SPI modes (0,0 & 1,1).

Chip Select ($\overline{CS}$): When the $\overline{CS}$ pin is low, the device is enabled. When the $\overline{CS}$ pin is high the device is disabled. $\overline{CS}$ high takes the SO output pin to high impedance and forces the devices into a Standby Mode (unless an internal write operation is underway). The devices draws zero current in the Standby mode. A high-to-low transition on $\overline{CS}$ is required prior to any sequence being initiated. A low-to-high transition on $\overline{CS}$ after a valid write sequence is what initiates an internal write cycle.

PIN DESCRIPTIONS Continued:

Write Protect ($\overline{WP}$) - The $\overline{WP}$ Pin will allow normal read/write operations when held high. When $\overline{WP}$ is tied low and the WPEN bit in the status register is set to "1", all write operations to the status register are inhibited. $\overline{WP}$ going low while CS is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation to the status register. The $\overline{WP}$ pin function is blocked when the WPEN bit is set to 0. Figure 10 illustrates the $\overline{WP}$ timing sequence during a write operation.

Hold ($\overline{HOLD}$): The $\overline{HOLD}$ pin is used to pause transmission to the device while in the middle of a serial sequence without having to retransmit entire sequence at a later time. To pause, $\overline{HOLD}$ must be brought low while SCK is low. The SO pin is in a high impedance state during the time the part is paused, and transition on the SI pins will be ignored. To resume communication, $\overline{HOLD}$ is brought high, while SCK is low. ($\overline{HOLD}$ should be held high any time this function is not being used.) $\overline{HOLD}$ may be tied high directly to Vcc or tied to Vcc through a resistor. The $\overline{HOLD}$ Timing Diagram illustrates hold timing sequence.

SERIAL INTERFACE DESCRIPTION

MASTER: This device that generates the serial clock.

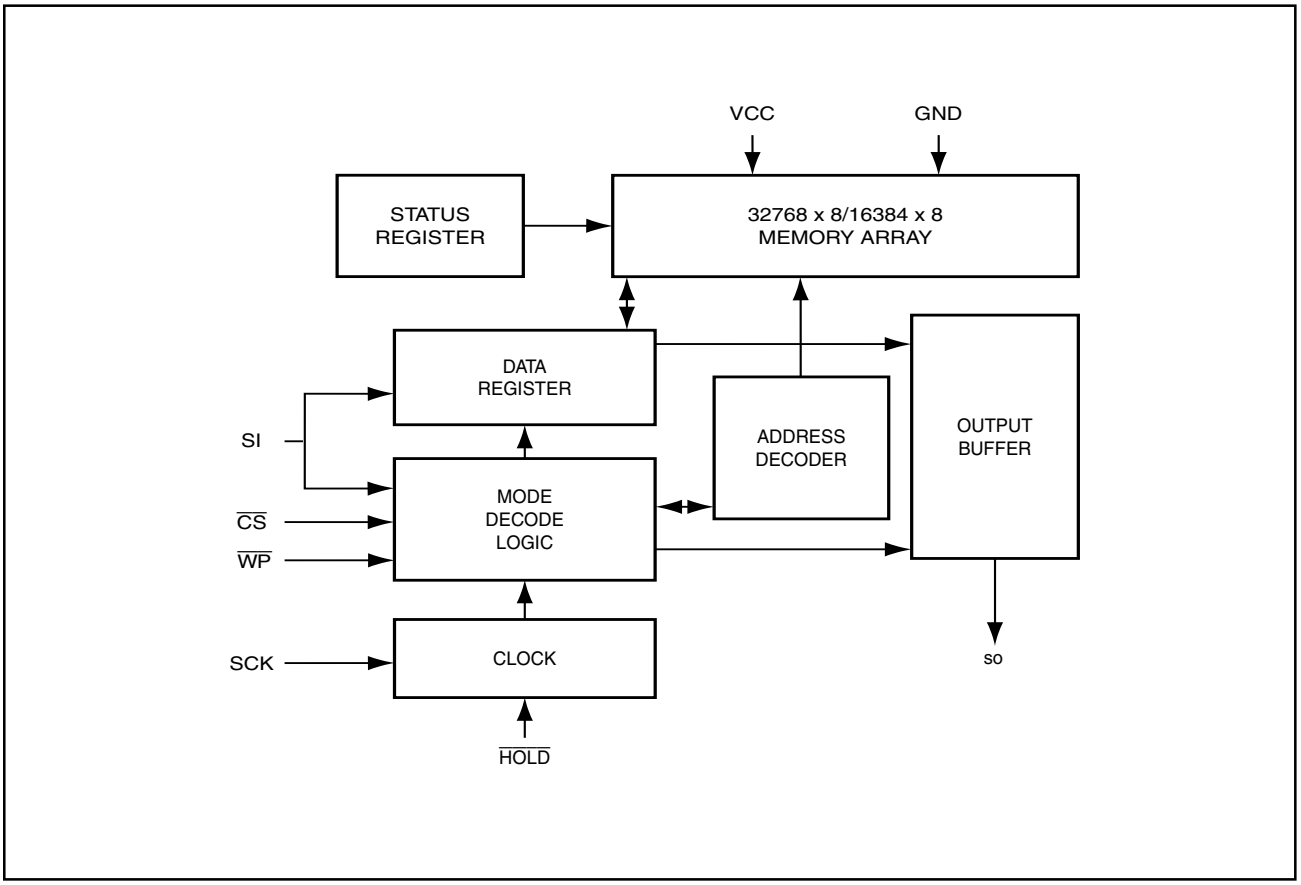
SLAVE: Because the Serial Clock pin (SCK) is always an input, the device always operates as a slave.

MSB: The Most Significant Bit (MSB) is the first bit transmitted and received.

SERIAL OP-CODE: After the device is selected with CS going low, the first byte will be received. This byte contains the op-code that defines the operations to be performed.

INVALID OP-CODE: If an invalid op-code is received, no data will be shifted into the device, and the serial output pin (SO) will remain in a high impedance state until the falling edge of CS is detected again. This will reinitialize the serial communications.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTIONS

The IS25C128/256 utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in Table 1. All instructions, addresses, and data are transferred with the MSB first and start with a high-to low CS transition.

Table 1. Instruction Set

Name	Instruction Format	Operation
WREN	0000 X110	Set Write Enable Latch
WRDI	0000 X100	Reset Write Enable Latch
RDSR	0000 X101	Read Status Register
WRSR	0000 X001	Write Status Register
READ	0000 X011	Read Data from Memory Array
WRITE	0000 X010	Write Data to Memory Array

WRITE ENABLE (WREN): This device will power-up in the write disable state when VCC is applied. All programming instructions must therefore be preceded by a Write Enable instruction.

WRITE DISABLE (WRDI): To protect the device against inadvertent writes, the Write Disable instruction disables all programming modes. The WRDI instruction is independent of the status of the $\overline{WP}$ pin.

READ STATUS REGISTER (RDSR):

The Read Status Register instruction provides access to the status register. The READY/BUSY and Write Enable status of the device can be determined by the RDSR instruction. Similarly, the Block Write Protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction.

Table 2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
WPEN	x	x	x	BP1	BP0	WEN	$\overline{RDY}$

Table 3. Read Status Register Bit Definition

Bit	Definition
Bit 0 ($\overline{RDY}$)	Bit 0 = 0 ($\overline{RDY}$) indicates the device is READY. Bit 0 = 1 indicates the write cycle is in progress.
Bit 1(WEN)	Bit 1 = 0 indicates the device is not WRITE ENABLED. Bit 1 = 1 indicates the device is WRITE ENABLED.
Bit 2 (BPO)	See Table 4
Bit 3 (BP1)	See Table 4
Bits 4 - 6 are 0s when the device is not an internal write cycle.	
Bits 7 (WPEN)	See Table 5.
Bits 0-7 are 1s during an internal write cycle.	

WRITE STATUS REGISTER (WRSR): The WRSR instruction allows the user to select one of four levels of protection. The device is divided into four array segments. One quarter (1/4), one half (1/2) or all of the memory segments can be protected. Any of the data within any selected segment will therefore be READ only. The block write protection levels and corresponding status register control bits are shown in Table 4.

The three bits, BP0, BP1 and WPEN are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g. WREN, twc, RDSR).

Table 4. Status Register Format

	Status Register Bits		Array Addresses Protected	
Level	BP1	BP0	IS25C128	IS25C256
0	0	0	None	None
1(1/4)	0	1	3000 -3FFF	6000 -7FFF
2(1/2)	1	0	2000 -3FFF	4000 -7FFF
3(All)	1	1	0000 -3FFF	0000 -7FFF

The WRSR instruction also allows the user to enable or disable the write protect ($\overline{WP}$) pin through the use of the Write Protect Enable (WPEN) bit. Hardware write protection is enabled when the $\overline{WP}$ pin is low and the WPEN bit is '"1". Hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is "0". When the device is hardware write protected, writes to the Status Register, including the Block Protect bits and the WPEN bit, and the block-protected sections in the memory array are disabled. Writes are only allowed to sections of the memory which are not block-protected.

Note: When the WPEN bit is hardware write protected, it cannot be changed back to "0", as long as the $\overline{WP}$ pin is held low.

Table 5. WPEN Operation

WPEN	$\overline{WP}$	WEN	Protected Blocks	Unprotected Blocks	Protected Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

READ SEQUENCE (READ): Reading the device via the SO (Serial Output) pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the READ op-code is transmitted via the SI line followed by the byte address to be read (A15-A0, Refer to Table 6). Upon completion, any data on the SI line will be ignored. The data (D7-D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the data comes out. The READ sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read in one continuous READ cycle.

WRITE SEQUENCE (READ): In order to program the device, two sperate instructions must be executed. First, the device must be write enabled via the Write Enable (WREN) Instruction. Then a Write (WRITE) Instruction may be executed. Also the address of the memory location(s) to be programmed must be outside the protected address field location selected by the Block Write Protection Level. During an internal write cycle, all commands will be ignored except the RDSR instruction.

A Write Instruction requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the WRITE op-code is transmitted via the SI line followed by the byte address (A15-A0) and the data (D7-D0) to be programmed (Refer to Table 6). Programming will start after the $\overline{CS}$ pin is brought high. (The Low to High transition of the $\overline{CS}$ pin must occur during the SCK low-time immediately after clocking in the D0 (LSB) data bit.

The READY/BUSY status of the device can be determined by initiating a READ STATUS REGISTER (RDSR) Instruction. If Bit 0 = 1, the WRITE cycle is still in progress. If Bit 0 = 0 , the WRITE cycle has ended. Only the READ STATUS REGISTER instruction is enabled during the WRITE programming cycle.

The device is capable of the 64-byte PAGE WRITE operation. After each byte of data is received, the five low order address bits are internally incremented by one; the high order bits of the address will remain constant. If more than 64 bytes of data are transmitted, the address counter will roll over the previously written data will be overwritten. The device is automatically returned to the write disable state at the completion of a WRITE cycle.

NOTE: If the device is not Write enabled (WREN), the device will ignore the Write instruction and will return to the standby state, when $\overline{CS}$ is brought high. A new $\overline{CS}$ falling edge is required to re-initiate the serial communication.

Table 6. Address Key

Name	IS25C128	IS25C256
A_N	A_{13}-A_0	A_{14}-A_0
Don't Care Bits	A_{15}-A_{14}	A_{15}

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	-0.5 to +6.25	V
V_P	Voltage on Any Pin	–1.0V to + 7.0V	V
T_{BIAS}	Temperature Under Bias	–40 to +85	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Output Current	5	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE (IS25C256-2 and IS25C128-2)

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	1.8V to 5.5V
Industrial	–40°C to +85°C	1.8V to 5.5V

OPERATING RANGE (IS25C256-3 and IS25C128-3)

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	2.5V to 5.5V
Industrial	–40°C to +85°C	2.5V to 5.5V

CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters and not 100% tested.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 5.0V.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OL1}	Output LOW Voltage	V_{CC} = 1.8V, I_{OL} = 0.15 mA	—	0.2	V
V_{OL2}	Output LOW Voltage	V_{CC} = 2.5V, I_{OL} = 1.0 mA	—	0.4	V
V_{OH1}	Output HIGH Voltage	V_{CC} = 1.8V, I_{OH}= -100uA	V_{CC} - 0.2	—	V
V_{OH2}	Output HIGH Voltage	V_{CC} = 2.5V, I_{OH}= -1mA	V_{CC} - 0.8	—	V
V_{IH}	Input HIGH Voltage		V_{CC} x 0.7	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage		–1.0	V_{CC} x 0.3	V
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} max.	-3.0	3	µA
I_{LO}	Output Leakage Current		-3.0	3	µA

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{CC1}	Vcc Operating Current	READ at 500 KHz (Vcc=5V)	—	1.0	mA
I_{CC2}	Vcc Operating Current	WRITE at 500 KHz (Vcc=5V)	—	3.0	mA
I_{SB1}	Standby Current	Vcc = 1.8V, V_{IN} = V_{CC} or GND	—	5	µA
I_{SB2}	Standby Current	Vcc = 5.5V, V_{IN} = V_{CC} or GND	—	10	µA

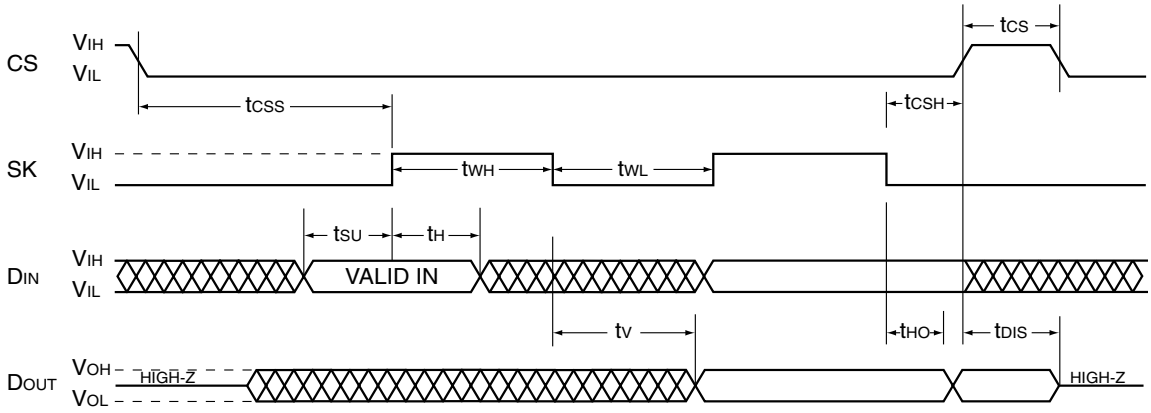
AC Characteristics

Applicable over recommended operating range from T_A= -40°C to +85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

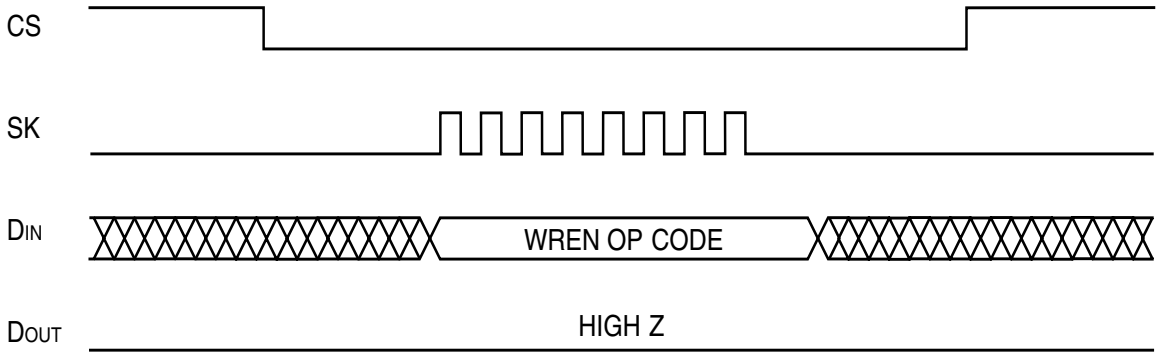
		1.8V		2.5V		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
f_{SCK}	SCK Clock Frequency	0	0.5	0	2.1	MHz
t_{RI}	Input Rise Time	—	2	—	2	µs
t_{FI}	Input Fall Time	—	2	—	2	µs
t_{WH}	SCK High Time	800	—	200	—	ns
t_{WL}	SCK Low Time	800	—	200	—	ns
t_{CS}	$\overline{CS}$ High Time	1000	—	250	—	ns
t_{CSS}	$\overline{CS}$ Setup Time	1000	—	250	—	ns
t_{CSH}	$\overline{CS}$ Hold Time	1000	—	250	—	ns
t_{SU}	Data In Setup Time	100	—	50	—	ns
t_H	Data In Hold Time	100	—	50	—	ns
t_{HD}	$\overline{Hold}$ Setup Time	400	—	100	—	ns
t_{CD}	$\overline{Hold}$ Time	400	—	300	—	ns
t_V	Output Valid	0	800	0	200	ns
t_{HO}	Output Hold Time	0	—	0	—	ns
t_{LZ}	$\overline{Hold}$ to Output Low Z	0	200	0	200	ns
t_{HZ}	$\overline{Hold}$ to Output High Z	—	200	—	200	ns
t_{DIS}	Output Disable Time	—	1000	—	250	ns
t_{WC}	Write Cycle Time	—	20	—	10	ms
Endurance[1]	5.0V, 25°C, Page Mode	1M	—	1M	—	Write Cycles

TIMING DIAGRAMS

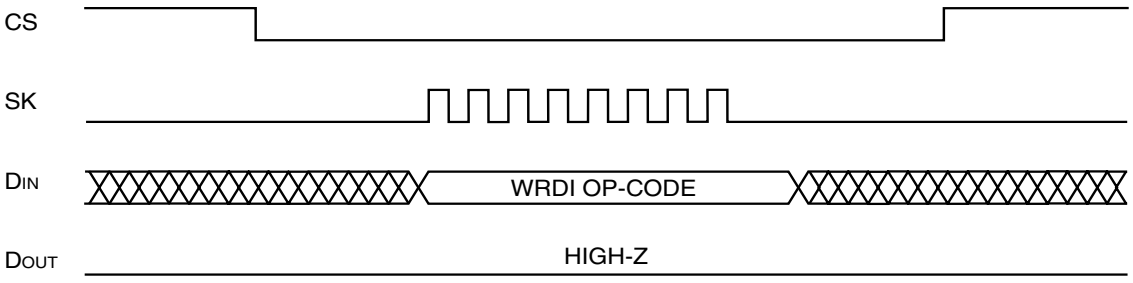
Synchronous Data Timing



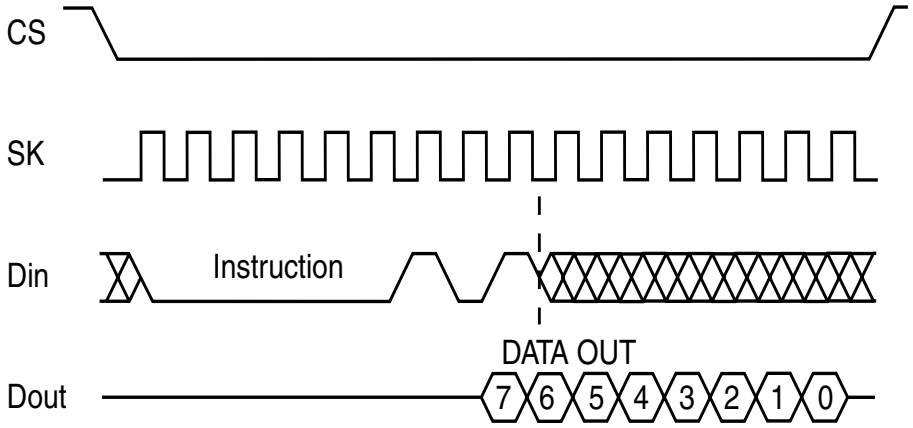
WREN Timing



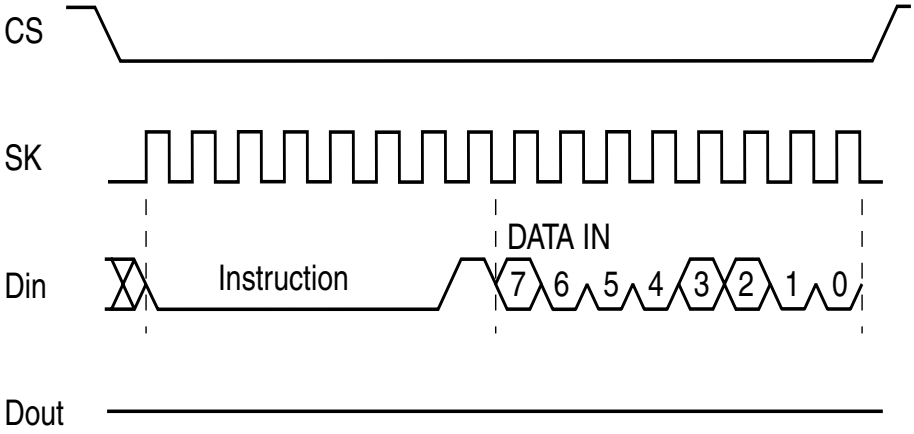
WRDI Timing



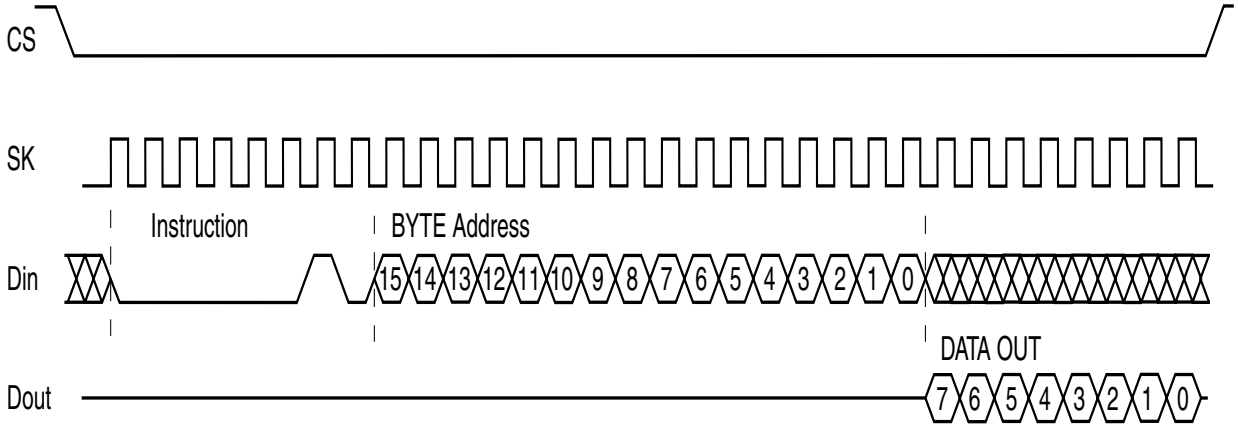
RDST Timing



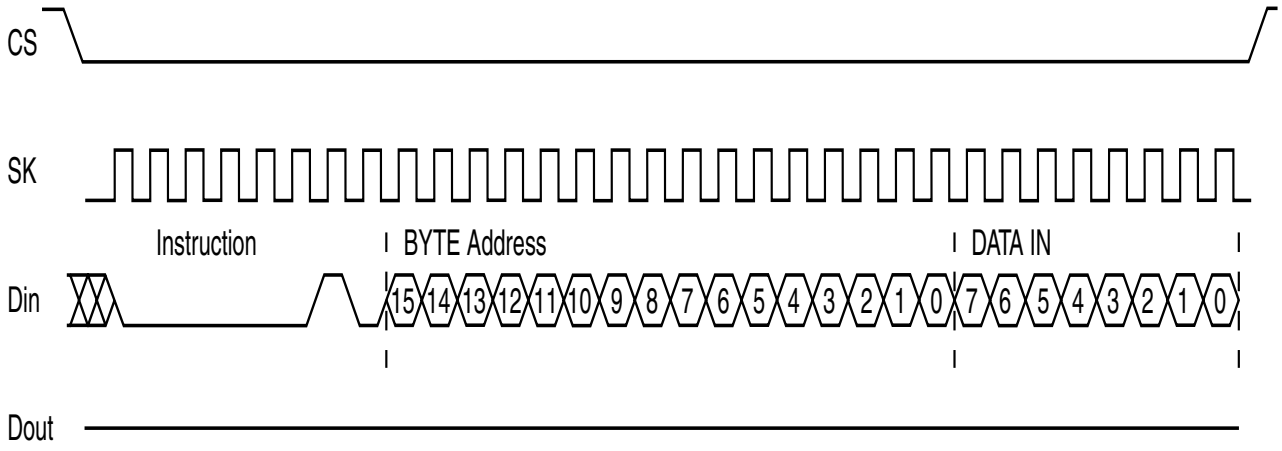
WRSR Timing



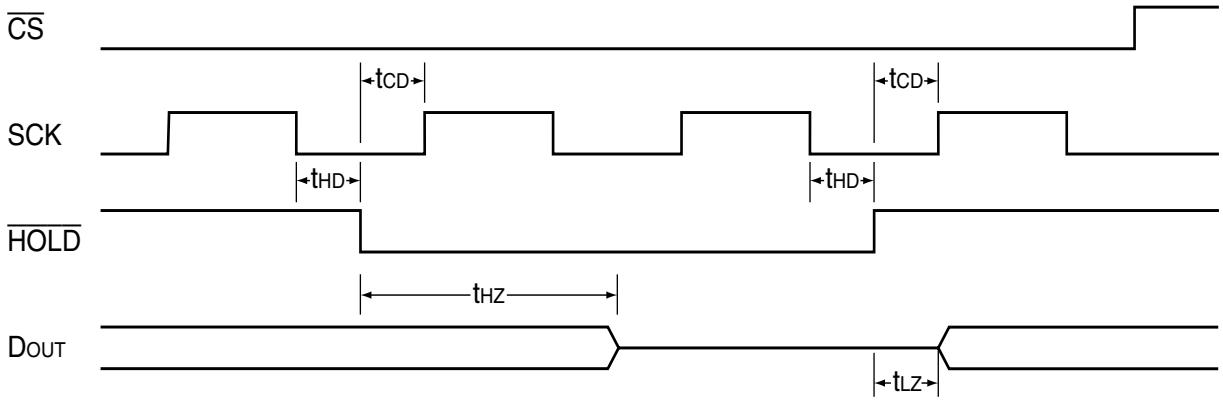
READ Timing



WRITE Timing



$\overline{\text{HOLD}}$ Timing



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Frequency	Voltage Range	Part Number	Package
500 KHz	1.8V to 5.5V	IS25C128-2P	300-mil Plastic DIP
		IS25C128-2G	Small Outline (JEDEC STD)
		IS25C128-2Z	14-pin TSSOP
500 KHz	1.8V to 5.5V	IS25C256-2P	300-mil Plastic DIP
		IS25C256-2G	Small Outline (JEDEC STD)
		IS25C256-2Z	14-pin TSSOP
2.1 MHz	2.5V to 5.5V	IS25C128-3P	300-mil Plastic DIP
		IS25C128-3G	Small Outline (JEDEC STD)
		IS25C128-3Z	14-pin TSSOP
2.1 MHz	2.5V to 5.5V	IS25C256-3P	300-mil Plastic DIP
		IS25C256-3G	Small Outline (JEDEC STD)
		IS25C256-3Z	14-pin TSSOP

ORDERING INFORMATION

Industrial Range: –40°C to +85°C

Frequency	Voltage Range	Part Number	Package
500 KHz	1.8V to 5.5V	IS25C128-2PI	300-mil Plastic DIP
		IS25C128-2GI	Small Outline (JEDEC STD)
		IS25C128-2ZI	14-pin TSSOP
500 KHz	1.8V to 5.5V	IS25C256-2PI	300-mil Plastic DIP
		IS25C256-2GI	Small Outline (JEDEC STD)
		IS25C256-2ZI	14-pin TSSOP
2.1 MHz	2.5V to 5.5V	IS25C128-3PI	300-mil Plastic DIP
		IS25C128-3GI	Small Outline (JEDEC STD)
		IS25C128-3ZI	14-pin TSSOP
2.1 MHz	2.5V to 5.5V	IS25C256-3PI	300-mil Plastic DIP
		IS25C256-3GI	Small Outline (JEDEC STD)
		IS25C256-3ZI	14-pin TSSOP

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