SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TC584000P/F/FT/TR

TENTATIVE

4MEGA BIT (524,288 WORD × 8 BIT) CMOS NAND E^2PROM

DESCRIPTION

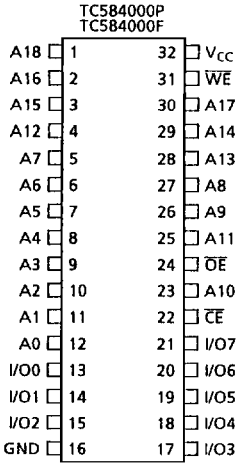
The TC584000P / F / FT / TR is a 4M bits electrically erasable and programmable nonvolatile memory equipped with a 512K×8 nonvolatile memory array and a 512K×8 data register, which can operate with a single 5V power supply. It has a 512-byte data register inside. A program operation and a read operation are performed by transferring the 512 byte page of data between the register and the memory cell array. Data in the register can be clocked out at a very high speed during page read operations. An erase operation can be performed on either a 4K-byte block or the whole chip.

The TC584000P / F / FT / TR is suitable for large capacity buffer memory applications such as semiconductor disk, voice recording and replaying, digital still camera, and so on where nonvolatality is necessary.

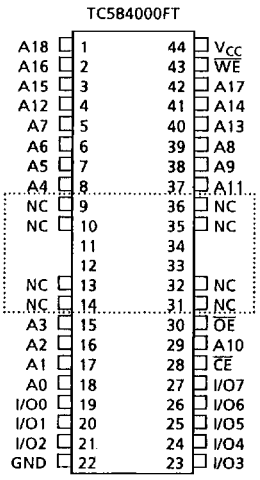
FEATURES

- Organization — Memory Cell Array : 512K × 8; Register : 512 × 8
- Single 5V Power Supply
- Operation
  - Page Program : 40μs×100 loops max.(TC584000P/F/FT/TR)
  - Chip Erase : 10ms (TC584000P/F/FT/TR)
  - Block Erase : 10ms (TC584000P/F/FT/TR) (4K byte / block)
  - Random Read : 15μs
  - Page Read : 120ns
- Input / Output Level : TTL Compatible
- Operation Control : Command Control
- Operation Current
  - Page Read : 30mA (tcycle = 120ns)
  - : 5mA (tcycle = 1μs)
  - Program : 60mA
  - Data Input : 70mA
  - Erase : 50mA
  - Stand by : 100μA
- W/E Endurance : 10^5 Cycles Target

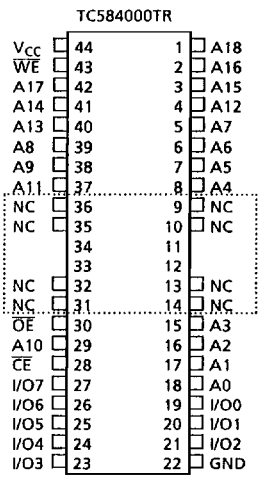
PIN CONNECTION (TOP VIEW)



32 Pin 600mil DIP
32 Pin 525mil SOP



44 (40) Pin 400mil TSOP type II
(0.8mm pitch) (Normal Bent)



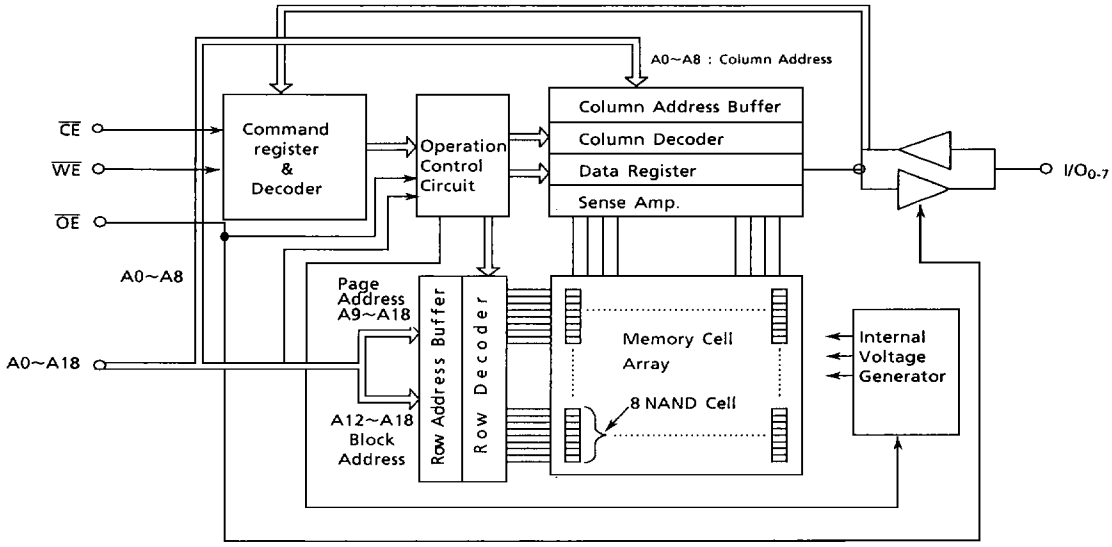
44 (40) Pin 400mil TSOP type II
(0.8mm pitch) (Reverse Bent)

PIN ASSIGNMENT

A_{0-18}	Address Inputs
I/O_{0-7}	Data Inputs / Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable input
V_{CC}	Power Supply (+5V)
GND	Ground
NC	No Connection

- Package
  - TC584000P : DIP32-P-600
  - TC584000F : SOP32-P-525
  - TC584000FT : TSOP44-P-400B
  - TC584000TR : TSOP44-P-400C

CIRCUIT BLOCK DIAGRAM



OPERATING MODE

Mode		$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	V_{CC}	I/O_{0-7}	Power
Read	Read	H	L	L	5V	Data Out	Active
	Output Deselect	*	*	H		Hi – Z	
	Standby	*	H	*			Standby
Command Input		⌐¬	L	H		Command In	Active
Program / Erase		H	*	H		Hi – Z	
Program / Erase Verify		H	L	L		Data Out	

* : V_{IH} or V_{IL}

COMMAND TABLE

	1st Step			2nd Step			3rd~513th Step			No. of Step
	Mode	Address	Data	Mode	Address	Data	Mode	Address	Data	
Program	Write	*1	40H	Write	A9 – 18 : Page Add. A0 – 8 : 000H	Program Data	Write	A9 – 18 : *1 A0 – 8 : 001H~1FFH	Program Data	513 *2
Program Verify	Write	*1	C0H	Write	A9 – 18 : Page Add. A0 – 8 : 000H	Data Out	Read	A9 – 18 : Page Add. A0 – 8 : 001H~1FFH	Data Out	2~513 *3
Chip Erase	Write	*1	20H	Write	*1	20H	–	–	–	2
Block Erase	Write	*1	60H	Write	A12 – 18 : Block Add. A0 – 11 : *1	60H	–	–	–	2
Read	Write	*1	00H	–	–	–	–	–	–	1
Reset	Write	55555H	FFH	Write	55555H	FFH	–	–	–	2

*1 : V_{IH} or V_{IL}

*2 : Detecting Add0~8 = 1FFH stops 512byte serial data input operation and starts program operation internally. Therefore 512 byte serial data must be input from Add0~8 = 000H to Add0~8 = 1FFH in serial.

*3 : The No. of steps of Program Verify depends on the address where the Program Verify fails.

ABSOLUTE MAXIMUM RATINGS

Symbols	Paramater	Rating	Units
V_{CC}	Power Supply Voltage	−0.6~7.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
$V_{I/O}$	Output Voltage	−0.6~Vcc + 0.5(≤ 7.0V)	V
P_D	Power Dissipation	1.0 [1] / 0.6 [2] / 0.5 [3]	W
T_{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	0~70	°C

1) : DIP, 2) : SOP, 3) : TSOP

CAPACITANCE *(Ta = 25°C, f = 1MHz)

Symbols	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	−	10	15	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	−	10	15	pF

* : This parameter is periodically sampled and is not 100% tested.

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

Symbols	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage	4.75	5.0	5.25	V
V_{IH}	Input High Voltage	2.2	−	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage	−0.3	−	0.8	V

* -2V at pulse width ≤ 20ns

D.C. CHARACTERISTICS (Ta = 0~70°C, V_{CC} = 5V ± 5%)

Symbols	Parameter	Condition		Min.	Max.	Units
I_{IL}	Input Leakage Current	V_{IN} = 0V~V_{CC}		−	± 10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4V~V_{CC}		−	± 10	μA
I_{CCO1}	Operating Current (Page Read)	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA	t_{cycle} = 120ns	−	30	mA
I_{CCO2}	Operating Current (Page Read)		t_{cycle} = 1μs	−	5	mA
I_{CCO3}	Operating Current (Command Input)	t_{cycle} = 100ns		−	30	mA
I_{CCO4}	Operating Current (512 byte Data Input)	t_{cycle} = 100ns		−	70	mA
I_{CCO5}	Operating Current (Program)			−	60	mA
I_{CCO6}	Operating Current (Erase)			−	50	mA
I_{CCS1}	Standby Current	$\overline{CE}$ = VIH		−	1	mA
I_{CCS2}	Standby Current	$\overline{CE}$ = VCC − 0.2V		−	100	μA
V_{OH}	Output High Voltage	I_{OH} = −400μA		2.4	−	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		−	0.4	V

A.C. CHARACTERISTICS (Ta = 0~70°C, V_{CC} = 5V ± 5%)

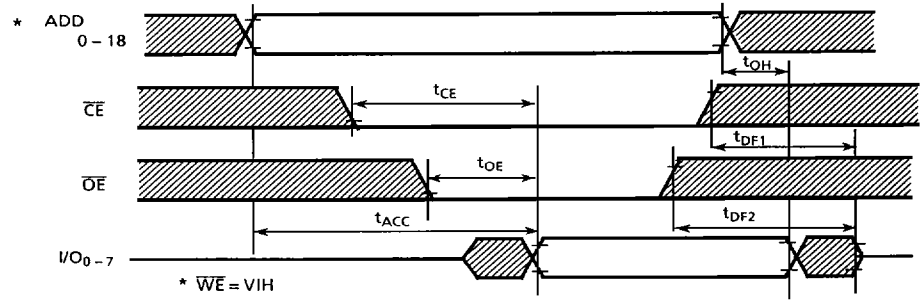
1. Read Operation

Symbol	Parameter	Min.	Max.	Unit
t_{ACC}	Address Access Time	–	15	μs
t_{PAC}	Page Mode Access Time	–	120	ns
t_{CE}	Chip Enable Access Time	–	15	μs
t_{OE}	Output Enable Access Time	–	50	ns
t_{DF1}	Chip Enable to Output in High-Z	0	50	ns
t_{DF2}	Output Enable to Output in High-Z	0	50	ns
t_{OH}	Output Data Hold Time	0	–	ns

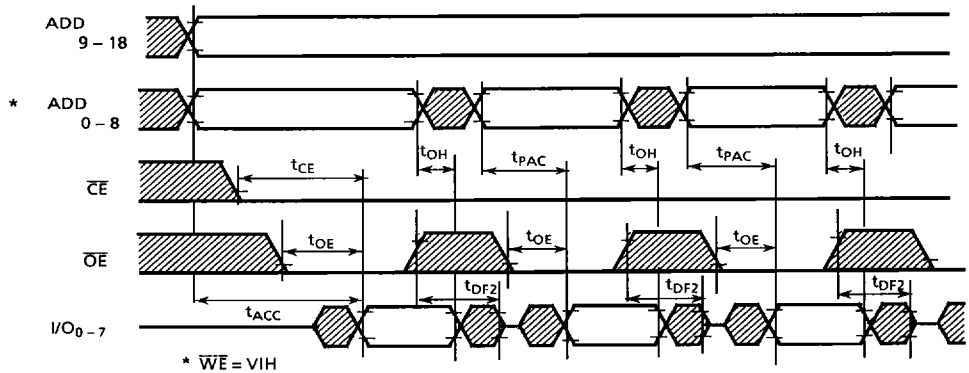
A.C. Test Conditions

- Output Load : 1TTL Gate and C_L = 100pF
- Input Pulse Rise and Fall Time (10~90%) : 5ns Max.
- Input Pulse Level : 0.4V / 2.6V
- Timing Reference Level : Input 0.8V / 2.2V, Output 0.8V / 2.0V

RANDOM READ TIMING WAVEFORM



PAGE READ TIMING WAVEFORM



* Column addresses A0 - 8 must be fixed and can not be changed in the time period of t_{ACC} and t_{CE} in a read operation.
* A skew among column addresses A0 - 8 must be less than 15ns.

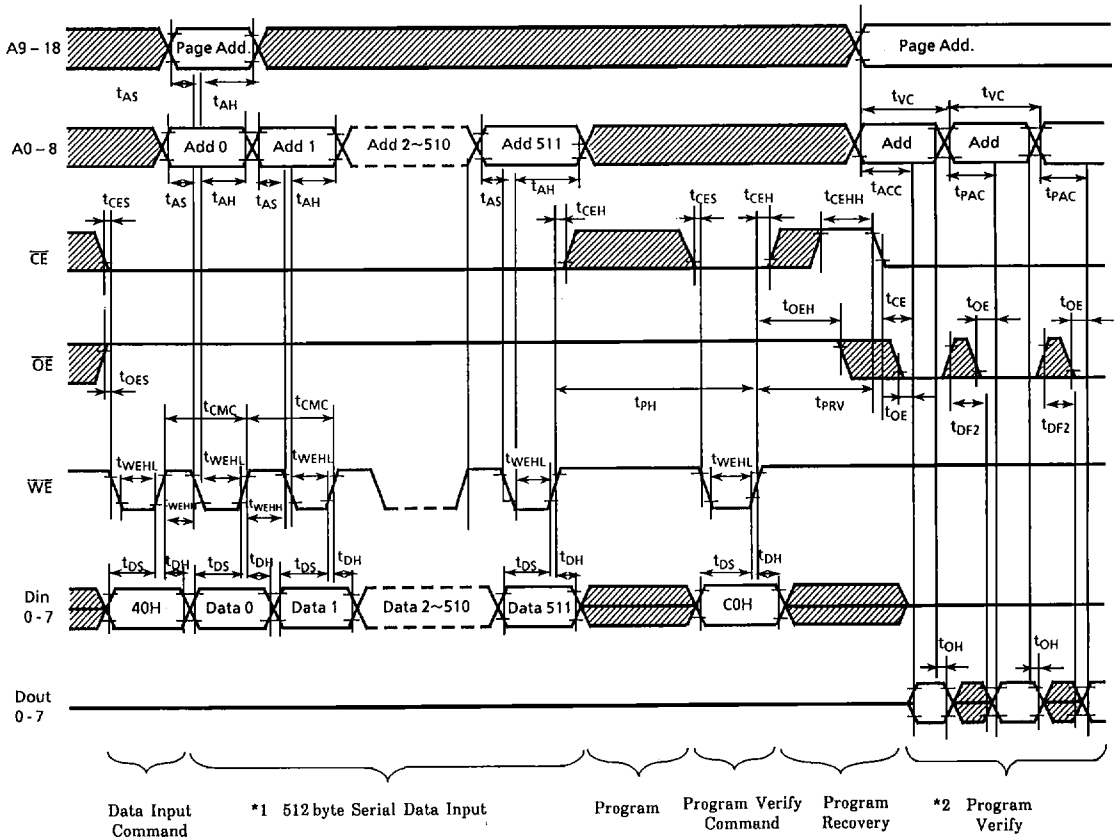
2. Program / Erase Operation (Ta = 0~70°C, V_{CC} = 5V ± 5%)

Symbol	Parameter		TC584000P/F/FT/TR MIN.	TYP.	MAX.	Units
t_{AS}	Address Setup Time		0	–	–	ns
t_{AH}	Address Hold Time		70	–	–	
t_{CES}	$\overline{CE}$ Setup Time (Command Cycle)		0	–	–	
t_{CEH}	$\overline{CE}$ Hold Time (Command Cycle)		10	–	–	
t_{OES}	$\overline{OE}$ Setup Time		0	–	–	
t_{OEH}	$\overline{OE}$ Hold Time		10	–	–	
t_{DS}	Data Setup Time		50	–	–	
t_{DH}	Data Hold Time		0	–	–	
t_{WEHL}	$\overline{WE}$ Low Level Hold Time		50	–	–	
t_{WEHH}	$\overline{WE}$ High Level Hold Time		40	–	–	
t_{CMC}	Command Cycle Time		100	–	–	
t_{PH}	Program Hold Time		35	40	45	μs
t_{PRV}	Program Recovery Time		5	–	–	
t_{EH}	Erase Hold Time		9.5	10.0	10.5	ms
t_{ERV}	Erase Recovery Time		2	–	–	
t_{ACC}	Address Access Time		–	–	15	μs
t_{PAC}	Page Mode Address Access Time		–	–	120	ns
t_{CE}	$\overline{CE}$ Access Time		–	–	15	μs
t_{OE}	$\overline{OE}$ Access Time		–	–	50	ns
t_{OH}	Output Data Hold Time		0	–	–	
t_{DF1}	$\overline{CE}$ to Output in High – Z		–	–	50	
t_{DF2}	$\overline{OE}$ to Output in High – Z		–	–	50	
t_{VC}	Verify Cycle Time	1st Cycle	15	–	–	μs
		2nd Cycle~	120	–	–	ns
t_{CEHH}	$\overline{CE}$ High Level Hold Time		100	–	–	

A.C. Test Condition

- Output Load : 1TTL Gate and C_L = 100pF
- Input Pulse Rise and Fall Time (10%~90%) : 5ns Max.
- Input Pulse Level : 0.4V / 2.6V
- Timing Reference Level : Input 0.8V / 2.2V, Output 0.8V / 2.0V

PROGRAM AND PROGRAM VERIFY TIMING WAVEFORM



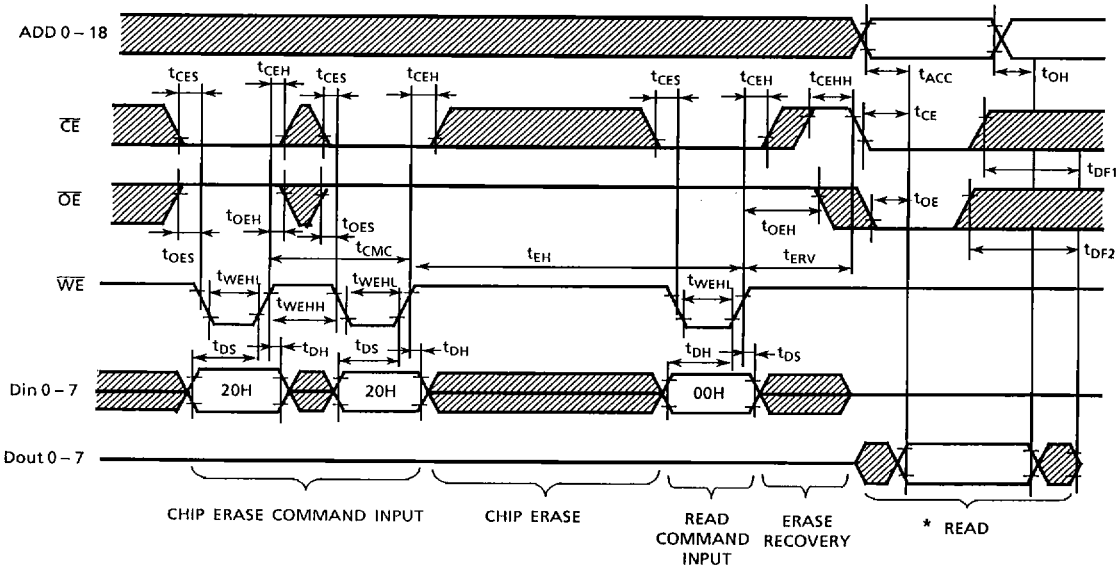
* : 512 byte Serial Data Input · · · · 512byte data must be input from Add 0 to Add 511 in serial in the page.

* : Program Verify · · · · Column Addresses A0 - 8 must be fixed and can not be changed in the time period of t_{ACC} and t_{CE}.
A skew among column addresses A0 - 8 must be less than 15ns.

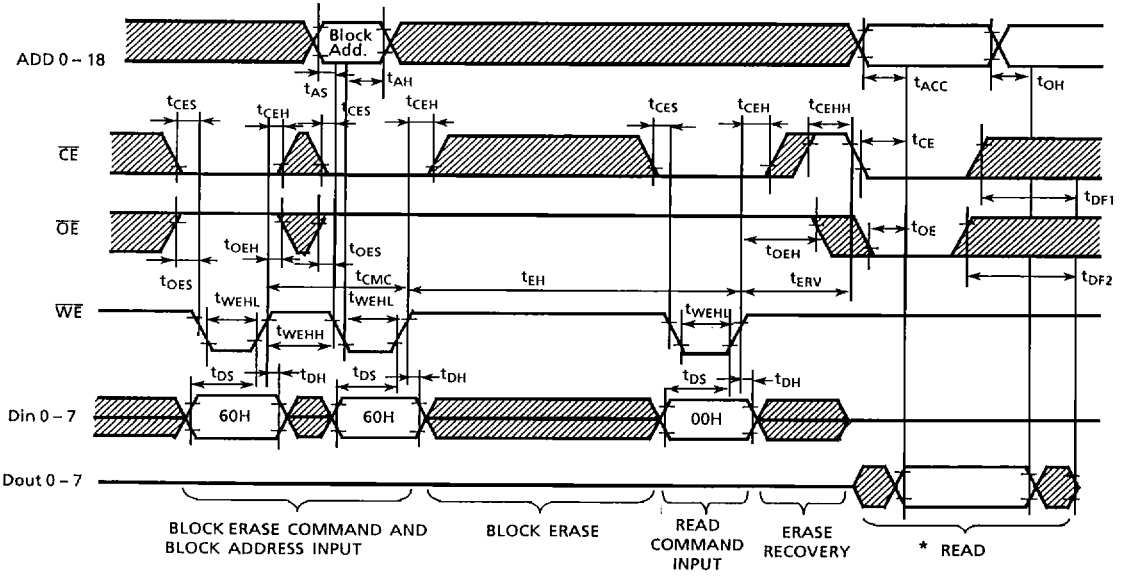
· · · · V_{IH} or V_{IL}

· · · · V_{IH} , V_{IL} or Hi – Z

CHIP ERASE AND ERASE VERIFY TIMING WAVEFORM

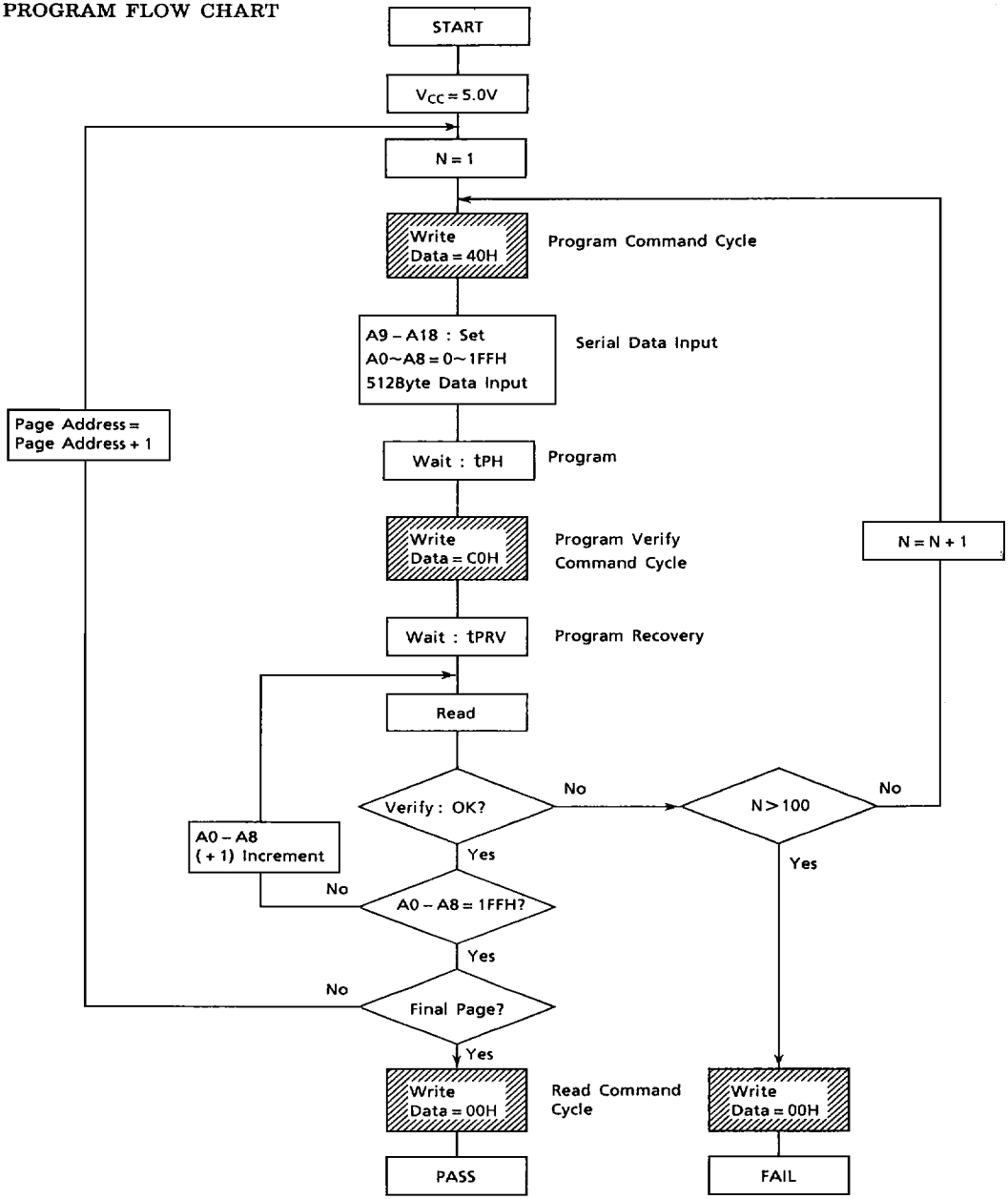


BLOCK ERASE AND ERASE VERIFY TIMING WAVEFORM

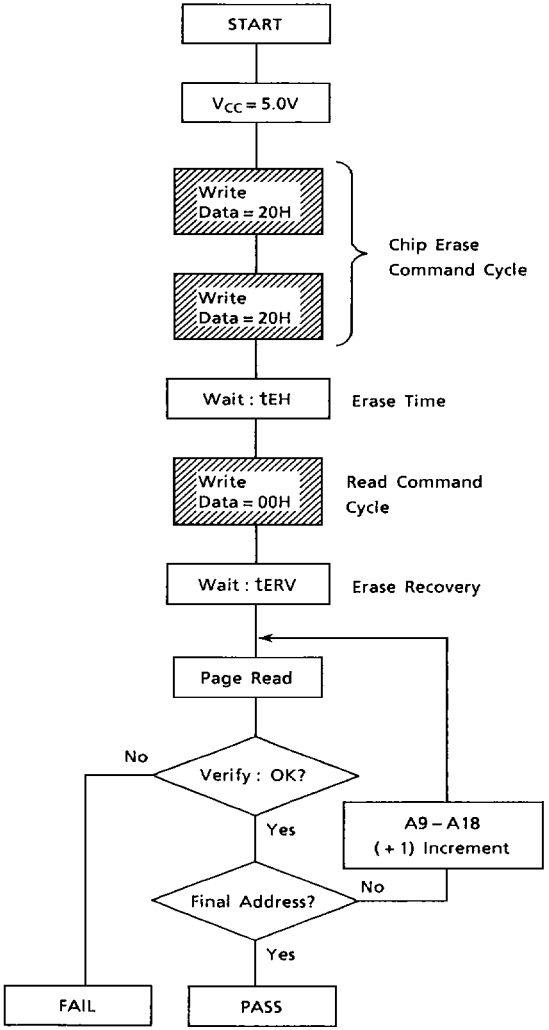


* READ : Column addresses A0 - 8 must be fixed and can not be changed in the time period of t_{ACC} and t_{CE}.
A skew among column addresses A0 - 8 must be less than 15ns.

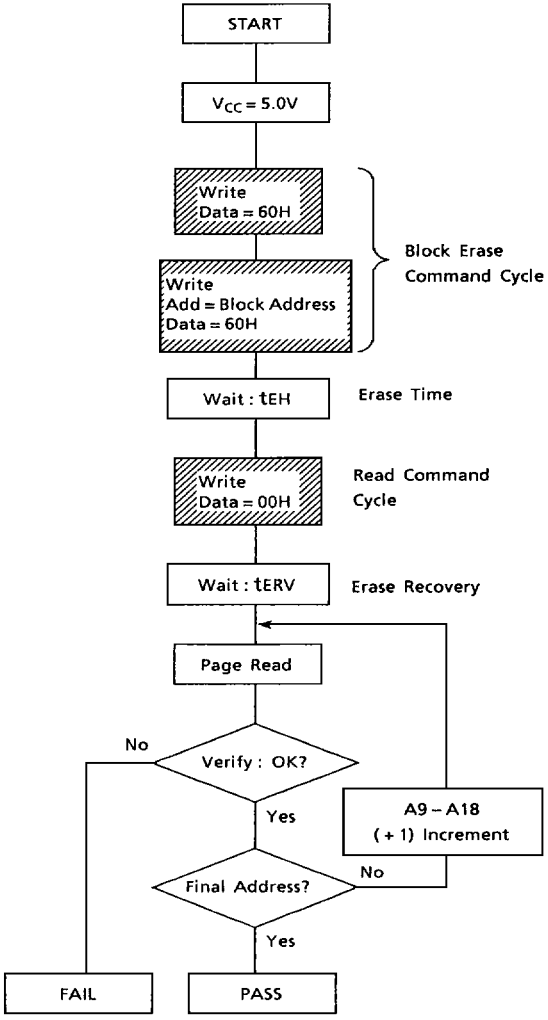
PROGRAM FLOW CHART



CHIP ERASE FLOW CHART



BLOCK ERASE FLOW CHART



DEVICE STRUCTURE AND OPERATION

The TC584000P/F/FT/TR consists of 8 sets corresponding to 8 I/Os of nonvolatile memory cell arrays organized as 512 columns by 1024 rows. A 512-bit data register is connected to each set of memory cell arrays. A NAND cell structure in which 8 cells are connected in serial is employed for memory cells. Each of the 8 cells is connected to a different page. (Fig.1)

A block is consisted of 512 NAND structures×8 I/Os.
The program and read operations are performed on a page level. The erase operation is performed either on a block or on the whole chip.

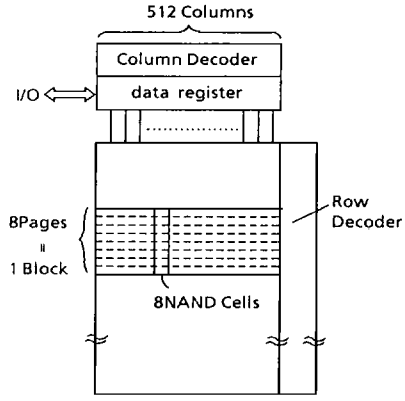
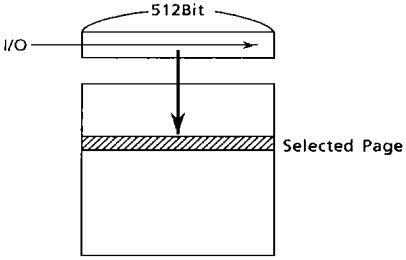


Fig.1 Structure of TC584000

PROGRAM OPERATION

Since the program operation of TC584000P/F/FT/TR is performed at every 512 bytes (=1page), 512 bytes data of the page must be input from the column address 000H to 1FFH (A0~A8) after the program command 40H is input. The address of the page on which the program operation is done must be input in the cycle in which the first byte data is input, however, no page address has to be valid in the following 511 cycles. The internal programming operation starts at the rising edge of $\overline{WE}$ in the last byte data input cycle and stops at the rising edge of $\overline{WE}$ in the following program verify command input cycle, thus this time period must be controlled by timing parameter t_{PH} (Program Hold Time).



A time delay of t_{PRV} after the program verify command is input, the programmed data can be read out and verified. The column address and page address must be input in these verify cycles.

The first verify cycle needs 15μs, however the following verify cycles can be done by page mode with the cycle time of 120ns. If the data read out is not correct in these verify cycles, return to the beginning of the program operation and repeat the same routine from the program command input cycle until all 512 bytes of data read out in verify cycles are correct. (cf. program and program verify timing, program flow chart).

CHIP ERASE OPERATION

The chip erase operation is initiated by two cycles of chip erase command 20H input. The internal chip erase operation starts at the rising edge of $\overline{WE}$ in the second cycle and stops at the rising edge of $\overline{WE}$ in the following read command input cycle. This time period must be controlled by t_{EH} (Erase Hold Time). The erase operation completes in 10ms.

BLOCK ERASE OPERATION

The TC584000P/F/FT/TR is organized as 8 pages/block×128 blocks internally and the block erase operation can be performed on any 4K bytes (8pages) block. The block erase operation is started by two cycles of block erase command 60H input with the block address (A_{12}~A_{18}) in the second cycle.

Like the chip erase operation, the internal block operation starts at the rising edge of $\overline{WE}$ in the second cycle and stops at the rising edge of $\overline{WE}$ in the following read command input cycle. The block erase operation completes in 10ms.

READ OPERATION

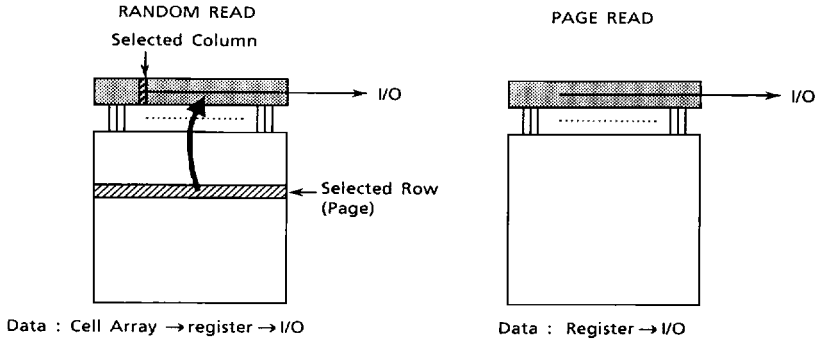
The read operation can be performed after read command 00H input. Two types of read operations are available; random read and page read.

The random read operation occurs when the page address is changed or $\overline{CE}$ is clocked. First, 512 bytes of data are transferred from the new selected page on a nonvolatile cell array to the register. Then, the data in the selected column address on the register is read out.

The page read operation occurs when no page address is changed and $\overline{CE}$ is not clocked. The 512 bytes data transfer is very slow and takes approximately 15μs, therefore, t_{ACC} (Random Address Access time) is 15μs.

However, the read out from the register is very fast and t_{PAC} (Page Address Access Time) is 120ns.

In the page read operation, the data is read out by fixing the page address and changing the column address.



RESET

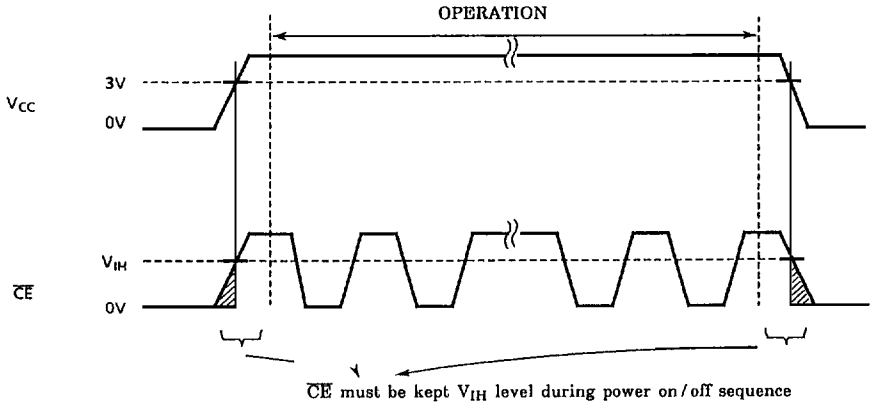
The reset operation is achieved by writing the reset command FFH into the address 55555H in two cycles. This operation is used in order to break the data input cycles in the program or program and erase operation. The reset does not necessarily have to be performed in a normal operation. The device mode after reset is a read operation.

OPERATION MODE AFTER POWER ON

The operation mode after the power-on becomes a read operation automatically. However, it is recommended to input the read command 00H at the beginning of device operation after the power supply becomes stable.

POWER ON / OFF SEQUENCE

An accidental command input cycle during power on / off sequence may cause data corruption, therefore $\overline{CE}$ must be kept high level when Vcc is higher than 3V during power on / off sequence.



OPERATION PRINCIPLE

PROGRAM OPERATION

Fig. 2 shows the program operation principle of the TC584000P / F / FT / TR. The program operation is to program data '0's into cells in the erased state (data '1') by employing tunneling phenomenon. The following explains the program operation principle with an example in which data '0' and '1' are programmed into the TR1 and TR2 individually in the selected page.

The select line 1 is given 'H' level and the select line 2 is given 'L' level so that 8 cells in the NAND are connected to the bit line and isolated from GND. Then V_{PP} (approximately 20V) is given to the word line of the selected page and V_{PI} (approximately 10V) is given to the word line of the other unselected pages.

On the other hand, 0V is given to the bit line connected to the NAND that has TR1 in which data '0' is going to be programmed and V_{DPI} (approximately 10V) is given to the bit line connected to the NAND that has TR2 in which data '1' is going to be programmed.

With this condition of voltages on each noad, TR1 has approximately 20V between its control gate and channel, and electrons are injected to the floating gate from the channel by tunneling phenomenon.

Once this happens, eventhough V_{PP} is cut off, the electrons are retained in the floating gate which is surrounded by SiO_2 until an erase operation is performed.

At TR2, 20V is given to the control gate, however 10V given to the channel make the potential difference between the control gate and channel approximately 10V which is not high enough for tunneling phenomenon. Thus, electron injection does not occur. The cells in the unselected page have approximately 10V on their control gate so no tunneling phenomenon will occur.

The floating gate of a '0' data cell is charged negative and that of a '1' data çell is charged positive, thus the '0' and '1' data are retained after the program operation has been done.

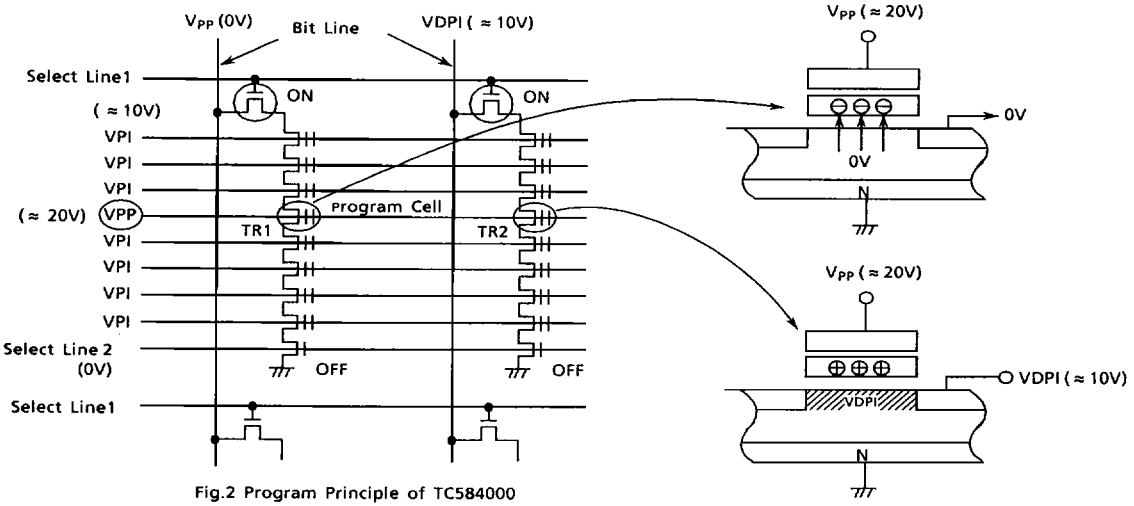


Fig.2 Program Principle of TC584000

ERASE OPERATION

The erase operation principle of the TC584000 is shown in Fig.3. The erase operation changes the cell state in a selected block or in a whole chip from '0' to '1' by pulling electrons out from the floating gate to the channel by tunneling phenomenon.

0V and VPP (approximately 20V) are given to the control gates and substrate respectively in the operation. This gives 20V potential difference between the control gates and substrate, and results in tunneling phenomenon which pulls electrons in the floating gate out to the substrate.

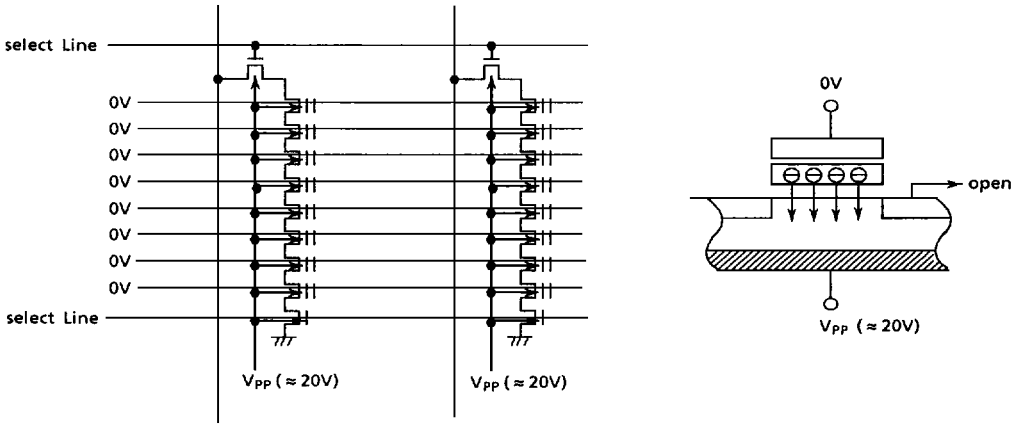


Fig.3. Erase Principle of TC584000

READ OPERATION

As explained in the program operation above, the state of the cells are '0' in which the floating gate is charged negative or '1' in which the floating gate is charged positive after the program operation. This is described by threshold voltage V_{TH}; the characteristics parameter of MOS transistor as shown in Fig.4.

The threshold voltage of '0' data cells distribute in positives side and that of '1' data cells distribute in negative side.

The reason why they distribute in a certain area is that the memory cell transistors have some dispersion.

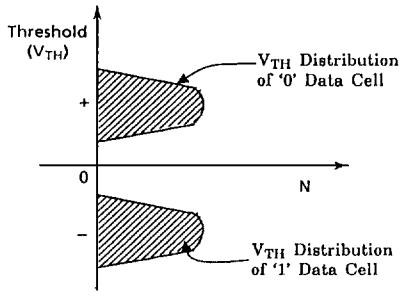


Fig.4. Threshold Voltage Distribution of '0' Data / '1' Data Cell

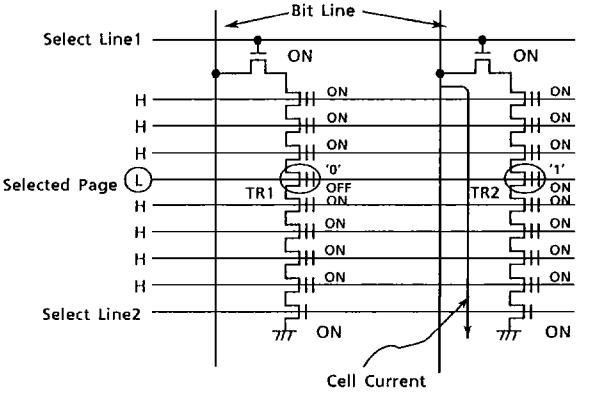


Fig.5 Read Principle of TC584000

Fig.5 shows the read operation principle.

The select line 1 and 2 of the block which has the selected page are biased 'H' level and 8 cells in the NAND are connected to the bit line and GND. The control gates of 7 unselected page are given 'H' level and that of the selected page is given 0V.

In Fig.5, TR2, since it is in '1' state, turns on and all the other unselected transistors also turn on, therefore cell current flows and the precharged bit line discharges. On the contrary, since it is in '0' state, TR1 does not turn on and cell current does not flow. The bit line levels at this point are sensed '1' and '0' respectively by the sense amplifier.

RECOMMENDATION FOR PROGRAM OPERATION

1) Over programming by t_{PH} (program Hold Time) being longer than the specified value may make it impossible to read data out of the cell correctly. If this happened, an erase operation will be necessary to recover from the over programmed state.
   Over program means that the threshold voltage of the programmed cells shifted too much in the positive direction. Thus, the cell transistors of the unselected pages during a read operation can not turn on.
2) The page address within a block (A_9~A_{11}) must be incremented in order from LSB to MSB when the device is programmed.
3) Comment on the program on a already programmed page : There is a resriction for the number of times of new date programming operations on a already programmed page.
4) In case of programming several devices in parallel, programming inhibit for a device which has already been programmed successfully should be done by command input instead of programming '1' data.