YDA165

D-4HP3

MONO 3.3W Non-Clip DIGITAL AUDIO POWER AMPLIFIER

■ Overview

YDA165 is a one-chip audio subsystem that integrates a monaural loudspeaker amplifier and a stereo headphone amplifier. Two sets of input signal are supported, and each can be configured either as an pair of single-ended stereo inputs or as a differential monaural input. Each set of input goes through mixing, volume-setting, and muting circuits that are controlled through the I2C compliant interface provided. Headphone amplifier employs an advanced class-G technology with an high efficiency charge-pump power supply, achieving higher output power (64mW) without compromising low-level output efficiencies. Speaker amplifier outputs 1000mW (4.2V, 8Ω, THD+N = 1%) the highest in its class, and introduces new Noise Gate function in addition to Yamaha Non-Clip and Power Limit. Noise Gate shuts off the output of the residual noise when output level is low, thus achieving very high SNR. Speaker amplifier also comes with over-current protection, high-temperature protection, and DC-output protection.

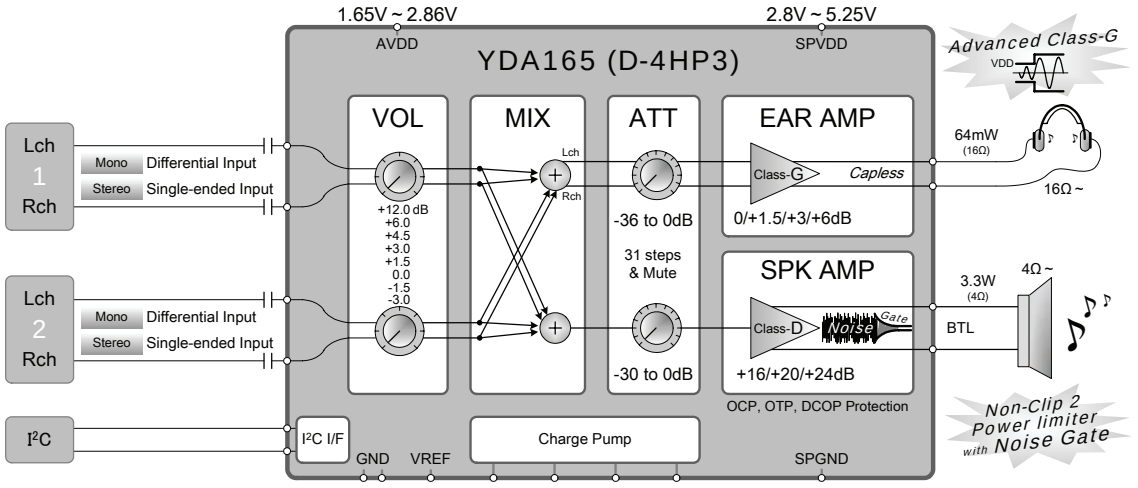
● Speaker Amplifier (Class-D)

・Max. Output 3.3W (5.0V, 4Ω, THD+N=10%)
1000mW (4.2V, 8Ω, THD+N=1%)
・THD+N 0.045% (3.6V, 8Ω, Po=0.35W, 1kHz)
・SNR 96.4dB (3.6V, THD+N=1%, Noise Gate)
・Non-Clip2, Power Limiter, and Noise Gate functions
・Overcurrent protection, high temperature protection, and DC output protection

● Headphone Amplifier (Capless Advanced Class-G)

・Max. Output 64mW (3.6V, 16Ω, THD+N=1%)
・THD+N 0.01% (3.6V, 32Ω, Po=5mW, 1kHz)
・SNR 97dB (3.6V, 16Ω)

・Ultra Low pop noise
・Lead-free package (YDA165-PZ; 20-ball, WLCSP)
・Size 2.07mm(W)×2.60mm(D)×0.60mm(H)



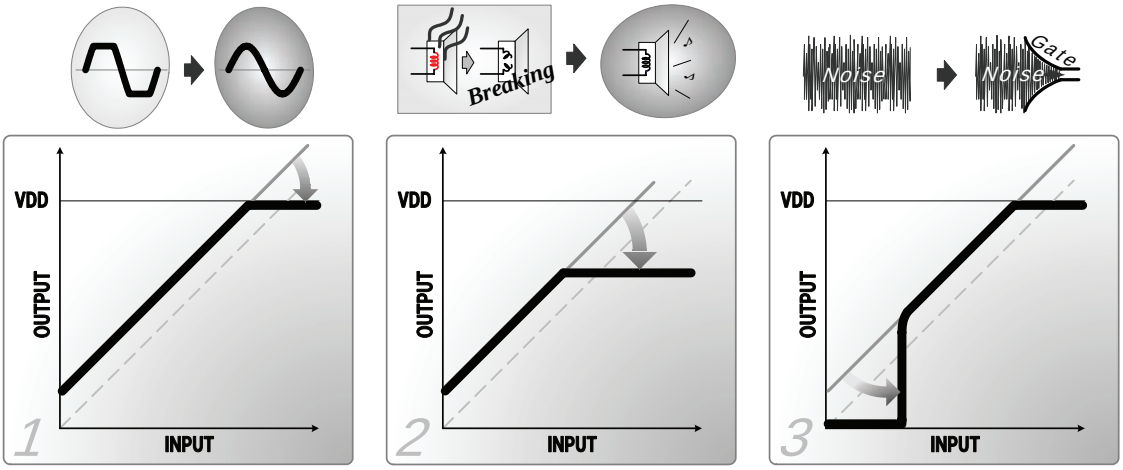
YAMAHA CORPORATION

YDA165 Catalog
CATALOG No. LSI-4DA165A20
2010.11

■ Features

● Speaker Amplifier Function

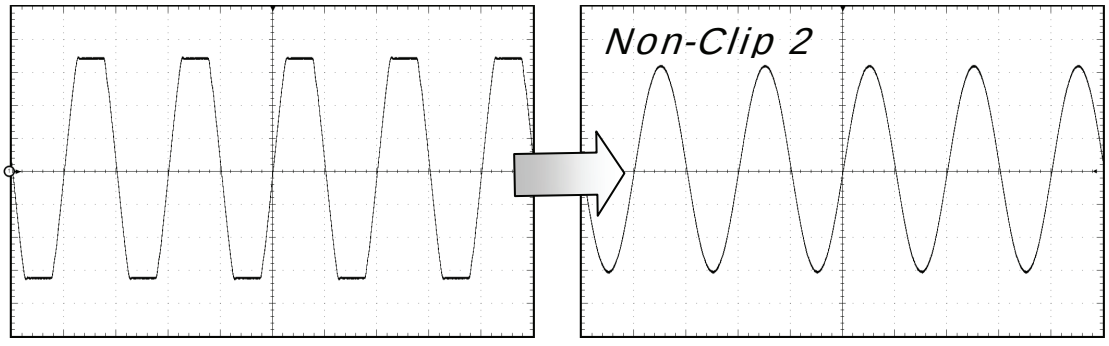
The YDA165 speaker amplifier has the following three special features:



Non-Clip2	*Power Limiter*	*Noise Gate*
Prevention of sound distortion	Precise control of the maximum output power	Prevention of TDMA (GSM) noise or white noise

● 1. Non-Clip2 Function

The Non-Clip2 is the function that reduces the output distortion by automatically controlling the PWM amplifier gain in case the speaker amplifier output is clipped at the supply voltage.



In addition, it is possible to set any amount of harmonic distortion of the PWM amplifier gain.

Setting values: THD= ≤1%, 3%, 5%, 10%, 13%, 15%, 20%

And this Non-Clip2 function is also useful for the application whose supply voltage (V_{SPVDD}), such as batteries etc, fluctuates.

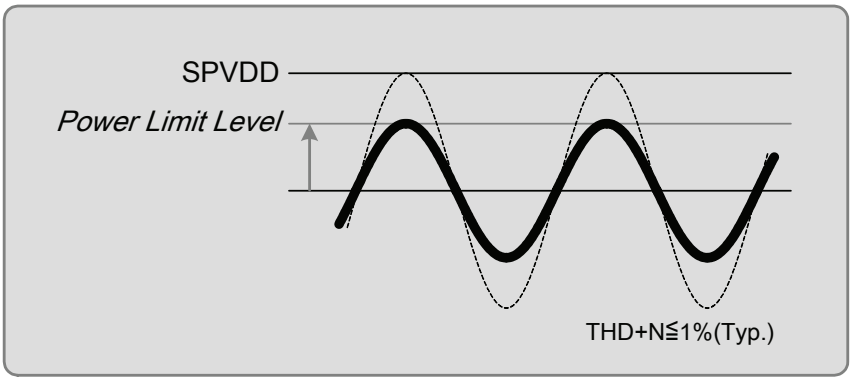
● 2. Power Limiter Function

The Power Limit function is provided for the purpose of limiting the output power to reduce the overload of a speaker.*
And, even in the distortion characteristics, this function limits the output distortion to THD+N ≤ 1% (as seen in Non-Clip function) to achieve high sound quality. The power limit level is constant regardless of the supply voltage because it is based on the internal absolute voltage of the device.

* This function does not always protect speakers.

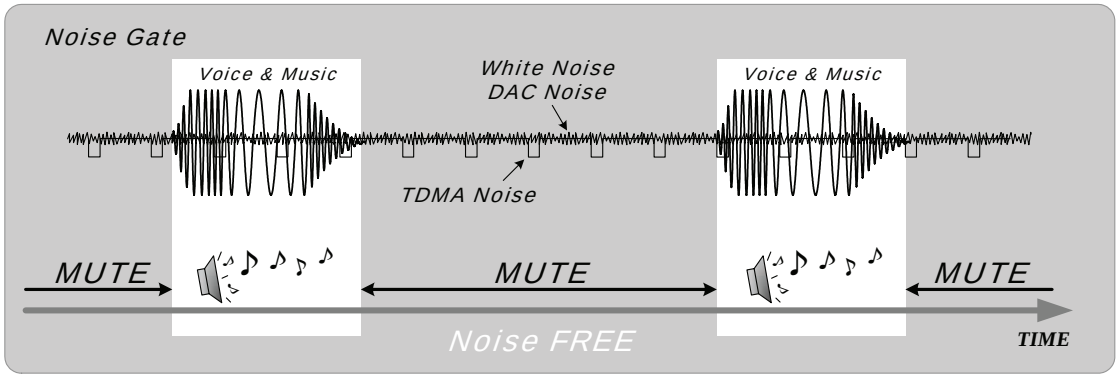
A power limit level, ranging from 570mW to 1000mW in 12 steps, can be set by using the register.

Limit levels: 570mW, 600mW, 635mW, 670mW, 700mW, 735mW
770mW, 800mW, 850mW, 900mW, 950mW, 1000mW



● 3. Noise Gate Function

The Noise Gate function is the function that removes unwanted noise coming in at no-signal state.
This function automatically mutes the output when a signal level becomes lower than the threshold level.
This removes TDMA or DAC noise etc. coming in at no-signal state, thus achieving the low-noise characteristics.
In addition, the following values can be configured precisely: threshold level, attack time, release time, etc.

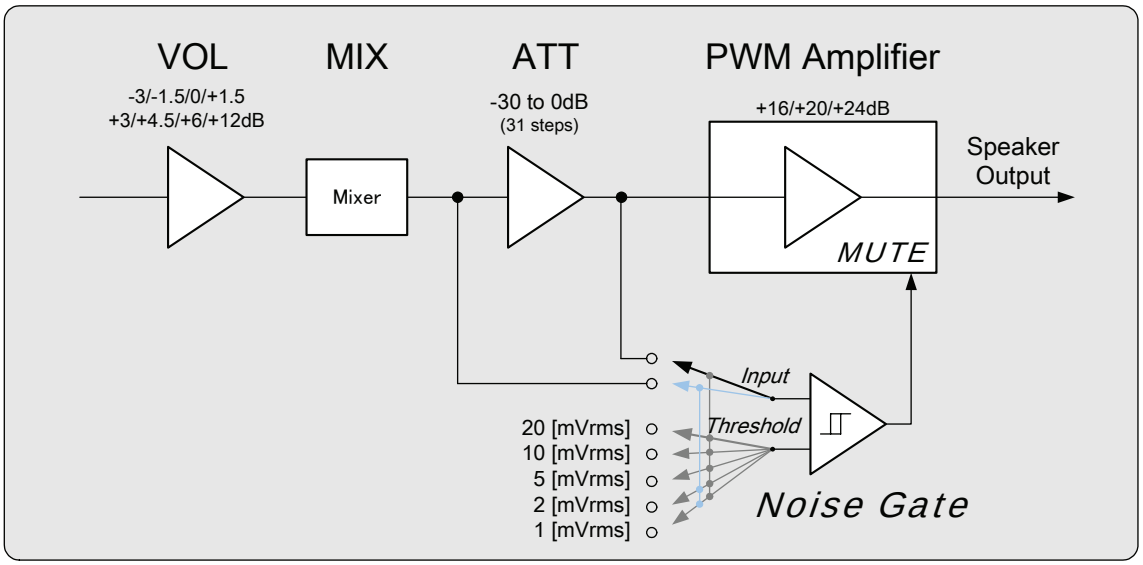


* MUTE: Attenuated by approx. -40dB (typ.)

This Noise Gate function is based on the Non-Clip technology, controlling the analog circuitry adequately, thus allowing for Yamaha's unique natural sound.

◆ Noise Gate Detection Method

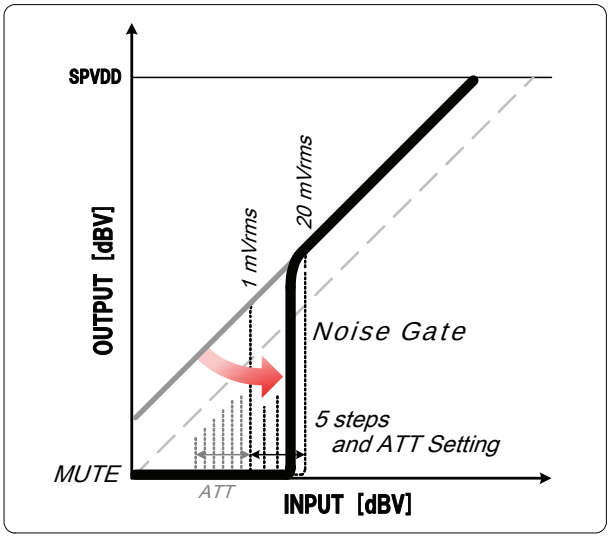
The Noise Gate detects the attenuator output level or the attenuator input level to mute the speaker output if the detection level is lower than the threshold level.



Noise Gate Detection - Conceptual Diagram

◆ Noise Gate Characteristics

The figure below shows the Noise Gate I/O characteristics:

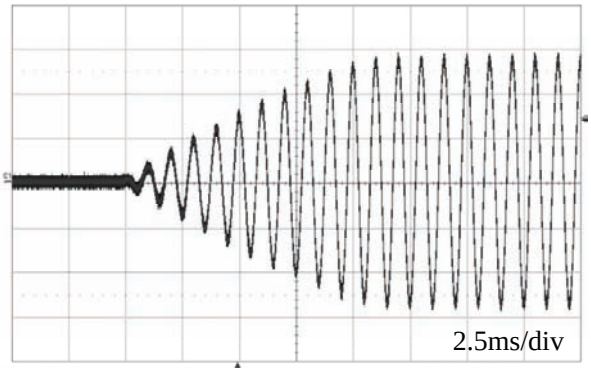


Noise Gate I/O characteristics

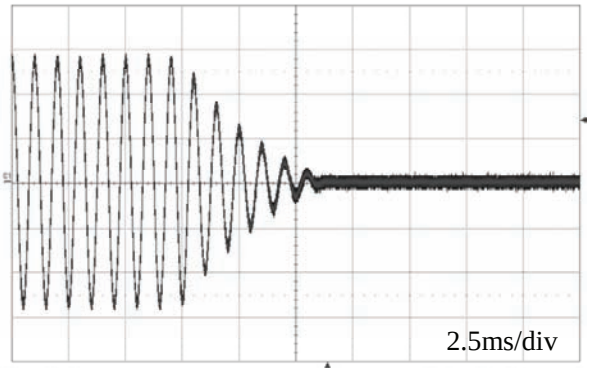
In addition, the Noise Gate can lower the threshold of the sound being heard by setting the detection level to the attenuator input signal level to lower the attenuation.

● 4.Quick Start/Quick Mute Function

This function reduces pop noise that may occur at startup/shutdown, by varying the envelope of a speaker amplifier output at a slow rate. This function, even in a high-speed startup/shutdown operation, reduces intermittent sound break considerably to eliminate uncomfortable sound.



Quick Start

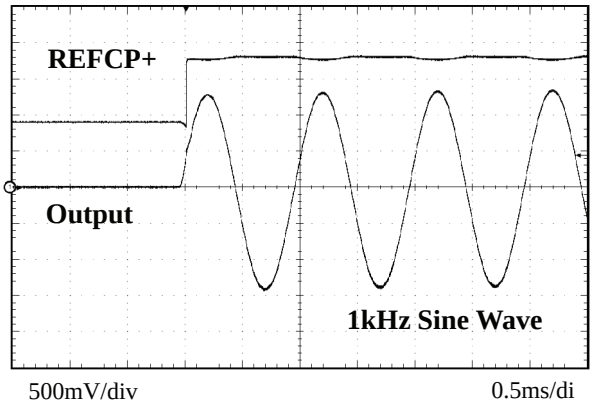


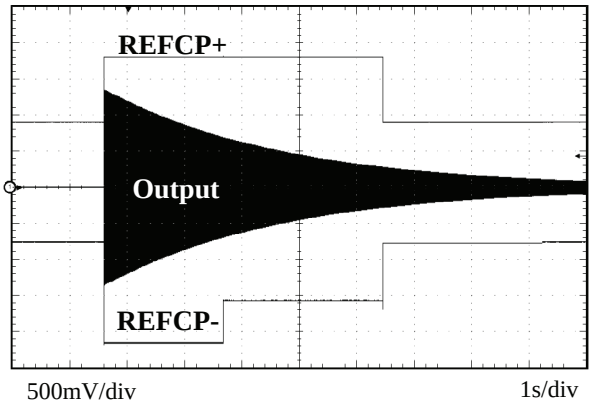
Quick Mute

● Headphone Amplifier's Features

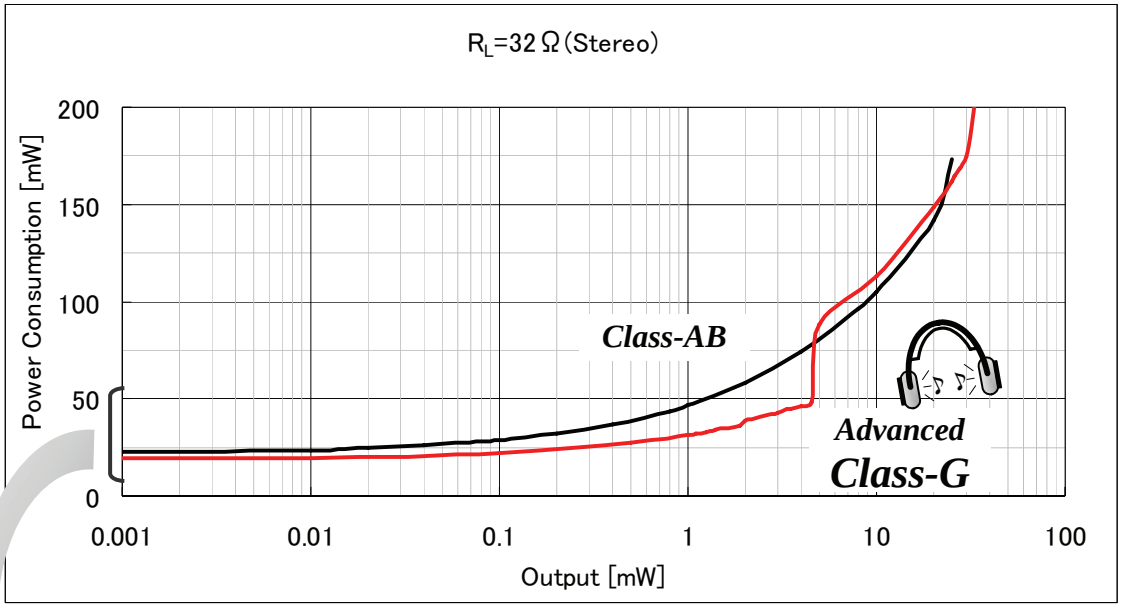
The YDA165's headphone amplifier is based on Yamaha's unique "Advanced Class-G" method and achieves high efficiency by optimizing its supply voltages according to the output power.

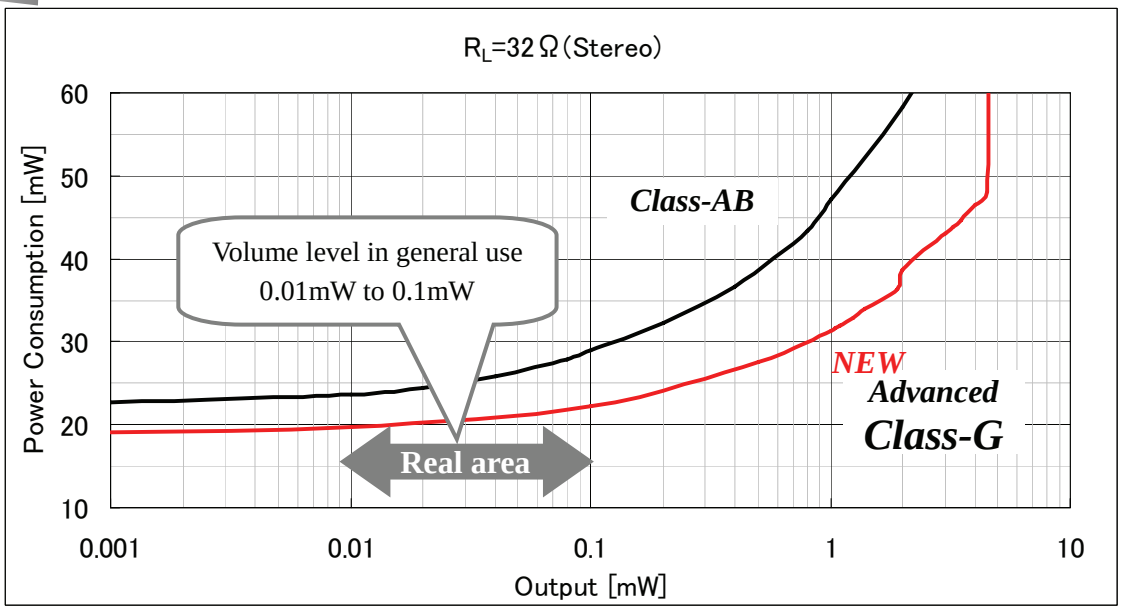
The headphone amplifier supply voltages (REFCP+, REFCP-) vary according to the output amplitude as shown below:





◆ Power Consumption (Measured value)



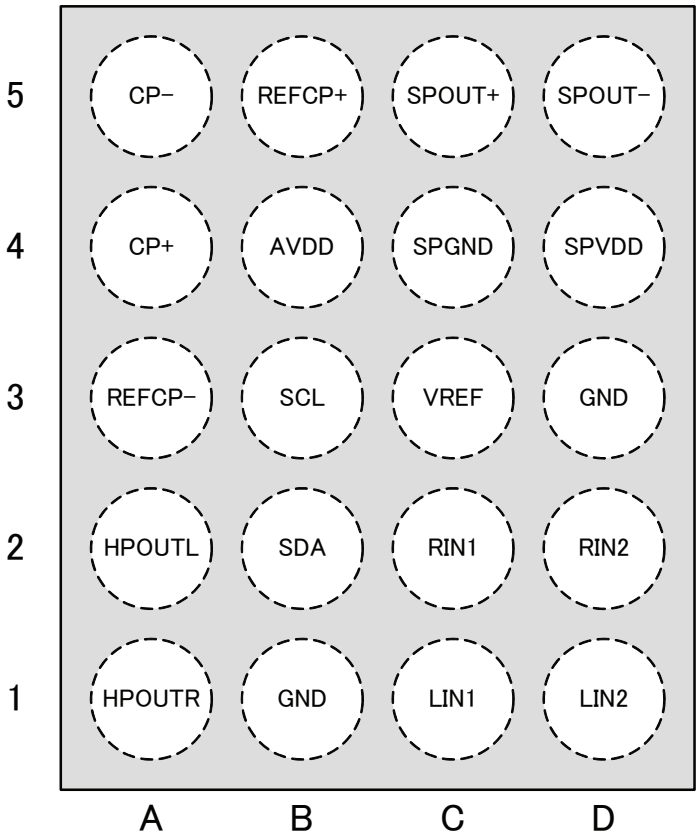


* Indicates the overall IC consumption power.

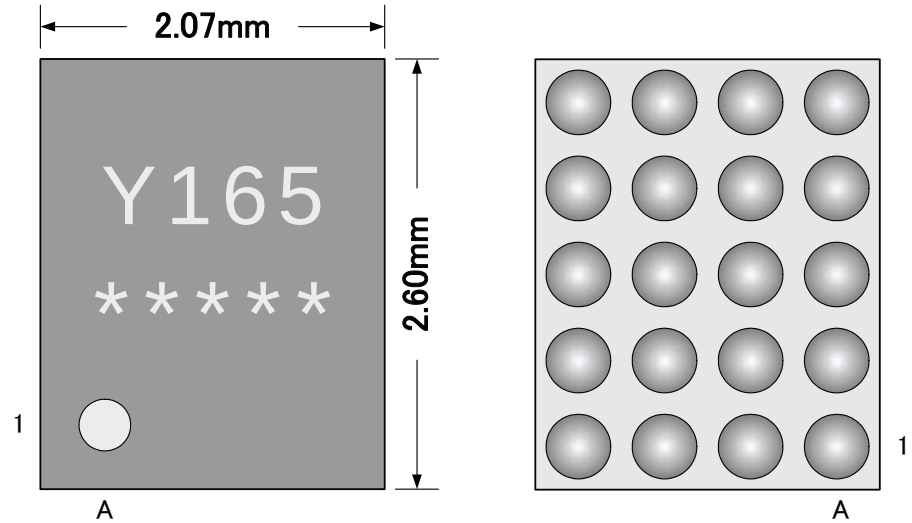
Advanced Class-G:

Amplifiers based on this method, reducing the power supply current capability in a very small output power, have higher efficiency than those based on the general Class-G method.

■ Pin Assignment



20-ball WLCSP Top View



Top Bottom

■ Pin Description

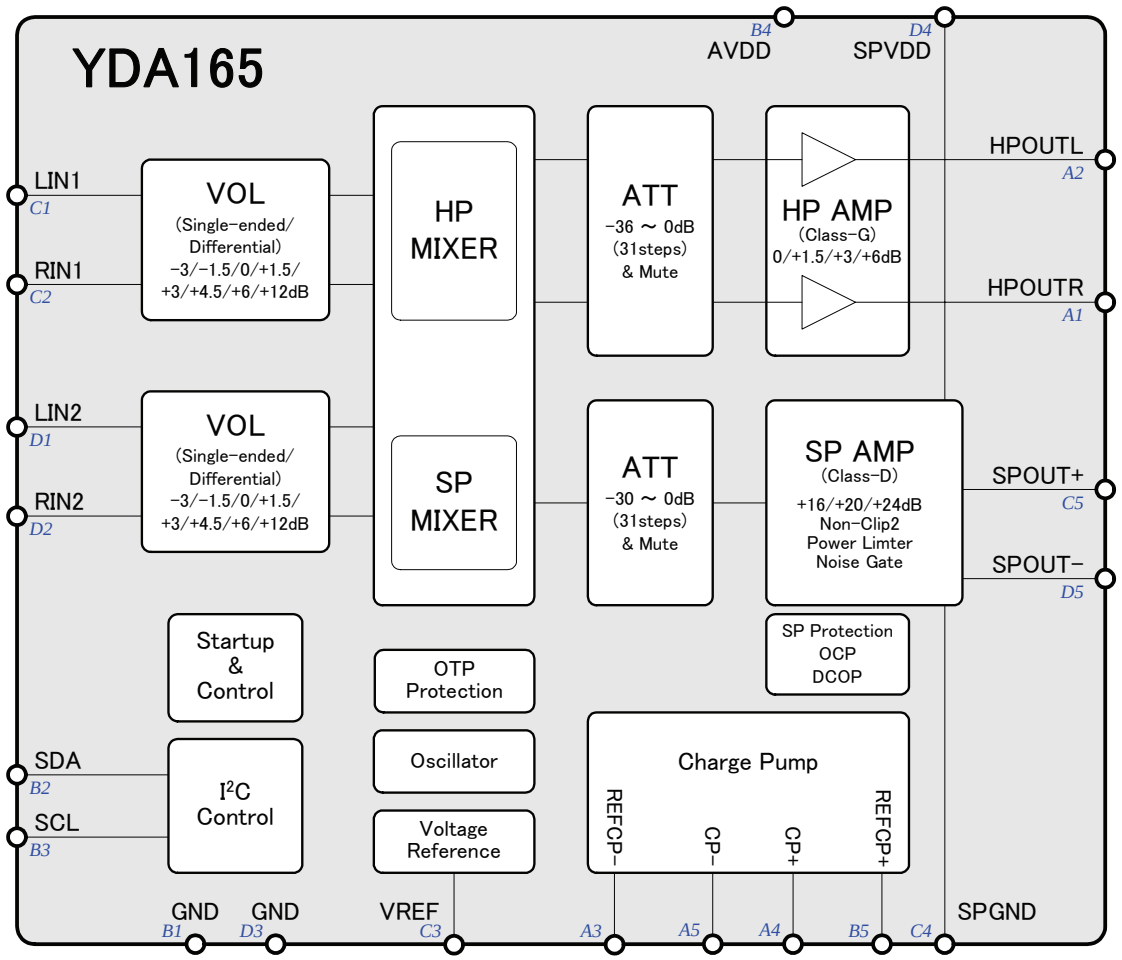
No.	Pin Name	I/O	Description
A1	HPOUTR	O	Headphone amplifier output pin (Rch.)
A2	HPOUTL	O	Headphone amplifier output pin (Lch.)
A3	REFCP-	O	Charge pump output pin (−)
A4	CP+	O	Charge pump pin (+)
A5	CP-	O	Charge pump pin (−)
B1	GND	GND	GND pin
B2	SDA	ISOD	I^2C serial data pin
B3	SCL	IS	I^2C serial clock pin
B4	AVDD	Power	Analog circuit power supply pin
B5	REFCP+	O	Charge pump output pin (+)
C1	LIN1	A	Stereo input pin 1 (Lch.) (See Note.)
C2	RIN1	A	Stereo input pin 1 (Rch.) (See Note.)
C3	VREF	A	Analog reference voltage pin
C4	SPGND	GND	Speaker amplifier output GND pin
C5	SPOUT+	O	Speaker amplifier output pin (+)
D1	LIN2	A	Stereo input pin 2 (Lch.) (See Note.)
D2	RIN2	A	Stereo input pin 2 (Rch.) (See Note.)
D3	GND	GND	GND pin
D4	SPVDD	Power	Speaker amplifier output power supply pin
D5	SPOUT-	O	Speaker amplifier output pin (−)

A: Analog pin, IS: Schmitt input pin, O: Output pin, ISOD: I/O pin (Schmitt input, Open-drain output)

Note : Note that leakage current flows through the protection circuit of PMOS Tr. when applying a voltage higher than AVDD to this pin.

When using a D/A Converter output with Noise-Shaping circuit used in its former stage, apply a signal whose signal components outside the audible frequency have been sufficiently attenuated (e.g. -90dBV at the frequency ranging from 150 kHz to 320 kHz). Otherwise, Beat Noise (i.e. noise caused by interference between two frequencies) may occur because of signal components in the same band as internal clocks used for PWM modulation.

■ Block Diagram



■ Electrical Characteristics

● Absolute Maximum Ratings (See Note 1.)

Item	Symbol	Condition	Min.	Max.	Unit
SPVDD voltage range	V_{SPVDD}		–0.3	6.0	V
AVDD voltage range	V_{AVDD}		–0.3	3.2	V
Input pin voltage range	V_{INA}	LIN1, RIN1, LIN2, RIN2	V_{GND} – 0.6	V_{AVDD} + 0.6	V
	V_{I2C}	SDA, SCL	V_{GND} – 0.3	4.2	
	V_{IN}	Input pins other than the above	V_{GND} – 0.3	V_{AVDD} + 0.3	
Power Dissipation	P_{D25}	T_A=25°C (See Note 2.)	-	2.85	W
	P_{D70}	T_A=70°C (See Note 2.)		1.57	
	P_{D85}	T_A=85°C (See Note 2.)		1.14	
Junction Temperature	T_{jmax}		-	125	°C
Storage Temperature	T_{STG}		–50	125	°C
Speaker Impedance	R_{LS}		3.2	-	Ω
Headphone Impedance	R_{HLS}		12.8	-	Ω

Note1: Absolute Maximum Ratings are values which must not be exceeded to guarantee device reliability and life, and when using a device in excess of the ratings for even a moment, it may immediately cause damage to the device or may significantly deteriorate its reliability. In the system where the voltage at an input pin may exceed the supply voltage (V_{AVDD} / GND), use an external diode etc. to limit it to the value lower than absolute maximum rating.

Note 2: θja＝35ºC/W (Conditions: Board; EVB-D4HP3 C20Z3 (4 layers), no wind)

Note: SPGND = GND = 0V

● Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SPVDD Supply Voltage	V_{SPVDD}		2.8	3.6	5.25	V
AVDD Supply Voltage	V_{AVDD}		1.65	2.6	2.86	V
Operating Ambient Temperature	T_A		–40	25	85	ºC

Note: ・Be sure to use the device within the recommended operating conditions.
・SPGND = GND = 0V
・SPVDD ≥ AVDD
・Power-up Sequence
1. SPVDD
2. AVDD (No specified restriction on the time difference between 1 and 2)
・Power-down Sequence
1. Elapse of the period of time $T_{PD\_SP,}$ T_{PD_HP}
2. AVDD
3. SPVDD (No specified restriction on the time difference between 2 and 3)
・AVDD slew rate should be less than 1V/μsec.

● Consumption Current

(SPVDD=3.6V, AVDD=2.6V, SPGND=GND=0V, T_A=25ºC, unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Speaker mode							
SPVDD consumption current	I_{SPVDD}	No load, No input		-	2.9	-	mA
AVDD consumption current	I_{AVDD}			-	2.2	-	mA
Headphone mode							
SPVDD consumption current	I_{SPVDD}	No load, No input		-	1.0	-	mA
AVDD consumption current	I_{AVDD}		ECO_MODE= "1"	-	5.7	-	mA
			ECO_MODE= "0"	-	6.8	-	mA
Power-down mode consumption current	I_{PD}	SRST(0x80) = "1" SCL = "AVDD" SDA = "AVDD"		-	1	-	μA

● DC Characteristics

(SPVDD=2.8 to 5.25V, AVDD=1.65 to 2.86V, SPGND=GND=0V, T_A= -40ºC to 85ºC, unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital input voltage H level	V_{IH}	SDA, SCL	1.5	-	3.6	V
Digital input voltage L level	V_{IL}	SDA, SCL	-	-	0.4	V
I^2C output voltage	V_{OL}	I_{OL}= 3mA, SDA	-	-	0.4	V
Input leakage current	I_{IN}	SDA, SCL, 2.86V (applied voltage)	–1	-	1	μA
Input capacitance	C_{IN}	SDA, SCL	-	-	10	pF
Schmitt width	V_{sh}	SDA, SCL	-	100	-	mV
VREF pin voltage	V_{REF}		-	V_{AVDD}/2	-	V
Input resistance	R_{IN}	LIN1, RIN1, LIN2, RIN2	5.3	-	36	kΩ
DC error detection voltage	V_{DCDET}		-	0.6	-	V

Note: The same measurement conditions as those for "I^2C Timing" are also required.

● AC Characteristics

(SPVDD=2.8 to 5.25V, AVDD=1.65 to 2.86V, SPGND=GND=0V, T_A= -40ºC to 85ºC, unless otherwise specified)

Item		Symbol	Condition		Min.	Typ.	Max.	Unit
Prohibited access time (I^2C)		T_{STI2C}			-	-	10	msec
Input DC-cut capacitance charge time		T_{CHG}			-	13.6	-	msec
Startup time		T_{STUP_SP}	Speaker Amplifier		-	13.6	-	msec
		T_{STUP_HP}	Headphone amplifier			13.6		
Power-down setting time		T_{PD_SP}	Speaker Amplifier		28.8	-	-	msec
		T_{PD_HP}	Headphone amplifier		28.8			
Mute setting time		T_{MUTE_SP}	Speaker Amplifier		-	10	14.4	msec
		T_{MUTE_HP}	Headphone amplifier		-	10	14.4	
DC error detection delay time		T_{DCDET}			-	2	-	sec
Non-Clip2, Power Limit	Attack time	T_{AT0}	DATRT[1:0] =	00	-	0.1	-	msec/dB
		T_{AT1}		01		0.1		
		T_{AT2}		10		0.5		
		T_{AT3}		11		1.0		
	Release time	T_{RL0}	DATRT[1:0] =	00	-	20	-	msec/dB
		T_{RL1}		01		200		
		T_{RL2}		10		200		
		T_{RL3}		11		200		
Noise Gate	Attack time	T_{NGAT0}	NG_ATRT[1:0] =	00	-	25	-	msec
		T_{NGAT1}		01		100		
		T_{NGAT2}		10		400		
		T_{NGAT3}		11		800		
	Release time	T_{NGRL0}	NG_ATRT[1:0] =	00	-	1.4	-	msec
		T_{NGRL1}		01		1.4		
		T_{NGRL2}		10		1.4		
		T_{NGRL3}		11		1.4		
	Hold time	T_{NGHD0}	NG_ATRT[1:0] =	00	-	44	-	msec
		T_{NGHD1}		01		44		
		T_{NGHD2}		10		44		
		T_{NGHD3}		11		44		

● Analog Characteristics

Speaker Amplifier (See Note 1.)

(SPVDD=3.6V, AVDD=2.6V, SPGND=GND=0V, 1kHz, T_A=25ºC, Av=+16dB, R_L=8Ω, unless otherwise specified)

Item	Symbol	Condition			Min.	Typ.	Max.	Unit
Maximum output	Po	SPVDD=5V, R_L=4Ω, THD+N=10%			-	3.3	-	W
		SPVDD=5V, R_L=4Ω, THD+N= 1%				2.6		
		R_L=8Ω, THD+N=10%				0.93		
		R_L=8Ω, THD+N= 1%				0.75		
		SPVDD=3.7V, R_L=8Ω, THD+N= 1%				0.79		
		SPVDD=4.2V, R_L=8Ω, THD+N= 1%				1.00		
Maximum output (under Non-Clip2 control)	$P_{ONC1\%}$	SPVDD=5V, R_L=4Ω		DALC[2:0]= 001	-	2.5	-	W
		R_L=8Ω				0.70		
	$P_{ONC3\%}$	SPVDD=5V, R_L=4Ω		DALC[2:0]= 010		2.8		W
		R_L=8Ω				0.79		
	$P_{ONC5\%}$	SPVDD=5V, R_L=4Ω		DALC[2:0]= 011		3.0		W
		R_L=8Ω				0.85		
	$P_{ONC10\%}$	SPVDD=5V, R_L=4Ω		DALC[2:0]= 100		3.3		W
		R_L=8Ω				0.93		
	$P_{ONC13\%}$	SPVDD=5V, R_L=4Ω		DALC[2:0]= 101		3.5		W
		R_L=8Ω				0.96		
	$P_{ONC15\%}$	SPVDD=5V, R_L=4Ω		DALC[2:0]= 110		3.6		W
		R_L=8Ω				1.0		
	$P_{ONC20\%}$	SPVDD=5V, R_L=4Ω		DALC[2:0]= 111		3.9		W
		R_L=8Ω				1.08		
Power Limiter output power (THD+N ≤ 1 [%])	P_{PL4}	DPLT[3:0] =	SPVDD =3.6V	0100	-	570	-	mW
	P_{PL5}			0101		600		
	P_{PL6}			0110		635		
	P_{PL7}			0111		670		
	P_{PL8}			1000		700		
	P_{PL9}		SPVDD =5V	1001		735		mW
	P_{PL10}			1010		770		
	P_{PL11}			1011		800		
	P_{PL12}			1100		850		
	P_{PL13}			1101		900		
	P_{PL14}			1110		950		
	P_{PL15}			1111		1000		

(SPVDD=3.6V, AVDD=2.6V, SPGND=GND=0V, 1kHz, T_A=25ºC, Av=+16dB, R_L=8Ω, unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Total harmonic distortion	THD+N	SPVDD=5V, R_L=4Ω, Po=1.5W, BW=20kHz		-	0.05	-	%
		SPVDD=3.6V, R_L=8Ω, Po=0.35W, BW=20kHz			0.045		
S/N ratio	SNR	BW=20kHz, A-weighted Filter, Noise Gate		-	96.4	-	dB
PSRR	PSRR	SPVDD	217Hz	-	80	-	dB
			1kHz		78		
			20kHz		64		
Efficiency	η	P_O=0.9W		-	93	-	%
Output offset voltage	Vo	No input, Noise Gate		-	±0.4	-	mV
Frequency characteristics	Fres	C_{IN}=0.47μF, 100Hz to 20kHz, DPLT= “0000”, DALC= “000”		-3	-	0.4	dB
Carrier clock frequency	F_{PWM}			-	470	-	kHz

Note1: All the analog characteristics were measured by using our evaluation board. Depending upon pattern layout etc., characteristics may vary.

Note: The measurement condition denoted by “R_L =8Ω” means a load composed of a pure 8-ohm resistor with an inductance (30μH) connected in series.

Headphone Amplifier (See Note 1.)

(SPVDD=3.6V, AVDD=2.6V, SPGND=GND=0V, 1kHz, T_A=25ºC, Av=0dB, R_L=16Ω, unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Maximum output power	P_O	R_L=16Ω, THD+N=1%, CPMOD=0	Av= 0dB	-	46	-	mW
			Av= +3dB		64		
			Av= +6dB		64		
		R_L=32Ω, THD+N=1%, CPMOD=0	Av= 0dB		24		
			Av= +3dB		44		
			Av= +6dB		44		
Maximum output power (AVDD=1.8V)	P_O	R_L=16Ω, THD+N=1%, CPMOD=0	Av= 0dB	-	21	-	mW
			Av= +3dB		35		
			Av= +6dB		35		
		R_L=32Ω, THD+N=1%, CPMOD=0	Av= 0dB		10		
			Av= +3dB		20		
			Av= +6dB		20		
Total harmonic distortion	THD+N	R_L=16Ω, P_O=5mW, BW=20kHz	ECO_MODE= “0”	-	0.015	-	%
			ECO_MODE= “1”		0.030		
		R_L=32Ω, P_O=5mW, BW=20kHz	ECO_MODE= “0”	-	0.010	-	%
			ECO_MODE= “1”		0.025		
S/N ratio	SNR	BW=20kHz, A-weighted Filter		-	97	-	dB
PSRR	PSRR	SPVDD	217Hz	-	95	-	dB
			1kHz		90		
			20kHz		80		
Output offset voltage	Vo	MUTE (See Note 2.)		-	±0.1	-	mV
Frequency characteristics	Fres	C_{IN}=0.47μF, 100Hz to 20kHz		-3	-	0.3	dB
Channel separation	CS	1kHz, BW=20kHz		-	85	-	dB
Gain error between channels				-	±0.2	-	dB
Drive capacitance	C_L			-	100	-	pF
Charge pump frequency	F_{CP}			-	333	-	kHz

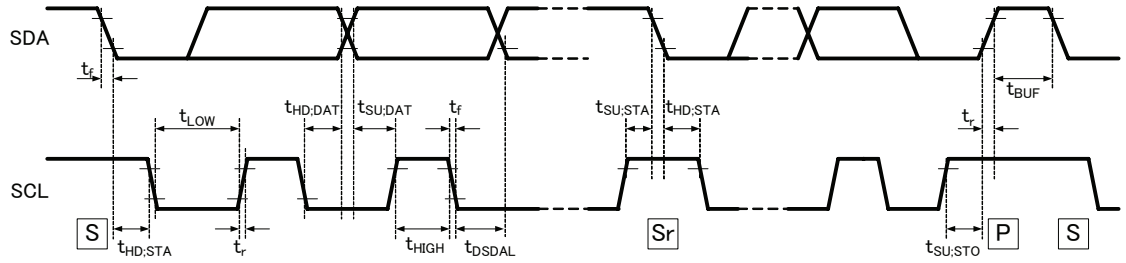
Note 1: All the analog characteristics were measured by using our evaluation board. Depending upon pattern layout etc., characteristics may vary.

Note 2: Headphone Attenuator “MUTE”

● I^2C Timing

The device supports both high-speed and standard modes.

The figure below shows the timing chart common to both modes:



S: start condition, Sr: repetitive start condition, P: stop condition

* The I^2C characteristics are measured under the following conditions:

Input conditions: $V_{IH} = 0.80 \times V_{AVDD}$, $V_{IL} = 0.10 \times V_{AVDD}$

Measurement point: $V_{IH} = 0.70 \times V_{AVDD}$, $V_{IL} = 0.30 \times V_{AVDD}$

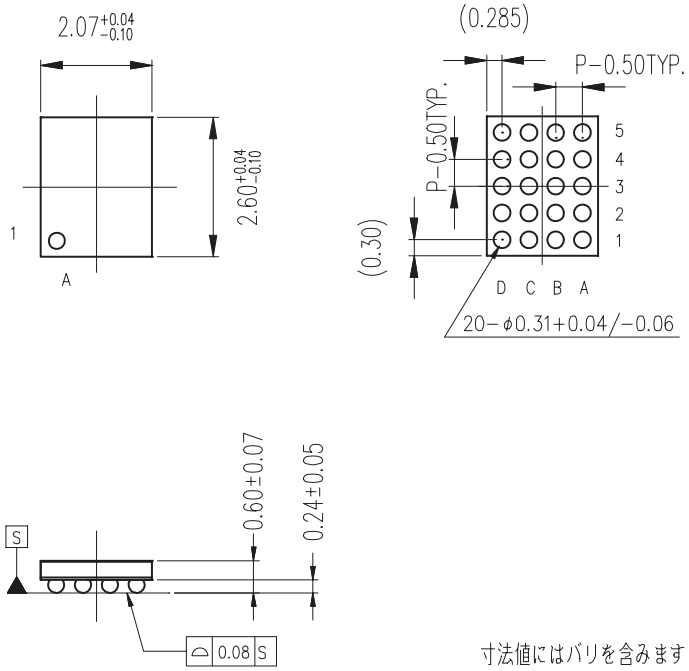
$V_{OH} = 0.70 \times V_{AVDD}$, $V_{OL} = 0.30 \times V_{AVDD}$

(SPVDD=2.8 to 5.25V, AVDD=1.65 to 2.86V, SPGND=GND=0V, T_A= -40ºC to 85ºC, unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input conditions						
SCL input clock frequency	f_{SCL}	Standard mode	0	-	100	kHz
		High-speed mode			400	
[START] condition hold time	$t_{HD;STA}$		0.6	-	-	µs
SCL input clock “L” time	t_{LOW}		1.3	-	-	µs
SCL input clock “H” time	t_{HIGH}		0.6	-	-	µs
Repetitive [START] condition setup time	$t_{SU;STA}$		0.6	-	-	µs
Data input hold time	$t_{HD;DAT}$		0	-	-	ns
Data input setup time	$t_{SU;DAT}$		100	-	-	ns
SDA, SCL input rise time	t_r	Standard mode	-	-	1000	ns
		High-speed mode			300	
SDA, SCL input fall time	t_f		-	-	300	ns
[STOP] condition setup time	$t_{SU;STO}$		0.6	-	-	µs
Bus free time between [STOP] and [START] conditions	t_{BUF}		1.3	-	-	µs
Capacitive load of each bus line	C_b		-	-	400	pF
Output conditions						
SDA “L” output delay time	t_{DSDAL}		-	-	1.15	µs
Data output hold time	$T_{HD;DAT}$		0	-	0.9	µs

■ Package Information

U-PK20PP2-07-1



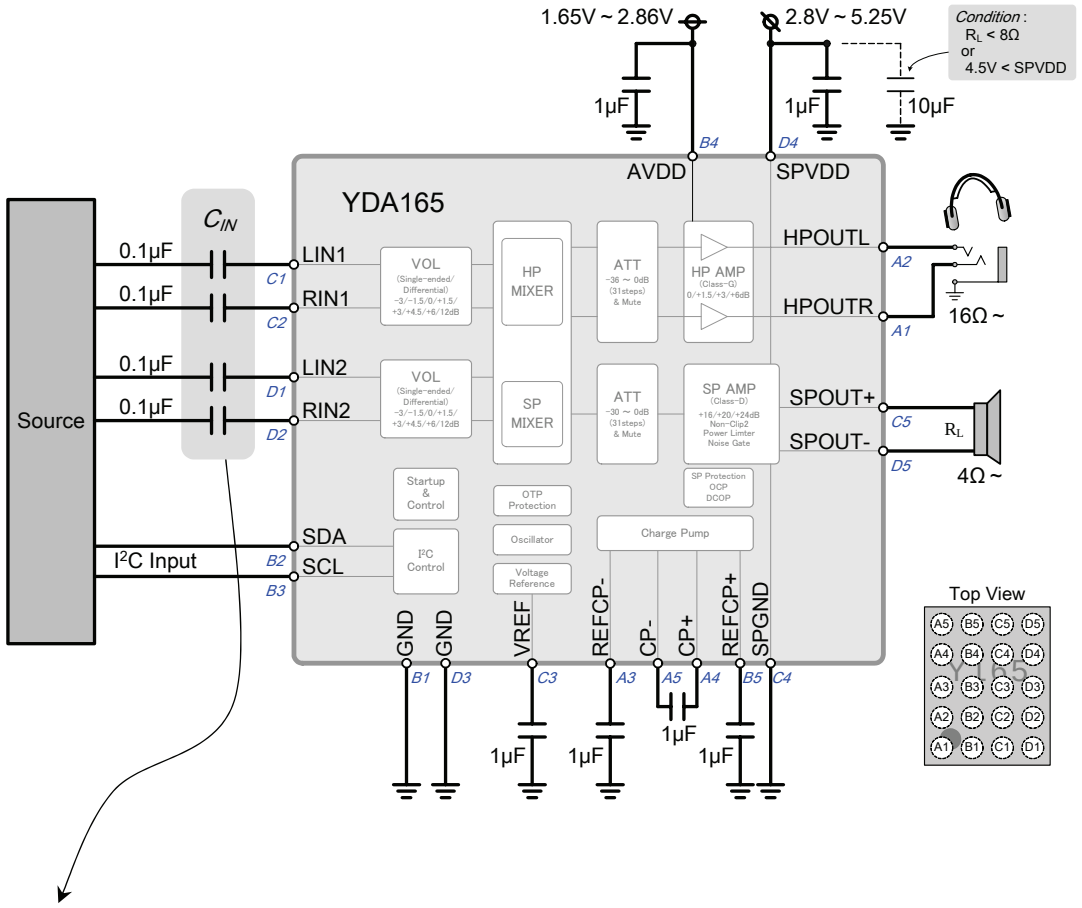
寸法値にはバリを含みます。
Dimensions include burr.
括弧内の寸法は参考値とします。
The value parenthesized is not specified.

UNIT: mm

注） 1. 表面実装LSIは、保管条件、および、半田付けについての特別な配慮が必要です。
2. 組立工場により、寸法や形状などが異なる場合があります。
詳しくはヤマハ代理店までお問い合わせください。

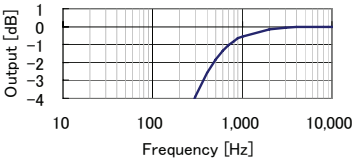
Note: 1. Special attention needs to be paid to the storage conditions and soldering method of the surface mount IC.
2. Dimension, form, etc. may differ depending on assembly plants.
For details, please contact your local Yamaha agent.

■ Typical Application Example



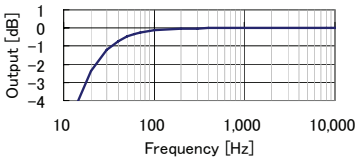
e.g., C_{IN} for the speaker
(common to Single-ended Input and Differential Input)

C_{IN}=0.022μF, VOL=0dB : $fc = \frac{1}{2\pi \times 20k\Omega \times 0.022\mu F} = 362Hz$



e.g., C_{IN} for the headphone
(common to Single-ended Input and Differential Input)

C_{IN}=0.47μF, VOL=0dB : $fc = \frac{1}{2\pi \times 20k\Omega \times 0.47\mu F} = 17Hz$



1. The following condition must be satisfied: SPVDD ≥ AVDD
2. Use a 1.0μF ceramic bypass capacitor for the AVDD pin and place it as closely to the device as possible.
3. Use a 1.0μF or higher ceramic bypass capacitor for the SPVDD pin; however, when using a lower R_L than 8 ohms or when using a higher SPVDD voltage than 4.5V, add a low ESR capacitor of 10μF or higher to the pin.
4. Connect a low ESR capacitor of 1μF between the CP+ and CP- pins, and the REFCP+ and REFCP- pins.
5. Use a DC-cut capacitor of 0.47μF or less for pop noise reduction.

PRECAUTIONS AND INSTRUCTIONS FOR SAFETY

	WARNING
Prohibited	Do not use the device under stresses beyond those listed in Absolute Maximum Ratings. Such stresses may become causes of breakdown, damages, or deterioration, causing explosion or ignition, and this may lead to fire or personal injury.
Prohibited	Do not mount the device reversely or improperly and also do not connect a supply voltage in wrong polarity. Otherwise, this may cause current and/or power-consumption to exceed the absolute maximum ratings, causing personal injury due to explosion or ignition as well as causing breakdown, damages, or deterioration. And, do not use the device again that has been improperly mounted and powered once.
Prohibited	Do not short between pins. In particular, when different power supply pins, such as between high-voltage and low-voltage pins, are shorted, smoke, fire, or explosion may take place.
Instructions	As to devices capable of generating sound from its speaker outputs, please design with safety of your products and system in mind, such as the consequences of unusual speaker output due to a malfunction or failure. A speaker dissipates heat in a voice-coil by air flow accompanying vibration of a diaphragm. When a DC signal (several Hz or less) is input due to device failure, heat dissipation characteristics degrade rapidly, thereby leading to voice-coil burnout, smoking or ignition of the speaker even if it is used within the rated input value.

	CAUTION
Prohibited	Do not use Yamaha products in close proximity to burning materials, combustible substances, or inflammable materials, in order to prevent the spread of the fire caused by Yamaha products, and to prevent the smoke or fire of Yamaha products due to peripheral components.
Instructions	Generally, semiconductor products may malfunction and break down due to aging, degradation, etc. It is the responsibility of the designer to take actions such as safety design of products and the entire system and also fail-safe design according to applications, so as not to cause property damage and/or bodily injury due to malfunction and/or failure of semiconductor products.
Instructions	The built-in DSP may output the maximum amplitude waveform suddenly due to malfunction from disturbances etc. and this may cause damage to headphones, external amplifiers, and human body (the ear). Please pay attention to safety measures for device malfunction and failure both in product and system design.
Instructions	As semiconductor devices are not nonflammable, overcurrent or failure may cause smoke or fire. Therefore, products should be designed with safety in mind such as using overcurrent protection circuits to control the amount of current during operation and to shut off on failure.
Instructions	Products should be designed with fail safe in mind in case of malfunction of the built-in protection circuits. Note that the built-in protection circuits such as overcurrent protection circuit and high-temperature protection circuit do not always protect the internal circuits. In some cases, depending on usage or situations, such protection circuit may not work properly or the device itself may break down before the protection circuit kicks in.
Instructions	Use a robust power supply. The use of an unrobust power supply may lead to malfunctions of the protection circuit, causing device breakdown, personal injury due to explosion, or smoke or fire.
Instructions	Product's housing should be designed with the considerations of short-circuiting between pins of the mounted device due to foreign conductive substances (such as metal pins etc.). Moreover, the housing should be designed with spatter prevention etc. due to explosion or burning. Otherwise, the spattered substance may cause bodily injury.
Instructions	The device may be heated to a high temperature due to internal heat generation during operation. Therefore, please take care not to touch an operating device directly.

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