FEATURES

- Functionally compliant with ANSI X3T11 Fibre Channel physical and transmission protocol standards and IEEE 802.3Z Gigabit Ethernet Applications
- Transmitter incorporates phase-locked loop (PLL) providing clock synthesis from low-speed reference
- Receiver PLL configured for clock and data recovery
- 1250 and 1062 Mb/s operation
- 10-bit parallel TTL compatible interface
- 800mW typical power dissipation
- +3.3V power supply
- Low-jitter serial PECL compatible interface
- Lock detect
- Local loopback
- 64 PQFP package
- Fibre Channel framing performed by receiver
- Continuous downstream clocking from receiver
- Drives 30m of Twinax cable directly

APPLICATIONS

High-speed data communications

- Workstation
- Frame buffer
- Switched networks
- Data broadcast environments
- Proprietary extended backplanes
- RAID drives
- Mass storage devices

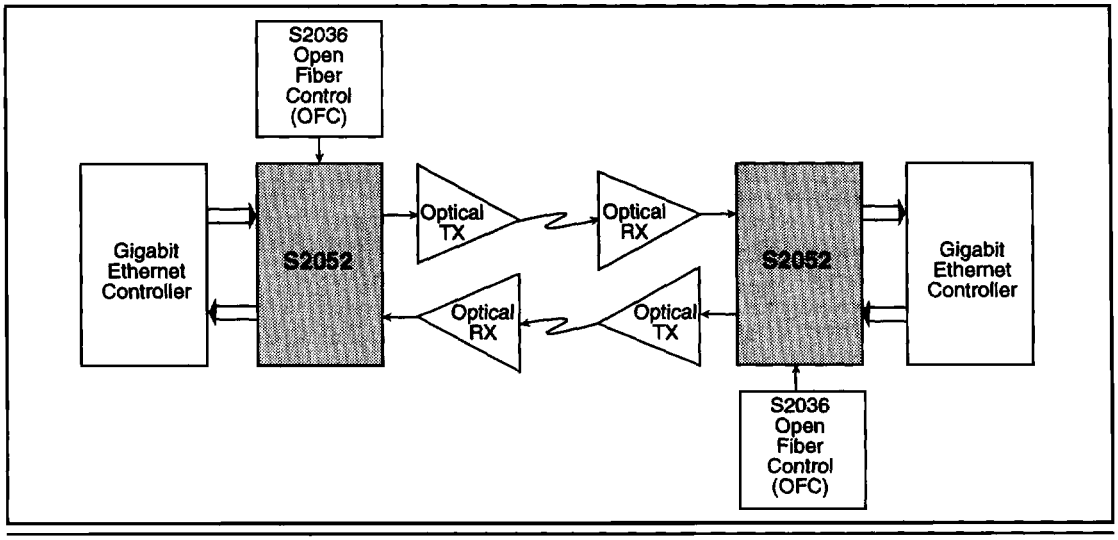
GENERAL DESCRIPTION

The S2052 transmitter and receiver chip is designed to perform high-speed serial data transmission over fiber optic or coaxial cable interfaces conforming to the requirements of the ANSI X3T11 Fibre Channel specification. The chip runs at 1250.0, and 1062.5 Mbit/s data rates with associated 10-bit data word.

The chip performs parallel-to-serial and serial-to-parallel conversion and framing for block-encoded data. The transmitter's on-chip PLL synthesizes the high-speed clock from a low-speed reference. The receiver's on-chip PLL synchronizes directly to incoming digital signal to receive the data stream. The transmitter and receiver each support differential PECL-compatible I/O for fiber optic component interfaces, to minimize crosstalk and maximize data integrity. Local loopback mode is provided for system diagnostics.

Figure 1 shows a typical configuration incorporating the chip, which is compatible with AMCC's S2036 Open Fiber Control (OFC) device.

Figure 1. System Block Diagram



S2052 OVERVIEW

The S2052 transmitter and receiver provide serialization and deserialization functions for block-encoded data to implement a Fibre Channel interface. Operation of the S2052 is straightforward, as depicted in Figure 2. The sequence of operations is as follows:

Transmitter
1. 10-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver
1. Clock and data recovery from serial input
2. Serial-to-parallel conversion
3. Frame detection
4. 10-bit parallel output

The 10-bit parallel data handled by the S2052 device should be from a DC-balanced encoding scheme, such as the 8B/10B transmission code, in which information to be transmitted is encoded 8 bits at a time into 10-bit transmission characters[1], and be compliant with ANSI X3.230 FC-PH (Fibre Channel Physical and Signaling Interface).

Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figure 4. A block diagram showing the basic chip operation is shown in Figure 3.

Loopback

Local loopback is supported by the chip, and provides a capability for performing offline testing of the interface to ensure the integrity of the serial channel before enabling the transmission medium. It also allows for system diagnostics.

Figure 2. Interface Diagram

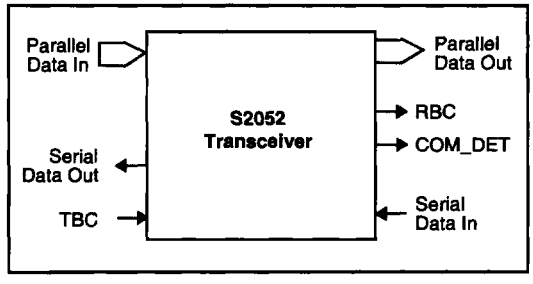


Figure 3. Functional Block Diagram