



NEC Electronics Inc.

μPD488130, 488170
18-Megabit Rambus DRAM

Advance Information

October 1992

Description

The μPD488130 and μPD488170 Rambus™ DRAMs (RDRAM™) are extremely-high-speed dynamic CMOS RAMs organized as 2M words by 8 or 9 bits. Using its sense amplifiers as a cache, the RDRAM bursts up to 256 bytes at a 500-megabyte/second rate. The RDRAM is ideal for main memory and graphics applications that require high performance at low cost.

Features

- Rambus interface
 - 500-megabits/second peak bandwidth per RDRAM per bus
 - Innovative, small-signal-swing interface
 - Synchronous, block-oriented protocol
 - Direct interface to Rambus ASICs, MPUs, and peripherals
- 28 ns from end of read request to first byte; 2 ns/byte thereafter
- Caches in RDRAM contribute to low latency
- Entirely self-contained—no external memory controller required
- Conventional plastic surface-mount package and PC board technology
- On-board registers for flexible addressing

System Benefits

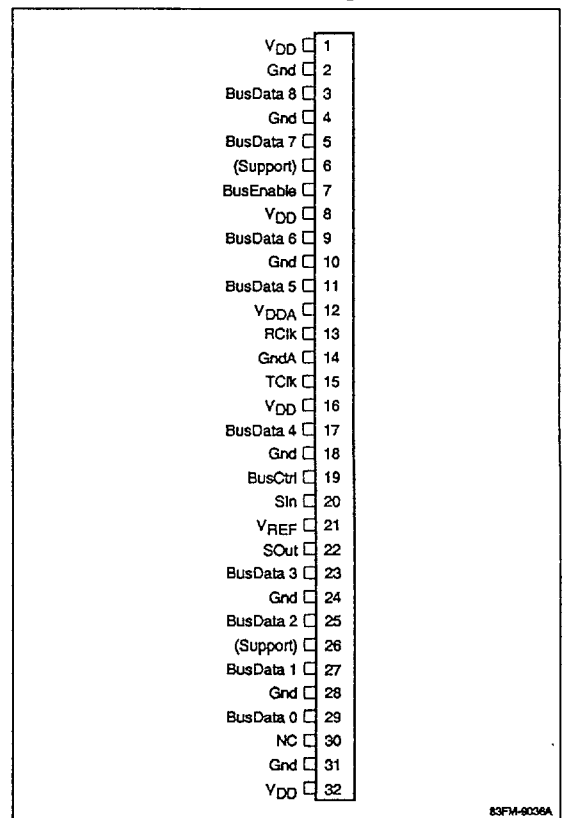
- Can eliminate second-level caches in uniprocessor designs
- Vastly improves graphics at lower cost
- Decreases parts count; eliminates memory controller, buffers, address decoders, etc.
- Same pinout as a 4.5-megabit RDRAM
- Incremental memory granularity is 2 megabits
- Alleviates need for expensive multichip modules at high system clock rates
- Systems can be modular; faster MPUs and larger Rambus memories can be installed without changing board layout or logic design
- Write-per-bit function available

Ordering Information

Part Number	Organization	Package
μPD488130	2M x 8 bits	32-pin SVP
μPD488170	2M x 9 bits	

Pin Configuration

32-Pin Surface Vertical Package



83FM-9036A

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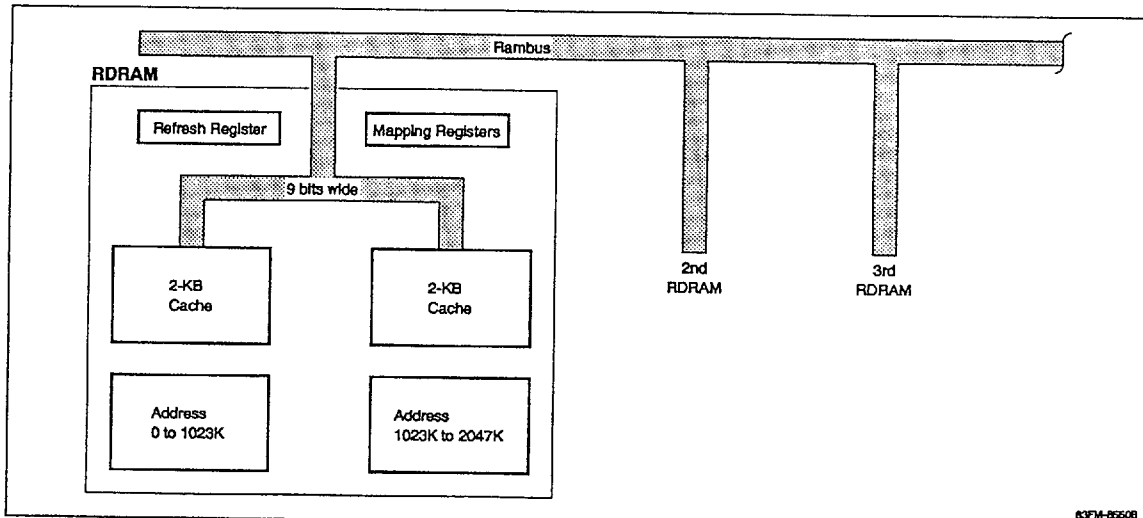
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Pin Identification

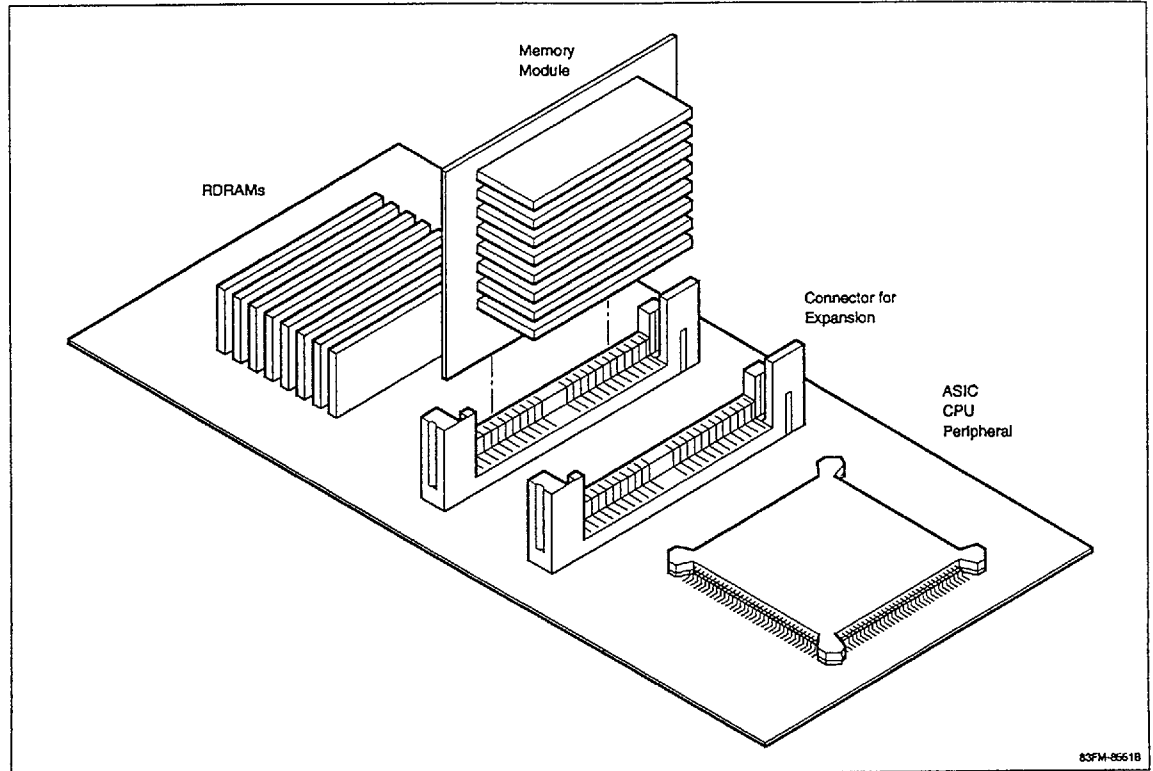
Signal	I/O	Description
BusData0 - BusData8	I/O	Bus data for request, write, and read protocols. These are low-swing signals referenced to V _{REF} . The data lines carry the request packet with the address, operation codes, and the count of the bytes to be transferred.
RClk	In	Receive clock. RClk is aligned with incoming request and write data packets. The clock is completely synchronized with the request and data sent out on the Rambus interface.
TClk	Out	Transmit clock. TClk is aligned with the data being sent out on reads as well as the acknowledge packets. The clock is a low-swing signal referenced to V _{REF} .
V _{REF}	In	This is the logic threshold voltage for low-swing signals.
BusCtrl	In	Control signal to frame packets, transmit opcode, and acknowledge requests. Signal is active low.
BusEnable	In	Control signal to enable the bus. The signal is pulsed to power up the bus. Long assertions of this active low signal will reset all devices on the bus.
V _{DD} , V _{DDA}		+3-volt power supply. V _{DDA} is a separate supply for clock receivers.
Gnd, GndA		Circuit ground. GndA is a separate ground for clock receivers.
SIn, SOut	I/O	Reset daisy chain. CMOS levels and active high.

Block Diagram



63FM-85508

Assembly Drawing



Protocol

The Rambus interface uses a simple, synchronous, block-oriented protocol. This is a transaction-based protocol with the data transport time determined by the master. RDRAMs do not arbitrate for the bus, eliminating the need for arbitration in single-master systems.

A Rambus device must be initialized before it takes part in bus transactions. One device, the configuration master, initializes the others. The configuration master begins by assigning a unique device identification (ID) to each device. Then, the configuration master polls each device's type register and initializes all control registers as appropriate to the number and types of devices.

A full initialization continues by assigning device ID values using the SIn and SOut pins. SIn and SOut are normal CMOS signals used only during configuration and power down. SOut of the configuration master connects to SIn of the first device and so on through

each bus device in daisy chain fashion. SOut of the last device connects to SIn of the configuration master.

Transactions

Transactions are composed of three packets: request, acknowledge, and data. Each packet is a sequence of bits presented continuously on a set of wires. Determining the point in time at which each packet begins is referred to as framing. The framing of the acknowledge and data packets of a transaction is referenced to the end of the request packet. To initiate a bus transfer, a master sends out a request packet that contains an address and control information.

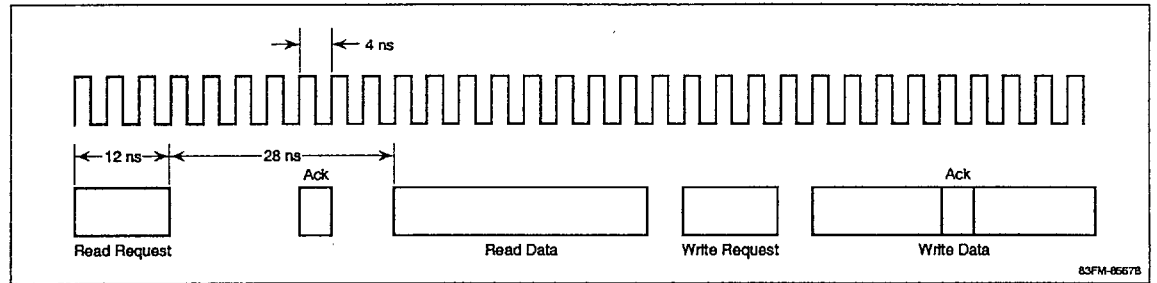
All RDRAM devices constantly monitor the bus looking for requests. When a request is received, they extract the requested device identification, determine whether it matches their own device identification, and, if so, drive an acknowledge packet back to the master.

The RDRAM also drives the data back to the master in the case of a read request or accepts the data from the master in the case of a write request. Also specified in the request packet is the number of bytes to transfer (4-256 bytes), making this a block-oriented protocol. The length of response time from a request to either an acknowledgment or an operation is always known and is based upon the clock frequency. Figure 1 is an example of a 16-byte read followed by a 16-byte write.

Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Receive clock frequency	RClk	100	250	MHz
Transmit clock frequency	TClk	100	250	MHz

Figure 1. Data Transactions



Recommended DC Operating Conditions

Parameter	Symbol	Min	Max	Unit
Junction operating temperature	T_j	0	100	°C
Supply voltage	V_{DD}, V_{DDA}	4.5	5.5	V
TTL input voltage, low	V_{IL}, TTL	-1.0	0.8	V
TTL input voltage, high	V_{IH}, TTL	2.0	$V_{DD} + 1.0$	V
TTL output voltage	V_{OL}, TTL	0.0	0.4	V
TTL output voltage, high	V_{OH}, TTL	2.4	V_{DD}	V
Termination voltage	V_{TERM}	2.2	2.7	V
Reference voltage	V_{REF}	1.7	2.4	V
Input voltage, high	V_{IH}	$V_{REF} + 0.2$		V
Input voltage, low	V_{IL}		$V_{REF} - 0.2$	V
Output voltage, high	V_{OH}	$V_{REF} + 0.3$		V
Output voltage, low	V_{OL}		$V_{REF} - 0.3$	V
Output current, (programmable)	I_{OL}	-35	-10	mA
Output current, high	I_{OH}	-10	10	μA
V_{REF} current	I_{REF}	-10	10	μA

Figure 2. Read Hit Timing Diagram

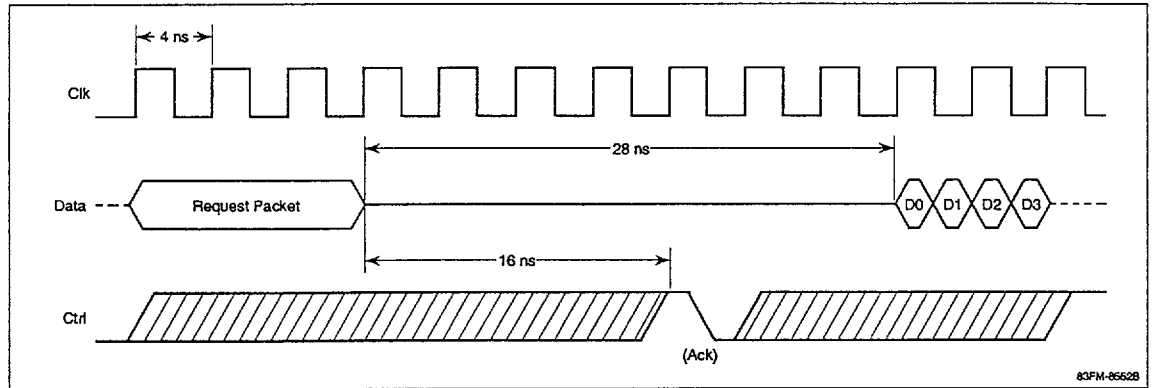


Figure 3. Write Hit Timing Diagram

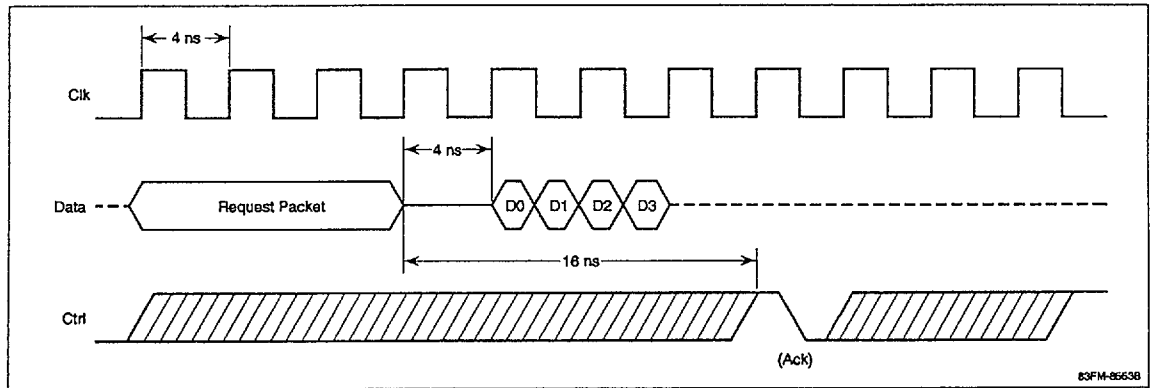


Figure 4. Read Miss Timing Diagram

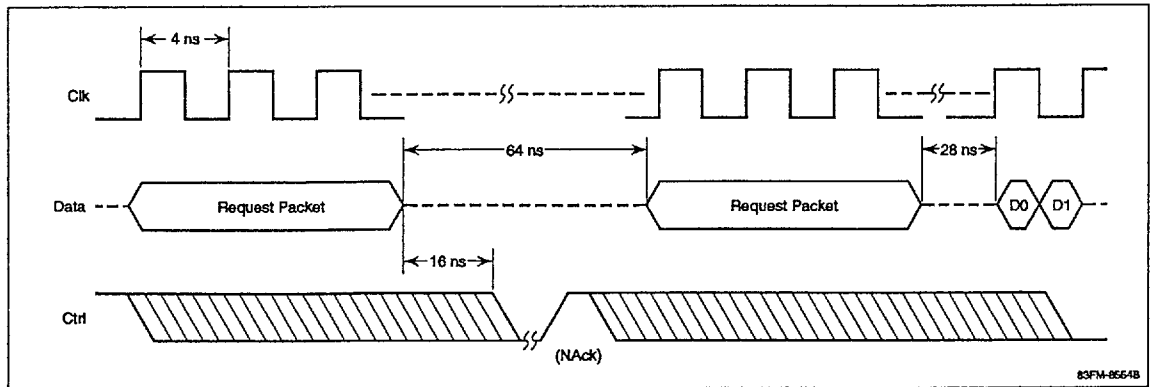
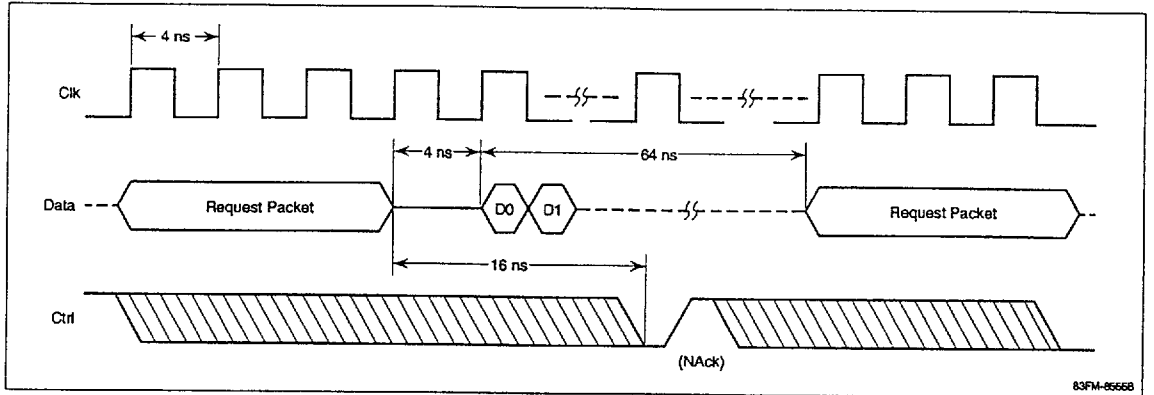


Figure 5. Write Miss Timing Diagram



Package Drawing

32-Pin Surface Vertical Package

