AN1833, AN1833S

Low Noise, High Slew Rate Operational Amplifiers

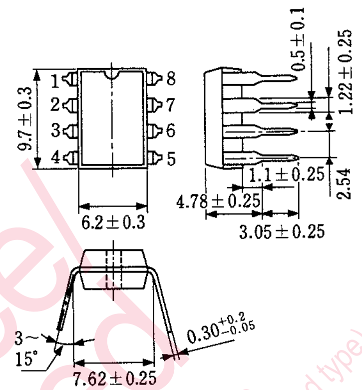
■ Outline

The AN1833 and the AN1833S are low noise, high slew rate type dual operational amplifiers with phase compensation circuits built-in. They have wide band and high stability, and suited for application to various electronic circuits such as active filters and audio preamplifiers.

■ Features

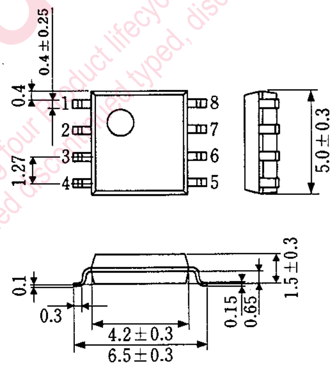
- Phase compensation circuit
- High gain : $G_V = 110dB$ typ.
- Low noise : $V_{ni} = 0.9\mu Vrms$ typ.
- High slew rate : $SR = 6V/\mu s$ typ.
- High stability

AN1833 Unit : mm



8-Lead DIL Plastic Package

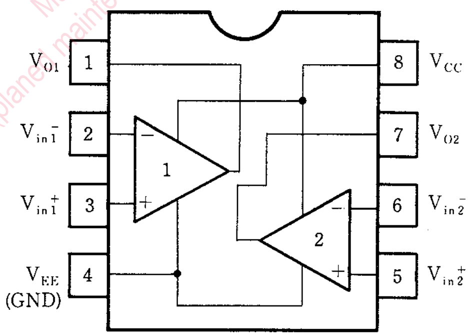
AN1833S Unit : mm



8-Lead PANAFLAT Package(SO-8D)

■ Block Diagram

AN1833
AN1833S



Panasonic

■ Pin

Pin No.	Pin Name
1	Ch. 1 Output
2	Ch. 1 Invert Input
3	Ch. 1 Non Invert Input
4	V_{EE} (GND)
5	Ch. 2 Non Invert Input
6	Ch. 2 Invert Input
7	Ch. 2 Output
8	Vcc

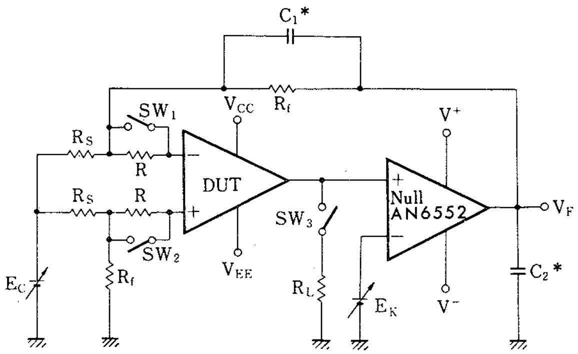
■ Absolute Maximum Ratings (Ta=25℃)

Item		Symbol	Rating	Unit
Voltage	Supply Voltage	V_{CC}	±18	V
	Differential Input Voltage	V_{ID}	±30	V
	Common-Mode Input Voltage	V_{ICM}	±15	V
Power Dissipation	AN1833	P_D	500	mW
	AN1833S		360	
Operating Ambient Temperature		T_{opr}	−20～+75	℃
Storage Temperature	AN1833	T_{stg}	−55～+150	℃
	AN1833S		−55～+125	

■ Electrical Characteristics (V_{CC}=15V, V_{EE}=−15V, Ta=25℃)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Input Offset Voltage	$V_{I(offset)}$	1	R_S≦10kΩ		0.3	5	mV
Input Offset Current	I_{IO}	1			5	200	nA
Input Bias Current	I_{Bias}	1			300	1000	nA
Voltage Gain	G_V	1		90	110		dB
Maximum Output Voltage	$V_{O(max.)}$	2	R_L≧10kΩ	±12	±13.5		V
Maximum Output Voltage	$V_{O(max.)}$	2	R_L≧2kΩ	±10	±13.4		V
Common-Mode Input Voltage Width	V_{CM}	3		±12	±14		V
Common-Mode Rejection Ratio	CMR	1		80	100		dB
Supply Voltage Rejection Ratio	SVR	1			10	100	dB
Power Consumption	P_C	4	R_L=∞		150	240	mW
Slew Rate	SR	5	R_L≧2kΩ		6		V/μs
Unity-gain Band Width	$f_{(T)}$	6	A_V=1		7		MHz
Equivalent Input Noise Voltage	V_{ni}	7	R_S=1kΩ, DIN/AUDIO		0.9		μV_{rms}

Test Circuit 1 ($V_{I(offset)}$, I_{IO}, I_{Bias}, G_V, CMR, SVR)



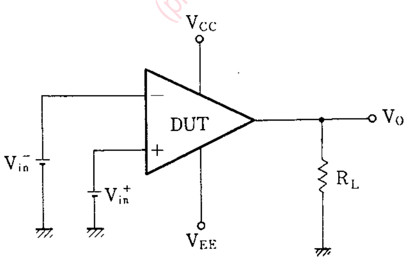
$R_S = 50\,\Omega$
$R = 10\,k\Omega$
$R_f = 20\,k\Omega$
$R_L = 2\,k\Omega$
$V_{CC} = 15\,V$
$V_{EE} = -15\,V$
$V^+ = 15\,V$
$V^- = -15\,V$

* C_1 and C_2 are capacitors for the prevention of oscillation.

Item	Measurement Conditions
Input Offset Voltage	V_{F1} is measured with the SW_1, SW_2 and SW_3 set to OFF and $E_C = E_K = 0V$. Can be given by $V_{I(offset)} = \frac{V_{F1}}{400}$ (V)
Input Offset Current	V_{F2} is measured with the SW_1 and SW_2 set to ON, the SW_3 set to OFF and $E_C = E_K = 0V$. Can be given by $I_{IO} = \frac{\lvert V_{F2} - V_{F1} \rvert}{4 \times 10^6}$ (A)
Input Bias Current	V_{F3} is measured with the SW_3 set to OFF, $E_C = E_K = 0V$, the SW_1 set to ON and the SW_2 set to OFF. V_{F4} is measured with the SW_1 and SW_2 reversed. Can be given by $I_{Bias} = \frac{\lvert V_{F3} - V_{F4} \rvert}{8 \times 10^6}$ (A)
Voltage Gain	V_{F5} is measured with the SW_1' SW_2 and SW_3 set to ON, $E_C = 0V$ and $E_K = 10V$. $V_F'_5$ is measured with $E_K = -10V$. Can be given by $G_V = 20\log\left(\left\lvert \frac{8000}{\lvert V_{F5} - V_{F5}' \rvert} \right\rvert\right)$
Common-Mode Rejection Ratio	V_{F6} is measured with both the SW_1 and SW_2 set to ON, the SW_3 set to OFF, $E_K = 0V$ and $E_C = 5V$. V_{F6}'is measured with $E_C = -5V$. Can be given by $CMR = 20\log\left(\frac{4000}{\lvert V_{F6} - V_{F6}' \rvert}\right)$
Supply Voltage Rejection Ratio I	V_{F7} is measured with both the SW_1 and SW_2 set to ON, the SW_3 set to OFF, $E_K = E_C = 0V$ and $V_{CC} = 10V$. Can be given by $SVR(+) = \frac{\lvert V_{F7} - V_{F2} \rvert}{2 \times 10^3}$
Supply Voltage Rejection Ratio II	V_{F8} is measured with both the SW_1 and SW_2 set to ON, the SW_3 set to OFF, $E_K = E_C = 0V$ and $V_{EE} = -10V$. Can be given by $SVR(-) = \frac{\lvert V_{F8} - V_{F2} \rvert}{2 \times 10^3}$

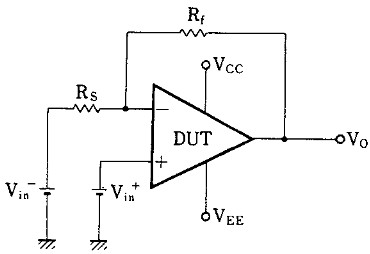
Note) When not specified in the above table, $V_{CC} = 15V$ and $V_{EE} = -15V$.

Test Circuit 2 ($V_{O(max.)}$)



$V_{CC} = 15\,V$
$V_{EE} = -15\,V$
$R_L = 2\,k\Omega$ or $10\,k\Omega$
$V_{in}^- = 0\,V$ or $1\,V$
$V_{in}^+ = 1\,V$ or $0\,V$

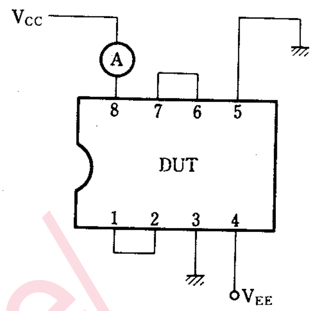
Test Circuit 3 (V_{CM})



$V_{CC}=15\,V$
$V_{EE}=-15\,V$
$R_S=200\,\Omega$
$R_f=2\,k\Omega$

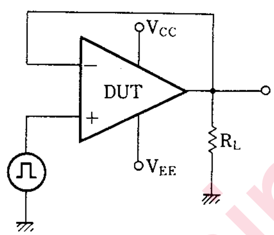
Note) Apply a voltage of $|V_{in}^+|>12V$ and check $V_O=V_{in}^+ + \frac{R_f}{R_s}(V_{in}^+ - V_{in}^-)$

Test Circuit 4 (P_C)



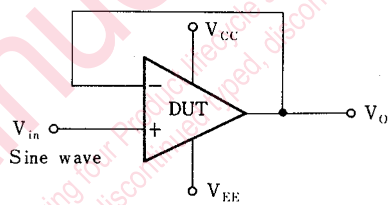
$V_{CC}=15V$
$V_{EE}=-15V$

Test Circuit 5 (SR)

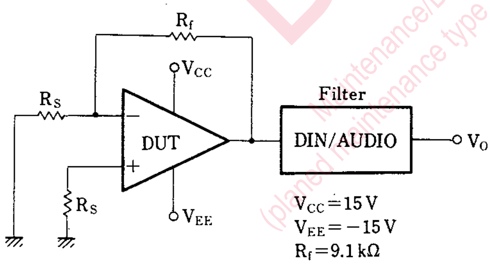


$V_{CC}=15\,V$
$V_{EE}=-15\,V$
$R_L=2\,k\Omega$

Test Circuit 6 ($f_{(T)}$)



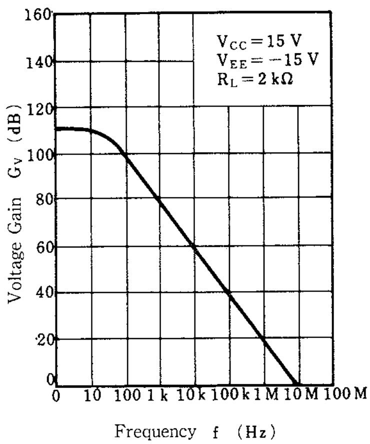
Test Circuit 7 (V_{ni})



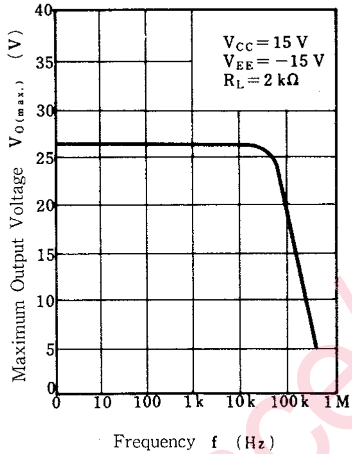
$V_{CC}=15\,V$
$V_{EE}=-15\,V$
$R_f=9.1\,k\Omega$
$R_S=1\,k\Omega$

Note) A noise voltage referred to Input: $V_{ni}=\frac{V_O}{(1+R_f/R_s)}$ (V) is given.

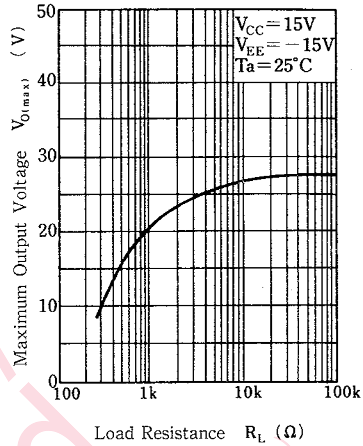
$G_V - f$



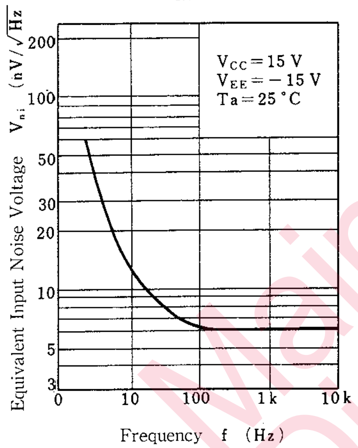
$V_{O(max.)} - f$



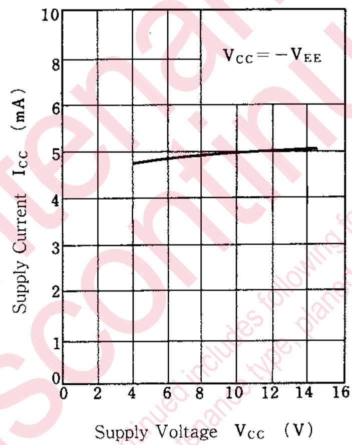
$V_{O(max.)} - R_L$



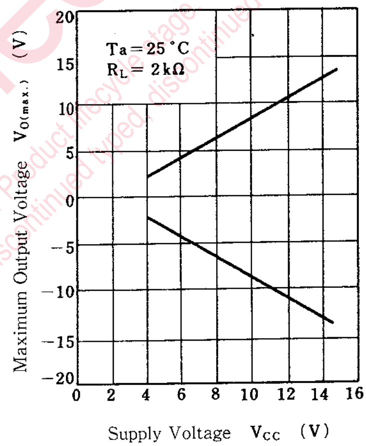
$V_{ni} - f$



$I_{CC} - V_{CC}$

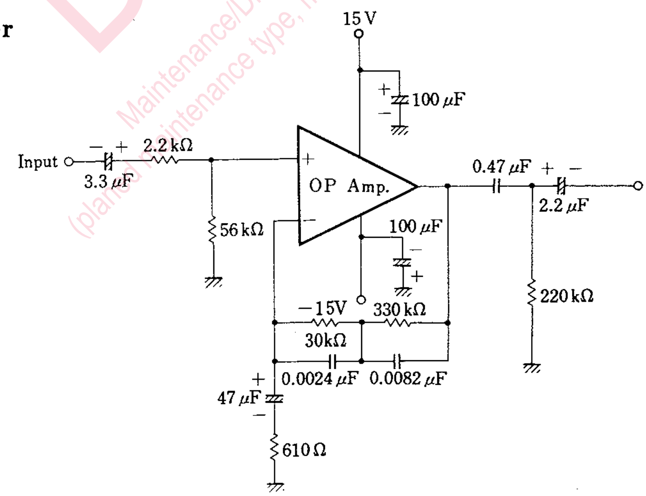


$V_{O(max.)} - V_{CC}$



■ Application Circuit

RIAA Amplifier



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