

# 8051AH/8031AH

Single-Chip 8-Bit Microcomputer

## DISTINCTIVE CHARACTERISTICS

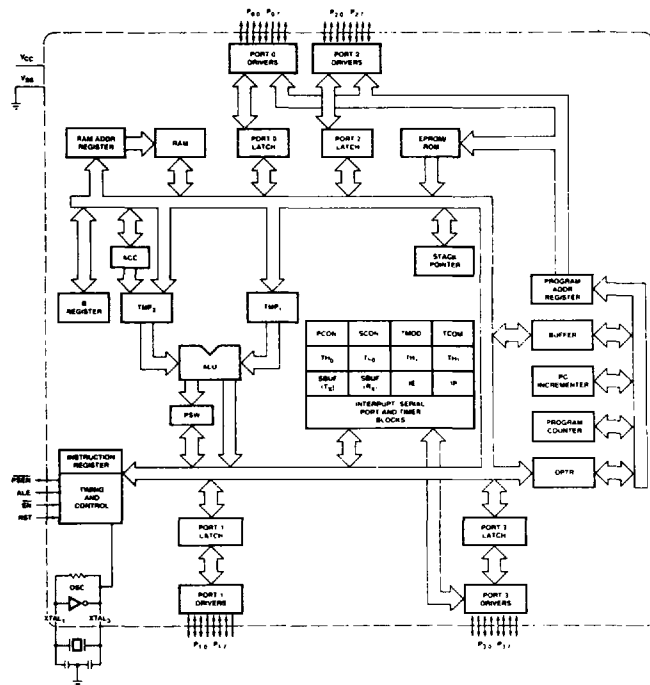
- 4K x 8 ROM, 128 x 8 RAM
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters, 5 interrupt sources
- High-Performance full-duplex serial channel
- Boolean processor, cycle multiply and divide
- External memory expandable to 128K bytes
- Most instructions execute in 1 $\mu$ s
- 4 $\mu$ s multiply and divide
- 8031AH
  - Control oriented CPU with RAM and I/O
- 8051AH
  - An 8031AH with factory mask-programmable ROM
- 100mA typical supply current

## GENERAL DESCRIPTION

The 8051AH/8031AH are members of a family of advanced single-chip microcomputers. The 8051AH contains 4K x 8 read-only program memory; 128 x 8 RAM; 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multiprocessor communications, I/O expansion, or full duplex UART; and on-chip oscillator and clock circuits. The 8031AH is identical, except that it lacks the program memory. For systems that require extra capability, the 8051AH can be expanded using standard TTL compatible memories and the byte oriented 8080 and 8085 peripherals.

The 8051AH microcomputer, like its 8048 predecessor, is efficient both as a controller and as a Boolean processor. The 8051AH has extensive facilities for binary and BCD arithmetic and excels in bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12MHz crystal, 58% of the instructions execute in 1 $\mu$ s, 40% in 2 $\mu$ s, and multiply and divide require only 4 $\mu$ s. Among the many instructions added to the standard 8048 instruction set are multiply, divide, subtract, and compare.

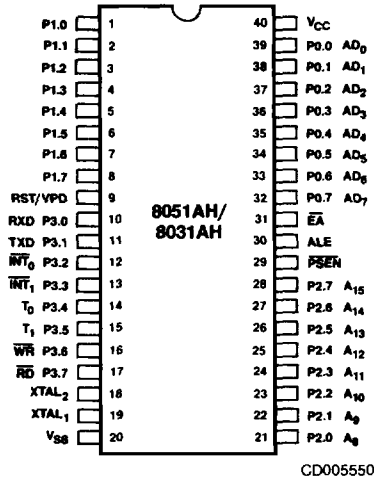
## BLOCK DIAGRAM



BD003780

Figure 1.

**CONNECTION DIAGRAM  
Top View  
D-40, P-40**



**SURFACE MOUNT PINOUT**

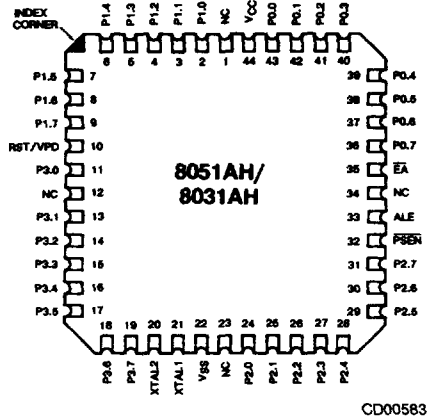


Figure 2.

**LOGIC SYMBOL**

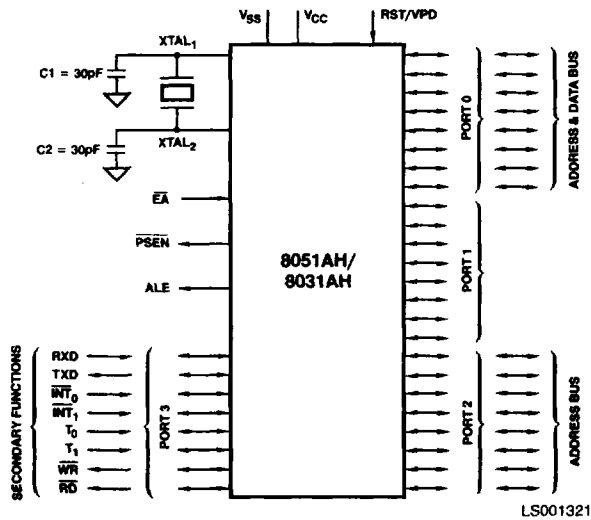
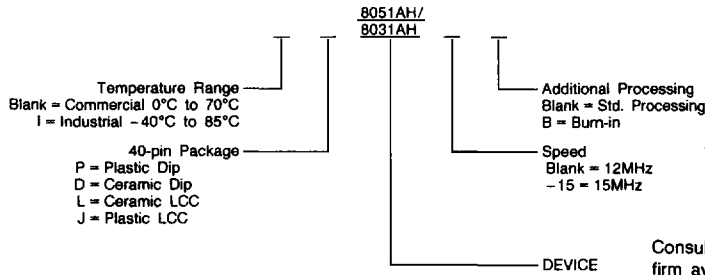


Figure 3.

## ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



Valid Combinations			
8031AH			P, D, IP, ID, L
8031AH	15		P, D, IP, ID, L
8031AH		B	P, D, IP, ID, L
8031AH	15	B	P, D, IP, ID, L
8051AH			P, D, IP, ID, L
8051AH		B	P, D, IP, ID, L

### Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, check for newly released valid combinations and/or obtain additional data on AMD's standard military grade product.

## PIN DESCRIPTION

Name	Description
V <sub>SS</sub>	Circuit ground potential.
V <sub>CC</sub>	+5V power supply during operation.
PORT 0	Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
PORT 1	Port 1 is an 8-bit quasi-bidirectional I/O port with internal pull-ups. It is also used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads.
PORT 2	Port 2 is an 8-bit quasi-bidirectional I/O port with internal pull-ups. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.
PORT 3	Port 3 is an 8-bit quasi-bidirectional I/O port with internal pull-ups. It also contains the interrupt, timer, serial port, and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. The secondary functions are assigned to the pins of Port 3, as follows: <ul style="list-style-type: none"> <li>- RXD/Data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous).</li> <li>- TXD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous).</li> <li>- <math>\overline{INT}_0</math> (P3.2). Interrupt 0 input or gate control input for counter 0.</li> <li>- <math>\overline{INT}_1</math> (P3.3). Interrupt 1 input or gate control input for counter 1.</li> <li>- T<sub>0</sub> (P3.4). Input to counter 0.</li> <li>- T<sub>1</sub> (P3.5). Input to counter 1.</li> <li>- <math>\overline{WR}</math> (P3.6). The write control signal latches the data byte from Port 0 into the External Data Memory.</li> <li>- <math>\overline{RD}</math> (P3.7). The read control signal enables External Data Memory to Port 0.</li> </ul>
RST/V <sub>PD</sub>	A high level on this pin resets the 8051AH. If V <sub>PD</sub> is held within its spec (approximately +5V) while V <sub>CC</sub> drops below spec, V <sub>PD</sub> will provide standby power to the RAM. When V <sub>PD</sub> is LOW, the RAM's current is drawn from V <sub>CC</sub> . A small external pull-down resistor ( $\approx 8.2k\Omega$ ) permits power-on reset using a capacitor connected to V <sub>CC</sub> .
ALE	Address Latch Enable output used for latching the low order byte of address during access to external memory. It is activated every six oscillator periods, except during an external data memory access at which time one ALE pulse is skipped. ALE can sink/source eight LS TTL inputs.
PSEN	The Program Store Enable output is a control signal that enables the external Program Memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
E $\overline{A}$	When held at a TTL high level, the 8051AH executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the 8051AH fetches all instructions from external Program Memory. Do not float E $\overline{A}$ during normal operation.
XTAL <sub>1</sub>	Input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to V <sub>SS</sub> when external source is used on XTAL <sub>2</sub> .
XTAL <sub>2</sub>	Output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature ..... -65 to +150°C  
 Voltage on Any Pin  
 with Respect to Ground ..... -0.5 to +7.0V  
 Power Dissipation ..... 1W

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

**OPERATING RANGES**

Part Number	Ambient Temperature	V <sub>CC</sub>	V <sub>SS</sub>
<b>Commercial</b>			
D8051AH D8031AH P8051AH P8031AH	0°C to 70°C	5V ± 10%	0V
<b>Industrial</b>			
ID8051AH ID8031AH IP8051AH IP8031AH	-40°C to 85°C	5V ± 10%	0V
<b>Commercial</b>			
L8031AH J8031AH L8051AH J8051AH	0°C to 70°C	5V ± 10%	0V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

**DC CHARACTERISTICS** T<sub>A</sub> = 0 to 70°C; V<sub>CC</sub> = 5V ± 10%; V<sub>SS</sub> = 0V)

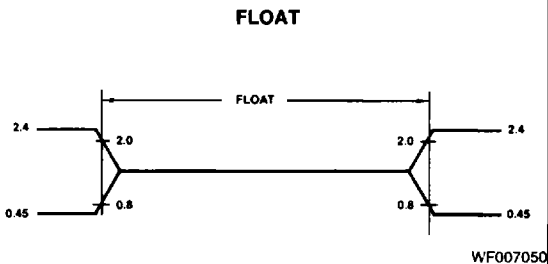
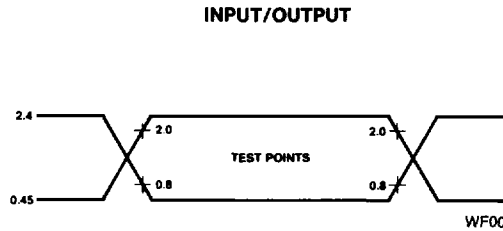
Parameters	Description	Test Conditions	Min	Typ	Max	Units
V <sub>IL</sub>	Input Low Voltage		-0.5		0.8	V
V <sub>IH</sub>	Input High Voltage (Except RST/V <sub>PD</sub> and XTAL <sub>2</sub> )		2.0		V <sub>CC</sub> +0.5	V
V <sub>IH1</sub>	Input High Voltage to RST/V <sub>PD</sub> for Reset, XTAL <sub>2</sub>	XTAL <sub>1</sub> to V <sub>SS</sub>	2.5		V <sub>CC</sub> +0.5	V
V <sub>PD</sub>	Power Down Voltage to RST/V <sub>PD</sub>	V <sub>CC</sub> = 0V	4.5		5.5	V
V <sub>OL</sub>	Output Low Voltage, Ports 1, 2, 3 (Note 1)	I <sub>OL</sub> = 1.6mA			0.45	V
V <sub>OL1</sub>	Output Low Voltage, Port 0, ALE, PSEN (Note 1)	I <sub>OL</sub> = 3.2mA			0.45	V
V <sub>OH</sub>	Output High Voltage, Ports 1, 2, 3	I <sub>OH</sub> = -80µA	2.4			V
V <sub>OH1</sub>	Output High Voltage, Port 0, ALE, PSEN	I <sub>OH</sub> = -400µA	2.4			V
I <sub>IL</sub>	Logical 0 Input Current, Ports 1, 2, 3	V <sub>IL</sub> = 0.45V			-800	µA
I <sub>IL2</sub>	Logical 0 Input Current for XTAL <sub>2</sub>	XTAL <sub>1</sub> = V <sub>SS</sub> V <sub>IN</sub> = 0.45V			-2.5	mA
I <sub>IH1</sub>	Input High Current to RST/V <sub>PD</sub> for Reset	V <sub>IN</sub> = V <sub>CC</sub> - 1.5V			500	µA
I <sub>I</sub>	Input Leakage Current to Port 0, E <sub>A</sub>	0.45 < V <sub>IN</sub> < V <sub>CC</sub>			± 10	µA
I <sub>CC</sub>	Power Supply Current	All Outputs Disconnected		100	125	mA
I <sub>PD</sub>	Power Down Current	V <sub>CC</sub> = 0V			10	mA
C <sub>O</sub>	Capacitance of I/O Buffer	f <sub>c</sub> = 1MHz			10	pF

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Note: 1. V<sub>OL</sub> is degraded when the 8051AH rapidly discharges external capacitance. This AC noise is most pronounced during emission of address data. When using external memory, locate the latch or buffer as close to the 8051AH as possible.

Datum	Emitting Ports	Degraded I/O Lines	V <sub>OL</sub> (peak) (max)
Address	P2, P0	P1, P3	0.8V
Write Data	P0	P1, P3, ALE	0.8V

## SWITCHING TEST INPUT/OUTPUT AND FLOAT WAVEFORMS



AC testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0."  
 Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0."  
 For timing purposes, the float state is defined as the point at which a P<sub>0</sub> pin sinks 3.2mA or sources 400μA at the voltage test levels.

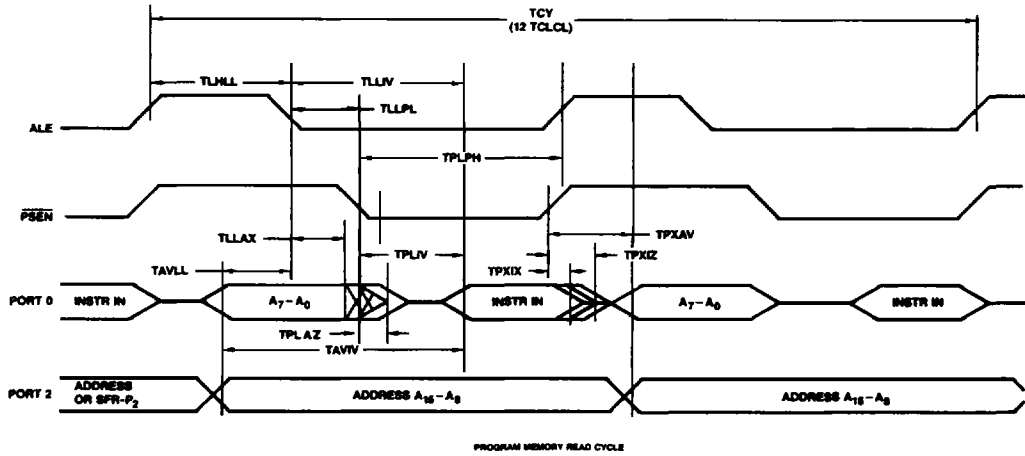
**SWITCHING CHARACTERISTICS** ( $T_A = 0$  to  $70^\circ\text{C}$ ;  $V_{CC} = 5V \pm 10\%$ ;  $V_{SS} = 0V$ ;  $C_L$  for Port 0, ALE and  $\overline{\text{PSEN}}$ ; Outputs = 100pF;  $C_L$  for All Other Outputs = 80pF)

Parameters	Description	12MHz Clock		15MHz Clock <sub>1</sub>		Variable Clock 1/TCLCL = 1.2MHz to 15MHz		Units
		Min	Max	Min	Max	Min	Max	
<b>PROGRAM MEMORY</b>								
TCY	Min Instruction Cycle Time (Note 3)	1000		800		12TCLCL	12TCLCL	ns
TLHLL	ALE Pulse Width	127		83		2TCLCL-40		ns
TAVLL	Address Set-up to ALE	43		37		TCLCL-40		ns
TLLAX	Address Hold After ALE	48		32		TCLCL-35		ns
TLLIV	ALE to Valid Instruction In		233		168		4TCLCL-100	ns
TLLPL	ALE to $\overline{\text{PSEN}}$	58		42		TCLCL-25		ns
TPLPH	$\overline{\text{PSEN}}$ Pulse Width	215		166		3TCLCL-35		ns
TPLIV	$\overline{\text{PSEN}}$ to Valid Instruction In		125		76		3TCLCL-125	ns
TPXIX	Input Instruction Hold After $\overline{\text{PSEN}}$	0		0		0		ns
TPXIZ	Input Instruction Float After $\overline{\text{PSEN}}$ (Note 2)		63		47		TCLCL-20	ns
TPXAV	Address Valid After $\overline{\text{PSEN}}$ (Note 2)	75		59		TCLCL-8		ns
TAVIV	Address to Valid Instruction In		302		220		5TCLCL-115	ns
TPLAZ	Address Float After $\overline{\text{PSEN}}$		+10		+10		+10	ns
<b>EXTERNAL DATA MEMORY</b>								
TRLRH	$\overline{\text{RD}}$ Pulse Width	400		302		6TCLCL-100		ns
TWLWH	$\overline{\text{WR}}$ Pulse Width	400		302		6TCLCL-100		ns
TLLAX	Address Hold After ALE (Note 1)	48		32		TCLCL-35		ns
TRLDV	$\overline{\text{RD}}$ to Valid Data In		250		170		5TCLCL-165	ns
TRHDX	Data Hold After $\overline{\text{RD}}$	0		0		0		ns
TRHDZ	Data Float After $\overline{\text{RD}}$		97		64		2TCLCL-70	ns
TLLDV	ALE to Valid Data In		517		386		8TCLCL-150	ns
TAVDV	Address to Valid Data In		585		438		9TCLCL-165	ns
TAVLL	Address Set-up to ALE	43		37		TCLCL-40		ns
TLLWL	ALE to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	200	300	151	251	3TCLCL-50	3TCLCL+50	ns
TAVWL	Address to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	203		138		4TCLCL-130		ns
TWHLH	$\overline{\text{WR}}$ or $\overline{\text{RD}}$ High to ALE High	43	123	27	107	TCLCL-40	TCLCL+40	ns
TDVWX	Data Valid to $\overline{\text{WR}}$ Transition	23		7		TCLCL-60		ns
TQVWH	Data Set-up Before $\overline{\text{WR}}$	433		319		7TCLCL-150		ns
TWHQX	Data Hold After $\overline{\text{WR}}$	43		27		TCLCL-50		ns
TRLAZ	Address Float After $\overline{\text{RD}}$		+10		+10		+10	ns

- Notes:
- 15MHz clock pertains only to 8031AH.
  - Interfacing the 8051AH to devices with float times up to 75ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.
  - TCY is the minimum instruction cycle time which consists of 12 oscillator clocks or two ALE cycles.

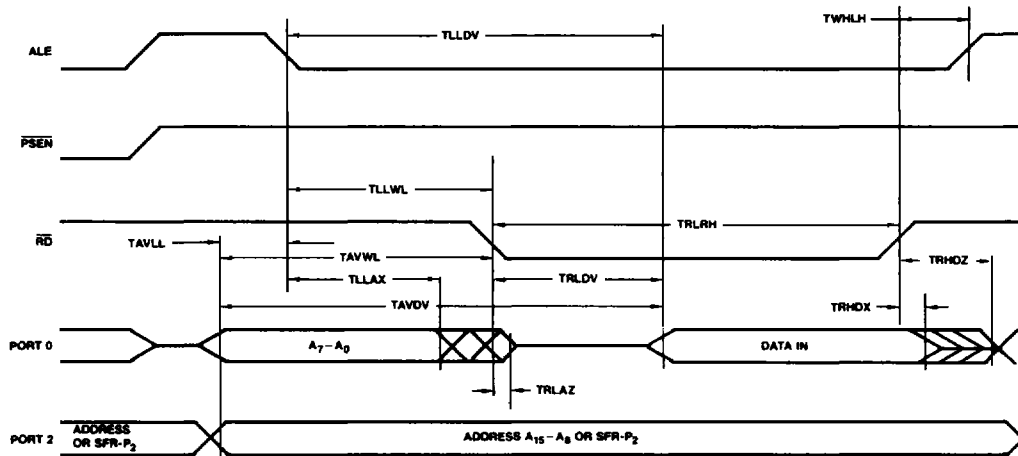
SWITCHING WAVEFORMS

EXTERNAL PROGRAM MEMORY READ CYCLE



WF007012

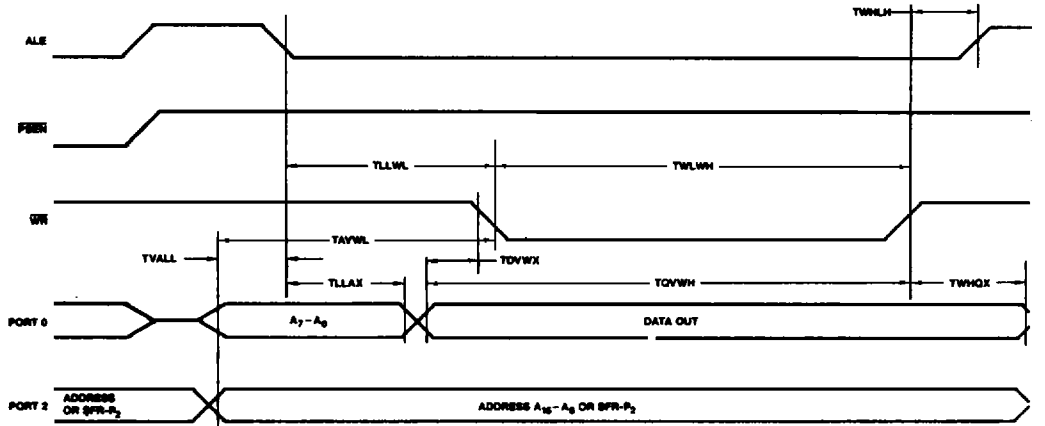
EXTERNAL DATA MEMORY READ CYCLE



WF007021

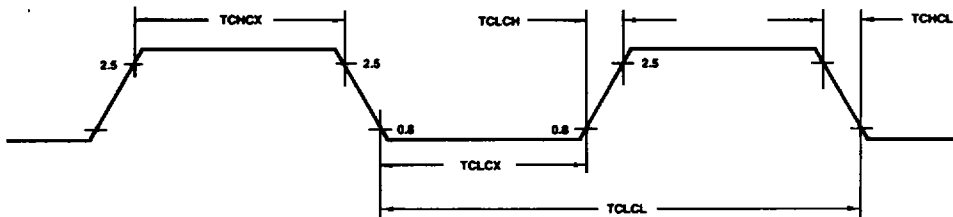
**SWITCHING WAVEFORMS (Cont.)**

**EXTERNAL DATA MEMORY WRITE CYCLE**



WF007031

**EXTERNAL CLOCK DRIVE XTAL<sub>2</sub>**

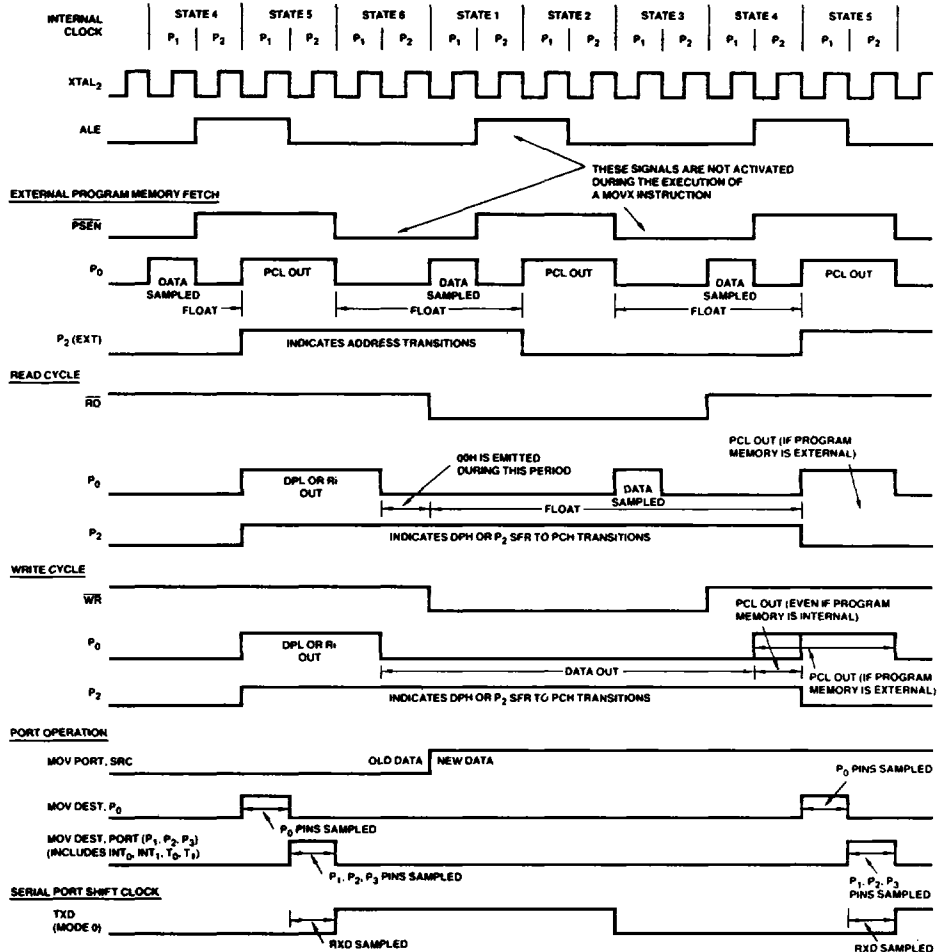


WF007060

**CLOCKING DETAILS**

Parameters	Description	Variable Clock Freq = 1.2MHz to 15MHz		Units
		Min	Max	
TCLCL	Oscillator Period	66.7	833.3	ns
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

### CLOCK WAVEFORMS



WF007070

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All internal timing is referenced to the internal time state shown on the top of the page. This waveform represents the signal on the X<sub>2</sub> input of the oscillator. This diagram represents when these signals are actually clocked within the chip. However, the time it takes a signal to propagate to the pins is in the range of 25 to 125ns. Prop delays are dependent on many variables, such as temperature, pin loading. Propagation also varies from output to output and component to component. Typically though, /RD and /WR have prop delays of approximately 50ns and the other timing signals approximately 85ns, at room temperature, fully loaded. These differences in prop delays between signals have been integrated into the timing specs.

TABLE 1. 8051AH/8031AH INSTRUCTION SET

## INSTRUCTIONS THAT AFFECT FLAG

## SETTING\*

Instruction	Flag			Instruction	Flag		
	C	OV	AC		C	OV	AC
ADD	X	X	X	CLR C	O		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C, bit	X		
MUL	O	X		ANL C,/bit	X		
DIV	O	X		ORL C, bit	X		
DA	X			ORL C,/bit	X		
RRC	X			MOV C, bit	X		
RLC	X			CJNE	X		
SETB C	1						

Interrupt Response Time: To finish execution of current instruction, respond to the interrupt request and push the PC; to vector to the first instruction of the interrupt service program requires 38 to 81 oscillator periods (3 to 7 $\mu$ s @ 12MHz).

\*Note that operations on SFR byte address 208 or bit addresses 209-215 (i.e., the PSW or bits in the PSW) will also affect flag settings.

## DATA TRANSFER

Mnemonic	Description	Byte	Cyc	Mnemonic	Description	Byte	Cyc
MOV A,Rn	Move register to Accumulator	1	1	ANL direct,#data	AND immediate data to direct byte	3	2
MOV A,direct	Move direct byte to Accumulator	2	1	ORL A,Rn	OR register to Accumulator	1	1
MOV A,@Ri	Move indirect RAM to Accumulator	1	1	ORL A,direct	OR direct byte to Accumulator	2	1
MOV A,#data	Move immediate data to Accumulator	2	1	ORL A,@Ri	OR indirect RAM to Accumulator	1	1
MOV Rn,A	Move Accumulator to register	1	1	ORL A,#data	OR immediate data to Accumulator	2	1
MOV Rn,direct	Move direct byte to register	2	2	ORL direct,A	OR Accumulator to direct byte	2	1
MOV Rn,#data	Move immediate data to register	2	1	ORL direct,#data	OR immediate data to direct byte	3	2
MOV direct,A	Move Accumulator to direct byte	2	1	XRL A,Rn	Exclusive-OR register to Accumulator	1	1
MOV direct,Rn	Move register to direct byte	2	2	XRL A,direct	Exclusive-OR direct byte to Accumulator	2	1
MOV direct,direct	Move direct byte to direct byte	3	2	XRL A,@Ri	Exclusive-OR indirect RAM to Accumulator	1	1
MOV direct,@Ri	Move indirect RAM to direct byte	2	2	XRL A,#data	Exclusive-OR immediate data to Accumulator	2	1
MOV direct,#data	Move immediate data to direct byte	3	2	XRL direct,A	Exclusive-OR Accumulator to direct byte	2	1
MOV @Ri,A	Move Accumulator to indirect RAM	1	1	XRL direct,#data	Exclusive-OR immediate data to direct	3	2
MOV @Ri,direct	Move direct byte to indirect RAM	2	2	CLR A	Clear Accumulator	1	1
MOV @Ri,#data	Move immediate data to indirect RAM	2	1	CPL A	Complement Accumulator	1	1
MOV DPTR,#data16	Move 16-bit constant to Data Pointer	3	2	RL A	Rotate Accumulator Left	1	1
MOVC A,@A+DPTR	Move Code byte relative to DPTR to Accumulator	1	2	RLC A	Rotate Accumulator Left through Carry Flag	1	1
MOVC A,@A+PC	Move Code byte relative to PC to Accumulator	1	2	RR A	Rotate Accumulator Right	1	1
MOVX A,@Ri	Move External RAM (8-bit address) to Accumulator	1	2	RRC A	Rotate Accumulator Right through Carry Flag	1	1
MOVX A,@DPTR	Move External RAM (16-bit address) to Accumulator	1	2	SWAP A	Exchange nibbles within the Accumulator	1	1
MOVX @Ri,A	Move Accumulator to External RAM (8-bit address)	1	2	<b>ARITHMETIC</b>			
MOVX @DPTR,A	Move Accumulator to External RAM (16-bit address)	1	2	<b>Mnemonic</b>	<b>Description</b>	<b>Byte</b>	<b>Cyc</b>
PUSH direct	Push direct byte onto stack	2	2	ADD A,Rn	Add register to Accumulator	1	1
POP direct	Pop direct byte off of stack	2	2	ADD A,direct	Add direct byte to Accumulator	2	1
XCH A,Rn	Exchange register with Accumulator	1	1	ADD A,@Ri	Add indirect RAM to Accumulator	1	1
XCH A,direct	Exchange direct byte with Accumulator	2	1	ADD A,#data	Add immediate data to Accumulator	2	1
XCH A,@Ri	Exchange indirect RAM with Accumulator	1	1	ADDC A,Rn	Add register to Accumulator with carry	1	1
XCHD A,@Ri	Exchange indirect RAM's least sig nibble with A's LSN	1	1	ADDC A,direct	Add direct byte to Accumulator with Carry Flag	2	1
<b>BOOLEAN VARIABLE MANIPULATION</b>				ADDC A,@Ri	Add indirect RAM and Carry Flag to Accumulator	1	1
<b>Mnemonic</b>	<b>Description</b>	<b>Byte</b>	<b>Cyc</b>	ADDC A,#data	Add immediate data and Carry Flag to Accumulator	2	1
CLR C	Clear Carry Flag	1	1	SUBB A,Rn	Subtract register from Accumulator with Borrow	1	1
CLR bit	Clear direct bit	2	1	SUBB A,direct	Subtract direct byte from Accumulator with Borrow	2	1
SETB C	Set Carry Flag	1	1	SUBB A,@Ri	Subtract indirect RAM from Accumulator with Borrow	1	1
SETB bit	Set direct bit	2	1	SUBB A,#data	Subtract immediate data from Accumulator with Borrow	2	1
CPL C	Complement Carry Flag	1	1	INC A	Increment Accumulator	1	1
CPL bit	Complement direct bit	2	1	INC Rn	Increment register	1	1
ANL C,bit	AND direct bit to Carry Flag	2	2	INC direct	Increment direct byte	2	1
ANL C,/bit	AND complement of direct bit to Carry	2	2	INC @Ri	Increment indirect RAM	-	1
ORL C,bit	OR direct bit to Carry Flag	2	2	DEC A	Decrement Accumulator	-	1
ORL C,/bit	OR complement of direct bit to Carry	2	2	DEC Rn	Decrement register	-	1
MOV C,bit	Move direct bit to Carry Flag	2	1	DEC direct	Decrement direct byte	2	1
MOV bit,C	Move Carry flag to direct bit	2	2	DEC @Ri	Decrement indirect RAM	1	1
<b>LOGIC</b>				INC DPTR	Increment Data Pointer	1	2
<b>Mnemonic</b>	<b>Description</b>	<b>Byte</b>	<b>Cyc</b>	MUL AB	Multiply Accumulator times B	1	4
ANL A,Rn	AND register to Accumulator	1	1	DIV AB	Divide Accumulator by B	1	4
ANL A,direct	AND direct byte to Accumulator	2	1	DA A	Decimal Adjust Accumulator	1	1
ANL A,@Ri	AND indirect RAM to Accumulator	1	1	<b>OTHER</b>			
ANL A,#data	AND immediate data to Accumulator	2	1	<b>Mnemonic</b>	<b>Description</b>	<b>Byte</b>	<b>Cyc</b>
ANL direct,A	AND Accumulator to direct byte	2	1	NOP	No Operation	1	1

CONROL TRANSFER (BRANCH)			Notes on data addressing modes:	
<b>Mnemonic</b>	<b>Description</b>	<b>Byte Cyc</b>	<b>Rn</b>	-Working register R0 - R7 of the currently selected Register bank.
AJMP addr11	Absolute Jump	2 2		
LJMP addr16	Long Jump	3 2		
SJMP rel	Short Jump (relative addr)	2 2	direct	-128 internal RAM locations, any I/O port, control, or status register.
JMP @A + DPTR	Jump indirect relative to the DPTR	1 2		
JZ rel	Jump if Accumulator is zero	2 2	@Ri	-Indirect internal RAM location addressed by register R0 or R1.
JNZ rel	Jump if Accumulator is not zero	2 2		
JC rel	Jump if Carry Flag is set	2 2	# data	-8-bit constant included in instruction.
JNC rel	Jump if carry is not set	2 2	# data16	-16-bit constant included as bytes 2 and 3 of instruction.
JB bit,rel	Jump relative if direct bit is set	3 2	bit	-128 software flags, any I/O pin, control, or status bit.
JNB bit,rel	Jump relative if direct bit is not set	3 2		
JBC bit,rel	Jump relative if direct bit is set, then clear bit	3 2		
CJNE A,direct,rel	Compare direct byte to Accumulator and Jump if not Equal	3 2		
CJNE A,#data,rel	Compare immediate to Accumulator and Jump if not Equal	3 2		
CJNE Rn,#data,rel	Compare immediate to reg and Jump if not Equal	3 2	addr16	-Destination address for LCALL and LJMP may be anywhere within the 64-Kilobyte program memory address space.
CJNE @Ri,#data,rel	Compare immediate to indirect RAM and Jump if not Equal	3 2	addr11	-Destination address for ACALL and AJMP will be within the same 2-Kilobyte page of program memory as the first byte of the following instruction.
DJNZ Rn,rel	Decrement register and Jump if not zero	2 2		
DJNZ direct,rel	Decrement direct byte and Jump if not zero	3 2		
<b>CONTROL TRANSFER (SUBROUTINE)</b>				
<b>Mnemonic</b>	<b>Description</b>	<b>Byte Cyc</b>	<b>rel</b>	-SJMP and all conditional jumps include as 8-bit offset by Range is +127, -128 bytes relative to first byte of the following instruction.
ACALL addr11	Absolute Subroutine Call	2 2		
LCALL addr16	Long Subroutine Call	3 2		
RET	Return from Subroutine Call	1 2		
RETI	Return from Interrupt Call	1 2		

TABLE 2. INSTRUCTION OPCODES IN HEXADECIMAL ORDER

Hex Code	Bytes	Mnemonic	Operands	Hex Code	Bytes	Mnemonic	Operands
00	1	NOP		2F	1	ADD	A,R7
01	2	AJMP	Code addr	30	3	JNB	Bit addr,code addr
02	3	LJMP	Code addr	31	2	ACALL	Code addr
03	1	RR	A	32	1	RETI	
04	1	INC	A	33	1	RLC	A
05	2	INC	Data addr	34	2	ADDC	A,#data
06	1	INC	@R0	35	2	ADDC	A,data addr
07	1	INC	@R1	36	1	ADDC	A,@R0
08	1	INC	R0	37	1	ADDC	A,@R1
09	1	INC	R1	38	1	ADDC	A,R0
0A	1	INC	R2	39	1	ADDC	A,R1
0B	1	INC	R3	3A	1	ADDC	A,R2
0C	1	INC	R4	3B	1	ADDC	A,R3
0D	1	INC	R5	3C	1	ADDC	A,R4
0E	1	INC	R6	3D	1	ADDC	A,R5
0F	1	INC	R7	3E	1	ADDC	A,R6
10	3	JBC	Bit addr,code addr	3F	1	ADDC	A,R7
11	2	ACALL	Code addr	40	2	JC	Code addr
12	3	LCALL	Code addr	41	2	AJMP	Code addr
13	1	RRC	A	42	2	ORL	Data addr,A
14	1	DEC	A	43	3	ORL	Data addr,#data
15	2	DEC	Data addr	44	2	ORL	A,#data
16	1	DEC	@R0	45	2	ORL	A,data addr
17	1	DEC	@R1	46	1	ORL	A,@R0
18	1	DEC	R0	47	1	ORL	A,@R1
19	1	DEC	R1	48	1	ORL	A,R0
1A	1	DEC	R2	49	1	ORL	A,R1
1B	1	DEC	R3	4A	1	ORL	A,R2
1C	1	DEC	R4	4B	1	ORL	A,R3
1D	1	DEC	R5	4C	1	ORL	A,R4
1E	1	DEC	R6	4D	1	ORL	A,R5
1F	1	DEC	R7	4E	1	ORL	A,R6
20	3	JB	Bit addr,code addr	4F	1	ORL	A,R7
21	2	AJMP	Code addr	50	2	JNC	Code addr
22	1	RET		51	2	ACALL	Code addr
23	1	RL	A	52	2	ANL	Data addr,A
24	2	ADD	A,#data	53	3	ANL	Data addr,#data
25	2	ADD	A,data addr	54	2	ANL	A,#data
26	1	ADD	A,@R0	55	2	ANL	A,data addr
27	1	ADD	A,@R1	56	1	ANL	A,@R0
28	1	ADD	A,R0	57	1	ANL	A,@R1
29	1	ADD	A,R1	58	1	ANL	A,R0
2A	1	ADD	A,R2	59	1	ANL	A,R1
2B	1	ADD	A,R3	5A	1	ANL	A,R2
2C	1	ADD	A,R4	5B	1	ANL	A,R3
2D	1	ADD	A,R5	5C	1	ANL	A,R4
2E	1	ADD	A,R6	5D	1	ANL	A,R5

Hex Code	Bytes	Mnemonic	Operands	Hex Code	Bytes	Mnemonic	Operands
5E	1	ANL	A,R6	AF	2	MOV	R7,data addr
5F	1	ANL	A,R7	B0	2	ANL	C,/bit addr
60	2	JZ	Code addr	B1	2	ACALL	Code addr
61	2	AJMP	Code addr	B2	2	CPL	Bit addr
62	2	XRL	Data addr,A	B3	1	CPL	C
63	3	XRL	Data addr,#data	B4	3	CJNE	A,#data,code addr
64	2	XRL	A,#data	B5	3	CJNE	A,data addr,code addr
65	2	XRL	A,data addr	B6	3	CJNE	@R0,#data,code addr
66	1	XRL	A,@R0	B7	3	CJNE	@R1,#data,code addr
67	1	XRL	A,@R1	B8	3	CJNE	R0,#data,code addr
68	1	XRL	A,R0	B9	3	CJNE	R1,#data,code addr
69	1	XRL	A,R1	BA	3	CJNE	R2,#data,code addr
6A	1	XRL	A,R2	BB	3	CJNE	R3,#data,code addr
6B	1	XRL	A,R3	BC	3	CJNE	R4,#data,code addr
6C	1	XRL	A,R4	BD	3	CJNE	R5,#data,code addr
6D	1	XRL	A,R5	BE	3	CJNE	R6,#data,code addr
6E	1	XRL	A,R6	BF	3	CJNE	R7,#data,code addr
6F	1	XRL	A,R7	C0	2	PUSH	Data addr
70	2	JNZ	Code addr	C1	2	AJMP	Code addr
71	2	ACALL	Code addr	C2	2	CLR	Bit addr
72	2	ORL	C,bit addr	C3	1	CLR	C
73	1	JMP	@A + DPTR	C4	1	SWAP	A
74	2	MOV	A,#data	C5	2	XCH	A,data addr
75	3	MOV	Data addr,#data	C6	1	XCH	A,@R0
76	2	MOV	@R0,#data	C7	1	XCH	A,@R1
77	2	MOV	@R1,#data	C8	1	XCH	A,R0
78	2	MOV	R0,#data	C9	1	XCH	A,R1
79	2	MOV	R1,#data	CA	1	XCH	A,R2
7A	2	MOV	R2,#data	CB	1	XCH	A,R3
7B	2	MOV	R3,#data	CC	1	XCH	A,R4
7C	2	MOV	R4,#data	CD	1	XCH	A,R5
7D	2	MOV	R5,#data	CE	1	XCH	A,R6
7E	2	MOV	R6,#data	CF	1	XCH	A,R7
7F	2	MOV	R7,#data	D0	2	POP	Data addr
80	2	SJMP	Code addr	D1	2	ACALL	Code addr
81	2	AJMP	Code addr	D2	2	SETB	Bit addr
82	2	ANL	C,bit addr	D3	1	SETB	C
83	1	MOVC	A,@A + PC	D4	1	DA	A
84	1	DIV	AB	D5	3	DJNZ	Data addr,code addr
85	3	MOV	Data addr,data addr	D6	1	XCHD	A,@R0
86	2	MOV	Data addr,@R0	D7	1	XCHD	A,@R1
87	2	MOV	Data addr,@R1	D8	2	DJNZ	R0,code addr
88	2	MOV	Data addr,R0	D9	2	DJNZ	R1,code addr
89	2	MOV	Data addr,R1	DA	2	DJNZ	R2,code addr
8A	2	MOV	Data addr,R2	DB	2	DJNZ	R3,code addr
8B	2	MOV	Data addr,R3	DC	2	DJNZ	R4,code addr
8C	2	MOV	Data addr,R4	DD	2	DJNZ	R5,code addr
8D	2	MOV	Data addr,R5	DE	2	DJNZ	R6,code addr
8E	2	MOV	Data addr,R6	DF	2	DJNZ	R7,code addr
8F	2	MOV	Data addr,R7	E0	1	MOVX	A,@DPTR
90	3	MOV	DPTR,#data	E1	2	AJMP	Code addr
91	2	ACALL	Code addr	E2	1	MOVX	A,@R0
92	2	MOV	Bit addr,C	E3	1	MOVX	A,@R1
93	1	MOVC	A,@A + DPTR	E4	1	CLR	A
94	2	SUBB	A,#data	E5	2	MOV	A,data addr
95	2	SUBB	A,data addr	E6	1	MOV	A,@R0
96	1	SUBB	A,@R0	E7	1	MOV	A,@R1
97	1	SUBB	A,@R1	E8	1	MOV	A,R0
98	1	SUBB	A,R0	E9	1	MOV	A,R1
99	1	SUBB	A,R1	EA	1	MOV	A,R2
9A	1	SUBB	A,R2	EB	1	MOV	A,R3
9B	1	SUBB	A,R3	EC	1	MOV	A,R4
9C	1	SUBB	A,R4	ED	1	MOV	A,R5
9D	1	SUBB	A,R5	EE	1	MOV	A,R6
9E	1	SUBB	A,R6	EF	1	MOV	A,R7
9F	1	SUBB	A,R7	F0	1	MOVX	@DPTR,A
A0	2	ORL	C,/bit addr	F1	2	ACALL	Code addr
A1	2	AJMP	Code addr	F2	1	MOVX	@R0,A
A2	2	MOV	C,bit addr	F3	1	MOVX	@R1,A
A3	1	INC	DPTR	F4	1	CPL	A
A4	1	MUL	AB	F5	2	MOV	Data addr,A
A5		Reserved		F6	1	MOV	@R0,A
A6	2	MOV	@R0,data addr	F7	1	MOV	@R1,A
A7	2	MOV	@R1,data addr	F8	1	MOV	R0,A
A8	2	MOV	R0,data addr	F9	1	MOV	R1,A
A9	2	MOV	R1,data addr	FA	1	MOV	R2,A
AA	2	MOV	R2,data addr	FB	1	MOV	R3,A
AB	2	MOV	R3,data addr	FC	1	MOV	R4,A
AC	2	MOV	R4,data addr	FD	1	MOV	R5,A
AD	2	MOV	R5,data addr	FE	1	MOV	R6,A
AE	2	MOV	R6,data addr	FF	1	MOV	R7,A