

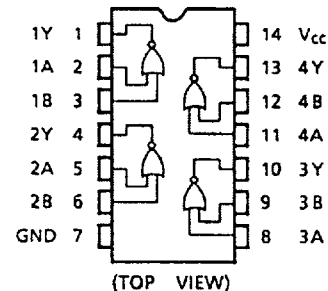
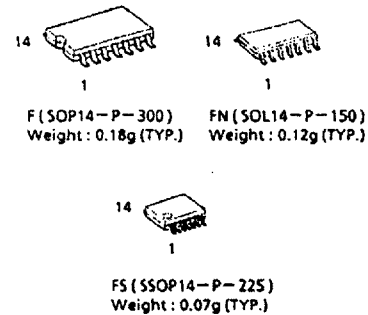
Quad 2-Input NOR Gate

The TC74LVQ02 is a high speed CMOS 2-INPUT NOR GATE fabricated with silicon gate and double-layer metal wiring C²MOS technology.

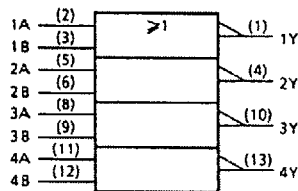
Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High Speed: $t_{pd} = 3.4\text{ns}$ (Typ.) at $V_{CC} = 3.3\text{V}$
- Low Power Dissipation: $I_{CC} = 2.5\mu\text{A}$ (Max.) at $T_a = 25^\circ\text{C}$
- Input Voltage Level:
 - $V_{IL} = 0.8\text{V}$ (Max.) at $V_{CC} = 3\text{V}$
 - $V_{IH} = 2.0\text{V}$ (Min.) at $V_{CC} = 3\text{V}$
- Symmetrical Output Impedance: $|I_{OH}| = I_{OL} = 12\text{mA}$ (Min.)
- Balanced Propagation Delays: $t_{pLH} \approx t_{pHL}$
- Pin and Function Compatible with 74HC02



Pin Assignment



IEC Logic Symbol

Truth Table

Inputs		Outputs
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

TC74LVQ02F/FN/FS

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 - 7.0	V
DC Input Voltage	V_{IN}	-0.5 - $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5 - $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 100	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	-65 - 150	$^{\circ}C$
Lead Temperature 10sec	T_L	300	$^{\circ}C$

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2.0 - 3.6	V
Input Voltage	V_{IN}	0 - V_{CC}	V
Output Voltage	V_{OUT}	0 - V_{CC}	V
Operating Temperature	T_{opr}	-40 - 85	$^{\circ}C$
Input Rise and Fall Time	dt/dv	0 - 100	ns/V

DC Electrical Characteristics

Parameter	Symbol	Test Condition	$T_a = 25^{\circ}C$			$T_a = -40 - 85^{\circ}C$		Unit	
			V_{CC} (V)	Min	Typ.	Max.	Min.		Max.
High-Level Input Voltage	V_{IH}		3.0	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}		3.0	-	-	0.8	-	0.8	
High-Level Output Voltage	V_{OH}	$V_{IN} = V_{IL}$ $I_{OH} = -50\mu A$ $I_{OH} = -12mA$	3.0	2.9	3.0	-	2.9	-	
			3.0	2.58	-	-	2.48	-	
Low-Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\mu A$ $I_{OL} = 12mA$	3.0	-	0.0	0.1	-	0.1	
			3.0	-	-	0.36	-	0.44	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	3.6	-	-	± 0.1	-	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	3.6	-	-	2.5	-	25.0	

AC Electrical Characteristics (Input $t_r = t_f = 3\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$)

Parameter	Symbol	Test Condition	V_{CC} (V)	Ta = 25°C			Ta = -40 ~ 85°C		Unit
				Min	Typ.	Max.	Min.	Max.	
Propagation Delay Time	t_{pLH}		2.7	–	5.2	10.6	1.0	12.0	ns
	t_{pHL}		3.3±0.3	–	4.3	7.5	1.0	8.0	
Output to Output Skew	t_{osLH}	(Note 1)	2.7	–	–	1.5	–	1.5	ns
	t_{osHL}		3.3±0.3	–	–	1.5	–	1.5	
Input Capacitance	C_{IN}	(Note 2)		–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)		–	26	–	–	–	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

Noise Characteristics (Input $t_r = t_f = 3\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$)

Parameter	Symbol	Test Condition	V_{CC}	Ta = 25°C		Unit
				Typ.	Max.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.3	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	-0.3	-0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	–	2.0	V
Maximum High Level Dynamic Input Voltage	V_{ILD}		3.3	–	0.8	V