

DRAM

1MEG x 1 DRAM

NIBBLE MODE

DRAM

FEATURES

- Industry standard x1 pin-out, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512 cycle refresh distributed across 8ms
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS, and HIDDEN
- Optional Nibble Mode access cycle

OPTIONS

- Timing
 - 80ns access
 - 100ns access
 - 120ns access
- Packages
 - Plastic DIP
 - Ceramic DIP
 - Plastic ZIP
 - Plastic SOJ

MARKING

- 8
- 10
- 12
- None
- C
- Z
- DJ

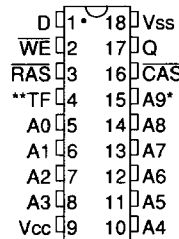
GENERAL DESCRIPTION

The MT4C1025 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{\text{RAS}}$ is used to latch the first 10 bits and $\overline{\text{CAS}}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. If $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{\text{CAS}}$ cycle. If $\overline{\text{WE}}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{\text{CAS}}$ remains LOW (regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This late $\overline{\text{WE}}$ pulse results in a READ-WRITE cycle.

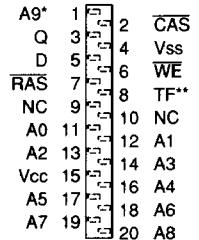
Returning $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during

PIN ASSIGNMENT (Top View)

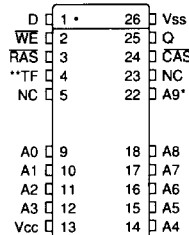
20 Pin DIP (PD, CD)



20 Pin ZIP (ZB)



20 Pin SOJ (DJA)

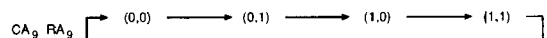


*Address not used for $\overline{\text{RAS}}$ ONLY refresh

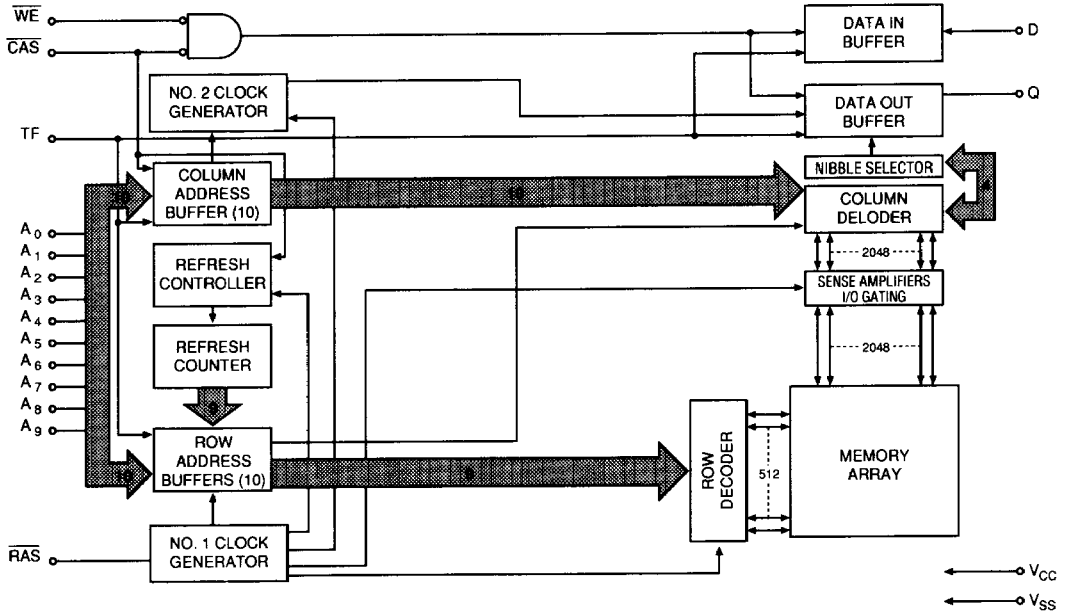
**TF = Test Function, Vin must be disconnected or between Vss and Vcc for normal operation.

the $\overline{\text{RAS}}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{\text{RAS}}$ cycle (READ, WRITE, $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$, or HIDDEN refresh) so that all 512 combinations of $\overline{\text{RAS}}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

NIBBLE MODE operation allows faster sequential serial data operations (READ, WRITE or READ-MODIFY-WRITE) up to 4 bits. The first of 4 bits is accessed in the usual manner with $\overline{\text{CAS}}$ address A9 (nibble MSB) and $\overline{\text{RAS}}$ address A9 (nibble LSB) selecting one of 4 bits within a nibble for initial access. By holding $\overline{\text{RAS}}$ LOW, $\overline{\text{CAS}}$ can be toggled incrementing the nibble address field in modulo 4 fashion with wrap around (see below).



FUNCTIONAL BLOCK DIAGRAM
NIBBLE MODE



TRUTH TABLE

Function	RAS	CAS	WE	TF	Addresses		
					tR	tC	
Standby	H	H	H	X	X	X	High Impedance
READ	L	L	H	X	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	X	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	X	ROW	COL	Valid Data Out, Valid Data In
NIBBLE READ	L	H→L→H	H	X	ROW	COL	Valid Data Out, Valid Data Out
NIBBLE WRITE	L	H→L→H	L	X	ROW	COL	Valid Data In, Valid Data In
NIBBLE READ-WRITE	L	H→L→H	H→L→H	X	ROW	COL	Valid Data Out, Valid Data In
RAS ONLY REFRESH	L	H	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	H	X	ROW	COL	Valid Data Out
CAS-BEFORE- RAS REFRESH	H→L	L	H	X	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss	-1.0V to +7.0V
Operating Temperature, TA(Ambient)	0°C to +70°C
Storage Temperature (Ceramic)	-65°C to +150°C
Storage Temperature (Plastic)	-55°C to +150°C
Power Dissipation	1 Watt
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V _{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V _{IH}	2.4	V _{CC} +1	V	1
Input Low (Logic 0) Voltage, All Inputs	V _{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input (0V ≤ V _{IN} ≤ V _{CC}), all other pins not under test = 0 volts)	I _I	-10	10	μA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V _{OUT} ≤ V _{CC})	I _{OZ}	-10	10	μA	
OUTPUT LEVELS					
Output High voltage (I _{OUT} = -5mA)	V _{OH}	2.4		V	
Output Low voltage (I _{OUT} = 4.2mA)	V _{OL}		0.4	V	

(Notes : 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES
		-8	-10	-12		
OPERATING CURRENT (\overline{RAS} and \overline{CAS} = Cycling: t _{rc} = t _{rc} (MIN))	I _{CC1}	70	60	50	mA	3, 4
OPERATING CURRENT: NIBBLE MODE (\overline{RAS} = V _{IL} , \overline{CAS} = Cycling: t _{pc} = t _{pc} (MIN))	I _{CC2}	70	60	50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current (\overline{RAS} = \overline{CAS} = V _{IH} after 8 \overline{RAS} cycles min.)	I _{CC3}	3	2	2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current (\overline{RAS} = \overline{CAS} = V _{CC} - 0.2V after 8 \overline{RAS} cycles min. All other inputs at V _{CC} -0.2V or V _{SS} + 0.2V)	I _{CC4}	1	1	1	mA	
REFRESH CURRENT: \overline{RAS} ONLY (\overline{RAS} = Cycling: \overline{CAS} = V _{IH})	I _{CC5}	70	60	50	mA	3
REFRESH CURRENT: \overline{CAS} -BEFORE- \overline{RAS} (\overline{RAS} and \overline{CAS} = Cycling)	I _{CC6}	70	60	50	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A ₀ -A ₉ , D	C _{I1}		5	pF	2
Input Capacitance: RAS, CAS, WE	C _{I2}		7	pF	2
Output Capacitance: Q	C _O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS	SYM	-8		-10		-12		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Random READ or WRITE cycle time	^t RC	150		180		220		ns	
READ-MODIFY-WRITE cycle time	^t RWC	175		210		255		ns	
Access time from RAS	^t RAC		80		100		120	ns	14
Access time from CAS	^t CAC		20		25		30	ns	15
Access time from column address	^t AA		40		50		60	ns	
Access time from CAS precharge	^t CPA		45		55		65	ns	
RAS pulse width	^t RAS	80	10,000	100	10,000	120	10,000	ns	
RAS hold time	^t RSH	20		25		30		ns	
RAS precharge time	^t RP	60		80		90		ns	
CAS pulse width	^t CAS	20	10,000	25	10,000	30	10,000	ns	
CAS hold time	^t CSH	80		100		120		ns	
CAS precharge time	^t CPN	10		10		20		ns	16
RAS to CAS delay time	^t RCD	20	60	10	75	15	90	ns	17
CAS to RAS precharge time	^t CRP	5		10		15		ns	
Row address set-up time	^t ASR	0		0		0		ns	
Row address hold time	^t RAH	10		15		20		ns	
RAS to column address delay time	^t RAD	15	40	20	50	15	60	ns	18
Column address set-up time	^t ASC	0		0		0		ns	
Column address hold time	^t CAH	15		20		25		ns	
Column address hold time (referenced to RAS)	^t AR	60		75		110		ns	
Column address to RAS lead time	^t RAL	40		50		60		ns	
Read command set-up time	^t RCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	19
CAS to output in low-Z	^t CLZ	0		0		0		ns	
Output buffer turn-off delay	^t OFF	0	20	0	20	0	25	ns	20
WE command set-up time	^t WCS	0		0		0		ns	21
Write command hold time	^t WCH	15		20		25		ns	
Write command hold time (referenced to RAS)	^t WCR	60		75		80		ns	
Write command pulse width	^t WP	15		20		25		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

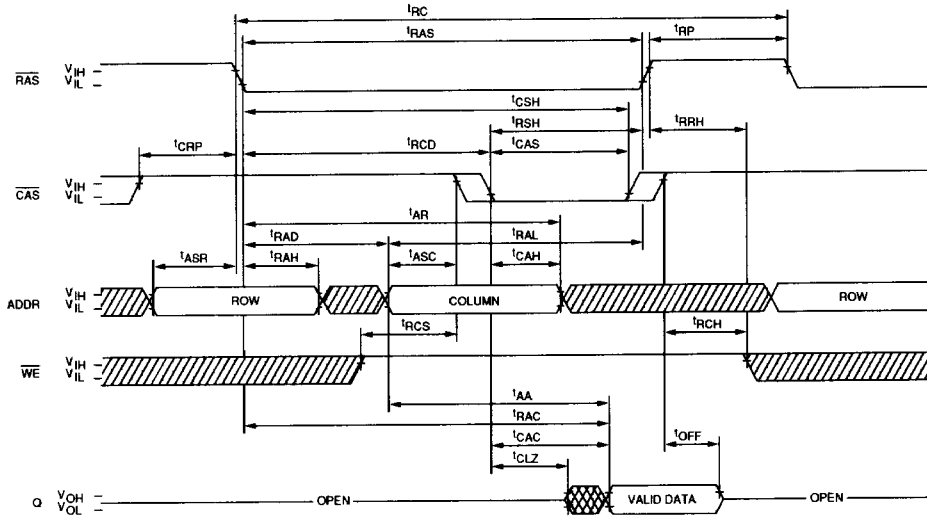
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command to $\overline{\text{RAS}}$ lead time	t^{RWL}	20		25		30		ns	
Write command to $\overline{\text{CAS}}$ lead time	t^{CWL}	20		25		30		ns	
Data-in set-up time	t^{DS}	0		0		0		ns	22
Data-in hold time	t^{DH}	15		20		20		ns	22
Data-in hold time (referenced to $\overline{\text{RAS}}$)	t^{DHR}	60		75		110		ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t^{RWD}	80		100		120		ns	21
Column address to $\overline{\text{WE}}$ delay time	t^{AWD}	40		50		60		ns	21
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	t^{CWD}	20		25		35		ns	21
Transition time (rise or fall)	t^{T}	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	t^{REF}		8		8		8	ms	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge time	t^{RPC}	0		0		0		ns	
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ refresh)	t^{CSR}	10		10		10		ns	5
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ refresh)	t^{CHR}	30		30		30		ns	5
$\overline{\text{RAS}}$ pulse width (NIBBLE MODE)	t^{RASN}	80	100,000	100	100,000	120	100,000	ns	
$\overline{\text{CAS}}$ precharge time (NIBBLE MODE)	t^{NCP}	10		10		15		ns	
NIBBLE MODE cycle time	t^{NC}	40		45		55		ns	
NIBBLE MODE READ-MODIFY- WRITE cycle time	t^{NRWC}	65		75		85		ns	
NIBBLE MODE access time	t^{NCAC}		20		20		35	ns	15
NIBBLE MODE pulse width	t^{NCAS}	20		25		35		ns	
NIBBLE MODE $\overline{\text{CAS}}$ precharge time	t^{NCP}	10		10		10		ns	
NIBBLE MODE $\overline{\text{RAS}}$ hold time	t^{NRSH}	20		25		30		ns	
NIBBLE MODE $\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	t^{NCWD}	20		25		35		ns	
NIBBLE MODE $\overline{\text{WE}}$ command to $\overline{\text{RAS}}$ lead time	t^{NRWL}	20		25		30		ns	
NIBBLE MODE $\overline{\text{WE}}$ command to $\overline{\text{CAS}}$ lead time	t^{NCWL}	20		25		30		ns	

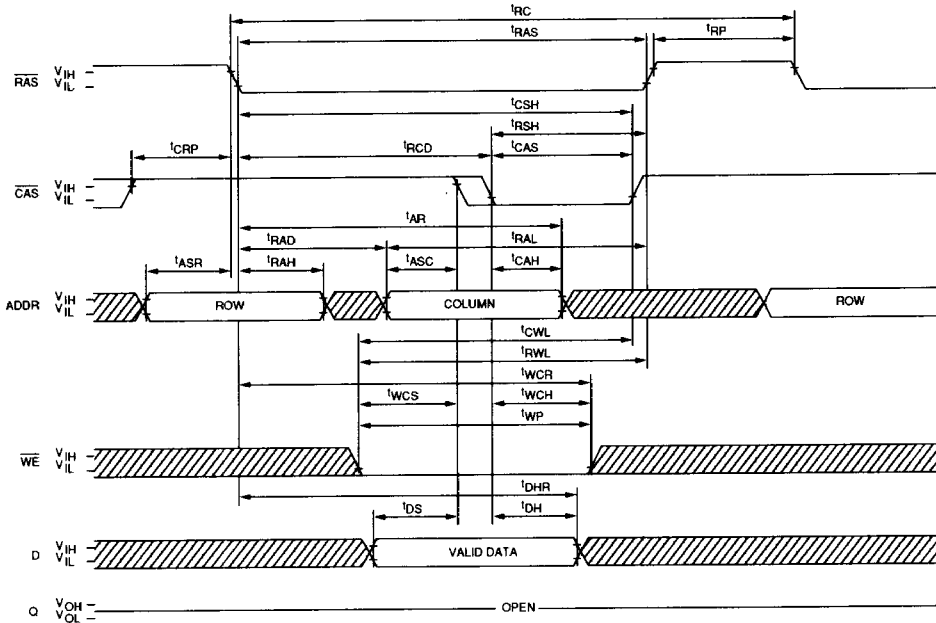
NOTES

1. All voltages referenced to V_{SS} .
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3V$ and $V_{CC} = 5V$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0^{\circ}C \leq T_A \leq 70^{\circ}C$) is assured.
7. An initial pause of $100\mu s$ is required after power-up followed by any 8 \overline{RAS} cycles before proper device operation is assured. The 8 \overline{RAS} cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume $t_T = 5ns$.
9. $V_{IH\ min}$ and $V_{IL\ max}$ are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, data output is high impedance.
12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and $100pF$.
14. Assumes that $t_{RCD} < t_{RCD\ (max)}$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
15. Assumes that $t_{RCD} \geq t_{RCD\ (max)}$.
16. If \overline{CAS} is LOW at the falling edge of \overline{RAS} , Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, \overline{CAS} must be pulsed HIGH for t_{CPN} .
17. Operation within the $t_{RCD\ (max)}$ limit ensures that $t_{RAC\ (max)}$ can be met. $t_{RCD\ (max)}$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD\ (max)}$ limit, then access time is controlled exclusively by t_{CAC} .
18. Operation within the $t_{RAD\ (max)}$ limit ensures that $t_{RCD\ (max)}$ can be met. $t_{RAD\ (max)}$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD\ (max)}$ limit, then access time is controlled exclusively by t_{AA} .
19. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
20. $t_{OFF\ (max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
21. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $t_{WCS} \geq t_{WCS\ (min)}$, the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{RWD} \geq t_{RWD\ (min)}$, $t_{AWD} \geq t_{AWD\ (min)}$ and $t_{CWD} \geq t_{CWD\ (min)}$, the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until \overline{CAS} goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to \overline{CAS} leading edge in early WRITE cycles and \overline{WE} leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE} = LOW$.

READ CYCLE

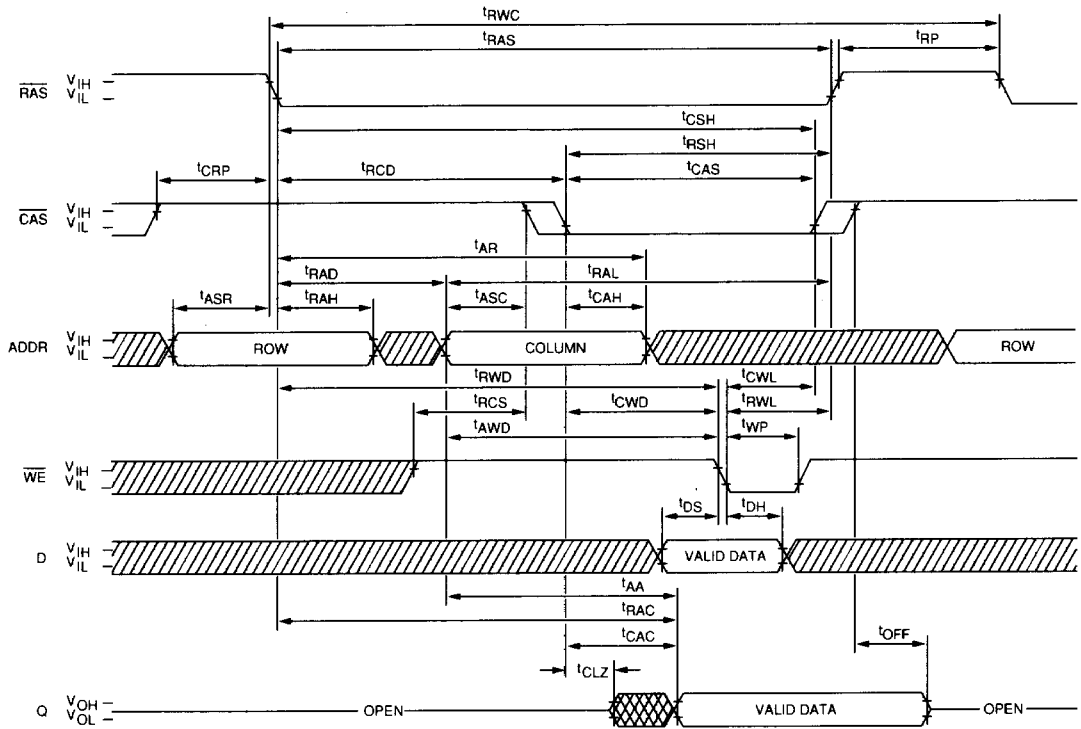


EARLY-WRITE CYCLE

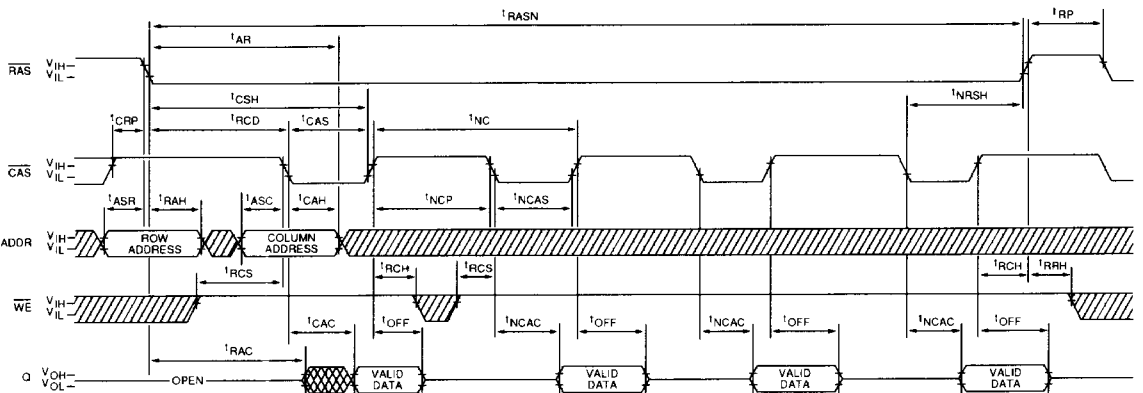




DON'T CARE
 UNDEFINED

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



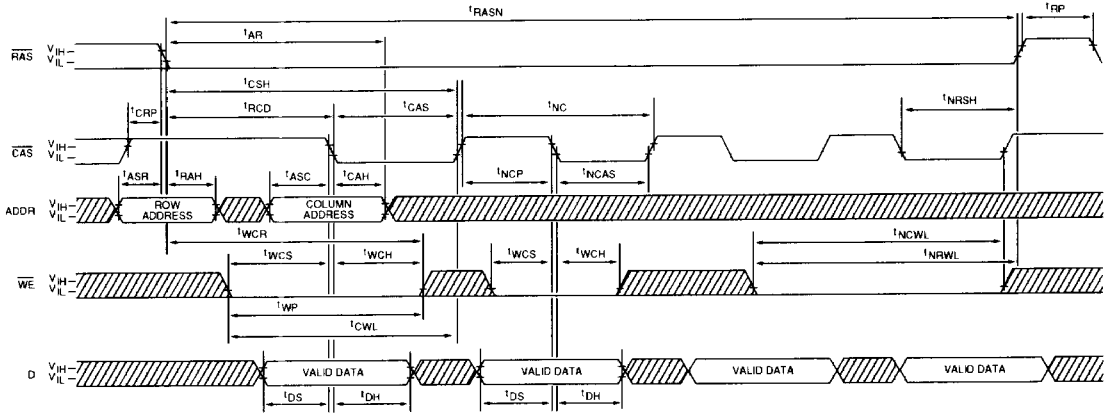
NIBBLE MODE READ CYCLE



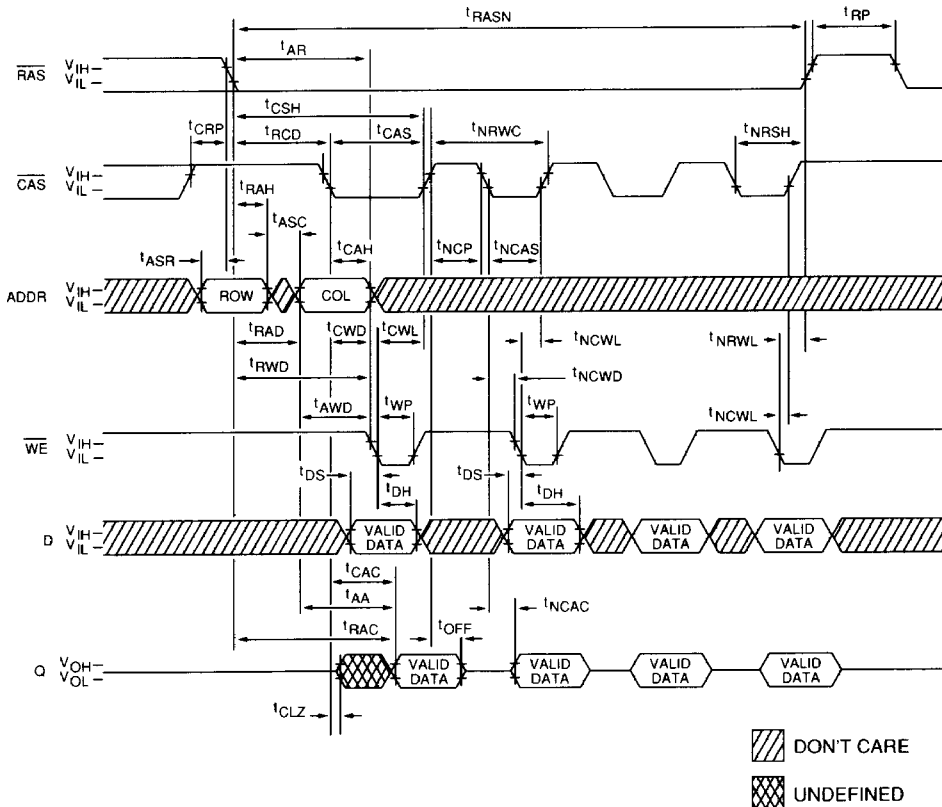
 DONT CARE
 UNDEFINED

DRAM

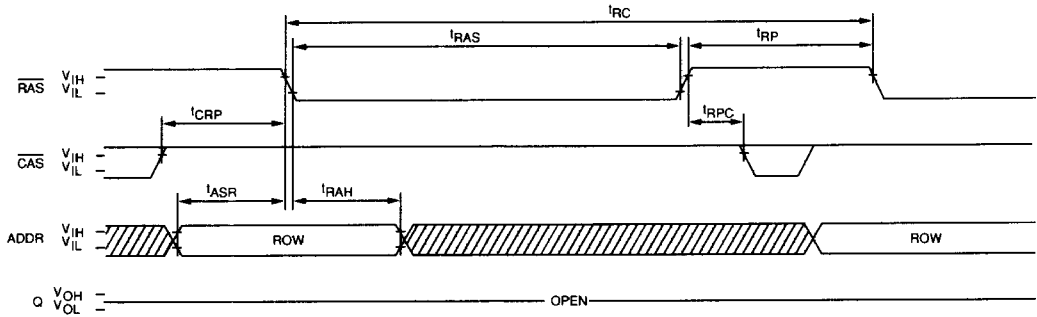
NIBBLE MODE EARLY-WRITE CYCLE



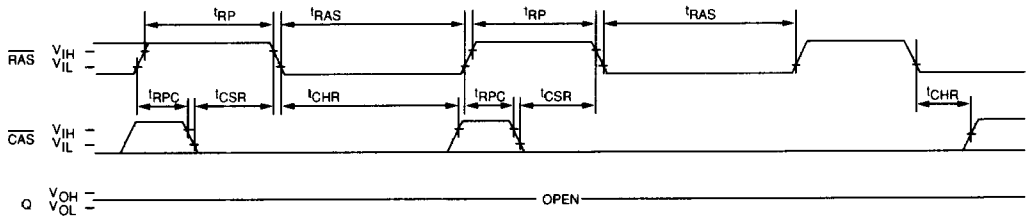
**NIBBLE MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)**



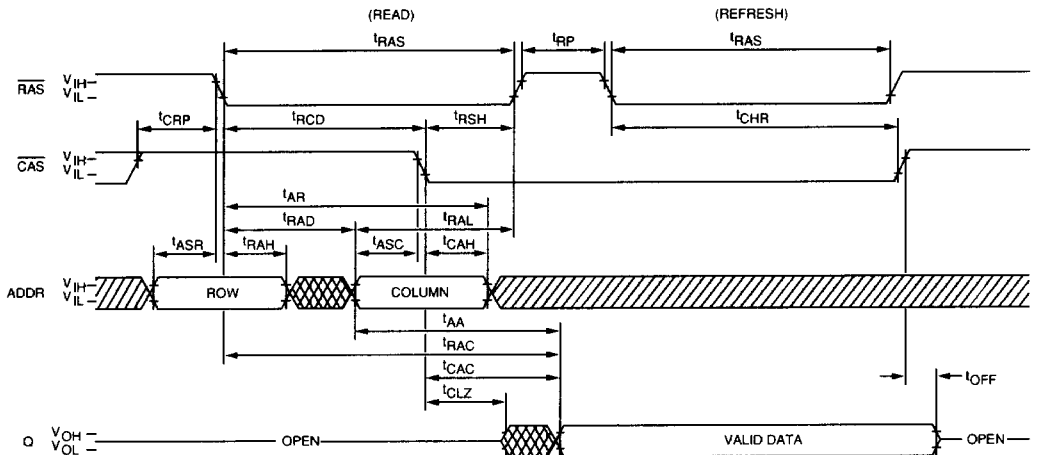
RAS ONLY REFRESH CYCLE
(ADDR = A₀ - A₈; A₉ and \overline{WE} = DON'T CARE.)





CAS-BEFORE-RAS REFRESH CYCLE
(A₀ - A₉ and \overline{WE} = DON'T CARE)



HIDDEN REFRESH CYCLE
(\overline{WE} = HIGH)²³



 DON'T CARE
 UNDEFINED