General Description

The SARE is specifically developed to build up ATM applications such as Network Interface Cards and ATM switches/hubs. This Segmentation And Reasssembly Element converts data (or video) frames to ATM cells. The flexible architecture enables it not only to handle the ATM-adaption layers AAL3/4 or AAL5, but also cell FIFO mode to support CBR. The interface for the ATM-physical layer is implemented as industry standard UTOPIA level 1. The device operates this UTOPIA interface in either slave mode, as required by switch/hub applications, or in master mode to be used in NIC (Network Interface Card) products. On the AAL side SARE features a PCI-bus interface. A 0.5-µ technology with 3.3-V supply ensures a highly integrated and cost effective system design. The SARE enables the implementation of glueless, truly cost optimized solutions for AAL-terminating equipment in ATM networks.

Type	Package
PXB 4110	P-MQFP-208-1 (SMD)

Features

- AAL 3/4 and 5 segmentation/reassembly
- Transparent mode to support constant bit rate
- On-chip support of 32 virtual connections
- Built-in FIFO (2+10 cell receive and 4 cell transmit)
- Full duplex transfer rate 155.52 Mbit/s
- VC level OAM-cell detection and CRC-10 calculation
- Cell rate shaping in transmit direction with up to 8 (dual) leaky buckets
- Bus master DMA with linked list structure and programmable buffer length
- Integrated MMU with packet scatter/gather capability
- Built-in data path loops for self-test purpose
- JTAG-(IEEE 1149.1) boundary scan
- 0.5 µ 3.3-V CMOS technology
- Optional ext. RAM supports up to 64 K virtual connections
- 32-bit PCI-bus interface
- UTOPIA level 1 interface
- P-MQFP-208 package