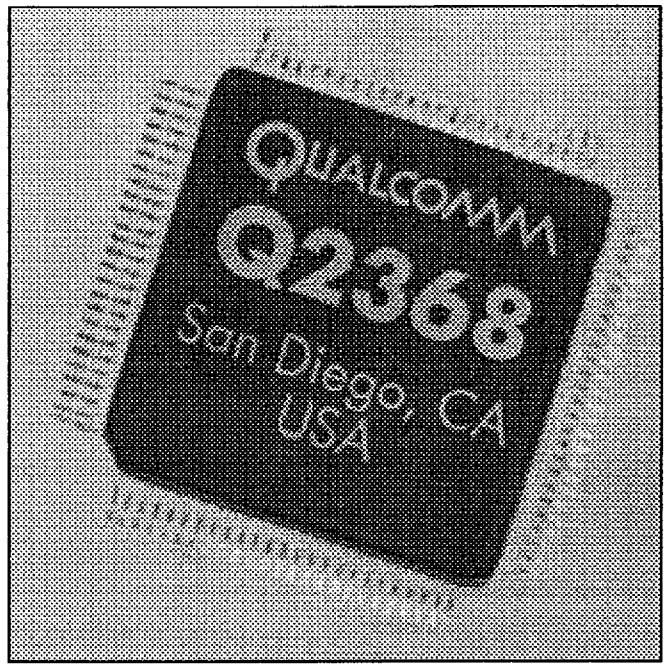
Q2368

DUAL DIRECT DIGITAL SYNTHESIZER



FEATURES

- Single High-Speed DDS up to 130 MHz or Two Independent DDSs, each up to 65 MHz Clock Speed
- 32-bit Input Resolution for Frequency and Phase
- 12-bit Output Resolution for Sine Wave Amplitude
- Noise Reduction Circuit (NRC)
- 8-bit Bus Control or Serial Control Interface
- Programmable HOP CLOCK Mode
- HOP OUT Signal (Output Trigger Pulse)
- Chirp Mode (Linear Frequency Sweep Function)
- Programmable Chirp Rate
- BURP Control (Hold Signal Function)
- Power Down Mode
- Modulation Control: BFSK, BPSK, QPSK, 8-PSK, I/Q Using Both Channels
- 14 x 14 mm, 100-pin PQFP Package
- Guaranteed Over Industrial Temperature and Voltage Range

APPLICATIONS

- Quadrature Oscillators
- Cellular Base Stations
- Magnetic Resonance Imaging/Medical Systems
- RADAR Systems and Simulators
- Paging Systems
- High Performance Test Equipment
- Digital Radios and Modems
- HF Transceivers
- Local Oscillator Generation for VSAT, DBS, and GPS Applications
- Missile Guidance Systems
- Scientific and Industrial Measurement Systems
- Scanners
- Image Processing
- Doppler Correction for Non-Geosynchronous Satellite Communications (LEO/MEO Systems)
- Hybrid Fiber/Coax (HFC) Networks

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CONTENTS

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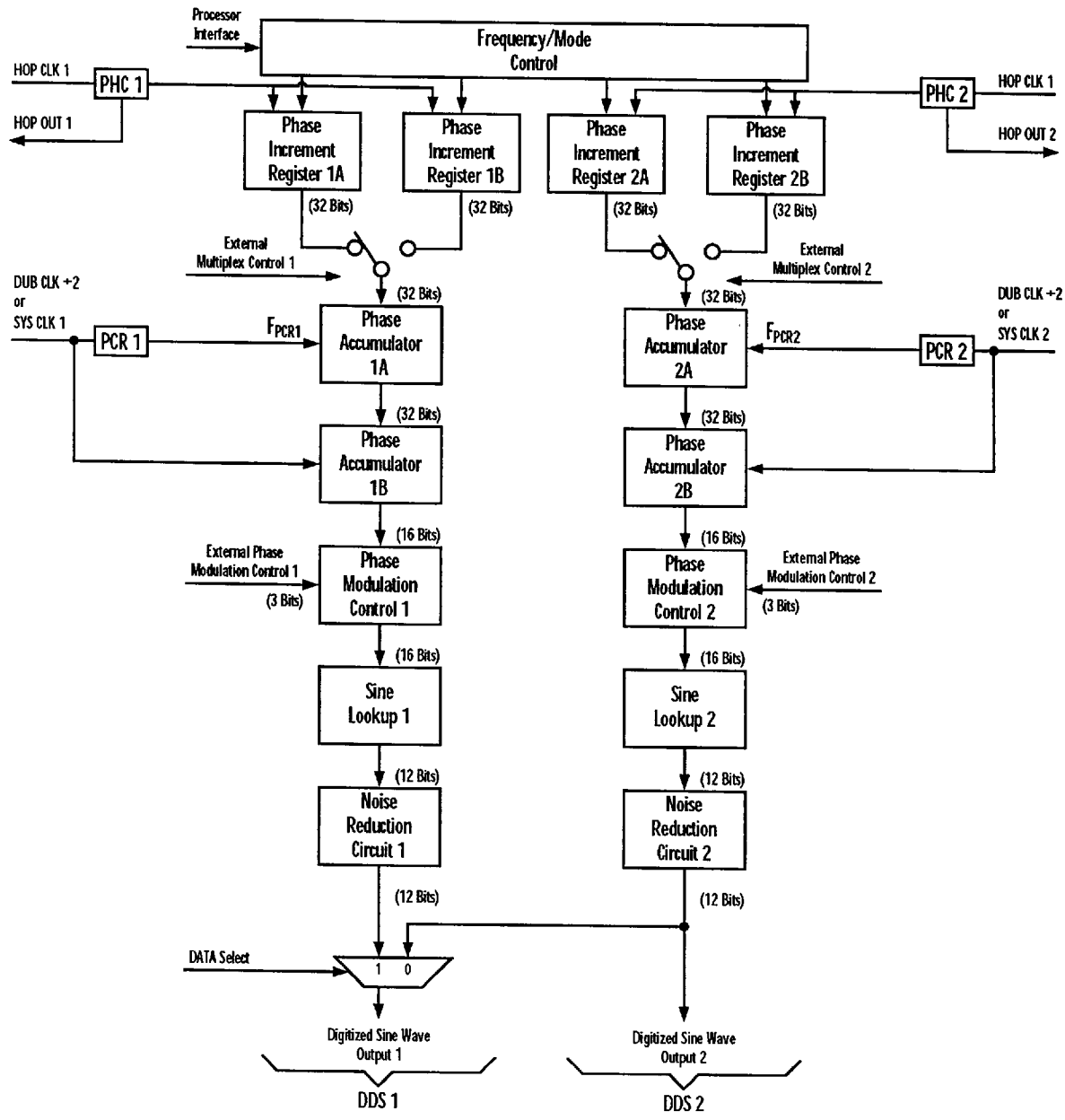
Q2368 GENERAL DESCRIPTION

A functional block diagram of the Q2368 is shown in Figure 1. The Q2368 can be configured as a single high-speed DDS capable of operating at 130 MHz clock speed when set for Double Mode, or as two independent DDS devices each capable of operating at 65 MHz clock speed when set for Dual DDS Mode. Configuring the Q2368 for either mode is accomplished by a simple pin setting. The Q2368 provides 32-bit digital input resolution for both frequency and phase control. This translates to ≤ .015 Hz minimum frequency step size depending on the frequency of the clock reference and 84 nano-degrees minimum resolution of phase control. The 12-bit output amplitude resolution also includes QUALCOMM's patented Noise Reduction Circuit (NRC) for reducing discrete spurious levels while only slightly increasing the wideband noise floor.

All phase, frequency and operating modes are controlled via a single microprocessor interface with user options for 8-bit bus control or serial control. The control interface selection is accomplished by a

Figure 1. Q2368 Dual DDS Block Diagram



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simple pin setting. Serial data output is provided to enable daisy-chaining of DDS1 to DDS2, or other serial-controlled devices. User control of all functions apply identically to either Double Mode or Dual Mode operation.

The processor interface controls the phase and frequency of the Q2368 DDS. The specific mode of the DDS operation is controlled by the Synchronous Mode Control (SMC) register and Asynchronous Mode Control (AMC) register.

The AMC register has an active value once the information has been written to it. This register does not require a hop clock signal to become active.

The SMC register and the two PIRs are double buffered. That is, these registers can be loaded at any time using the processor interface, but the values become active only when the hop clock signal is asserted. This makes possible the advanced synchronous phase and frequency change features of the Q2368 which are especially important when using the device in modulation or phase-locked loop applications.

The Asynchronous Hop Clock (AHC) can also be used to activate the double-buffered settings. See the *Asynchronous Hop Clock* section.

MODULATION TECHNIQUES

The Q2368 DDS provides features which allow the basic frequency synthesis function to be expanded and used in a variety of phase and frequency modulation schemes. Aside from the 32-bit control available for frequency and/or phase manipulations using the processor interface, external FSK and PSK modulation inputs are also provided as convenient control ports. The Q2368 can generate BFSK modulation up to 16.25 Mbps using the external multiplex control to toggle between two pre-loaded frequencies. Using the 3-bit external phase modulation control, either BPSK, QPSK, or 8-PSK modulation can be generated up to 16.25 Mbps for continuous data transmission. Additionally, when operating in Dual DDS Mode, quadrature I and Q channels can be generated quite simply by using the external phase control to produce two signals which are 90° offset from one another.

INTERNAL ARCHITECTURE

The Q2368 includes two identical, independent DDS functions with a common microprocessor interface (see Figure 1). Each DDS includes two double-buffered phase increment registers, two mode control registers (SMC and AMC), a phase increment multiplexer, two phase accumulators, a phase modulation control, a sine lookup function, and a noise reduction function. These components, and the processor interface, are described in detail in the following sections.

DOUBLE MODE OPERATION

When operating in Double Mode, the Q2368 is configured as one DDS capable of generating twice the output frequency compared to DDS operation in Dual Mode. The Double Mode is activated when the DUB EN input is set to a logic "High". Operating in Double Mode requires a separate clock source input (DUB CLK) to be used, rather than the system clock inputs (SYS CLK1, SYS CLK2) used for Dual Mode, since it is used for the multiplexing of both DDSs. Therefore, the maximum rated clock speed for DUB CLK is double that of the maximum rated clock speed for SYS CLK1 and SYS CLK2 in Dual Mode operation (130 MHz vs. 65 MHz).

The frequency output is directed through a mux to become the digitized sine wave outputs of DDS1; these are denoted separately as DUB OUT0 -11 and share the same pins as the DAC1 BIT0 -11 outputs.

Internally, the DDS multiplexing involves connecting the DUB CLK source to a 2-times mux for interleaving DDS1 and DDS2 and then is divided-by two and connected to each DDS for their associated operation. However, Double Mode operation only requires user control of DDS1 functions and modes of operation to generate the desired output signal. That is to say, all signal generation in Double Mode is performed using the DDS1 interface, and accomplished in an identical manner as with the controlling of DDS1 when operating in Dual Mode. The only exception to this is the setting of the initialization commands and activation of Power-down Mode.

During the initialization of the Q2368 operating in Double Mode, the AMC register of both DDS1 and

DDS2 have to be loaded with identical values in order to obtain the proper digitized output signals. Since the Q2368 registers come up in a random state after supply voltage is first applied, the initialization commands must also include setting the SMC register of both DDS1 and DDS2 in a known state such that the PWDE bit is set to "0". This will prevent the PWDE bit of either SMC register from enabling an unwanted power-down condition and interfering with Double Mode operation. If activating the Power-down Mode is desired, both SMC registers must have the PWDE bit set to "1" in order to apply a complete power-down condition. Alternatively, hardware control of power-down requires both PWR DN/ signals to be set to a logic "Low" and the respective DDS hop clock signals asserted. The only other distinction between Double Mode and Dual Mode operation is that in Double Mode, all DDS operations are performed and implemented with respect to the internal system clock rate of DUB CLK/2. This means that all clock-related calculations are performed in their usual method but with respect to a system clock value of DUB CLK/2.

DIGITAL PROCESSOR INTERFACE (DPI) MODES

8-BIT BUS MODE

The 8-bit Bus Mode interface is compatible with commonly used 8-bit microprocessors. This mode is selected when the BUSSELECT input (pin 51) is set "Low". The interface includes address decoding, chip selection, and write controls to load all on-chip control and phase increment registers in accordance with the timing requirements shown in Figure 16 and Table 15. Table 1 provides the register address map for the device. Each register is write-only and is decoded from the six-bit input address bus.

SERIAL BUS MODE

Serial Mode addressing is accomplished in a standard fashion using four signals: SDATA IN, SER CLK, SENABLE, and HOP CLK. With the BUSSELECT input set "High", the Serial Bus Mode is selected and data is shifted serially into SDATA IN on the falling edge of the SER CLK input while the shift enable control input, SENABLE, is set "High". The serial

Table 1. Q2368 Microprocessor Interface Register Address Map: 8-bit Parallel Loading

DDS1 REGISTER ADDRESS (HEX)	DDS2 REGISTER ADDRESS (HEX)	FUNCTION
00	20	PIRA Bits 0-7
01	21	PIRA Bits 8-15
02	22	PIRA Bits 16-23
03	23	PIRA Bits 24-31
04	24	PIRB Bits 0-7
05	25	PIRB Bits 8-15
06	26	PIRB Bits 16-23
07	27	PIRB Bits 24-31
08	28	SMC
09	29	AMC
0A	2A	ARR
0B	2B	AHC
0C	2C	PHC Bits 0-7
0D	2D	PHC Bits 8-15
0E	2E	PHC Bits 16-23
0F	2F	PHC Bits 24-31
14	34	HOP OUT 0-3
10	30	PCR Bits 0-7
11	31	PCR Bits 8-15
12	32	PCR Bits 16-19

programming register sequence for each DDS consists of 144 bits. The data for all 144 programming bits is shifted into the registers in accordance to the sequence shown in Table 2, starting with the MSB of the PCR register and ending with the LSB of the PIRA register. Even though the PCR register has effectively 20 bits and the HOP OUT register 4 bits, the serial update must treat them as 24 bits and 8 bits, respectively. In this case a logic "0" should be used for bits 1 through 4

Table 2. Q2368 Serial Programming Register Sequence

Number of Bits	Register*
24	PCR (23...0)
8	HOP OUT (7...0)
32	PHC (31... 0)
8	AMC (7...0)
8	SMC (7...0)
32	PIRB (31...0)
32	PIRA (31...0)

* MSB is always input first, LSB input last.

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and 25 through 28. A serial data output, SDATA OUT, is provided for each DDS to enable daisy-chaining of DDS1 to DDS2, or other serial-controlled devices. The serial data output timing is shown in Figure 17 and Table 15. The SENABLE input must be held "High" for the entire serial programming sequence and then set "Low". Letting SENABLE go "Low" before all of the serial programming bits are loaded into the serial registers will result in invalid programming to the serial registers. The ARR and AHC registers are not accessible in Serial Programming Mode. These registers can only be accessed through their respective external pins. After the SENABLE input is set "Low", the contents are activated on the rising edge of the HOP CLK input according to the timing requirements shown in Figure 17 and Table 16.

PHASE INCREMENT REGISTERS (PIRs)

Two independent 32-bit phase increment registers (A and B) are provided for each DDS function in the Q2368. Each phase increment register is 32-bits wide. Phase Increment Register A (PIRA) of each DDS provides the phase increment for the most basic single-frequency operation. Phase Increment Register B (PIRB) provides the phase increment for a range of functions useful in various modes of operation of the DDS. The 32-bit value for each register is loaded using four 8-bit write operations, or via serial programming. As stated previously, each PIR is double-buffered and the phase increment used by the phase accumulator is unaffected by this new stored value until the assertion of the hop clock signal occurs.

MODE CONTROL REGISTERS

Each DDS function on the Q2368 includes two mode control registers: Synchronous Mode Control (SMC) register and Asynchronous Mode Control (AMC) register. The SMC is used for operations that may change throughout the operation of the DDS. The AMC should be setup once during initialization. (Please note that in Figures 2 and 3, the unused bits must be set to "0" for proper operation.)

SYNCHRONOUS MODE CONTROL (SMC) REGISTER

The Synchronous Mode Control (SMC) register is double buffered to update control information, which will affect the actual DDS operation only when synchronously enabled by the transition of the hop clock signal. Figure 2 provides the bit definition for this SMC register. Bit 5, and 7 are reserved and should be set to logic "0". The remaining bits of the SMC register are the Power-down Enable (PWDE), Programmable Hop Clock Enable (PHCE), Hop Clock Phase Modulation Enable (HPME), External Multiplexer Enable (EME), External Phase Modulation Enable (EPME), and the Chirp Enable (CHE). Each of these bits is described below.

POWER DOWN ENABLE (PWDE)

The Power-down Mode is armed by the PWDE bit. This function provides independent power-down control for each DDS when operating in Dual Mode, or a combined power-down function while operating the Q2368 as one DDS in Double Mode. The PWDE bit allows processor control of power-down in an identical

Figure 2. Q2368 Synchronous Mode Control (SMC) Register

D7	D6	D5	D4	D3	D2	D1	D0
0*	POWER DOWN ENABLE (PWDE)	0*	PROG HOP CLK ENABLE (PHCE)	HOP CLK PHASE MOD ENABLE (HPME)	EXT MUX ENABLE (EME)	EXT PHASE MOD ENABLE (EPME)	CHIRP ENABLE (CHE)

* These bits must be set to 0.

ADDRESS 08 or 28 [hex]

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fashion as with the assertion of the PWR DN/ signal to a logic "Low". When the PWDE bit is set to "1", the power-down function is armed. The next time the hop clock signal is asserted, DDS current consumption is reduced to within the 0.1 to 20 mA range, depending on the clock frequency and whether the device is operating in Dual Mode or Double Mode. (See Table 3 for current consumption with different operating conditions.) When the Q2368 is operating in Double Mode, both DDS register addresses will have to be set to "1" in order to apply a complete power-down condition. All data residing in the programming registers is retained during power-down, although new information can still be addressed via the processor interface. Since the Q2368 registers come up in a random state after supply voltage is first applied, the initialization of the DDS must also include setting the SMC register in a known state such that the PWDE bit is set to "0". This will prevent the PWDE bit from enabling an unwanted power-down condition and interfering with normal DDS operation.

Table 3. Q2368 Typical Current Consumption at Different Operating Conditions

Operating Conditions	Current Consumption (mA)	
	Power-up Active	Power-down Active
Dual Mode*, F_{CLK} = 20 MHz	60	0.5
Dual Mode*, F_{CLK} = 35 MHz	105	1.0
Dual Mode*, F_{CLK} = 50 MHz	150	2.0
Dual Mode*, F_{CLK} = 65 MHz	200	2.0
Double Mode, F_{CLK} = 80 MHz	125	11.0
Double Mode, F_{CLK} = 100 MHz	150	13.0
Double Mode, F_{CLK} = 115 MHz	180	15.0
Double Mode, F_{CLK} = 130 MHz	205	16.0

*Includes both DDSs (DDS1 and DDS2) operating concurrently.

PROGRAMMABLE HOP CLOCK ENABLE (PHCE)

The Programmable Hop Clock Mode is armed when the PHCE bit is set to "1". This mode activates a programmable 32-bit duration counter (PHC register) derived from the DDS system clock to produce the PHC time period, T_{PHC}. The PHCE bit allows processor control of the programmable hop clock in an identical fashion as with the assertion of the PHOPEN signal to a logic "High". The next time the hop clock signal is asserted, the PHC register is activated. This is used by the Q2368 as a built-in timer function which allows precision timed intervals of the hop clock command to be automatically and continuously reasserted at the pre-programmed intervals of T_{PHC}. The sequence continues repetitively once it is started until the Programmable Hop Clock Mode is disabled. This significantly eases the control burden and "housekeeping" from the microprocessor required for programmable routines and sequential modes of operation.

HOP CLOCK PHASE MODULATION ENABLE (HPME)

The HPME bit is used when operating in the Internal Phase Modulation Mode and Chirp Mode. When the HPME bit is set to logic "1", the phase increment value stored in PIRB is added to the phase accumulator once each time the hop clock signal is asserted. In the case of using the Internal Phase Modulation Mode with the Phase Modulation Add Enable (PMAE) bit set to logic "0", all 32 bits of PIRB are used for the one time. However, if the PMAE bit is set to "1", the 8 MSB of PIRB are added to the 8 MSB of PIRA to form the 8 MSB to be accumulated with the 24 LSB of PIRA.

The Chirp Mode and the Internal Phase Modulation Mode utilize the HPME bit. When the HPME bit is set to "1", the hop clock signal is internally extended to two system clock cycles. The two system clock cycles make it possible for Phase Accumulator A to add the contents from PIRB once, and then switch the process immediately back to PIRA.

It is necessary to reset the HPME to "0" when you want to stop Chirp Mode, or disable the Internal Phase Modulation Mode and reconfigure operation to the Basic Oscillator Mode, for example. The hop clock command is required to initiate this change and during the HPME's transition from "1" to "0", the hop clock signal is correspondingly extended to two system clock cycles. This results in an automatic switch of the accumulation process back to PIRA.

EXTERNAL MULTIPLEXER ENABLE (EME)

The EME bit enables the External Multiplex Control. When this bit is set to logic "1", the EXT MUX signal

Figure 3. Q2368 Asynchronous Mode Control (AMC) Register

D7	D6	D5	D4	D3	D2	D1	D0
DAC STB	PHASE MOD ADD ENABLE (PMAE)	0*	0*	OUTPUT FORMAT**	NRC ENABLE BITS***		

ADDRESS 09 or 29 [hex]

* These bits must be set to 0.

**Output Format	D3
Two's Complement	0
Offset Binary	1

***DAC SIZE (# OF BITS)	D2	D1	D0
6	0	0	0
7	0	0	1
8	0	1	0
9	0	1	1
10	1	0	0
11	1	0	1
12	1	1	0
DISABLE NRC	1	1	1

determines whether the value stored in PIRA or PIRB will be used for the phase accumulation process. The selection on the EXT MUX signal is synchronously activated on the rising edge of the MUX CLK signal when the EME is set to logic "1". If the EME bit is set to logic "0", then the External Multiplex Control is disabled and the signal on EXT MUX is ignored. In this case, the contents of PIRA will be used for the accumulation process.

EXTERNAL PHASE MODULATION ENABLE (EPME)

The EPME enables the External Phase Modulation function. When this bit is set to "1", the PM EXT BITS are read and the corresponding phase offset is latched into the Q2368 each time the PM CLK is asserted. If External Phase Modulation is not used, set the EPME bit to "0". (See the *External Phase Modulation* section.)

CHIRP ENABLE (CHE)

The Chirp Mode is armed when the CHE bit is set to "1". To initiate a chirp waveform, both the HPME bit and the CHE bit in the SMC register must be set to "1", however the CHE bit is used for chirp waveform generation only and should be disabled whenever a non-chirp waveform is desired. (See *Chirp Mode* section under *Modes of Operation.*)

ASYNCHRONOUS MODE CONTROL (AMC) REGISTER

The Asynchronous Mode Control (AMC) register of each DDS function includes control bits which should only be configured during initialization of the Q2368. During the initialization of the Q2368 operating in Double Mode, the AMC register of both DDS1 and DDS2 have to be loaded with identical values in order to obtain the proper digitized output signals. These control bits, as shown in Figure 3, include the DAC Strobe or DAC Strobe Invert (DACSTB, DACSTB/), Phase Modulation Add Enable (PMAE), Output Format, and NRC Enable. Each of these is described below. Bits 4 and 5 of the AMC register are reserved and should be set to "0".

DAC STROBE, DAC STROBE INVERT (DACSTB, DACSTB/)

The DAC Strobe is a delayed version of the system clock which is provided along with the DAC BIT outputs in order to facilitate strobing this digitized sine value into a sample-and-hold DAC or other

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register. A non-inverted or inverted DAC Strobe is provided so that DAC devices with different triggering requirements can be easily accommodated. The DAC Output Timing specifications must be synchronized with respect to the falling edge of SYS CLK (or DUB CLK) and are therefore only guaranteed in relation to the falling edge of SYS CLK (or DUB CLK). Trying to use the DACSTB timing associated with the rising edge of SYS CLK (or DUB CLK) could potentially violate DAC setup time and result in strobing erroneous DAC BIT data.

When the AMC's D7 register is set to a "0", the DAC Strobe is non-inverted in relation to the system clock. This allows the falling edge of DACSTB to be used in compliance with SYS CLK (or DUB CLK). When the D7 register is set to a "1", the sense of the DAC Strobe is inverted in relation to the system clock. This allows the rising edge of DACSTB to be used in compliance with SYS CLK (or DUB CLK).

PHASE MODULATION ADD ENABLE (PMAE)

The PMAE bit is not used unless the HPME bit is set to "1" when operating in the Internal Phase Modulation Mode. The PMAE bit controls the way in which the value stored in PIRB is used for the one-time accumulation by the phase accumulator. When the PMAE bit is set to logic "1" and PIRB is active for accumulation, the 8 MSB of PIRB are added to the 8 MSB of PIRA to form the 8 MSB to be accumulated. The 24 LSB of PIRA are used as the 24 LSB of the phase accumulator input value. This technique allows efficient control for systems utilizing the Internal Phase Modulation Mode of operation. By storing the synthesizer frequency in the PIRA and modifying only the most significant byte of the PIRB, a 256-state phase modulator is implemented. This feature saves computation time in the processor controlling the DDS operation when a phase modulation system with 256-state (i.e., 360°/256 = 1.41 degrees) phase resolution is adequate. Using only the 8 MSB of PIRB to control the phase modulation allows the user to establish a byte-wide Direct Memory Access (DMA) control from the processor to the DDS function phase modulation register (i.e., PIRB), thus simplifying the processor overhead required to control the DDS function in rapidly switching phase modulation systems. When the PMAE bit is set to logic "0", all 32-bits of PIRB will be accumulated in the phase accumulator when PIRB is active allowing a phase resolution of $360^{\circ}/2^{32}$, i.e, 84 nano-degrees.

OUTPUT FORMAT

The Output Format bit determines the binary coding of the DAC output bits of each DDS function. When this bit is set to logic "1", the DAC output is encoded in offset binary format. When this bit is set to logic "0", the DAC output bits are encoded in two's complement format. Table 4 shows the effect of the setting of the Output Format bit.

Table 4. Q2368 DAC Output Formats

VALUE	OUTPUT FORMAT = 1 (OFFSET BINARY) MSB LSB	OUTPUT FORMAT = 0 (TWO's COMPLEMENT) MSB LSB
MAX Value	111111111111	011111111111
...	111111111110	011111111110
...	...	...
...	...	...
Half MAX + 1	100000000000	000000000000
Half MAX – 1	011111111111	111111111111
...	...	...
...	...	...
...	000000000001	100000000001
MIN Value	000000000000	100000000000

NRC ENABLE

When using the on-chip Noise Reduction Circuit (NRC) function, the number of significant bits to be used from the DAC outputs must be programmed into NRC Enable bits. The DAC bit-width is encoded in three bits as shown in Figure 3. When using a DAC with fewer than 12-bits resolution, the most significant DAC output bits are valid. The NRC function is disabled when the NRC Enable bits are set to 111 (binary). The function of the NRC circuit is described in the *Noise Reduction Circuit*section.

ACCUMULATOR RESET REGISTER (ARR)

Each DDS function on the Q2368 device includes an

accumulator reset register (ARR) and an external accumulator reset which is applied to the ARE/ input pin. By writing any value to the ARR register or by setting the ARE/ input to a logic "Low", the accumulator reset function is armed. The next time the hop clock signal is asserted, all activated phase accumulators are reset to zero.

ASYNCHRONOUS HOP CLOCK (AHC)

Each DDS function includes an Asynchronous Hop Clock (AHC) register. When any value is written to this register, the previously stored values in the double-buffered PIRA, PIRB, and SMC registers are activated. This allows processor control of activation of these settings in an identical fashion as with the assertion of the HOP CLK signal. Note that the HOP CLK signal must be low when the AHC register is accessed in order to activate the new register values. Also note that the timing for the AHC is exactly the same as the HOP CLK signal. Activation of the stored settings occurs within four SYS CLK or eight DUB CLK periods after writing to the AHC register.

PROGRAMMABLE HOP CLOCK (PHC) REGISTER

A desired duration, τ , over which a given DDS operation is directed, can be controlled very precisely using the Programmable Hop Clock Mode. This mode introduces a programmable counter derived from the DDS clock reference. The Programmable Hop Clock Mode gets armed using either the PHOPEN input pin or the PHCE bit in the SMC register. In conjunction with this, the 32-bit PHC register is loaded with the corresponding value to count the number of system clock periods before another hop clock command gets automatically issued and activates the latest instruction routine programmed to follow. The PHC register value corresponding to the desired duration for a given programmable hop clock period is determined as follows:

$$PHC = [(\tau/T_{CLK}) - 1],$$

where $T_{CLK} = 1/F_{CLK}$, and $\tau = T_{PHC}$ = the desired PHC time period. (Please refer to *Modes of Operation* in the *Chirp Mode* section.)

HOP OUT REGISTER

While operating in the Programmable Hop Clock Mode, an output pulse is generated at the HOP OUT pin when the programmable hop clock resets itself according to its programmed time interval, T_{PHC} . The 4-bit HOP OUT register is included to adjust the HOP OUT output pulse up to ± 7 system clock cycles of delay to compensate for any circuit path delay matching. The programming for this ± 7 clock cycles adjustment is done using the sign magnitude format, as shown in Table 5.

Table 5. Q2368 Programming for HOP OUT Register

HOP OUT Register Programming MSB LSB	Adjustable Delay in # of System Clock Cycles (t_{CYC})*
0111	+7
0110	+6
0101	+5
0100	+4
0011	+3
0010	+2
0001	+1
0000	0
1001	-1
1010	-2
1011	-3
1100	-4
1101	-5
1110	-6
1111	-7

* When operating in Dual Mode, t_{CYC} = the equivalent number of SYS CLK cycles.
When operating in Double Mode, multiply t_{CYC} by 2.

PROGRAMMABLE CHIRP RATE (PCR) REGISTER

While operating in the Chirp Mode, the chirp rate control introduces a programmable counter derived from the DDS clock reference. The 20-bit PCR register divides down the DDS system clock, F_{CLK} , to produce the chirp rate clock, F_{PCR}, for Phase Accumulator A used in the chirp implementation. If a new PCR value is programmed and then activated by a hop clock during a Chirp Mode sequence, the chirp rate clock will not change to the new F_{PCR} rate until after the

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PCR register has completed its divide count down to the current F_{PCR} clock cycle and then it will reset to start its new F_{PCR} divide cycle. In conjunction with the increment value in PIRA , the chirp rate control is used by the Q2368 to achieve < 1Hz/sec minimum chirp sweep rate over the entire clock speed range. The PCR register value corresponding to the chirp rate clock for a desired chirp sweep rate is determined as follows:

$$PCR = (F_{CLK} / \Delta F_{PCR}) - 1$$

where ΔF_{PCR} is the desired switching speed. (Additional reference is found under *Modes of Operation* in the *Chirp Mode* section.)

PHASE INCREMENT MULTIPLEXER CONTROL

The Phase Increment Multiplexer function selects which PIR (A or B) is used for the accumulation process. This multiplexing function provides a simple Binary Frequency Shift Keying (BFSK) interface to the DDS. The signal EXT MUX controls the selection of the value stored in either PIRA or PIRB. For EXT MUX = 0, PIRA is selected; for EXT MUX = 1, PIRB is selected. The signal MUX CLK enables the selection made by the EXT MUX signal. The selection made by the EXT MUX signal is activated synchronously once during the low-to-high transition on the MUX CLK signal. The MUX CLK signal is internally synchronized to the system clock signal of the DDS. The selection of the EXT MUX control may occur as frequently as once every four periods of SYS CLK or every eight periods of DUB CLK. (Refer to the *External Control Timing* section.)

PHASE ACCUMULATOR

Two 32-bit wide phase accumulators, cascaded serially, are included in each DDS of the Q2368. The first accumulator (Phase Accumulator A) is used for all signal generation including chirp waveforms. The second accumulator (Phase Accumulator B) is enabled exclusively for chirp waveform generation in conjunction with the first accumulator when Chirp Mode operation is activated. These accumulators compute and store the sum of the previously computed phase value and the phase increment value from either PIRA or PIRB.

PHASE MODULATION CONTROL

Using the external phase modulation inputs, PM EXT BIT0-2, the output of the phase accumulator can be offset by phase increments of 45 degrees (from 0 degrees to 315 degrees) without affecting the operation of the phase accumulator. Table 6 shows the phase offset for the possible settings of the 3-bit external phase modulation inputs. These inputs are latched into the DDS function when the signal PM CLK is asserted. Changes in the external phase modulation are synchronized internally to the DDS function. This provides a simple 8-Phase Shift Keying (8PSK) interface to the DDS.

Refer to the *Modes of Operation* section for more detailed information on phase modulation.

Table 6. Q2368 External Phase Modulation Offset Settings

PM EXT BIT			ABSOLUTE PHASE
0	1	2	OFFSET (degrees)
0	0	0	0
0	0	1	45
0	1	0	90
0	1	1	135
1	0	0	180
1	0	1	225
1	1	0	270
1	1	1	315

SINE LOOKUP FUNCTION

The Q2368 DDS implements a patented technique to generate a sine wave lookup (see *Patent Reference* 1). This algorithm takes the 16 MSB from the phase accumulator to generate a 12-bit sine wave value. Using this high precision lookup function, the phase truncation noise of the sine wave output is kept below 84 dB. This technique differs considerably from the traditional method of using a ROM lookup function. This advanced look-up technique provides highly accurate and precise sine wave generation.

NOISE REDUCTION CIRCUIT (NRC)

Noise due to amplitude quantization is often assumed

to be random and uniformly distributed. However, because a sine wave function is periodic, this is not always the case. At certain output frequencies, amplitude quantization errors become highly correlated, thereby causing spurs.

Spurs associated with round-off errors of the quantized sine wave outputs can be significantly reduced by enabling the on-chip Noise Reduction Circuit (NRC). This patented circuit distributes the noise energy evenly across the frequency band, thus reducing the amplitudes of peak spurious components (see *Patent Reference* 2).

It is important to properly set the NRC Enable bits, because the operation of the NRC is scaled to the LSB. If an incorrectly sized DAC is specified, performance will be reduced.

If the Q2368 is used to generate narrowband outputs and a low noise floor is required, the signal should be bandpass filtered and the NRC disabled. As stated above, when the NRC is enabled it distributes the noise evenly across the frequency band and raises the noise floor. When the NRC is disabled, the noise floor is slightly lower and the quantization errors show up as discrete spurious. However, since the signal is bandpass filtered, the broadband spurious will be negligible.

The output of the NRC (a 12-bit wide digitized sine wave) is normally connected to an external DAC function. This output value can be encoded in offset binary or two's complement format.

Figures 4 and 5 show typical spectra of the analog converted outputs from the Q2368 with the NRC enabled and disabled. These spectra were measured with the DDS using a 10-bit DAC. The synthesized frequency in each of these figures is 10.8 MHz from a 30 MHz system clock frequency. The measurement frequency spans from 0 to 15 MHz, the resolution bandwidth is 30 kHz, the video bandwidth is 3 kHz, and the scale is 10 dB per vertical division.

Figure 6 shows the typical performance of the Q2368 DDS when operating with a 10-bit DAC with NRC disabled and no LPF. This figure shows a 5 MHz output generated from a 20 MHz system clock frequency and the image at 15 MHz. This 15 MHz spur results from the negative image folded around the 30 MHz clock frequency. This image would normally be filtered by a LPF at the output of the DAC.

Figure 4. Q2368 Typical Spectrum with NRC Enabled (10-bit DAC)

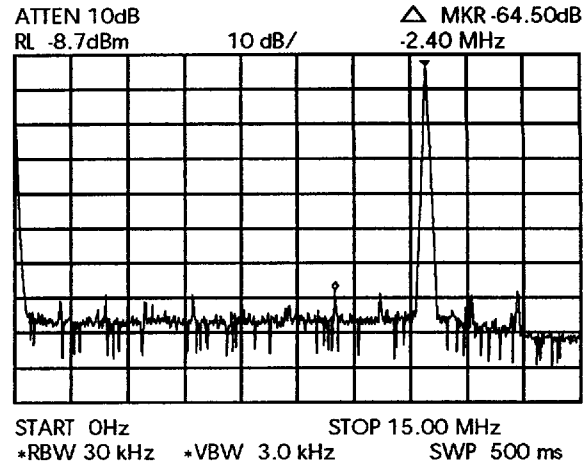


Figure 5. Q2368 Typical Spectrum with NRC Disabled (10-bit DAC)

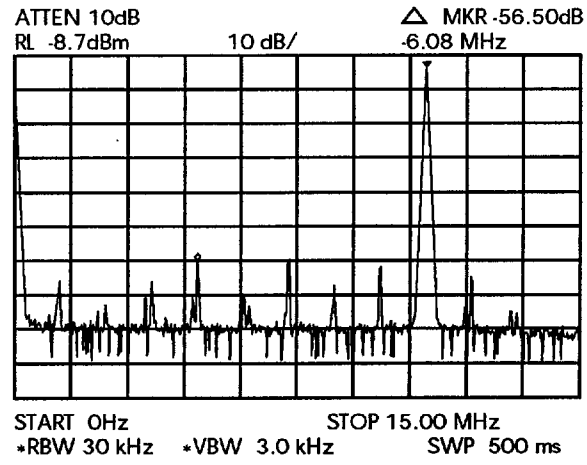
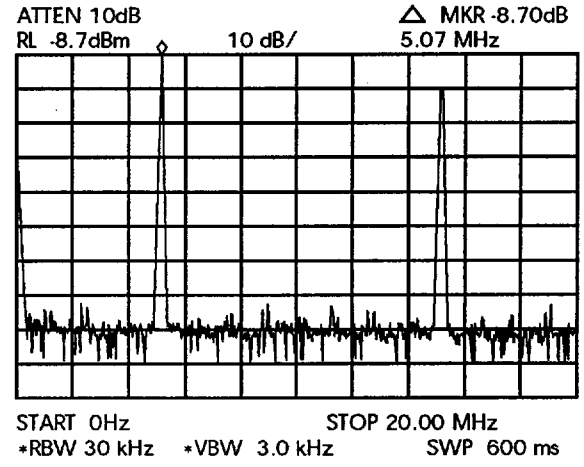


Figure 6. Q2368 Typical Spectrum with LPF Disabled (10-bit DAC)



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INPUT/OUTPUT SIGNALS

Figure 7 provides the pin configuration of the Q2368 DDS package and Tables 7-10 provide a summary of the input/output signal pin assignments.

Figure 7. Q2368 Package Pin Configuration

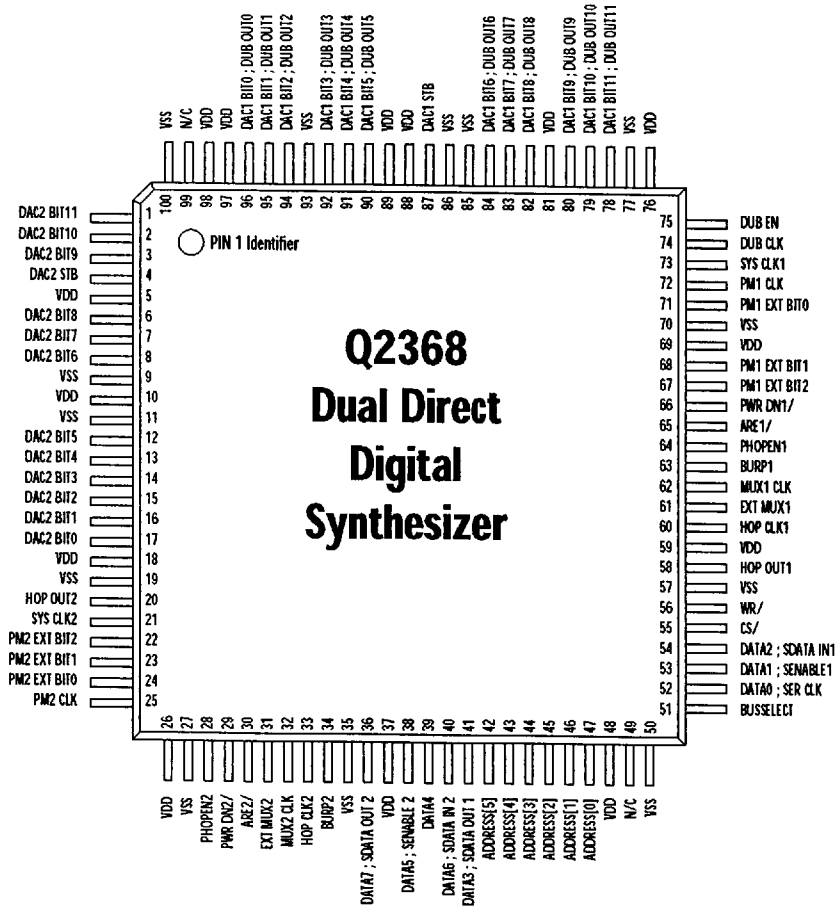

Table 7. Q2368 Processor Interface/Serial Data Bus Pin Functions

SYMBOL	PINS	I/O Type	NAME AND FUNCTION
DATA7; SDATA OUT2	36	INPUT/OUTPUT ± 8mA	Data Bus Bit 7 Input; DDS2 Serial Data Output
DATA6; SDATA IN2	40	INPUT TTL	Data Bus Bit 6; DDS2 Serial Data
DATA5; SENABLE2	38	INPUT TTL	Data Bus Bit 5; DDS2 Serial Enable
DATA4	39	INPUT TTL	Data Bus Bit 4
DATA3; SDATA OUT1	41	INPUT/OUTPUT ± 8mA	Data Bus Bit 3 Input; DDS1 Serial Data Output
DATA2; SDATA IN1	54	INPUT TTL	Data Bus Bit 2; DDS1 Serial Data
DATA1; SENABLE1	53	INPUT TTL	Data Bus Bit 1; DDS1 Serial Enable
DATA0; SER CLK	52	INPUT TTL	Data Bus Bit 0; DDS Serial Clock
ADDRESS[5-0]	42–47	INPUT TTL	Address Bus, Bit5(MSB) – Bit 0(LSB)
CS/	55	INPUT TTL	Chip Select (Active Low)
WR/	56	INPUT TTL	Write Strobe (Active Low)
BUSSELECT	51	INPUT TTL	8-Bit Bus Mode/Serial Bus Mode Select (8 Bit Bus = Low, Serial = High)

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Table 8. Q2368 DDS #1 Input/Output Pin Functions

SYMBOL	PINS	I/O Type	NAME AND FUNCTION
HOP CLK1	60	INPUT TTL	Hop Clock
EXT MUX1	61	INPUT TTL	Controls which PIR is Being Accumulated
MUX1 CLK	62	INPUT TTL	Enables the Value on EXT MUX1
SYS CLK1	73	INPUT CMOS	Clock Input for Dual Mode
PM1 EXT BIT[2 – 0]	67, 68, 71	INPUT TTL	External Phase Modulation Value, Bit 2(MSB) – Bit 0(LSB)
PM1 CLK	72	INPUT TTL	Enables the Value on PM1 EXT BITs
DAC1 BIT[11 – 0]; DUB OUT[11 – 0]	78–80, 82–84 90–92, 94–96	OUTPUT TTL ± 12mA	Digitized Sine Wave Output, Bit 11(MSB) – Bit 0(LSB); Doubled Output, Bit 11(MSB) – Bit 0(LSB)
DAC1 STB	87	OUTPUT TTL ± 16mA	Synchronous Strobe to Facilitate Clocking the DAC BITs into a DAC
PHOPEN1	64	INPUT TTL	Programmable Hop Clock Enable (Active High)
HOP OUT1	58	OUTPUT TTL ± 8mA	Programmable Hop Clock Output
BURP1	63	INPUT TTL	Hold Signal Control (Active High)
ARE1/	65	INPUT TTL	Accumulator Reset Enable (Active Low)
DUB EN	75	INPUT TTL	Selects Double Mode (Active High)
DUB CLK	74	INPUT CMOS	Clock Input for Double Mode
PWR DN1/	66	INPUT TTL	Hardware DDS1 Power Down (Active Low)

Table 9. Q2368 DDS #2 Input/Output Pin Functions

SYMBOL	PINS	I/O Type	NAME AND FUNCTION
HOP CLK2	33	INPUT TTL	Hop Clock
EXT MUX2	31	INPUT TTL	Controls which PIR is Being Accumulated
MUX2 CLK	32	INPUT TTL	Enables the Value on EXT MUX2
SYS CLK2	21	INPUT CMOS	Clock Input for Dual Mode
PM2 EXT BIT[2 – 0]	22, 23, 24	INPUT TTL	External Phase Modulation Value, Bit 2(MSB) – Bit 0(LSB)
PM2 CLK	25	INPUT TTL	Enables the Value on PM2 EXT BITs
DAC2 BIT[11 – 0]	1–3, 6–8, 12–17	OUTPUT TTL ± 8mA	Digitized Sine Wave Output, Bit 11(MSB) – Bit 0(LSB)
DAC2 STB	4	OUTPUT TTL ± 12mA	Synchronous Strobe to Facilitate Clocking the DAC BITs into a DAC
PHOPEN2	28	INPUT TTL	Programmable Hop Clock Enable (Active High)
HOP OUT2	20	OUTPUT TTL ± 8mA	Programmable Hop Clock Output
BURP2	34	INPUT TTL	Hold Signal Control (Active High)
ARE2/	30	INPUT TTL	Accumulator Reset Enable (Active Low)
PWR DN2/	29	INPUT TTL	Hardware DDS2 Power Down (Active Low)

Table 10. Q2368 Voltage Supply Pin Functions

SYMBOL	PINS	I/O Type	NAME AND FUNCTION
V_{DD}	5, 10, 18, 26, 37, 48, 59, 69, 76, 81, 88, 89, 97, 98	POWER	Power Supply (+5 VDC)
V_{SS}	9, 11, 19, 27, 35, 50, 57, 70, 77, 85, 86, 93, 100	GROUND	Ground
N/C	49, 99	NO CONNECT	Unconnected Pin

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SIGNALS COMMON FOR BOTH DDSs

The following signals are used in common for both DDS functions on the Q2368.

DATA0...DATA7

INPUTS (52, 53, 54, 41, 39, 38, 40, 36)

8-bit data bus for writing values to the on-chip processor interface registers. This bus is used for write operations only. DATA0 is the LSB.

ADDRESS0...ADDRESS5

INPUTS (47, 46, 45, 44, 43, 42)

6-bit address bus to select the internal processor interface registers. Addresses must be held fixed during the active period of the WR/ signal. ADDRESS0 is the LSB.

CS/

INPUT (55)

Chip Select. Must be held "Low" during processor write accesses to the Q2368. Can be held "Low" all the time, if desired.

WR/

INPUT (56)

When "Low" while CS/ is "Low", writes the value of the data bus to the register determined by the address bus.

SER CLK

INPUT (52)

Serial Data Clock. Shifts serial data into SDATA IN with each falling edge.

BUSSELECT

INPUT (51)

Bus Select. A logic "Low" sets Q2368 for control via 8-bit Bus Mode. A logic "High" sets for control via Serial Bus Mode.

V_{SS}

INPUT (9, 11, 19, 27, 35, 50, 57, 70, 77, 85, 86, 93, 100)

Provides electrical ground reference for signal and power inputs.

V_{DD}

INPUT (5, 10, 18, 26, 37, 48, 59, 69, 76, 81, ,88, 89, 97, 98)

Provides power to all Q2368 circuitry.

N/C

INPUT (49, 99)

These pins are unconnected.

SIGNALS INDEPENDENT FOR EACH DDS

The following signals pertain to a specific DDS function (1 or 2) on the Q2368.

SDATA IN1, SDATA IN2

INPUTS (54, 40)

Serial Data Input. Data is shifted in serially on falling edge of SER CLK. The data format is with the most significant bit (MSB) first.

SENABLE1, SENABLE2

INPUTS (53, 38)

Serial Shift Enable. Active "High" control for loading input serial data, SDATA IN.

SDATA OUT1, SDATA OUT2

OUTPUTS (41, 36)

Serial Data Output. Provided for each DDS to enable daisy-chaining of DDS1 to DDS2, or other serial-controlled devices.

SYS CLK1, SYS CLK2

INPUT (73, 21)

Provides the fundamental clock frequency of the synthesized sine waveform when operating in Dual Mode. Internal operations of the phase accumulator, external phase modulation, and phase increment registers for each respective DDS are synchronized to this clock signal.

DUB EN

INPUT (75)

Double Mode Enable. The Double Mode is activated when the DUB EN input is set to a logic "High". Enabling DUB EN activates the DUB CLK input which is the clock source input for Double Mode operation.

Setting DUB EN to a logic "Low" disables the DUB CLK input and configures the Q2368 for Dual Mode operation. (See *Double Mode Operation*section under *Internal Architecture* .)

DUB CLK

INPUT (74)

Provides the fundamental clock reference of the synthesized sine waveform when operating in Double Mode. Internal operations of the phase accumulators, external phase modulation and phase increment registers for both DDSs are synchronized to one-half the rate of this clock signal. Therefore, although the DUB CLK is a single clock source for the multiplexing of both DDSs, all DDS operations are performed and implemented with respect to the internal system clock rate of DUB CLK/2. (See *Double Mode Operation* section under *Internal Architecture .)*

HOP CLK1, HOP CLK2

INPUT (60, 33)

The HOP CLK signal controls the activation of the selection of the double buffered registers programmed via the 8-bit bus or serial bus interface. HOP CLK must be active "High" for at least one SYS CLK period or two DUB CLK periods. It can be asserted once every four SYS CLK periods, or eight DUB CLK periods.

HOP OUT1, HOP OUT2

OUTPUTS (58, 20)

While operating in the Programmable Hop Clock Mode, an output pulse is generated at the HOP OUT pin when the programmable hop clock resets itself according to its programmed time interval, T_{PHC}. This is useful for designing systems which are synchronously locked to the DDS system clock or require precise triggering of other system events with DDS operations. The HOP OUT signal is a positive pulse, one DDS system clock cycle wide. If the HOP OUT signal is unused when operating in the Programmable Hop Clock Mode, this output should be terminated into an RC-type termination. This will ensure that any potential for the repeating HOP OUT pulse to radiate noise or corrupt other circuit areas is filtered out.

PHOPEN1, PHOPEN2

INPUTS (64, 28)

Programmable Hop Clock Enable. The Programmable Hop Clock Mode is armed when the PHOPEN input is set to a logic "High". This mode activates a programmable 32-bit duration counter (PHC register) derived from the DDS system clock to produce the PHC time period, T_{PHC}. The next time the hop clock signal is asserted, the PHC register is activated. (See *Programmable Hop Clock Enable (PHCE)* section under *SMC Register.)* The Programmable Hop Clock Mode will be disabled when the PHOPEN input is set to a logic "Low" and a hop clock signal is reasserted.

BURP1, BURP2

INPUTS (63, 34)

The Q2368's BURP control function allows instant interruption of operating modes to produce a stationary (fixed) output. BURP control is active when it is set to a logic "High". When operating in the Chirp Mode, enabling the BURP signal will produce a constant output frequency corresponding to the exact position of where the chirp waveform was interrupted. Enabling the BURP signal during any other non-chirp DDS mode of operation (i.e., fixed frequency or phase modulation) will result in a zero frequency (DC) output, as in a burst-mode fashion, until the BURP signal is disabled (set to a logic "Low"). In the same manner, the Programmable Hop Clock Mode is simultaneously interrupted (if it is active) when the BURP signal is enabled. This allows the programmed time interval, T_{PHC}, to be maintained and resume counting the PHC time period as soon as the BURP signal is disabled. Moreover, all DDS operations transition in a phase-continuous fashion when the BURP control is enabled or disabled making it attractive for many generic functions such as *burst-mode, auto-scan,* or *seek* control. (Additional reference is found under *Modes of Operation* in the *Chirp Mode* section.)

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ARE1/, ARE2/

INPUTS (65, 30)

Accumulator Reset Enable. Each DDS function on the Q2368 includes an accumulator reset register (ARR) and an external accumulator reset which is applied to the ARE/ input pin. By setting the ARE/ input to a logic "Low", the accumulator reset function is armed. The next time the hop clock signal is asserted, all activated phase accumulators are reset to zero. (See *Accumulator Reset Register (ARR)*section.)

PWR DN1/, PWR DN2/

INPUTS (66, 29)

Power-down Enable. The Power-down Mode is armed when the PWR DN/ input is set to a logic "Low". This function provides independent power-down control for each DDS when operating in Dual Mode, or a combined power-down function while operating the Q2368 as one DDS in Double Mode. The next time the hop clock signal is asserted, DDS current consumption is reduced to within the 0.1 to 20 mA range, depending on the clock frequency and whether the device is operating in Dual Mode or Double Mode. (See Table 3 for current consumption with different operating conditions.) When the Q2368 is operating in double mode, hardware control of power-down requires both PWR DN/ signals to be set to a logic "Low" in order to apply a complete power-down condition. All data residing in the programming registers is retained during power-down, although new information can still be addressed via the processor interface. (See *PWDE* section under *SMC Register*.) The Power-down Mode will be disabled when the PWR DN/ input is set to a logic "High" and a hop clock signal is reasserted. When power-down is disabled and the DDSs are activated to a power-up condition, previous phase continuity will not be maintained, although the DDS can be put into a known state by loading an accumulator reset along with the desired frequency and modulation mode commands.

EXT MUX1, EXT MUX2

INPUT (61, 31)

When latched into the DDS with the signal MUX1 CLK (or MUX2 CLK) this signal determines whether PIRA or PIRB will be used for the incremental phase accumulator input value. When the EXT MUX signal is set to "1", the value stored in PIRB will be used by the phase accumulator. When the EXT MUX signal is set to "0", the value stored in PIRA will be used.

MUX1 CLK, MUX2 CLK

INPUT (62, 32)

The rising edge of this signal latches and enables the value on the EXT MUX inputs. This signal must be held "High" for a minimum of three SYS CLK periods, or six DUB CLK periods. Activation of the EXT MUX inputs is synchronized internally to the system clock.

PM1 EXT BIT0...PM1 EXT BIT2, PM2 EXT BIT0...PM2 EXT BIT2

INPUTS (67, 68, 71, 22, 23, 24)

External phase modulation inputs which control 45 degree phase offsets in the phase accumulated values in accordance with the settings provided in Table 6. PM EXT BITs are active when the signal PM CLK is asserted and are synchronized internally to the system clock.

PM1 CLK, PM2 CLK

INPUT (72, 25)

The rising edge of this signal latches and enables the value on the PM EXT BIT inputs. This signal must be held "High" for a minimum of three SYS CLK periods, or six DUB CLK periods. The PM EXT BIT inputs are synchronized internally to the system clock.

DAC1 BIT0...DAC1 BIT11, DAC2 BIT0...DAC2 BIT11

OUTPUTS (96, 95, 94, 92, 91, 90, 84, 83, 82, 80, 79, 78, 17, 16, 15, 14, 13, 12, 8, 7, 6, 3, 2, 1)

Digitized sine wave outputs when operating in Dual Mode. Encoded in offset binary or two's complement format, depending on settings in the AMC Registers. One sample is generated during each period of SYS CLK. DAC BIT 0 is the LSB.

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DAC1 STB, DAC2 STB

OUTPUT (87, 4)

Provides a synchronous strobe to facilitate clocking of the DAC BIT outputs (or DUB OUT outputs) into an external register or sampled DAC. One DAC STB is generated during each period of SYS CLK or DUB CLK. Essentially, the DAC STB (or DAC STB/) is a delayed version of the system clock. A low-value series resistor (100 Ω value typical) connected between this output and the DAC's clock input is recommended to mitigate noise feedthrough from the high energy switching transients on these pulses.

DUB OUT0...DUB OUT11

OUTPUTS (96, 95, 94, 92, 91, 90, 84, 83, 82, 80, 79, 78)

Digitized sine wave outputs when operating in Double Mode. Encoded in offset binary or 2's complement format, depending on settings in the AMC register. One sample is generated during each period of DUB CLK. DUB OUT0 is the LSB.

MODES OF OPERATION

Each DDS can be independently set to perform a wide range of expanded functions of the basic operation, as described in the following paragraphs. Control of all functions apply identically for Double Mode operation. (See *Double Mode Operation*section under *Internal Architecture* .)

BASIC SYNTHESIZER MODE

In its most Basic Operational Mode, each DDS on the Q2368 can provide a fixed frequency digitized sine wave output. The frequency of this sine output is determined by the frequency of the clock input and the value stored in the PIRs. (See formula (1) in the *Phase Increment Value*section.)

To set the Q2368 up in a single frequency output mode, the SMC should be set to "00" (hex). The AMC should be set according to the size of the DAC selected and the desired output format. The PMAE bit should also be set to "0" and the DAC STB bit set to provide the best DAC triggering. (Reference the *Simple Oscillator Mode* example section.)

PHASE MODULATION MODE

The Q2368 provides two means to implement phase modulation of a basic frequency output, referred to as Internal Phase Modulation and External Phase Modulation.

Internal Phase Modulation provides extremely fine resolution up to 0.00000008° of the phase adjustment (2^{32} - state phase resolution), while External Phase Modulation is designed for 45° increment phase shifts.

INTERNAL PHASE MODULATION

Internal Phase Modulation operates as a differential phase adjustment technique and requires use of the processor interface. The Internal Phase Modulation Mode is activated by loading PIRA with the correct phase increment for the basic frequency without phase modulation. PIRB is then loaded with the phase increment value equal to the phase increment value stored in PIRA plus the value of the desired phase offset. The phase accumulator uses PIRA for most phase accumulations.

Setting the HPME bit in the SMC register to logic "1" arms the DDS to use the 32-bit value in PIRB for one phase accumulation cycle when the hop clock signal is asserted. Since the phase increment value in PIRB is only used once for each hop clock assertion, the net effect is to cause a phase change to the generated sine wave.

When the PMAE bit is set to logic "1", the 8 MSB of PIRB are added to the 8 MSB of PIRA to form the 8 MSB to be accumulated with the 24 LSB of PIRA. This 32-bit value is used for one-time accumulation. If PMAE is "0", all 32 units of PIRB will be used for the accumulation.

The one-time phase shift occurs every time the hop clock signal is asserted and can occur as often as the hop clock signal can be asserted. (See *Timing Specifications* section.)

If it is desired to change the phase offset value, PIRB must be reloaded with the new phase offset before the next hop clock cycle. The HPME bit will remain set to "1" until reset by the processor. (Reference the *Hop Clock Phase Modulation Enable* section.)

In general, the formula for calculating the phase

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offset value using all 32-bits is the following:

$$Z = Y \cdot (2^{32}-1)/360,$$

Where Z is the decimal value of the desired phase offset, Y.

E.G., Calculate for a phase offset of 355° using the above formula:

Z = 355 • 4,294,967,295/360
= 4,235,314,971
= FC71C71B (hex)

The corresponding value to be loaded into
PIRB = PIRA + Z

EXTERNAL PHASE MODULATION

External Phase Modulation operates as an absolute phase adjustment technique and utilizes special synchronous inputs separate from the processor interface. When using the External Phase Modulation Mode, the phase increment value for the unmodulated input is written into PIRA. PIRB is not used in the External Phase Modulation Mode.

The External Phase Modulation Enable (EPME) bit in the SMC register is set to logic "1" to enable the External Phase Modulation Mode. When the EPME bit is set to "1", the phase offset determined by the PM EXT BITs are latched into the DDS function each time the signal PM CLK is asserted. This PM EXT BIT setting causes a phase offset in 45° increments as indicated in Table 6. This mode of operation allows very simple control of the DDS as a binary, quartenary, or 8-ary phase shift keyed (8PSK) modulator.

QUADRATURE SIGNAL GENERATION WITH THE Q2368

Quadrature (sine and cosine) outputs are generated by operating the Q2368 in Dual Mode and setting each DDS to the same frequency, but 90° apart in phase. Implementation:

1. You must tie the clocks together, thus allowing no drift between the DDS1 and DDS2.
2. Using the External Phase Modulation Mode, you can easily set the two DDSs to be exactly 90° apart by setting the 3 EXT PM bits to 0 1 0. Two possible methods are shown in Figures 8a and 8b.

As per Figure 8a, all external control lines for both DDS functions (HOP CLK, MUX CLK, PM CLK, and EXT MUX) are tied together and the external PM inputs of one DDS are set to 90°. As per Figure 8b, two external logic gates permit the use of the external PM control bits if phase modulation of the quadrature outputs is also required. In this case, the DDS2 output waveform will always be 90° advanced in phase with respect to DDS1.

DDS-generated quadrature signals have the advantage of precise phase and amplitude balance over the entire DDS bandwidth since it does not rely on analog components with their associated frequency response, tolerances, and aging effects. Using the Internal Phase Modulation Mode, the Q2368 can produce outputs which differ in phase from 90° with a

Figure 8a. Q2368 Quadrature Signal Implementation (Quadrature Oscillator)

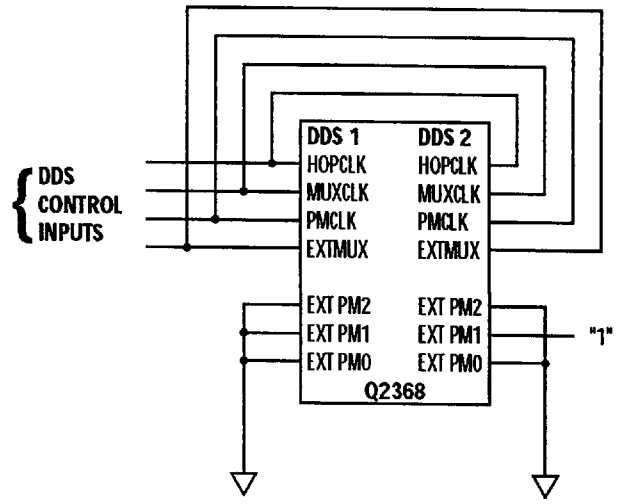
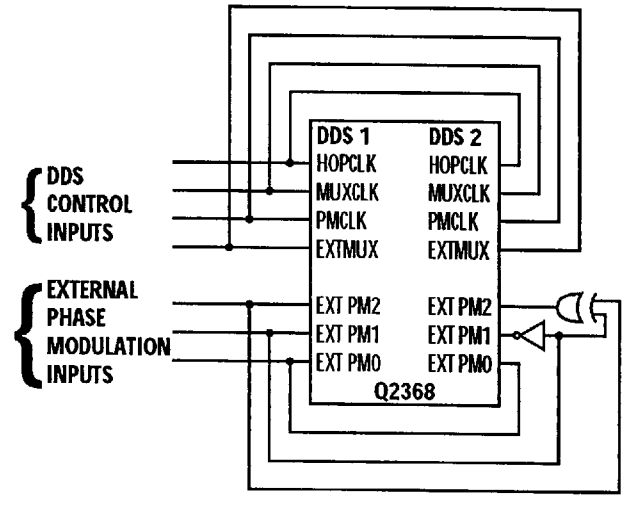


Figure 8b. Q2368 Quadrature Signal Implementation (Phase Modulated Quadrature Oscillator)



minimum resolution of $360°/2^{32}$. Since a microprocessor-controlled system can store open-loop compensation data vs. frequency, phase compensation can be made as an adjustment during equipment calibration. Alternatively, a closed-loop system can be constructed, given a suitable detector, which will allow feedback control of fine resolution offsets from quadrature for compensation of phase errors elsewhere in the system.

BINARY FREQUENCY SHIFT KEYING (BFSK) MODULATION MODE

Two PIRs are provided for each DDS function allowing for Binary Frequency Shift Keyed (BFSK) modulation without any additional hardware. The Q2368 provides signals allowing this switch to occur synchronously.

BFSK Modulation is achieved by setting the phase increment value in PIRA to generate the first frequency and the value in the PIRB to generate the second frequency. The EME bit in the SMC register is then set to logic "1" to enable the external multiplexer controls.

If the EXT MUX signal is set to logic "1" when the MUX CLK signal is asserted, the phase accumulator will choose the phase increment value from PIRB. If the EXT MUX signal is set to logic "0" when the MUX CLK is asserted, the phase accumulator will choose the phase increment value from PIRA. Changing the value of the EXT MUX input causes the alternation between the frequency controlled by PIRA and the frequency controlled by PIRB.

After the BFSK Mode is set up and the PIRA and PIRB contents are active, the EXT MUX signal can be changed as fast as the MUX CLK can be asserted. (See *External Control Timing* shown in Figure 20 and Table 18.) The MUX CLK timing is the only restriction on how fast the accumulation can be switched from PIRA to PIRB.

MINIMUM SHIFT KEYING (MSK) MODULATION MODE

The Minimum Shift Keying (MSK) Modulation Mode is a subset of the BFSK Mode described above. The operation is the same, but the two frequencies are selected at a known mathematically determined rate. The MSK Modulation Mode is linear MSK and can be generated by setting the frequency shift rate equal to the separation between the two frequencies. This is where MSK got its name, since it is the minimum spacing between the two frequencies that can be accomplished while still recovering the signal with a given shift rate. If the frequency spacing is closer than the frequency shift rate, the information cannot be recovered. If the spacing is too far apart, the information can be retrieved using FSK demodulation techniques, although MSK will not be generated from the resultant spectra. To produce the two MSK frequencies, the values in PIRA and PIRB correspond to incrementing and decrementing phase values (respectively) that must change through ±90 degrees for each symbol time of the frequency shift rate. This is obtained by loading PIRA and PIRB with frequency values such that the mid-point value between them is separated by ± FSK rate/2. This must occur without any phase discontinuities but since the DDS changes frequencies in a phase continuous fashion, this is not a problem. The overall result due to the slow phase transitions between the frequencies is a reduction in the high-frequency spectral content, thus attenuating the sidelobes. The spectrum is said to be more efficient since more power is contained in the main lobe and less in the sidelobes. The EME bit of the SMC register is set to logic "1", as in the BFSK Mode, and the EXT MUX and MUX CLK signals control the shift between the values of PIRA and PIRB.

FREQUENCY HOPPING MODE

Simple frequency hopping can be enabled by writing a new phase increment value of the desired frequency in PIRA. Since PIRA is a double buffered register, this value will be activated at the next assertion of the hop clock signal.

Assuming each frequency to be generated requires all 32 bits to be changed, then four 8-bit writes to PIRA would be needed if programming via 8-bit bus control is used. After PIRA has been loaded, the assertion of the hop clock will activate these settings and the resulting frequency will be output from the Q2368 within 32 clock cycles. The frequency value can be

changed as fast as the new phase increment value can be written to PIRA and a hop clock signal asserted. Once all 32 bits have been activated, the contents will remain until the register is written again. Subsets within the register may also be written. This allows for the changing of an existing register value using a single 8-bit write as opposed to four 8-bit writes, if programming via 8-bit bus control is used.

CHIRP MODE

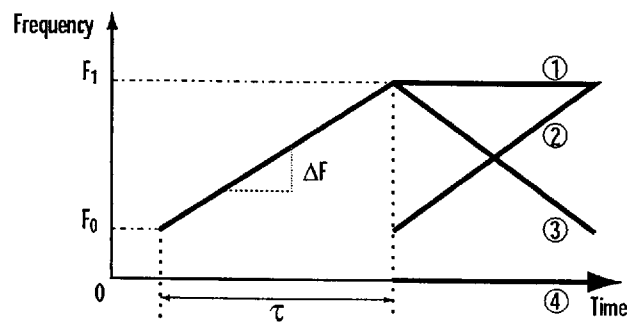
The Q2368 implements an additional mode in which a second-order phase accumulator process is used to implement a linearly changing frequency output. In this mode, the output frequency changes at a constant rate in an increasing or decreasing frequency direction. This linear frequency sweep mode is referred to as a "chirp" output. A chirp output can be described in terms of a start and stop frequency (F_0 and F_1, respectively) and the time it takes for the signal to travel between the two frequencies (τ).

CHIRP WAVEFORM VARIATIONS

The Q2368 can be operated to perform various chirp waveform sequences which will be determined by the actual design requirements involved. As an example, the chirp output can begin at F_0 as an upward ramping signal to F_1. When the signal reaches the stopping frequency, F_1, after τ seconds, the waveform can be controlled in many fashions as illustrated in Figure 9:

1. The signal can stop at F_1 and produce a constant F_1 value.
2. The signal can repeat itself, thus producing a sawtooth waveform.
3. The signal can begin a downramping waveform from F_1. When the signal reaches F_0, it can begin ramping up again (triangular waveform).
4. The signal can be reset to 0 (zero) frequency and phase to stop the output.

Figure 9. Q2368 Examples of Chirp Waveforms



CHIRP IMPLEMENTATION

The Chirp Mode requires two phase accumulators, cascaded serially, to create the linearly changing frequency output. To generate a chirp waveform, a linear frequency change is added to the first phase accumulator to produce an instantaneous frequency, f. The first accumulator's output is then integrated by the second accumulator to produce an instantaneous phase, $\phi = \int f dt$.

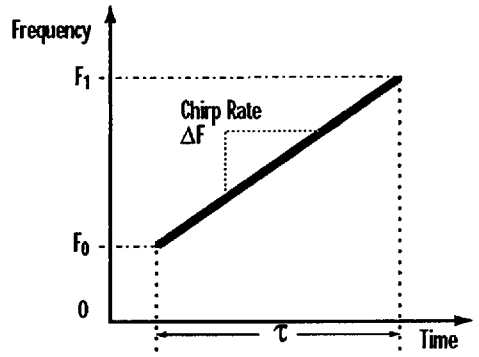
PROGRAMMABLE CHIRP RATE (PCR)

This feature provides for independent control of the chirp sweep rate and the output frequency. The limitations on the resolution of the sweep rate come from the system clock frequency and the size of the phase accumulator. The chirp rate control was implemented to allow the user to vary the slope of the chirp signal by varying the clock frequency used in the Chirp Mode. The programmable chirp rate introduces a 20-bit counter (PCR register) derived from the DDS clock reference to produce the chirp rate clock, F_{PCR}, for Accumulator A. In conjunction with the phase increment value in PIRA, this is used by the Q2368 to achieve < 1Hz/sec minimum chirp sweep rate over the entire clock speed range.

PIECEWISE LINEAR CHIRP

As mentioned earlier, if a strictly linear sweep is desired, the chirp output can be described in terms of a start and stop frequency and the time (τ) it takes for the signal to travel between the two frequencies, as shown in Figure 10. Alternatively, if the desired output response cannot be implemented in one chirp waveform, the programmable chirp rate control can be used to dynamically adjust the slope of the chirp response to achieve a near-parabolic or piecewise linear frequency output, as shown in Figure 11. This requires the assertion of a hop clock signal to affect the change in the PCR register which will change the

Figure 10. Q2368 Linear Chirp Waveform Example



chirp rate. However, because the HPME bit in the SMC register is enabled during Chirp Mode, a hop clock will also cause the contents of PIRB to be reloaded into Phase Accumulator A once and then switch back to PIRA. (See *Chirp Operations and Initialization* sections.)

In order to dynamically adjust chirp rate under this constraint, PIRB must be reloaded with the same value as PIRA and then the PCR register can be loaded with a new counter value during the chirp operation. All of this has to occur before the next hop clock signal is asserted to change the chirp rate, although subsequent changes to the PCR register value will not require reloading the PIRB value since it will remain as it was last programmed.

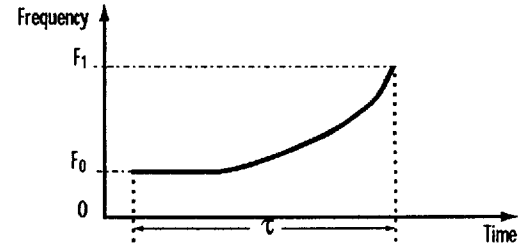
PROGRAMMABLE HOP CLOCK (PHC)

The Hop Clock command is used to activate new data information or enable the various operating modes. The Programmable Hop Clock Mode utilizes the Hop Clock command by introducing a programmable 32-bit duration counter (PHC register) derived from the DDS clock reference to produce the PHC time period, T_{PHC}. This is used by the Q2368 as a built-in timer function which allows precision timed intervals of the Hop Clock command to be automatically and continuously reasserted at the pre-programmed time intervals.

BURP CONTROL

The Q2368's BURP control function allows instant interruption of operating modes to produce a stationary (fixed) output. BURP control is active when it is set to a logic "High". When operating in the

Figure 11. Q2368 Piecewise-Linear Chirp Waveform



Chirp Mode, enabling the BURP signal will produce a constant output frequency corresponding to the exact position of where the chirp waveform was interrupted. In the same manner, the Programmable Hop Clock Mode is simultaneously interrupted when the BURP signal is enabled which allows the programmed time interval, T_{PHC}, to be maintained irrespective of the BURP interruption time, as illustrated in Figure 12. Moreover, all chirp operations transition in a phase-continuous fashion when the BURP control is enabled or disabled.

CHIRP OPERATIONS AND INITIALIZATION

To initiate a chirp waveform, the HPME bit and the CHE bit in the SMC register must be set to a logic "1" and the accumulators reset (assert the ARR or ARE/). Enabling the HPME bit allows the one time accumulation of the contents of PIRB. When the hop clock signal is activated, both phase accumulator contents reset to "0", and the first accumulator adds the contents of PIRB for one cycle of the system clock, F_{CLK}, and then adds the increment value of PIRA for each subsequent cycle of the chirp rate clock, F_{PCR}. PIRB contains the $\Delta\phi$ value of F_0, so the chirp output signal will begin at F_0 with the HPME bit enabled and PIRA contains the delta frequency value (frequency step size). The CHE bit enables the second phase accumulator, thus enabling the function to produce the frequency ramp. The PCR register contains the counter value which divides the system clock to produce the chirp rate clock, F_{PCR}. The result will be an output frequency ramp with a designated starting frequency (PIRB), frequency resolution (PIRA), and chirp sweep rate, ΔF_{RATE}. The frequency output from the Q2368 will continue to change at the programmed rate until the next assertion of the hop clock resets any

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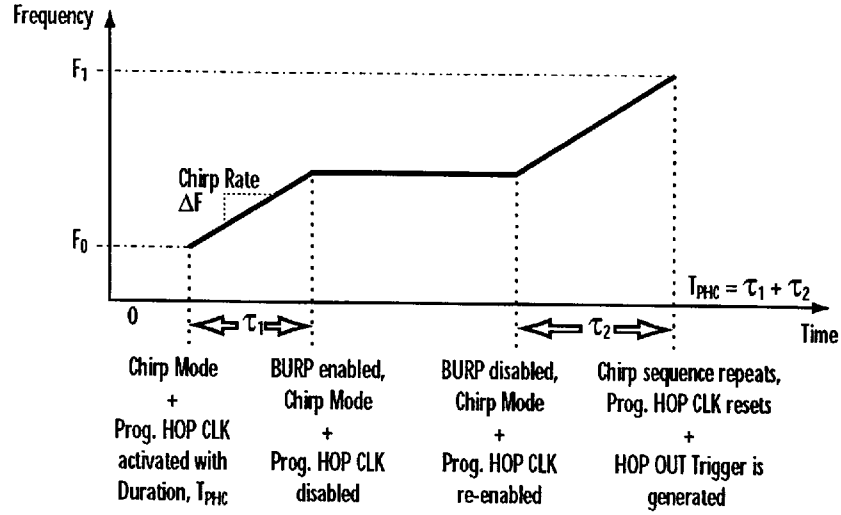
Figure 12. Q2368 BURP Function Illustrated



conditions. The external phase modulation capabilities of the Q2368 can be used while in the Chirp Mode, so the External Phase Modulation Enable (EPME) bit in the SMC register can be set as desired. However, the External Mux Enable (EME) bit in the SMC register should be set to a logic "0".

The HPME and CHE bits must remain "High" as long as a chirp output is desired. When supply voltage is first applied, the Q2368's internal registers emerge in a random state which necessitates proper loading of the AMC and SMC registers, and resetting the accumulators. The accumulator reset must be enabled to clear the contents of both phase accumulators at the beginning of every chirp waveform. If the accumulator reset is not enabled at the beginning of a chirp, then the output signal will begin at a value that will equal the contents of the second phase accumulator plus the PIRB value. To ensure a correct waveform, assert the accumulator reset at the beginning of each chirp waveform. Note that the waveform will not be phase continuous when the accumulator reset is used.

PROGRAMMING OPERATIONS FOR CHIRP MODE

To begin a chirp at F_0, the associated phase increment value ($\Delta\phi$) must be loaded into the PIRB. The $\Delta\phi$ value is calculated in the normal fashion using equation (1),

$$\Delta\phi_B = (F_0 \cdot 2^N)/F_{CLK} \quad (1)$$

The chirp frequency resolution (or frequency step size) is equal to:

$$\Delta F_{RES} = \Delta\phi_A \, (F_{CLK}/2^N) \text{ Hz} \quad (2)$$

Where

F_0 = starting frequency value.

$\Delta\phi_B$ = the phase increment value in PIRB which corresponds to the chirp starting frequency.

N = # of phase bits in Accumulator 2

F_{CLK} = the system clock frequency (i.e., SYS CLK for Dual Mode operation, and DUB CLK/2 for Double Mode operation).

$\Delta\phi_A$ = the phase increment value in PIRA which controls the amount of output frequency change with each Accumulator 1 clock cycle.

The desired switching speed associated with the given chirp frequency resolution, ΔF_{RES}, is equal to:

$$\Delta F_{PCR} = F_{CLK}/(PCR+1) \text{ Hz} \quad (3)$$

Where

PCR = the preset value of the 20-bit chirp rate counter to generate F_{PCR}.

The chirp switching speed is sometimes referred to as the "dwell time" of the incremental ΔF_{RES} frequencies and is equivalent to $1/\Delta F_{PCR}$.

The chirp sweep rate (or chirp ramp rate) is equal to:

$$\Delta F_{RATE} = \Delta F_{RES} \cdot \Delta F_{PCR}$$
$$= \Delta\phi_A \, (F_{CLK})^2/[(PCR+1) \cdot 2^N] \text{ Hz/sec} \quad (4)$$

The smallest non-zero slope for a constant clock period is obtained when the phase increment value in PIRA = 1, resulting in a minimum sweep rate of:

$$\Delta F_{RATE} \text{ minimum} = (F_{CLK})^2/[(PCR+1) \cdot 2^N] \text{ Hz/sec} \quad (5)$$

The determination of the ΔF_{RATE} parameters ensures that the appropriate frequency rate will occur between F_0 and F_1 in the specified duration, τ, as redefined below:

$$\Delta F_{RATE} = |F_1 - F_0|/\tau \quad \text{Hz/sec} \quad (6)$$

Since PIRA is used to store the frequency resolution associated with the desired ramp, the value of $\Delta\phi_A$ will be an integer representing a multiple value of the minimum resolution and hence determines the *frequency granularity* of the corresponding chirp waveform. This concept can be useful as a relative measure in deciding how granular or "smooth" a chirp waveform should be made for a given application. By substituting in equations (4) and (6), the value of $\Delta\phi_A$ can also be determined as:

$$\Delta\phi_A = [(PCR+1) \cdot 2^N \cdot |F_1 - F_0|] / [(F_{CLK})^2 \cdot \tau] \quad (7)$$

The specified duration, τ, over which a given chirp sequence is directed, can be controlled very precisely by the programmable hop clock. In this mode, the 32-bit PHC register is loaded with the corresponding value to count the number of system clock periods before another hop clock command gets automatically issued and activates the latest instruction routine programmed to follow. The preset value of the 32-bit counter corresponding to the desired chirp duration is determined using the following relation:

$$PHC = [(\tau/T_{CLK}) - 1] \quad (8)$$

Where

$T_{CLK} = 1/F_{CLK}$

$\tau = T_{PHC}$ = the desired PHC time period

LIMITS ON THE CHIRP SEQUENCE DURATION, τ

τ has underlying restrictions that must be considered when implementing a chirp output. The user must make sure that the duration (τ) will be long enough so the changes for the next output waveform can be implemented before the chirp signal reaches its stopping frequency. For example, if the user wants to change the chirp to begin at a new frequency and have a new stopping point, then the device must be reset to do so. This change would require re-loading PIRA and PIRB, which requires up to eight 8-bit write functions using 8-bit bus control. The accumulator reset must also be reset and a hop clock is needed to activate all of the new settings. Therefore, τ must be set accordingly to accommodate for the minimum timing needed to make these changes.

CHANGING FROM A CHIRP WAVEFORM TO A NON-CHIRP WAVEFORM

When the HPME bit is set to a logic "1", the hop clock signal is internally extended to two system clock cycles. The two system clock cycles make it possible for the phase accumulator to add the contents from PIRB once, and then switch the process immediately back to PIRA.

In order to change the output signal from a chirp to a non-chirp waveform, the HPME bit and the CHE bit in the SMC register must be disabled by setting them to a logic "0". The hop clock command is required to initiate this change and during the HPME's transition from "1" to "0", the hop clock signal is correspondingly extended to two system clock cycles. This results in an automatic switch of the accumulation process back to PIRA. The CHE bit is used for chirp waveform generation only and should be disabled whenever a non-chirp waveform is desired. It is necessary to reset the HPME to "0" in the case when you want to stop Chirp Mode, or disable the Internal Phase Modulation Mode and reconfigure operation to the Basic Oscillator Mode, for example. If phase offsetting control is desired, as in the case of operating in the Internal Phase Modulation Mode, then the HPME bit should remain set to a logic "1".

Additionally, it is worth noting that while operating

in the Chirp Mode, a non-chirp waveform can be instantly achieved by utilizing the BURP control function. The BURP signal allows independent interruption of the chirp function without losing phase continuity since the accumulator reset function does not have to be employed. The Chirp Mode, however, is still activated and is merely being suspended to a fixed frequency state until BURP is disabled.

Table 11. Q2368 Control Inputs vs. Latency Affect

Control Signal	Latency Affect in # of System Clock Cycles (t_{cyc})*
Hop Clock	31 - 32 to DAC BIT or DUB OUT Outputs; 3 for Activated Power-down State
MUX CLK	31 - 32 to DAC BIT or DUB OUT Outputs
PM CLK	21 - 22 to DAC BIT or DUB OUT Outputs
BURP	20 - 21 to DAC BIT or DUB OUT Outputs; 1 - 2 for PHC Counter 1 - 2 for PCR Counter

* When operating in Dual Mode, t_{cyc} = the equivalent number of SYS CLK cycles.
When operating in Double Mode, multiply t_{cyc} by 2.

PIPELINE DELAY

Table 11 shows the associated latency for the affect by the hop clock, PM CLK, or MUX CLK control signals on the DDS outputs. Also included is the latency for the affect of the BURP control signal on the DDS outputs and PHC and PCR registers, and the affect of hop clock when activating the Power-down Mode.

A one system clock ambiguity occurs because the MUX CLK, PM CLK, BURP, and hop clock signals are allowed to be asynchronous in relation to the system clock. To keep the internal operation of the Q2368 synchronous, the signals are input to synchronizing circuitry which resolves the signal to within one clock period.

TYPICAL EXAMPLES AND INITIAL SETUP OPERATIONS

The Q2368 offers many flexible and powerful operational modes, each of which requires a slightly varying setup to implement. These examples are intended to assist the designer in understanding the "flow" of these setup procedures.

During the following examples, it is assumed that the device is operated in Dual Mode with the DDS1 function being used, and the method of programming is via the 8-bit Bus Mode. It is also assumed that the NRC circuit is to be used and that these applications are implementing a 12-bit wide D/A converter using offset binary notation and the DAC STB/ (DAC STB Invert) is used. If your application differs from the above specifications, please make the appropriate changes. Some specific configuration steps and additional setup comments, which are common to all the modes of operation, are listed below:

1. Set the configuration of the D/A converter into the Asynchronous Mode Control (AMC) register, address "09" (hex). This is accomplished by writing a value of "8E" (hex) to address "09". This sets the AMC register value to operate with an Offset Binary notation D/A converter which is 12-bits wide and is triggered by the DAC STB/ signal.
2. Set the configuration of the SMC register in a known state such that the Power-down Enable bit (PWDE) is set to "0". This will prevent the PWDE bit from enabling an unwanted power-down condition since the Q2368 registers come up in a random state after supply voltage is first applied. This is accomplished by writing a value of "00" (hex) to address "08".
3. The DDS accumulator may be reset to a zero-phase output by "arming" the Asynchronous Reset Register (ARR). This step is performed by writing any data value to address "0A" (hex) . Alternatively, the ARE1/ input pin could be set to a logic "Low". This reset function will become active at the next hop clock signal and essentially gives the output signal a zero-phase starting point.
4. None of the settings written to the Q2368 DDS will be activated until the assertion of a hop clock signal (with the exception of the AMC register). This may be performed by pulsing the HOP CLK signal to an active "High" according to the timing requirements shown in the *Timing Specifications* section. Alternatively, this assertion of the hop

clock signal may be performed by writing any data value to the Asynchronous Hop Clock (AHC) register (address "0B" (hex)).

SIMPLE OSCILLATOR MODE

When using the Simple Oscillator Mode, the Q2368 DDS outputs a digitized sine wave at a fixed frequency ranging from essentially D.C. to ½ the frequency of SYS CLK. Practical limitations on anti-alias filtering will limit the range of frequencies to a maximum of approximately 40% of the SYS CLK frequency.

During the following example, the desired output frequency is ¼ of the SYS CLK frequency. That is, if the SYS CLK frequency is 30 MHz, the desired output frequency is 7.5 MHz. The following steps should be followed:

1. Set the mode of the device to be the Simple Oscillator Mode. Setting the operation mode is accomplished by disabling all modes in the Synchronous Mode Control (SMC) register, address 08(hex). In this case, the value of "00" (hex) should be loaded into this device. This is performed by setting the address bus (ADDRESS0 through ADDRESS5) to "08" and the data bus (DATA0 through DATA7) to "00". Set the Chip Select signal (CS/) to active "0" and pulse the Write Strobe (WR/) "Low" according to the timing requirements shown in Figure 16 and Table 14. The PMAE bit D6 of the AMC register is set to "0" because the internal phase modulation operation is disabled.
2. The actual phase increment value (32-bits) is next loaded into the Phase Increment Register A (PIRA), addresses "00" through "03" (hex). The least significant byte of the 4-byte value is written into address "00" and the most significant byte is written into address "03". The write operations are performed using the process described in Step 1 and four. Such operations are required to load all four byte-wide PIRA register addresses. For this example of a desired output frequency which is ¼ of the SYS CLK frequency, the 32-bit value to be written to PIRA is "40000000" (hex). In this case, the registers at address "00", "01", and "02" are written with a data value of "00" while address "03" is written with a data value of "40" (hex).
3. The assertion of a hop clock signal will cause the Q2368 to begin synthesizing an unmodulated sine wave at a frequency equal to ¼ the frequency of the SYS CLK input.

BINARY FREQUENCY SHIFT KEYING (BFSK) MODE

The following procedure will initialize the Q2368 to operate in the BFSK Mode. For this example, the desired frequencies to be generated are ¼ and ⅛ of the SYS CLK frequency. That is, if the SYS CLK frequency is 30 MHz, the desired output frequencies are 7.5 MHz, and 3.75 MHz respectively.

It is assumed that the phase increment value associated with generating 7.5 MHz will be stored in PIRA and 3.75 MHz will be stored in PIRB. The following steps should be followed:

1. Setting up the BFSK Mode is accomplished by disabling all modes in the Synchronous Mode Control (SMC) register, address "08" (hex) except EXT MUX ENABLE (EME) bit D2. The EME bit should be set to logic "1". In this case, the value of "04" (hex) should be loaded into this device. This is performed by writing the address bus (ADDRESS0 through ADDRESS5) with a data value of "08" (hex) and the data bus (DATA0 through DATA7) with a data value of "04" (hex). The PMAE bit D6 of the AMC register is set to "0" because the internal phase modulation operation is disabled.
2. The actual phase increment values (32-bits) are loaded into their respective Phase Increment Register. For PIRA, use addresses "00" through "03" (hex) and for PIRB use addresses "04" through "07" (hex). The least significant byte (LSB) of the 4-byte value is written into address "00" (PIRA) or "04" (PIRB) and the most significant byte (MSB) is written into address "03" (PIRA) or "07" (PIRB). Since the phase increment registers are 32-bits wide, four such operations are required to load all four byte-wide PIRA and PIRB register addresses.

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For this example, the 32-bit phase increment value written to PIRA is "40000000" (hex). In this case, the registers at address "00", "01", and "02" are written with a data value of "00" while address "03" is written with a data value of "40" (hex). The 32-bit phase increment value to be written to PIRB is "2000000" (hex). In this case, the registers at address "04", "05", and "06" are written with a data value of "00" while address "07" is written with a data value of "20" (hex).

3. The EME bit is set to logic "1" to enable the external multiplexer controls. This will make the settings at the EXT MUX1 pin (pin 61) select which PIR to use for accumulation purposes. If EXT MUX1 is set to logic "1", then PIRB will be accumulated. If it is set to logic "0", then the contents of PIRA will be accumulated.

EXTERNAL PHASE MODULATION MODE

When using the External Phase Modulation Mode, the Q2368 DDS has the capability to shift its output signal in 45° increments from 45° to 315°. Since the Q2368 is a dual device, it is ideal to use as a quadrature oscillator because it requires only one Q2368 device; this is further described in the *Quadrature Signal Generation* section.

The following procedure will initialize the Q2368 to operate in the External Phase Modulation Mode. The desired phase shift will be 90° for this example (see Table 6 for other phase settings) and the frequency to be generated is ¼ of the SYS CLK frequency. That is, if the SYS CLK frequency is 30 MHz, the desired output frequency is 7.5 MHz.

The following steps should be followed:

1. Setting the operation mode is accomplished by disabling all modes in the Synchronous Mode Control (SMC) register, address 08(hex) except EXT PHASE MOD ENABLE (EPME) bit D1. The EPME bit should be set to logic "1". In this case, the value of "02" (hex) should be loaded into this device. This is performed by writing the address bus (ADDRESS0 through ADDRESS5) with a data value of "08" and the data bus (DATA0 through DATA7) with a data value of "02". The PMAE bit D6 of the AMC register is set to "0" because the internal phase modulation operation is disabled.
2. The actual phase increment value (32-bits) is loaded into the Phase Increment Register A (PIRA), addresses "00" through "03" (hex). The least significant byte (LSB) of the 4-byte value is written into address "00" and the most significant byte (MSB) is written into address "03". The desired output frequency is ¼ of the SYS CLK frequency; the 32-bit value to be written to PIRA is "40000000" (hex). In this case, the registers at address "00", "01", and "02" are written with a data value of "00" while address "03" is written with a data value of "40" (hex).
3. To affect the 90° phase shift, set PM1 EXT BIT2, PM1 EXT BIT1, PM1 EXT BIT0 to 0 1 0 respectively. (See Table 6 for the settings.) These inputs are latched into the DDS by pulsing the signal PM1 CLK "High" according to the timing specifications in Figure 20 and Table 18.

FREQUENCY HOPPING MODE

The example of frequencies to be hopped between are 1/16, ⅛ and ¼ of the SYS CLK frequency. That is, if the SYS CLK frequency is 30 MHz, the desired frequencies are 1.875 MHz, 3.75 MHz, and 7.5 MHz respectively.

It is assumed that the first frequency to be generated will be 1.875 MHz, then 3.75 MHz and last 7.5 MHz. The user can hop between as many different frequencies as desired, however for example purposes we will limit the number to three. The following steps should be followed:

1. Setting the operation mode is accomplished by disabling all modes in the Synchronous Mode Control (SMC) register, address 08(hex). In this case, the value of "00" (hex) should be loaded into this device. This is performed by writing the address bus (ADDRESS0 through ADDRESS5) with a data value of "08" and the data bus (DATA0 through DATA7) with a data value of "00". The PMAE bit D6 of the AMC register is set to "0" because the internal phase modulation operation is disabled.

2. The actual phase increment value (32-bits) is loaded into the Phase Increment Register A (PIRA), addresses "00" through "03" (hex). The least significant byte (LSB) of the 4-byte value is written into address "00" and the most significant byte (MSB) is written into address "03". For this example, three frequencies are to be generated in succesion. The first 32-bit value to be written to PIRA is "10000000" (hex). The second 32-bit value to be written to PIRA is "20000000" (hex) and the third is "40000000". Note, that in this case the last 24-bits of each three phase increment values are the same. Once the first 32-bit value has been written to the PIRA, all you have to do is change the 8 MSB to generate the three designated frequencies. (The 24 LSB will remain the same until they are re-written and activated by the hop clock signal.) In this case, initially the registers at address "00", "01", and "02" are written with a data value of "00" while address "03" is written with a data value of "10" (hex). To hop from 1/16 to 1/8 of the SYS CLK, address "03" is written with a data value of "20" (hex). The same operation is followed to hop between 1/8 and 1/4 of the SYS CLK frequency: address "03" is written with a data value of "40" (hex). If the hopping frequencies did not have any bits in common, then all 32-bits of PIRA would need to be re-written according to the instructions above.

INTERNAL PHASE MODULATION MODE

When using the Internal Phase Modulation Mode, the Q2368 DDS has the capability to shift its output signal in 84 nano-degree increments ($360°/2^{32}$) throughout the complete 360° range. The phase shift can occur as often as the HOP CLK signal can be asserted according to the timing requirements shown in Figure 16 and Table 14.

The following procedure will initialize the Q2368 to operate in the Internal Phase Modulation Mode to output a synchronous preset frequency and phase. The intended starting phase offset will be 5° for this example and the frequency to be generated is 19.14 MHz using a SYS CLK frequency of 50 MHz.

The following steps should be followed:

1. Setting the operation mode is accomplished by disabling all modes in the Synchronous Mode Control (SMC) register, address 08 (hex) except HOP CLK PHASE MOD ENABLE (HPME) bit D3. The HPME bit should be set to logic "1". In this case, the value of "08" (hex) should be loaded into this device. This is performed by writing the address bus (ADDRESS0 through ADDRESS5) with a data value of "08" and the data bus (DATA0 through DATA7) with a data value of "08".
2. The actual phase increment values (32-bits) are loaded into their respective Phase Increment Register. For PIRA, use addresses "00" through "03" (hex) and for PIRB use addresses "04" through "07" (hex). The least significant byte (LSB) of the 4-byte value is written into address "00" (PIRA) or "04" (PIRB) and the most significant byte (MSB) is written into address "03" (PIRA) or "07" (PIRB). For this example, the 32-bit phase increment value to be written to PIRA is "61FF2E49" (hex). In this case, the registers at address "00", "01", "02", and "03" are written with a data value of "49", "2E", "FF", and "61" (hex), respectively. The 32-bit phase increment value to be written to PIRB is "658D672D" (hex) according to the Internal Phase Modulation description under the *Modes of Operation* section. In this case, the registers at address "04", "05", "06", and "07" are written with a data value of "2D", "67", "8D", and "65" (hex), respectively.
3. The DDS accumulator should be cleared to cause the intended starting phase offset to begin with respect to a zero-phase reference position. This is performed by writing any data value to address "0A" (hex).
4. The PMAE bit D6 of the AMC register is set to "0" because the internal phase modulation operation will be utilizing all 32 bits of PIRB for the accumulation. If only 8-bit phase resolution is required (i.e., 256-state, 1.41° resolution minimum), then PMAE is set to "1" to utilize only the most significant byte of the PIRB.

CHIRP MODE

The following examples are some commonly implemented chirp waveform types. Since the methodology of programming the Q2368 has already been outlined in the preceding cases, the emphasis here is to show the step-by-step calculations of the chirp parameters for a given sequence. Each example will also include a chronology of the basic initialization commands and instruction set to obtain a repeating chirp sequence. (Additional reference is found under *Modes of Operation* in the *Chirp Mode* section.)

EXAMPLE 1. INCREMENTING CHIRP (POSITIVE SAWTOOTH WAVEFORM)

Figure 13 illustrates this example.

Given F_{CLK} = 50 MHz, F_0 = 5 MHz, F_1 = 10 MHz, ΔF_{RES} = 1 kHz, ΔF_{PCR} = 1 MHz, repeat

(a) Using equation 1, the starting frequency delta value is:
$\Delta\phi_B = (F_0 \cdot 2^N)/F_{CLK} = (5\ MHz \cdot 2^{32})\ /50\ MHz$
= 429496729.6 = 19999999 (H)
This value is loaded into PIRB.

(b) Rearranging equation (2), the frequency resolution delta value is:
$\Delta\phi_A = \Delta F_{RES}\ /(F_{CLK}\ /2^N) = (1\ kHz \cdot 2^{32})/50\ MHz$
= 85899.3 = 14F8B (H)
This value is loaded into PIRA.

(c) Rearranging equation (3), the chirp rate counter value is:
$PCR = [F_{CLK}\ /\Delta F_{PCR}]-1 = [50\ MHz/1\ MHz] - 1$
= 49 = 31 (H)
This value is loaded into the PCR register.

(d) Using equation (4), the chirp sweep rate value is:
$\Delta F_{RATE} = \Delta F_{RES} \cdot \Delta F_{PCR} = 1\ kHz \cdot 1\ MHz$
= 1 GHz/sec

(e) Rearranging equation (6), the required chirp sweep time is:
$\tau = |\ F1 - F0\ |\ /\Delta F_{RATE}$
$= |\ 10\ MHz - 5\ MHz\ |\ /1\ GHz/sec$
= 5 msec

(f) Using equation (8), the programmable hop clock counter value is:
$PHC = [(\tau/T_{CLK}) -1] = [(5\ msec/20\ nsec)] - 1$
= 244999 = 3D08F (H)
This value is loaded into the PHC register

INITIALIZATION COMMANDS

AMC: Desired Output Format, NRC status, & DAC STB

SMC: Load "00" (hex) to register. This step is optional at this point but is a good practice to prevent an unwanted power-down condition.

Accumulator Reset: ARR or ARE/ armed

Assert Hop Clock: HOP CLK signal or AHC register

INSTRUCTION SET FOR REPEATING SEQUENCE

SMC: HPME, CHE, & PHCE enabled; PWDE, EME, & EPME disabled

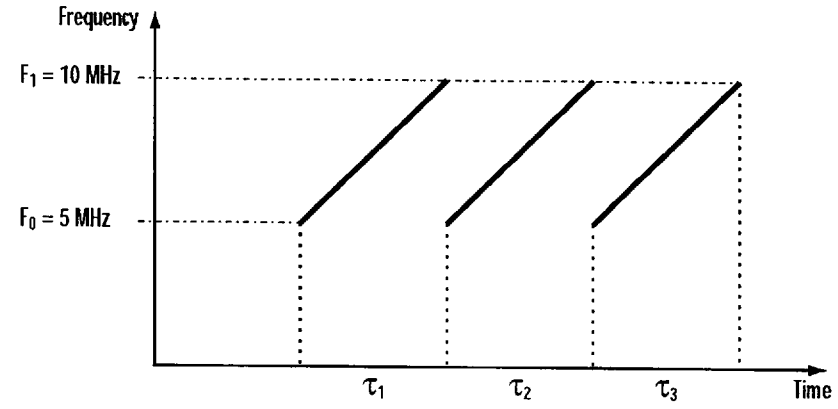
PIRA

PIRB

PHC

PCR

Figure 13. Q2368 Incrementing Chirp Example



Assert starting Hop Clock: HOP CLK signal or AHC register

Accumulator Reset: Since the programmable hop clock will be automatically asserted at each PHC *time interval*, T_{PHC} , the ARR must be written to before each PHC period for the sequence to repeat itself. Alternatively, the ARE/ pin may be pulled "Low".

EXAMPLE 2. DECREMENTING CHIRP (NEGATIVE SAWTOOTH WAVEFORM)

Figure 14 illustrates this example.

Given F_{CLK} = 50 MHz, F_0 = 10 MHz, F_1 = 5 MHz, ΔF_{RES} = 1 kHz, ΔF_{PCR} = 1 MHz, repeat

(a) Using equation (1), the starting frequency delta value is:
$\Delta\phi_B = (F_0 \cdot 2^N)/F_{CLK} = (10\ MHz \cdot 2^{32})/50\ MHz$
$= 858993459 = 33333333$ (H)
This value is loaded into PIRB.

(b) Since it is a negative chirp, the 2's complement of $\Delta\phi_A$ must be taken.
Rearranging equation (2), the frequency resolution delta value is:
$\Delta\phi_A = \Delta F_{RES}/(F_{CLK}/2^N) = (1\ kHz \cdot 2^{32})/50\ MHz$
$= 85899.3 = 14F8B$ (H)
2's complement $\Delta\phi_A = (2^{32} - \Delta\phi_A) =$ FFFEB075
The 2's complement $\Delta\phi_A$ value is loaded into PIRA.

(c) Rearranging equation (3), the chirp rate counter value is:
$PCR = [F_{CLK}/\Delta F_{PCR}]-1 = [50\ MHz/1\ MHz] - 1$
$= 49 = 31$ (H)
This value is loaded into the PCR register.

(d) Using equation (4), the chirp sweep rate value is:
$\Delta F_{RATE} = \Delta F_{RES} \cdot \Delta F_{PCR} = 1\ kHz \cdot 1\ MHz$
$= 1$ GHz/sec

(e) Rearranging equation (6), the required chirp sweep time is:
$\tau = |F_1 - F_0|/\Delta F_{RATE}$
$= |5\ MHz - 10\ MHz|/1\ GHz/sec = 5$ msec

(f) Using equation (8), the programmable hop clock counter value is:
$PHC = [(\tau/T_{CLK}) - 1] = [(5\ msec/20\ nsec)] - 1$
$= 244999 = 3D08F$ (H)
This value is loaded into the PHC register.

INITIALIZATION COMMANDS

AMC: Desired Output Format, NRC status, & DAC STB

SMC: Load "00" (hex) to register. This step is optional at this point but is a good practice to prevent an unwanted power-down condition.

Accumulator Reset: ARR or ARE/ armed

Assert Hop Clock: HOP CLK signal or AHC register

INSTRUCTION SET FOR REPEATING SEQUENCE

SMC: HPME, CHE, & PHCE enabled; PWDE, EME, & EPME disabled

PIRA

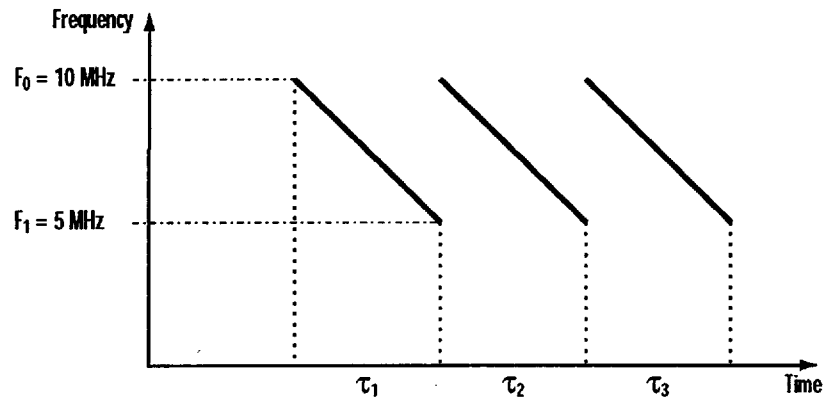
PIRB

PHC

PCR

Assert starting Hop Clock: HOP CLK signal or

Figure 14. Q2368 Decrementing Chirp Example



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AHC register

Accumulator Reset: Since the programmable hop clock will be automatically asserted at each PHC time interval, T_{PHC} , the ARR must be written to before each PHC period for the sequence to repeat itself. Alternatively, the ARE/ pin may be pulled "Low".

EXAMPLE 3. INCREMENTING AND DECREMENTING CHIRP (TRIANGULAR WAVEFORM)

Figure 15 illustrates this example.

Given F_{CLK} = 50 MHz, F_0 = 5 MHz, F_1 = 10 MHz, then reverse with F_0 = 10 MHz, F_1 = 5 MHz, ΔF_{RES} = 1 kHz, ΔF_{PCR} = 1 MHz, repeat:

(a) The determination of the chirp parameters will follow the same calculations performed through both Examples 1 & 2. This results, in effect, to joining these chirp sequences together which creates the triangular chirp waveform. The primary distinction between this and generating a sawtooth chirp will be in the setup of the instruction set to sequence from an incrementing chirp to a decrementing chirp and then repeat. Whereas in the first two examples the chirp waveform itself was never altered except to repeat the sequence, in this example the chirp waveform is changing before the sequence gets repeated. This will naturally mean writing additional instructions during each PHC time interval in comparison to the previous cases.

INITIALIZATION COMMANDS

AMC: Desired Output Format, NRC status, & DAC STB

SMC: Load "00" (hex) to register. This step is optional at this point but is a good practice to prevent an unwanted power-down condition.

Accumulator Reset: ARR or ARE/ armed

Assert Hop Clock: HOP CLK signal or AHC register

INSTRUCTION SET FOR REPEATING SEQUENCE

SMC: HPME, CHE, & PHCE enabled; PWDE, EME, & EPME disabled

PHC

PCR

Begin Sequence #1

PIRA: Value for Incrementing Chirp

PIRB: Value for Incrementing Chirp

End Sequence #1

Assert starting Hop Clock: HOP CLK signal or AHC register

Begin Sequence #2

PIRA: Value for Decrementing Chirp

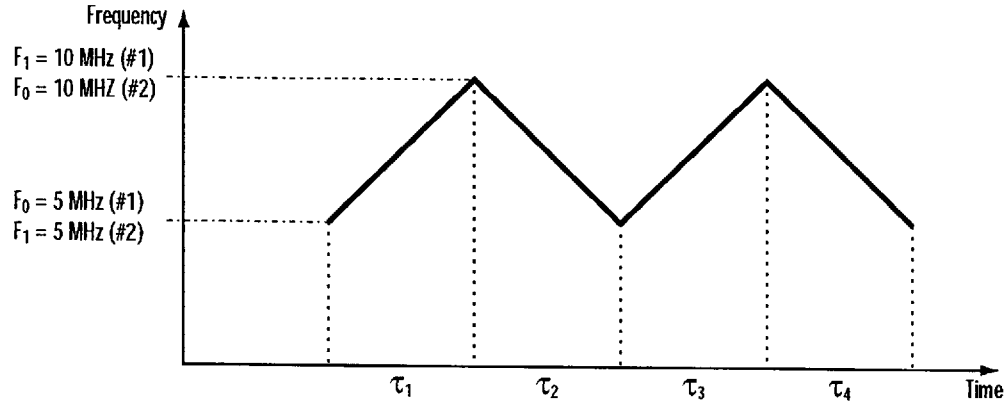
PIRB: Value for Decrementing Chirp

End Sequence #2

Sequence #1/Sequence #2: From this point on sequence #1 and sequence #2 are programmed alternately before each PHC time interval.

Accumulator Reset: The accumulator reset must also be armed before each PHC period. For this application it is easiest to pull the ARE/ pin "Low" before each PHC period.

Figure 15. Q2368 Incrementing and Decrementing Chirp Example



EXAMPLE 4. INCREMENTING CHIRP IN DOUBLE MODE (POSITIVE SAWTOOTH WAVEFORM)

Given F_{CLK} = 100 MHz, F_0 = 20 MHz, F_1 = 40 MHz, ΔF_{RES} = 100 Hz, ΔF_{PCR} = 5 MHz, repeat. Note that when operating in Double Mode, the effective value for F_{CLK} is DUB CLK/2, therefore F_{CLK} = 100 MHz/2 for all associated calculations.

(a) Using equation (1), the starting frequency delta value is:
$\Delta\phi_B = (F_0 \cdot 2^N)/F_{CLK} = (20\ MHz \cdot 2^{32})/50\ MHz$
= 1717986918 = 66666666 (H)
This value is loaded into PIRB.

(b) Rearranging equation (2), the frequency resolution delta value is:
$\Delta\phi_A = \Delta F_{RES}/(F_{CLK}/2^N) = (100\ Hz \cdot 2^{32})/50\ MHz$
= 8589.9 = 218D (H)
This value is loaded into PIRA.

(c) Rearranging equation (3), the chirp rate counter value is:
$PCR = [F_{CLK}/\Delta F_{PCR}]-1 = [50\ MHz/5\ MHz] - 1$
= 9 = 9 (H)
This value is loaded into the PCR register.

(d) Using equation (4), the chirp sweep rate value is:
$\Delta F_{RATE} = \Delta F_{RES} \cdot \Delta F_{PCR} = 100\ Hz \cdot 5\ MHz$
= 500 MHz/sec

(e) Rearranging equation (6), the required chirp sweep time is:
$\tau = |F_1 - F_0|/\Delta F_{RATE}$
= | 40 MHz - 20 MHz | /500 MHz/sec
= 40 msec

(f) Using equation (8), the programmable hop clock counter value is:
$PHC = [(\tau/T_{CLK}) -1] = [(40\ msec/20\ nsec)] - 1$
= 1999999 = 1E847F (H)
This value is loaded into the PHC register.

INITIALIZATION COMMANDS

AMC (DDS1): Desired Output Format, NRC status, & DAC STB
AMC (DDS2): Same as for DDS1
SMC (DDS1): Load "00" (hex) to register.
SMC (DDS2): Load "00" (hex) to register.
Accumulator Reset (DDS1): ARR or ARE/ armed
Accumulator Reset (DDS2): ARR or ARE/ armed
Assert Hop Clock (DDS1): HOP CLK signal or AHC register to both DDSs
Assert Hop Clock (DDS2): HOP CLK signal or AHC register to both DDSs

INSTRUCTION SET FOR REPEATING SEQUENCE

Same as for Examples 1 & 2; performed on DDS1.

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TECHNICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 12 shows the absolute maximum ratings, and Table 13 shows the operating ranges of the Q2368. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 12. Q2368 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Storage Temperature	T_S	-65	+150	°C	–
Junction Temperature	T_J	–	+150	°C	–
Voltage on any Input or Output Pin	–	-0.3	V_{DD} + 0.3	V	–
Supply Voltage	V_{DD}	-0.3	+7.0	V	–
I/O Electrostatic Discharge Protection	V_{ESD}	-2000	+2000	V	1
I/O Latch-up Trigger Current Protection	I_{IN}	-150	+150	mA	2

Notes:

1. Test method meets the intent MIL-STD-883C Method 3015.
2. Test method meets the intent of JEDEC STD 17 publication. This is the maximum allowable current flow through the input and output protection devices.

Table 13. Q2368 Operating Range

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNITS	NOTES
Operating Temperature (Ambient)	T_A	-40	–	+85	°C	–
Operating Supply Voltage	V_{DD}	4.5	–	5.5	V	–
Junction to Ambient Resistance	θ_{JA}	–	51	–	°C/W	1
Junction to Case Resistance	θ_{JC}	–	14	–	°C/W	2

Notes:

1. θ_{JA} measured in still-air room temperature test conditions.
2. θ_{JC} measured with package held against an "infinite" heatsink test condition.

DC ELECTRICAL CHARACTERISTICS

Table 14 shows the DC electrical characteristics for the Q2368.

Table 14. Q2368 DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
High-Level Input Voltage, TTL	V_{IHT}	2.0	V_{DD} + 0.3	V	–
Low-Level Input Voltage, TTL	V_{ILT}	-0.3	0.8	V	–
High-Level Input Voltage, CMOS	V_{IHC}	V_{DD} * 0.7	V_{DD} + 0.3	V	–
Low-Level Input Voltage, CMOS	V_{ILC}	-0.3	V_{DD} * 0.3	V	–
Input High Leakage Current TTL / CMOS	I_{IH}	–	+1.0	µA	1
Input Low Leakage Current TTL / CMOS	I_{IL}	-1.0	–	µA	2
High-Level Output Voltage	V_{OH}	V_{DD} - 0.8	–	V	3
Low-Level Output Voltage	V_{OL}	–	0.4	V	3
Power Dissipation @ Maximum SYS CLK	P_D	–	0.63 @ 65 MHz	W	4,5
Power Dissipation @ Maximum DUB CLK	P_D	–	1.25 @ 130 MHz	W	6

Notes:

1. Input = V_{DD} = V_{DDMAX}.
2. Input = V_{SS}, V_{DD} = V_{DDMAX}.
3. Refer to Tables 7-9 for the I_{OL}/I_{OH} currents (measured at V_{DDMIN}).
4. Power rating is per DDS. If both DDS1 and DDS2 are operating at same conditions, the power will be doubled.
5. For other clock frequencies,
   Power per DDS ≤ (8.5 mW/MHz) * (Clock Frequency) typical;
   Current per DDS ≤ (1.7 mA/MHz) * (Clock Frequency) typical.
6. For other clock frequencies,
   Power ≤ (8.3 mW/MHz) * (Clock Frequency) typical;
   Current ≤ (1.66 mA/MHz) * (Clock Frequency) typical.

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TIMING SPECIFICATIONS

Figures 16 through 21 and Tables 15 through 20 show the timing specifications of the Q2368.

Figure 16. Q2368 8-bit Bus Mode Interface Timing Diagram

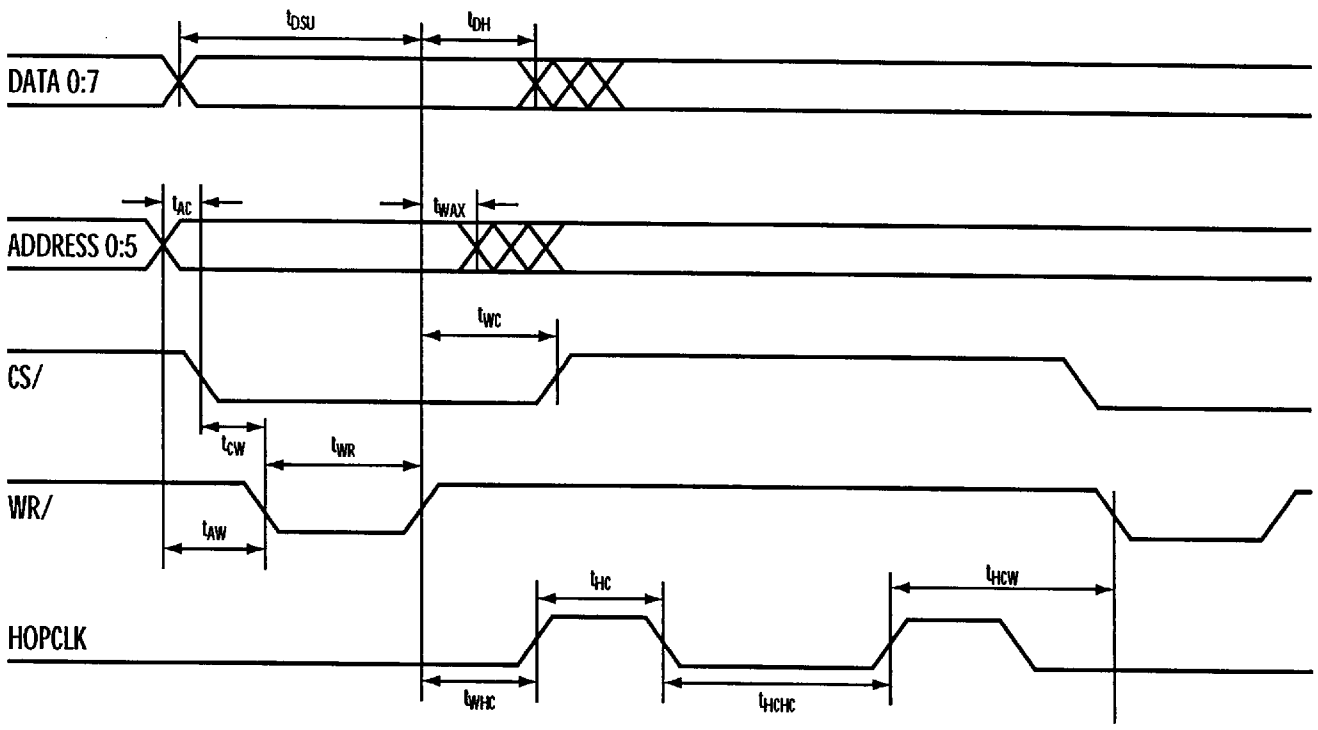

Table 15. Q2368 8-bit Bus Mode Interface Timing Parameters

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Data Setup to WR/ Rising	t_{DSU}	5	–	ns	–
Data Hold After WR/ Rising	t_{DH}	2	–	ns	–
Address Valid to CS/ Falling	t_{AC}	0	–	ns	–
Address Hold After WR/ Rising	t_{WAX}	5	–	ns	–
CS/ Setup to WR/ Falling	t_{CW}	5	–	ns	–
CS/ Hold After WR/ Rising	t_{WC}	5	–	ns	–
WR/ Rising to HOP CLK Rising	t_{WHC}	0	–	ns	1
HOP CLK Pulse Width	t_{HC}	t_{CYC}	–	ns	2
HOP CLK Falling Edge to HOP CLK Rising Edge	t_{HCHC}	3 * t_{CYC}	–	ns	2
HOP CLK Rising Edge to WR/	t_{HCW}	4 * t_{CYC}	–	ns	1,2
Address Valid to WR/ Falling	t_{AW}	0	–	ns	–
WR/ Period	t_{WR}	16	–	ns	–

Notes:

1. When CS/ is active "Low".
2. When operating in Dual Mode, t_{CYC} = the equivalent number of SYS CLK cycles. When operating in Double Mode, multiply t_{CYC} by 2.

Figure 17. Q2368 Serial Mode Interface Timing Diagram

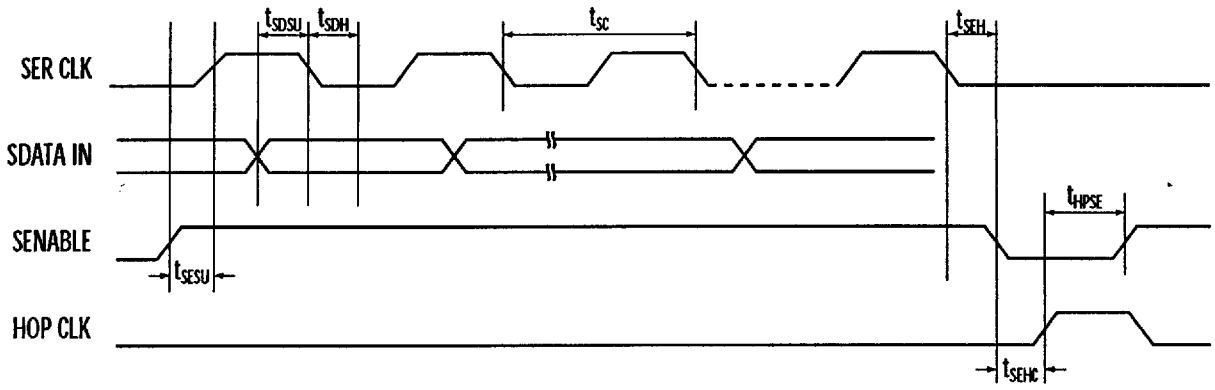

Table 16. Q2368 Serial Mode Interface Timing Parameters

PARAMETER	SYMBOL	MIN	MAX	UNITS	Notes
Serial Data Setup to Serial Clock Falling	t_{SDSU}	0	–	ns	–
Serial Data Hold After Serial Clock Falling	t_{SDH}	4	–	ns	–
Serial Enable Setup to Serial Clock Rising	t_{SESU}	2	–	ns	–
Serial Enable Hold After Serial Clock Falling	t_{SEH}	0	–	ns	–
Serial Clock Period	t_{SC}	16.66	–	ns	1
Serial Enable Falling to Hop Clock Rising	t_{SEHC}	0	–	ns	–
Hop Clock Rising to Next Serial Enable High	t_{HPSE}	4 * t_{CYC}	–	ns	2

Notes:

1. Corresponding Duty Cycle Specification is 30% / 70% maximum.
2. When operating in Dual Mode, t_{CYC} = the equivalent number of SYS CLK cycles. When operating in Double Mode, multiply t_{CYC} by 2.

Figure 18. Q2368 Output Timing Diagram

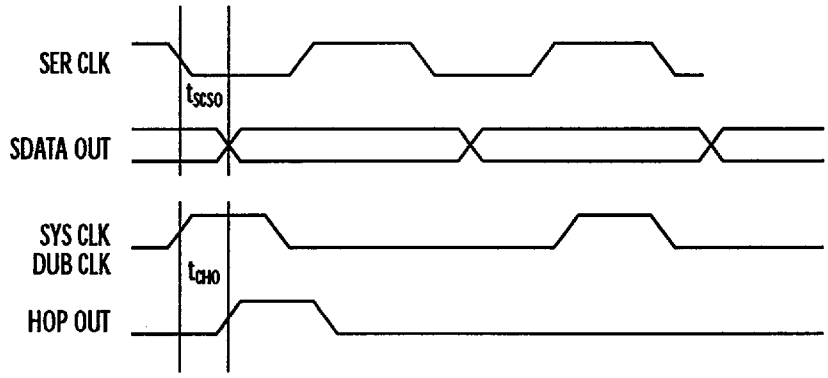

Table 17. Q2368 Output Timing Parameters

PARAMETER	SYMBOL	MIN	MAX	UNITS
Serial Clock to Serial Data Out	t_{SCSO}	7	14	ns
SYS CLK to Hop Clock Out	t_{CHO}	10	18	ns
DUB CLK to Hop Clock Out	t_{CHO}	13	23	ns

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Figure 19. Q2368 DAC Strobe Signal Timing Diagram

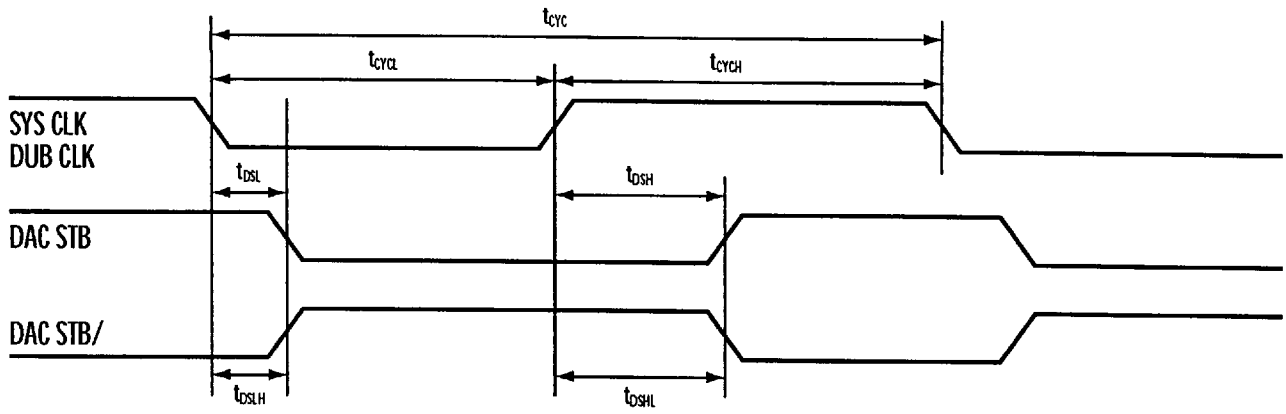

Table 18a. Q2368 DAC Strobe Signal Timing Parameters (Dual Mode)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
SYS CLK Cycle Period	t_{CYC}	15.38	1000	ns	1,2
SYS CLK Low to DAC STB Low	t_{DSL}	4.5	11	ns	3
SYS CLK Low to DAC STB/ High	t_{DSLH}	4.5	11	ns	3
SYS CLK High to DAC STB High	t_{DSH}	4.5	11	ns	3
SYS CLK High to DAC STB/ Low	t_{DSHL}	4.5	11	ns	3

Table 18b. Q2368 DAC Strobe Signal Timing Parameters (Double Mode)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DUB CLK Cycle Period	t_{CYC}	7.69	–	ns	4
DUB CLK Low to DAC STB Low	t_{DSL}	5.5	12	ns	3
DUB CLK Low to DAC STB/ High	t_{DSLH}	5.5	12	ns	3
DUB CLK High to DAC STB High	t_{DSH}	6	12	ns	3
DUB CLK High to DAC STB/ Low	t_{DSHL}	6	12	ns	3

Notes:

1. The Q2368 contains dynamic Logic. Minimum SYS CLK frequency is 1.0 MHz.
2. Corresponding Duty Cycle Specification is 35% / 65% maximum.
3. Assumes a 15 pF capacitive loading.
4. Corresponding Duty Cycle Specification is 40% / 60% maximum.

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Figure 20. Q2368 External Control Timing Diagram

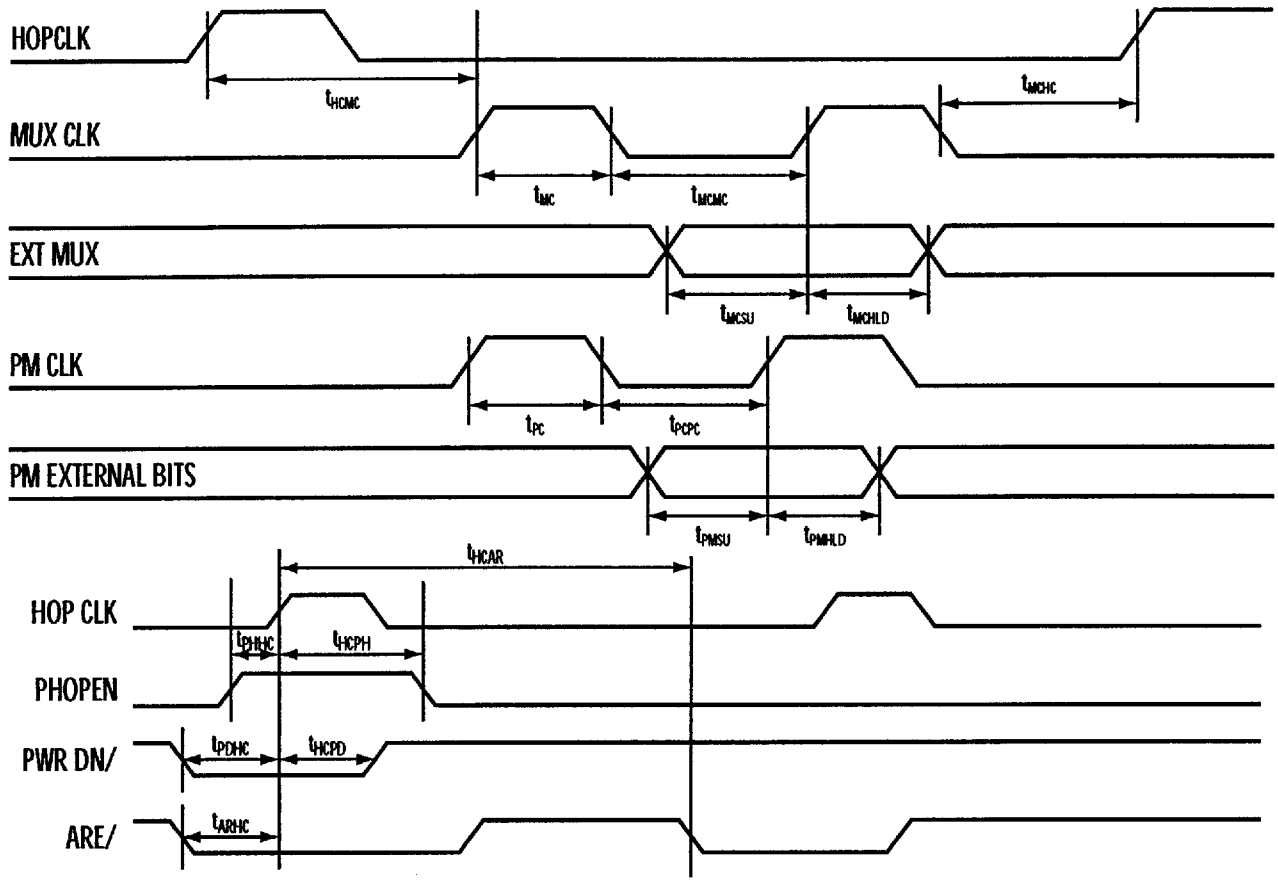

Table 19. Q2368 External Control Timing Parameters

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
HOP CLK Rising to MUX CLK Rising	t_{HCMC}	2 * t_{CYC}	–	ns	1
MUX CLK High Period	t_{MC}	3 * t_{CYC}	–	ns	1
MUX CLK Low Period	t_{MCMC}	t_{CYC}	–	ns	1
MUX CLK Falling to HOP CLK Rising	t_{MCHC}	0	–	ns	–
EXT MUX Setup to MUX CLK	t_{MCSU}	2	–	ns	–
EXT MUX Hold After MUX CLK	t_{MCHLD}	2	–	ns	–
PM CLK High Period	t_{PC}	3 * t_{CYC}	–	ns	1
PM CLK Low Period	t_{PCPC}	t_{CYC}	–	ns	1
PM Data Setup to PM CLK	t_{PMSU}	2	–	ns	–
PM Data Hold After PM CLK	t_{PMHLD}	4	–	ns	–
Programmable Hop Clock Enable to Hop Clock	t_{PHHC}	0	–	ns	–
Hop Clock to Programmable Hop Clock Enable	t_{HCPH}	4 * t_{CYC}	–	ns	1
Power-down Enable to Hop Clock	t_{PDHC}	0	–	ns	–
Hop Clock to Power-down Enable	t_{HCPD}	4 * t_{CYC}	–	ns	1
Accumulator Reset to Hop Clock	t_{ARHC}	0	–	ns	–
Hop Clock to Next Accumulator Reset	t_{HCAR}	4 * t_{CYC}	–	ns	1

Notes:

1. When operating in Dual Mode, t_{CYC} = the equivalent number of SYS CLK cycles. When operating in Double Mode, multiply t_{CYC} by 2.

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Figure 21. Q2368 DAC Interface Timing Diagram

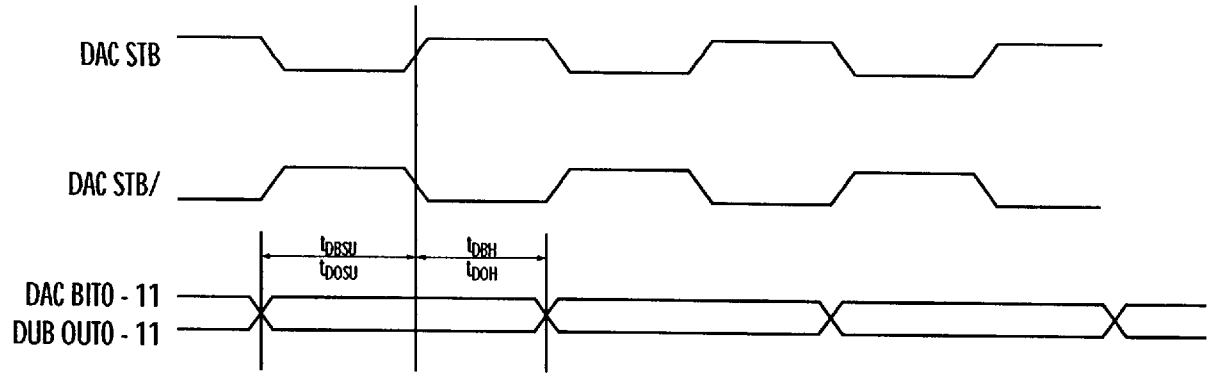


Table 20a. Q2368 DAC Interface Timing Parameters (Dual Mode)

		20 MHz Max Clock		65 MHz Max Clock		
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS
DAC BIT0 - 11 Setup to DAC Strobe Rising, DAC Strobe Invert Falling	t_{DBSU}	40	–	7	–	ns
DAC BIT0 - 11 Hold After DAC Strobe Rising, DAC Strobe Invert Falling	t_{DBH}	3.5	–	3.5	–	ns

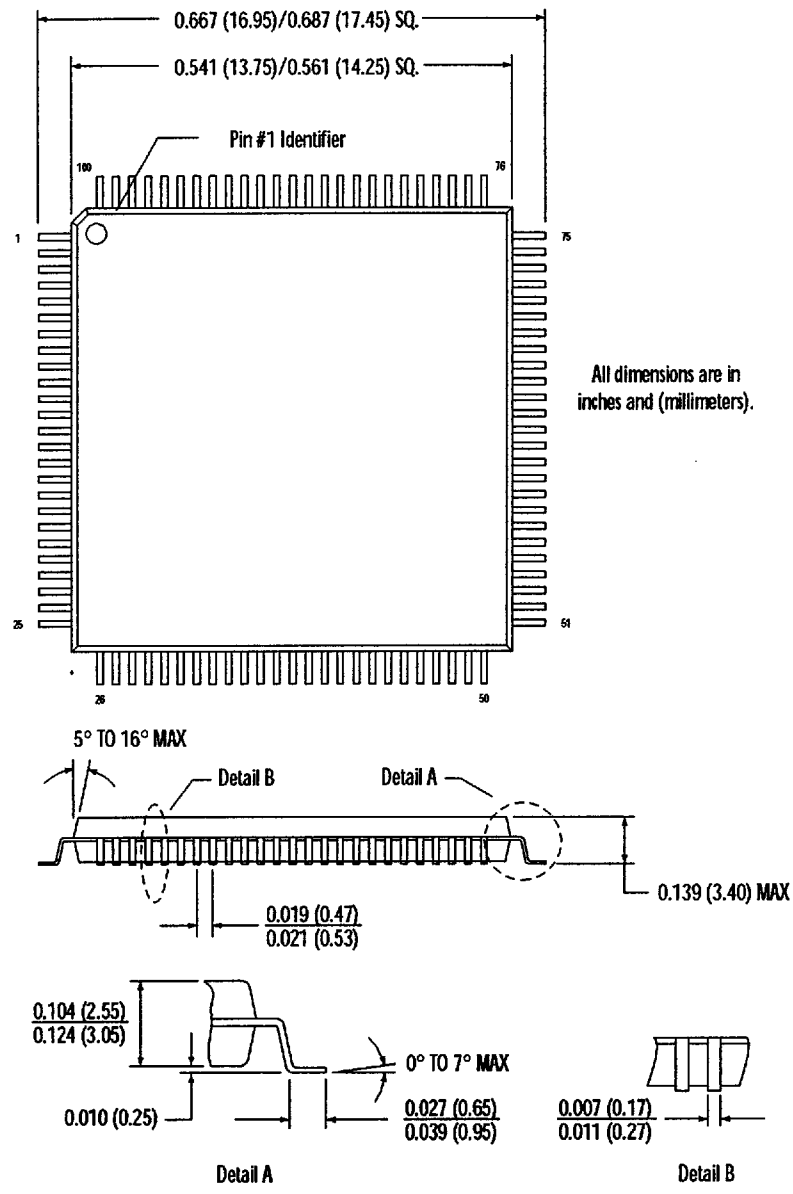
Table 20b. Q2368 DAC Interface Timing Parameters (Double Mode)

		80 MHz Max Clock		100 MHz Max Clock		115 MHz Max Clock		130 MHz Max Clock		
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
DUB OUT0 - 11 Setup to DAC Strobe Rising, DAC Strobe Invert Falling	t_{DOSU}	6	–	5	–	4	–	3	–	ns
DUB OUT0 - 11 Hold After DAC Strobe Rising, DAC Strobe Invert Falling	t_{DOH}	1	–	1	–	1	–	1	–	ns

PQFP PACKAGING

The Q2368 is packaged in a 100-pin Plastic Quad Flat Pack (PQFP) shown in Figure 22.

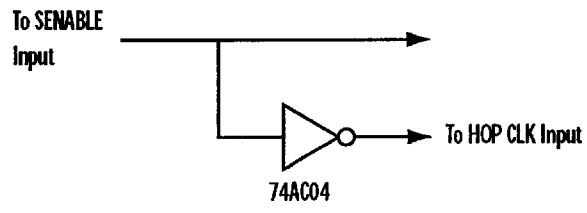
Figure 22. Q2368 100-pin PQFP Package Outline



USING 3-WIRE EQUIVALENT SERIAL CONTROL FOR THE Q2368

Although serial control for the Q2368 is accomplished using four signals (SDATA IN, SER CLK, SENABLE and HOP CLK), a 3-wire control method can be easily implemented with the addition of a simple CMOS Inverter as shown in Figure 23. Additional reference is found under *Digital Processor Interface Modes* in the *Serial Bus Mode* section and in the *Serial Mode Interface Timing*information contained in Figure 17 and Table 16.

Figure 23. 3-wire Serial Control Implementation



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PATENT REFERENCES

1.) U.S. Patent No. 4,905,177 - "High Resolution Phase to Sine Amplitude Conversion," QUALCOMM, Feb. 27, 1990.

2.) U.S. Patent No. 4,901,265 - "Pseudorandom Dither for Frequency Synthesis Noise," QUALCOMM, Feb. 13, 1990.

EVALUATION SYSTEM FOR THE Q2368 DDS

The Q0315 DDS Evaluation System was designed to demonstrate the capabilities and operating modes of the Q2368 dual DDS on a compact 5" X 7" printed circuit board. The Q0315 contains several features that will speed integration of the Q2368 into your design. The evaluation platform allows customers to evaluate the Q2368 as a dual DDS operating at 65 MHz or a single high-speed DDS operating at 130 MHz. A block diagram of the Q0315 Evaluation System is shown in Figure 24.

The evaluation board contains a Q2368 device coupled with a 125 MHz 10-bit Digital-to-Analog Converter (DAC), a 100 MHz 12-bit DAC and the necessary analog output circuitry to provide optimum DDS performance.

The evaluation platform is computer controlled through a digital I/O board that resides in the user's personal computer and Windows™ based software. The menu driven Control Software provides access to all Q2368 programmable registers and will automatically compute all desired register values based upon the user's input and program the Q2368 in the following modes:

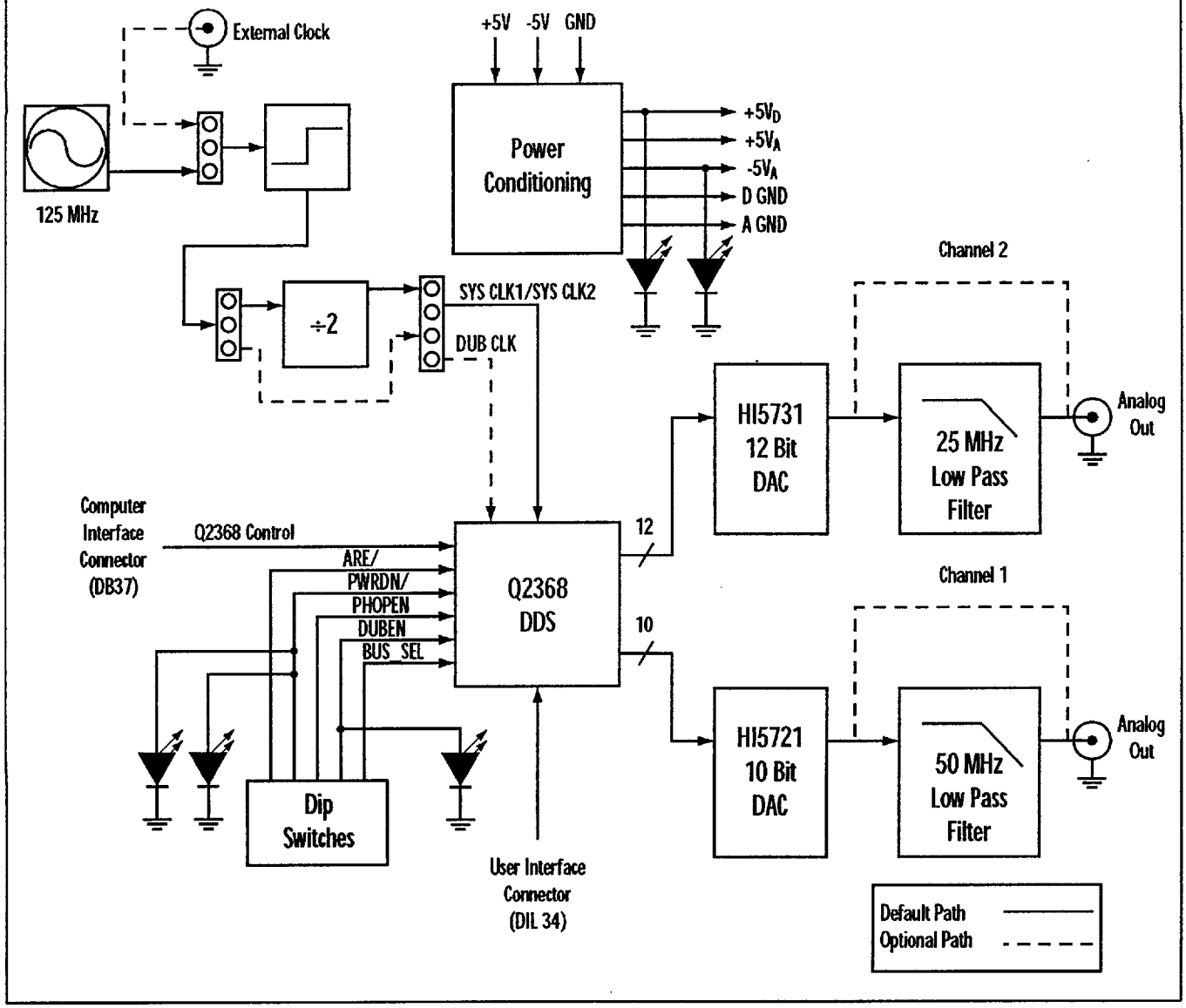
- Dual Mode Control
- Double Mode Control
- Dual Mode Chirp Control
- Double Mode Chirp Control
- Register Mode

The User's Guide provides all the information required to operate the Q0315 and exercise all built-in functionality of the Q2368. Appendices are also provided which contain the schematics, layout and complete parts list. The Q0315 consists of a DDS Evaluation Board, Control Software, Control Cable, Digital I/O (DIO) Board and DIO Board Installation Software. In order to operate the DDS Evaluation Board, the DIO Board needs to be installed in a PC. The DIO Driver Software and the Q0315 Control Software need to be installed on the hard drive of the PC. The Q0315 DDS Evaluation System requires the following computer hardware as a minimum to operate in Remote Mode:

- PC 80386 or Better
- 4 MB RAM
- Math Co-processor
- Hard Drive
- Mouse
- Windows™ Version 3.1 or Windows '95™
- SVGA Video Card (1024 X 768 Resolution, Small Fonts)

Note: Windows™ is a trademark of Microsoft ® Corporation

Figure 24. Q0315 Evaluation System Block Diagram



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