

# TMS4256, TMS4257 262,144-BIT DYNAMIC RANDOM-ACCESS MEMORIES

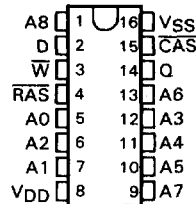
MAY 1983—REVISED JANUARY 1988

- 262,144 × 1 Organization
- Single 5-V Power Supply
  - 5% Tolerance Required for TMS4256-8
  - 10% Tolerance Required for TMS4256-10, -12, -15, and TMS4257-10, -12, -15
- JEDEC Standardized Pinouts
- Performance Ranges:

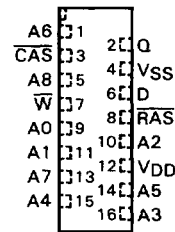
DEVICE	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	VDD TOLERANCE
'4256-8	80 ns	40 ns	160 ns	± 5%
'4256-10 '4257-10	100 ns	50 ns	200 ns	± 10%
'4256-12 '4257-12	120 ns	60 ns	220 ns	± 10%
'4256-15 '4257-15	150 ns	75 ns	260 ns	± 10%

- Long Refresh Period . . . 4 ms (Max)
- Operations of the TMS4256/TMS4257 Can Be Controlled by TI's SN74ALS2967, SN74ALS2968, and THCT4502 Dynamic RAM Controllers
- All Inputs, Outputs, and Clocks Fully TTL Compatible
- 3-State Unlatched Outputs
- Common I/O Capability with "Early Write" Feature
- Page Mode ('4256) or Nibble-Mode ('4257)
- Low Power Dissipation
- RAS-Only Refresh Mode
- Hidden Refresh Mode
- CAS-Before-RAS Refresh Mode
- Available with MIL-STD-883B Processing and L(0°C to 70°C), E(-40°C to 85°C), or S(-55°C to 100°C) Temperature Ranges (SMJ4256, with 10% Power Supply)

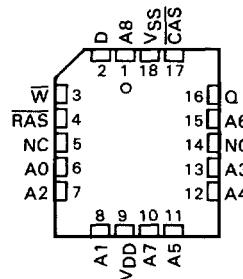
N PACKAGE  
(TOP VIEW)



SD PACKAGE  
(TOP VIEW)



FM PACKAGE  
(TOP VIEW)



PIN NOMENCLATURE

A0-AB	Address Inputs
CAS	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
RAS	Row-Address Strobe
VDD	5-V Power Supply
VSS	Ground
W	Write Enable

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# TMS4256, TMS4257

## 262,144-BIT DYNAMIC RANDOM-ACCESS MEMORIES

### description

The TMS4256 and TMS4257 are high-speed, 262,144-bit dynamic random-access memories, organized as 262,144 words of one bit each. They employ state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

The '4256-8 with a 5% voltage tolerance has a maximum  $\overline{\text{RAS}}$  access time of 80 ns. The '4256/'4257-10, -12, and -15 with 10% voltage tolerances have maximum  $\overline{\text{RAS}}$  access times of 100 ns, 120 ns, and 150 ns, respectively.

New SMOS technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout.  $\text{I}_{\text{DD}}$  peaks are 125 mA typical, and a -1 V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The '4256 and '4257 are offered in 16-pin plastic dual-in-line, 16-pin plastic zig-zag in-line (ZIP), and 18-lead plastic chip carrier packages. They are guaranteed for operation from 0°C to 70°C. The dual-in-line package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers.

### operation

#### address (A0 through A8)

Eighteen address bits are required to decode 1 of 262,144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ( $\overline{\text{RAS}}$ ). Then the nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ( $\overline{\text{CAS}}$ ). All addresses must be stable on or before the falling edges of  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$ .  $\overline{\text{RAS}}$  is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder.  $\overline{\text{CAS}}$  is used as a chip select, activating the column decoder and the input and output buffers.

#### write enable ( $\overline{\text{W}}$ )

The read or write mode is selected through the write-enable ( $\overline{\text{W}}$ ) input. A logic high on the  $\overline{\text{W}}$  input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When  $\overline{\text{W}}$  goes low prior to  $\overline{\text{CAS}}$ , data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

#### data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of  $\overline{\text{CAS}}$  or  $\overline{\text{W}}$  strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle,  $\overline{\text{W}}$  is brought low prior to  $\overline{\text{CAS}}$  and the data is strobed in by  $\overline{\text{CAS}}$  with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle,  $\overline{\text{CAS}}$  will already be low, thus the data will be strobed in by  $\overline{\text{W}}$  with setup and hold times referenced to this signal.

#### data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until  $\overline{\text{CAS}}$  is brought low. In a read cycle the output goes active after the access time interval  $t_{\text{a}}(\text{C})$  that begins with the negative transition of  $\overline{\text{CAS}}$  as long as  $t_{\text{a}}(\text{R})$  is satisfied. The output becomes valid after the access time has elapsed and remains valid while  $\overline{\text{CAS}}$  is low;  $\overline{\text{CAS}}$  going high returns it to a high-impedance state. In a read-modify-write cycle, the output will follow the sequence for the read cycle.

**refresh**

A refresh operation must be performed at least once every four milliseconds to retain data. This can be achieved by strobing each of the 256 rows (A0-A7). A normal read or write cycle will refresh all bits in each row that is selected. A  $\overline{\text{RAS}}$ -only operation can be used by holding  $\overline{\text{CAS}}$  at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state.

**$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh**

The  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh is utilized by bringing  $\overline{\text{CAS}}$  low earlier than  $\overline{\text{RAS}}$  (see parameter  $t_{\text{CLRL}}$ ) and holding it low after  $\overline{\text{RAS}}$  falls (see parameter  $t_{\text{RLCHR}}$ ). For successive  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles,  $\overline{\text{CAS}}$  can remain low while cycling  $\overline{\text{RAS}}$ . The external address is ignored and the refresh address is generated internally.

**hidden refresh**

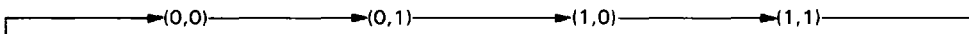
Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding  $\overline{\text{CAS}}$  at  $V_{\text{IL}}$  after a read operation and cycling  $\overline{\text{RAS}}$  after a specified precharge period, similar to a  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle. The external address is also ignored during the hidden refresh cycles. The data at the output pin remains valid up to the maximum  $\overline{\text{CAS}}$  low pulse duration,  $t_{\text{W}}(\text{CL})$ .

**page mode (TMS4256)**

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe sequential row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by  $t_{\text{W}}(\text{RL})$ , the maximum  $\overline{\text{RAS}}$  low pulse duration.

**nibble mode (TMS4257)**

Nibble-mode operation allows high-speed serial read, write, or read-modify-write access of 1 to 4 bits of data. The first bit is accessed in the normal manner with read data coming out at  $t_{\text{a}}(\text{C})$  time. The next sequential nibble bits can be read or written by cycling  $\overline{\text{CAS}}$  while  $\overline{\text{RAS}}$  remains low. The first bit is determined by the row and column addresses, which need to be supplied only for the first access. Column A8 and row A8 (CA8, RA8) provide the two binary bits for initial selection of the nibble addresses. Thereafter, the falling edge of  $\overline{\text{CAS}}$  will access the next bit of the circular 4-bit nibble in the following sequence:



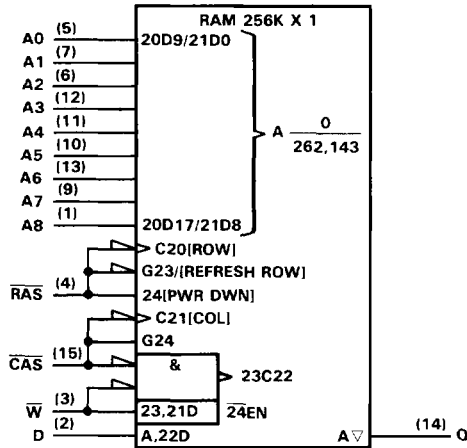
In nibble-mode, all normal memory operations (read, write, or read-modify-write) may be performed in any desired combination.

**power-up**

To achieve proper device operation, an initial pause of 200  $\mu\text{s}$  is required after power up, followed by a minimum of eight initialization cycles.

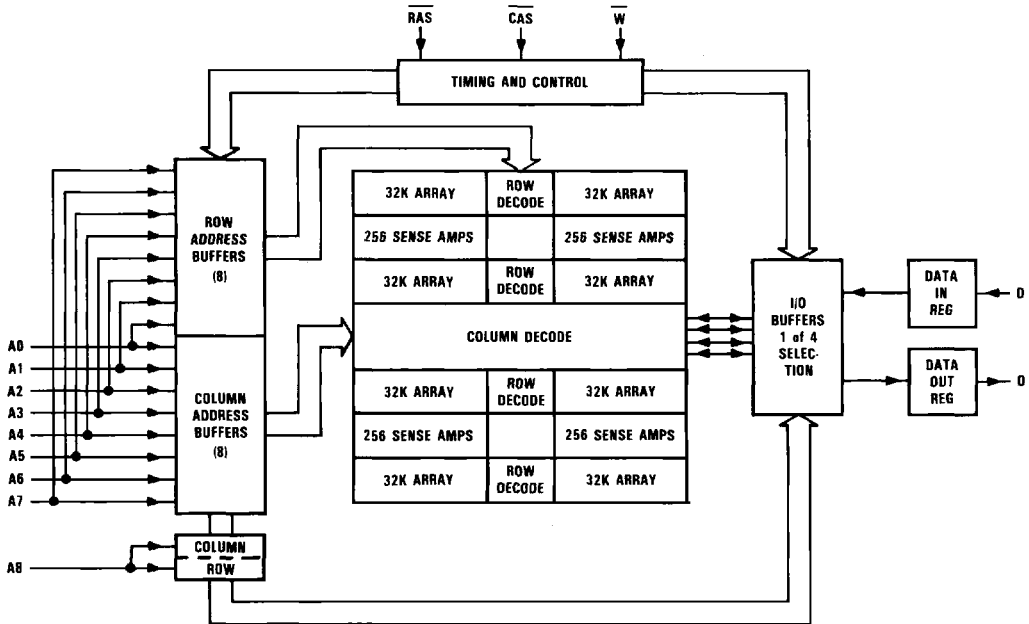
**TMS4256, TMS4257  
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logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1084 and IEC Publication 617-12. The pin numbers shown are for the 16-pin dual-in-line package.

functional block diagram



**TMS4256, TMS4257**  
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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Voltage range for any pin, including V <sub>DD</sub> supply (see Note 1)	-1 V to 7 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V<sub>SS</sub>.

**recommended operating conditions**

	MIN	NOM	MAX	UNIT
V <sub>DD</sub> Supply voltage ('4256/'4257-10, -12, -15)	4.5	5	5.5	V
V <sub>DD</sub> Supply voltage ('4256-8)	4.75	5	5.25	V
V <sub>SS</sub> Supply voltage		0		V
V <sub>IH</sub> High-level input voltage	2.4		6.5	V
V <sub>IL</sub> Low-level input voltage (see Note 2)	-1		0.8	V
T <sub>A</sub> Operating free-air temperature		0	70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as maximum, is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TMS4256-8		TMS4256-10 TMS4257-10		UNIT	
		MIN	MAX	MIN	MAX		
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -5 mA		2.4		V	
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4.2 mA		0.4		V	
I <sub>I</sub>	Input current (leakage)	V <sub>I</sub> = 0 V to 6.5 V, V <sub>DD</sub> = 5 V, All other pins = 0 V to 6.5 V		±10		μA	
I <sub>O</sub>	Output current (leakage)	V <sub>O</sub> = 0 V to 5.5 V, V <sub>DD</sub> = 5 V, $\overline{\text{CAS}}$ high		±10		μA	
I <sub>DD1</sub>	Average operating current during read or write cycle	t <sub>c</sub> = minimum cycle, Output open		70		mA	
I <sub>DD2</sub>	Standby current	After 1 memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high, Output open		4.5		mA	
I <sub>DD3</sub>	Average refresh current	t <sub>c</sub> = minimum cycle, $\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ high, Output open		70		58	mA
I <sub>DD4</sub>	Average page-mode current	t <sub>c(P)</sub> = minimum cycle, $\overline{\text{RAS}}$ low, $\overline{\text{CAS}}$ cycling, Output open		60		50	mA
I <sub>DD5</sub>	Average nibble-mode current	t <sub>c(N)</sub> = minimum cycle, $\overline{\text{RAS}}$ low, $\overline{\text{CAS}}$ cycling, Output open				45	mA

PARAMETER	TEST CONDITIONS	TMS4256-12 TMS4257-12		TMS4256-15 TMS4257-15		UNIT	
		MIN	MAX	MIN	MAX		
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -5 mA		2.4		V	
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4.2 mA		0.4		V	
I <sub>I</sub>	Input current (leakage)	V <sub>I</sub> = 0 V to 6.5 V, V <sub>DD</sub> = 5 V, All other pins = 0 V to 6.5 V		±10		μA	
I <sub>O</sub>	Output current (leakage)	V <sub>O</sub> = 0 V to 5.5 V, V <sub>DD</sub> = 5 V, $\overline{\text{CAS}}$ high		±10		μA	
I <sub>DD1</sub>	Average operating current during read or write cycle	t <sub>c</sub> = minimum cycle, Output open		65		60	mA
I <sub>DD2</sub>	Standby current	After 1 memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high, Output open		4.5		4.5	mA
I <sub>DD3</sub>	Average refresh current	t <sub>c</sub> = minimum cycle, $\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ high, Output open		53		48	mA
I <sub>DD4</sub>	Average page-mode current	t <sub>c(P)</sub> = minimum cycle, $\overline{\text{RAS}}$ low, $\overline{\text{CAS}}$ cycling, Output open		45		40	mA
I <sub>DD5</sub>	Average nibble-mode current	t <sub>c(N)</sub> = minimum cycle, $\overline{\text{RAS}}$ low, $\overline{\text{CAS}}$ cycling, Output open		40		35	mA

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**capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz**

PARAMETER	MAX	UNIT
C <sub>i(A)</sub> Input capacitance, address inputs	5	pF
C <sub>i(D)</sub> Input capacitance, data input	5	pF
C <sub>i(RC)</sub> Input capacitance strobe inputs	5	pF
C <sub>i(W)</sub> Input capacitance, write enable input	7	pF
C <sub>o</sub> Output capacitance	7	pF

**switching characteristics over recommended supply voltage range and operating free-air temperature range**

PARAMETER	TEST CONDITIONS	ALT. SYMBOL	TMS4256-8		TMS4256-10 TMS4257-10		UNIT
			MIN	MAX	MIN	MAX	
t <sub>a(C)</sub> Access time from $\overline{\text{CAS}}$	t <sub>RLCL</sub> ≥ MAX, C <sub>L</sub> = 100 pF, Load = 2 Series 74 TTL gates	t <sub>CAC</sub>	40		50		ns
t <sub>a(R)</sub> Access time from $\overline{\text{RAS}}$	t <sub>RLCL</sub> = MAX, C <sub>L</sub> = 100 pF, Load = 2 Series 74 TTL gates	t <sub>RAC</sub>	80		100		ns
t <sub>dis(CH)</sub> Output disable time after $\overline{\text{CAS}}$ high	C <sub>L</sub> = 100 pF, Load = 2 Series 74 TTL gates	t <sub>OFF</sub>	0	20	0	30	ns

PARAMETER	TEST CONDITIONS	ALT. SYMBOL	TMS4256-12 TMS4257-12		TMS4256-15 TMS4257-15		UNIT
			MIN	MAX	MIN	MAX	
t <sub>a(C)</sub> Access time from $\overline{\text{CAS}}$	t <sub>RLCL</sub> ≥ MAX, C <sub>L</sub> = 100 pF, Load = 2 Series 74 TTL gates	t <sub>CAC</sub>	60		75		ns
t <sub>a(R)</sub> Access time from $\overline{\text{RAS}}$	t <sub>RLCL</sub> = MAX, C <sub>L</sub> = 100 pF, Load = 2 Series 74 TTL gates	t <sub>RAC</sub>	120		150		ns
t <sub>dis(CH)</sub> Output disable time after $\overline{\text{CAS}}$ high	C <sub>L</sub> = 100 pF, Load = 2 Series 74 TTL gates	t <sub>OFF</sub>	0	30	0	30	ns

# TMS4256, TMS4257

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timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER	ALT. SYMBOL	TMS4256-8		TMS4256-10 TMS4257-10		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(P)}$ Page-mode cycle time (read or write cycle)	$t_{PC}$	70		100		ns
$t_{c(PM)}$ Page-mode cycle time (read-modify-write cycle)	$t_{PCM}$	95		135		ns
$t_{c(rd)}$ Read cycle time <sup>†</sup>	$t_{RC}$	160		200		ns
$t_{c(W)}$ Write cycle time	$t_{WC}$	160		200		ns
$t_{c(rdW)}$ Read-write/read-modify-write cycle time	$t_{RWC}$	185		235		ns
$t_w(CH)P$ Pulse duration, $\overline{CAS}$ high (page mode)	$t_{CP}$	20		40		ns
$t_w(CH)$ Pulse duration, $\overline{CAS}$ high (non-page mode)	$t_{CPN}$	25		25		ns
$t_w(CL)$ Pulse duration, $\overline{CAS}$ low <sup>‡</sup>	$t_{CAS}$	40	10,000	50	10,000	ns
$t_w(RH)$ Pulse duration, $\overline{RAS}$ high	$t_{RP}$	70		90		ns
$t_w(RL)$ Pulse duration, $\overline{RAS}$ low <sup>§</sup>	$t_{RAS}$	80	10,000	100	10,000	ns
$t_w(W)$ Write pulse duration	$t_{WP}$	20		30		ns
$t_t$ Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	$t_t$	3	50	3	50	ns
$t_{su(CA)}$ Column-address setup time	$t_{ASC}$	0		0		ns
$t_{su(RA)}$ Row-address setup time	$t_{ASR}$	0		0		ns
$t_{su(D)}$ Data setup time	$t_{DS}$	0		0		ns
$t_{su(rd)}$ Read-command setup time	$t_{RCS}$	0		0		ns
$t_{su(WCL)}$ Early write-command setup time before $\overline{CAS}$ low	$t_{WCS}$	0		0		ns
$t_{su(WCH)}$ Write-command setup time before $\overline{CAS}$ high	$t_{CWL}$	20		30		ns
$t_{su(WRH)}$ Write-command setup time before $\overline{RAS}$ high	$t_{RWL}$	20		30		ns
$t_h(CLCA)$ Column-address hold time after $\overline{CAS}$ low	$t_{CAH}$	15		15		ns
$t_h(RA)$ Row-address hold time	$t_{RAH}$	15		15		ns
$t_h(RLCA)$ Column-address hold time after $\overline{RAS}$ low	$t_{AR}$	55		65		ns
$t_h(CLD)$ Data hold time after $\overline{CAS}$ low	$t_{DH}$	20		30		ns
$t_h(RLD)$ Data hold time after $\overline{RAS}$ low	$t_{DHR}$	60		80		ns
$t_h(WLD)$ Data hold time after $\overline{W}$ low	$t_{DH}$	20		30		ns
$t_h(CHrd)$ Read-command hold time after $\overline{CAS}$ high	$t_{RCH}$	0		0		ns
$t_h(RHrd)$ Read-command hold time after $\overline{RAS}$ high	$t_{RRH}$	10		10		ns
$t_h(CLW)$ Write-command hold time after $\overline{CAS}$ low	$t_{WCH}$	20		30		ns
$t_h(RLW)$ Write-command hold time after $\overline{RAS}$ low	$t_{WCR}$	65		80		ns

Continued next page.

NOTE 3: Timing measurements are referenced to  $V_{IL}$  max and  $V_{IH}$  min.

<sup>†</sup>All cycle times assume  $t_t = 5$  ns.

<sup>‡</sup>In a read-modify-write cycle,  $t_{CLWL}$  and  $t_{su(WCH)}$  must be observed. Depending on the user's transition times, this may require additional  $\overline{CAS}$  low time ( $t_w(CL)$ ). This applies to page-mode read-modify-write also.

<sup>§</sup>In a read-modify-write cycle,  $t_{RLWL}$  and  $t_{su(WRH)}$  must be observed. Depending on the user's transition times, this may require additional  $\overline{RAS}$  low time ( $t_w(RL)$ ).

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**timing requirements over recommended supply voltage range and operating free-air temperature range (continued)**

PARAMETER	ALT. SYMBOL	TMS4256-8		TMS4256-10 TMS4257-10		UNIT
		MIN	MAX	MIN	MAX	
t <sub>RLCH</sub> Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t <sub>CSH</sub>	80		100		ns
t <sub>CHRL</sub> Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t <sub>CRP</sub>	0		0		ns
t <sub>CLRHL</sub> Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t <sub>RSH</sub>	40		50		ns
t <sub>RLCHR</sub> Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high <sup>†</sup>	t <sub>CHR</sub>	20		20		ns
t <sub>CLRL</sub> Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low <sup>†</sup>	t <sub>CSR</sub>	10		10		ns
t <sub>RHCL</sub> Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low <sup>†</sup>	t <sub>RPC</sub>	0		0		ns
t <sub>CLWL</sub> Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t <sub>CWD</sub>	40		50		ns
t <sub>RLCL</sub> Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t <sub>RCD</sub>	25	40	25	50	ns
t <sub>RLWL</sub> Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t <sub>RWD</sub>	80		100		ns
t <sub>rf</sub> Refresh time interval	t <sub>REF</sub>		4		4	ms

Continued next page.

NOTE 3: Timing measurements are referenced to V<sub>IL</sub> max and V<sub>IH</sub> min.

<sup>†</sup>CAS-before-RAS refresh only.

# TMS4256, TMS4257 262,144-BIT DYNAMIC RANDOM-ACCESS MEMORIES

timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

PARAMETER	ALT. SYMBOL	TMS4256-12 TMS4257-12		TMS4256-15 TMS4257-15		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(P)}$ Page-mode cycle time (read or write cycle)	tPC	120		145		ns
$t_{c(PM)}$ Page-mode cycle time (read-modify-write cycle)	tPCM	160		190		ns
$t_{c(rd)}$ Read cycle time <sup>†</sup>	tRC	220		260		ns
$t_{c(W)}$ Write cycle time	tWC	220		260		ns
$t_{c(rdW)}$ Read-write/read-modify-write cycle time	tRWC	260		305		ns
$t_w(CH)P$ Pulse duration, $\overline{CAS}$ high (page mode)	tCP	50		60		ns
$t_w(CH)$ Pulse duration, $\overline{CAS}$ high (non-page mode)	tCPN	25		25		ns
$t_w(CL)$ Pulse duration, $\overline{CAS}$ low <sup>‡</sup>	tCAS	60	10,000	75	10,000	ns
$t_w(RH)$ Pulse duration, $\overline{RAS}$ high	tRP	90		100		ns
$t_w(RL)$ Pulse duration, $\overline{RAS}$ low <sup>§</sup>	tRAS	120	10,000	150	10,000	ns
$t_w(W)$ Write pulse duration	tWP	30		45		ns
$t_t$ Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	tT	3	50	3	50	ns
$t_{su(CA)}$ Column-address setup time	tASC	0		0		ns
$t_{su(RA)}$ Row-address setup time	tASR	0		0		ns
$t_{su(D)}$ Data setup time	tDS	0		0		ns
$t_{su(rd)}$ Read-command setup time	tRCS	0		0		ns
$t_{su(WCL)}$ Early write-command setup time before $\overline{CAS}$ low	tWCS	0		0		ns
$t_{su(WCH)}$ Write-command setup time before $\overline{CAS}$ high	tCWL	35		45		ns
$t_{su(WRH)}$ Write-command setup time before $\overline{RAS}$ high	tRWL	35		45		ns
$t_h(CLCA)$ Column-address hold time after $\overline{CAS}$ low	tCAH	20		25		ns
$t_h(RA)$ Row-address hold time	tRAH	15		15		ns
$t_h(RLCA)$ Column-address hold time after $\overline{RAS}$ low	tAR	80		100		ns
$t_h(CLD)$ Data hold time after $\overline{CAS}$ low	tDH	30		45		ns
$t_h(RLD)$ Data hold time after $\overline{RAS}$ low	tDHR	90		120		ns
$t_h(WLD)$ Data hold time after $\overline{W}$ low	tDH	30		45		ns
$t_h(CHrd)$ Read-command hold time after $\overline{CAS}$ high	tRCH	0		0		ns
$t_h(RHrd)$ Read-command hold time after $\overline{RAS}$ high	tRRH	10		10		ns
$t_h(CLW)$ Write-command hold time after $\overline{CAS}$ low	tWCH	30		45		ns
$t_h(RLW)$ Write-command hold time after $\overline{RAS}$ low	tWCR	90		120		ns

Continued next page.

NOTE 3: Timing measurements are referenced to  $V_{IL}$  max and  $V_{IH}$  min.

<sup>†</sup>All cycle times assume  $t_t = 5$  ns.

<sup>‡</sup>In a read-modify-write cycle,  $t_{CLWL}$  and  $t_{su(WCH)}$  must be observed. Depending on the user's transition times, this may require additional  $\overline{CAS}$  low time ( $t_w(CL)$ ). This applies to page-mode read-modify-write also.

<sup>§</sup>In a read-modify-write cycle,  $t_{RLWL}$  and  $t_{su(WRH)}$  must be observed. Depending on the user's transition times, this may require additional  $\overline{RAS}$  low time ( $t_w(RL)$ ).

**TMS4256, TMS4257**  
**262,144-BIT DYNAMIC RANDOM-ACCESS MEMORIES**

**timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)**

PARAMETER	ALT. SYMBOL	TMS4256-12 TMS4257-12		TMS4256-15 TMS4257-15		UNIT
		MIN	MAX	MIN	MAX	
t <sub>RLCH</sub> Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t <sub>CSH</sub>	120		150		ns
t <sub>CHRL</sub> Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t <sub>CRP</sub>	0		0		ns
t <sub>CLR<sub>H</sub></sub> Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t <sub>RSH</sub>	60		75		ns
t <sub>RLCHR</sub> Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high <sup>†</sup>	t <sub>CHR</sub>	25		30		ns
t <sub>CLRL</sub> Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low <sup>†</sup>	t <sub>CSR</sub>	10		20		ns
t <sub>RHCL</sub> Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low <sup>†</sup>	t <sub>RPC</sub>	0		0		ns
t <sub>CLWL</sub> Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t <sub>CWD</sub>	60		70		ns
t <sub>RLCL</sub> Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t <sub>RCD</sub>	25	60	25	75	ns
t <sub>RLWL</sub> Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t <sub>RWD</sub>	120		145		ns
t <sub>rf</sub> Refresh time interval	t <sub>REF</sub>		4		4	ms

NOTE 3: Timing measurements are referenced to V<sub>IL</sub> max and V<sub>IH</sub> min.  
<sup>†</sup> $\overline{CAS}$ -before- $\overline{RAS}$  refresh only.

**NIBBLE-MODE CYCLE**

**switching characteristics over recommended supply voltage range and operating free-air temperature range**

PARAMETER	ALT. SYMBOL	TMS4257-10		TMS4257-12		TMS4257-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>a(CN)</sub> Nibble-mode access from $\overline{CAS}$	t <sub>NCAC</sub>	25		30		40		ns

**timing requirements over recommended supply voltage range and operating free-air temperature range**

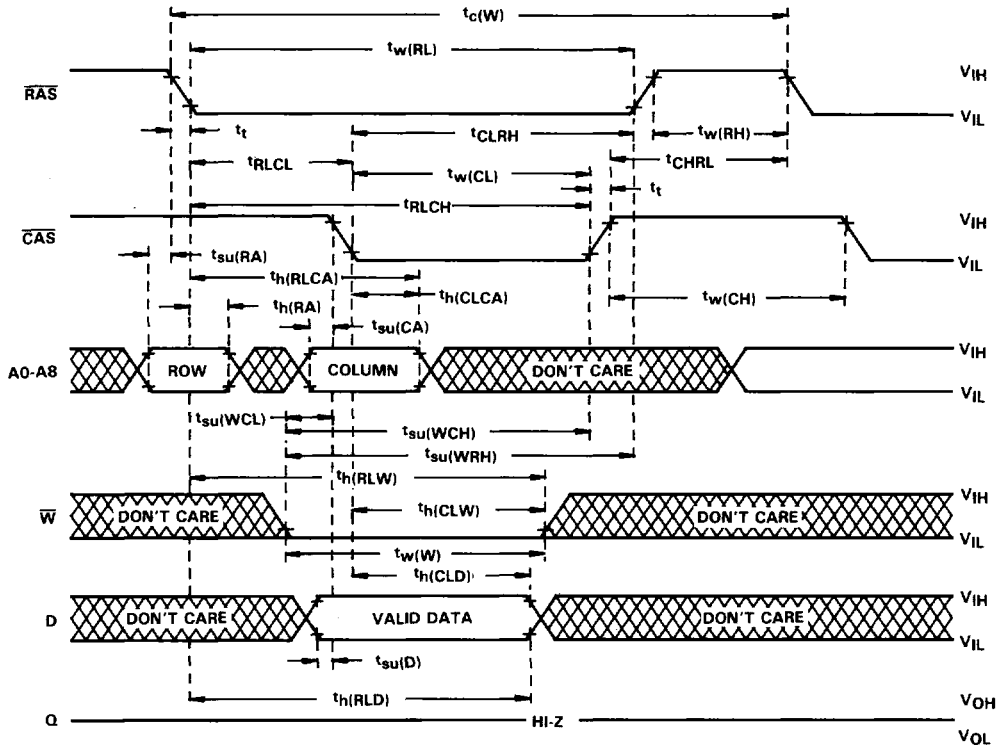
PARAMETER	ALT. SYMBOL	TMS4257-10		TMS4257-12		TMS4257-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>c(N)</sub> Nibble-mode cycle time	t <sub>NC</sub>	50		60		75		ns
t <sub>c(rdWN)</sub> Nibble-mode read-modify-write cycle time	t <sub>NRMW</sub>	70		85		105		
t <sub>CLR<sub>HN</sub></sub> Nibble-mode delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t <sub>NRSH</sub>	25		30		40		
t <sub>CLWLN</sub> Nibble-mode delay time, $\overline{CAS}$ to $\overline{W}$ delay	t <sub>NCWD</sub>	20		25		30		
t <sub>w(CL<sub>N</sub>)</sub> Nibble-mode pulse duration, $\overline{CAS}$ low	t <sub>NCAS</sub>	25		30		40		
t <sub>w(CH<sub>N</sub>)</sub> Nibble-mode pulse duration, $\overline{CAS}$ high	t <sub>NCP</sub>	15		20		25		
t <sub>su(WCH<sub>N</sub>)</sub> Nibble-mode write command setup before $\overline{CAS}$ high	t <sub>NCWL</sub>	20		25		35		

NOTE 3: Timing measurements are referenced to V<sub>IL</sub> max and V<sub>IH</sub> min.



TMS4256, TMS4257  
262,144-BIT DYNAMIC RANDOM-ACCESS MEMORIES

early write cycle timing

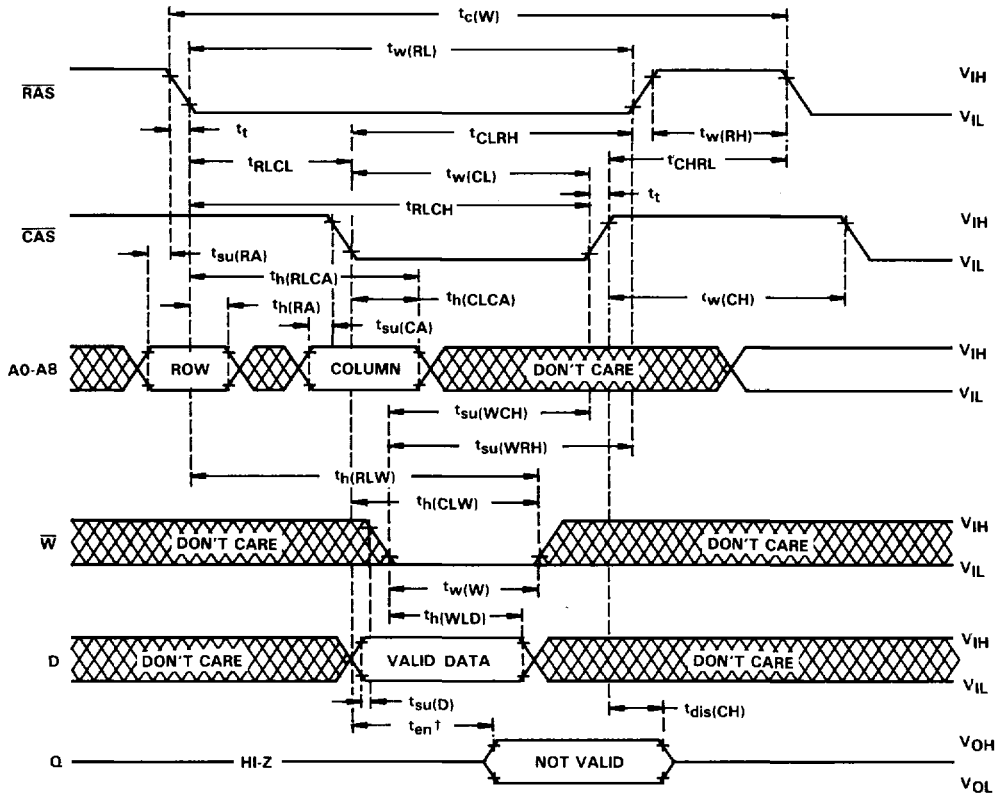


**TMS4256, TMS4257**  
**262,144-BIT DYNAMIC RANDOM-ACCESS MEMORIES**

Dynamic RAMs

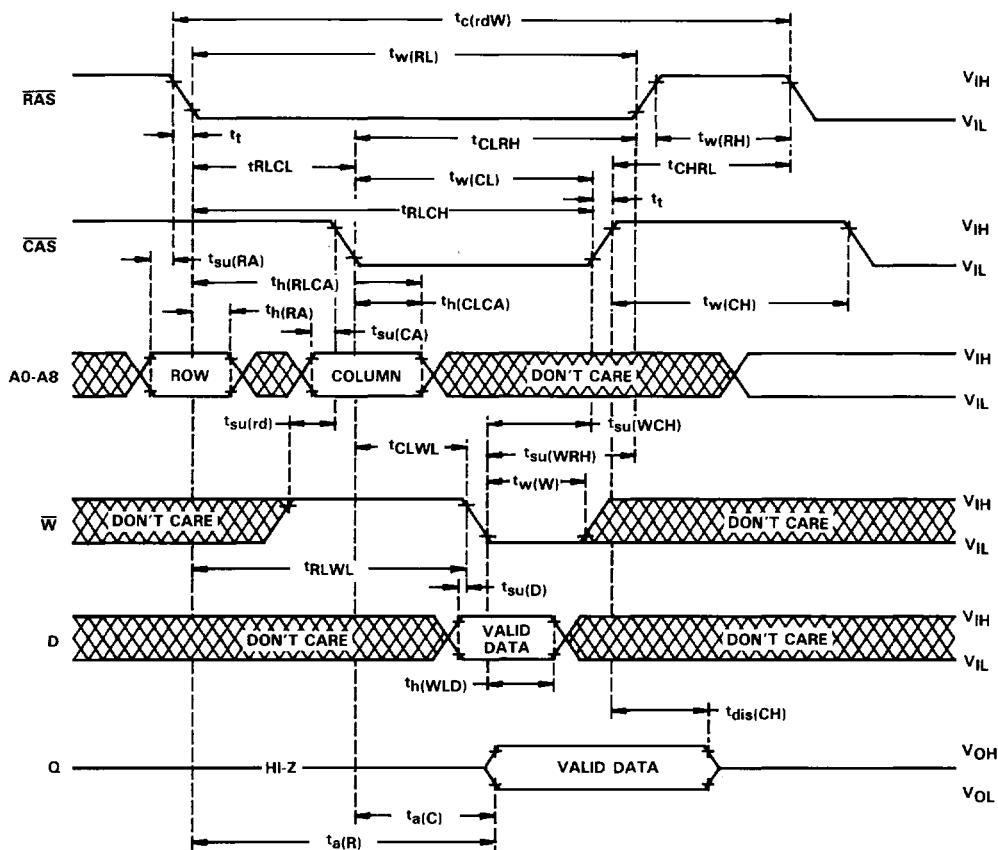
4

write cycle timing



†The enable time ( $t_{en}$ ) for a write cycle is equal in duration to the access time from  $\overline{CAS}$  ( $t_{a(C)}$ ) in a read cycle; but the active levels at the output are invalid.

read-write/read-modify-write cycle timing

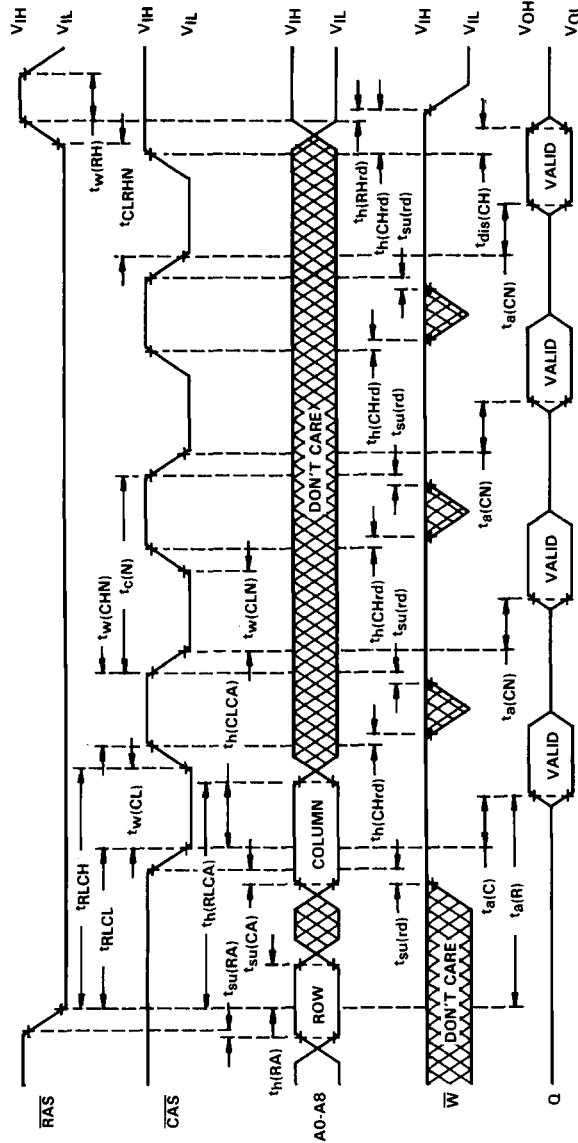






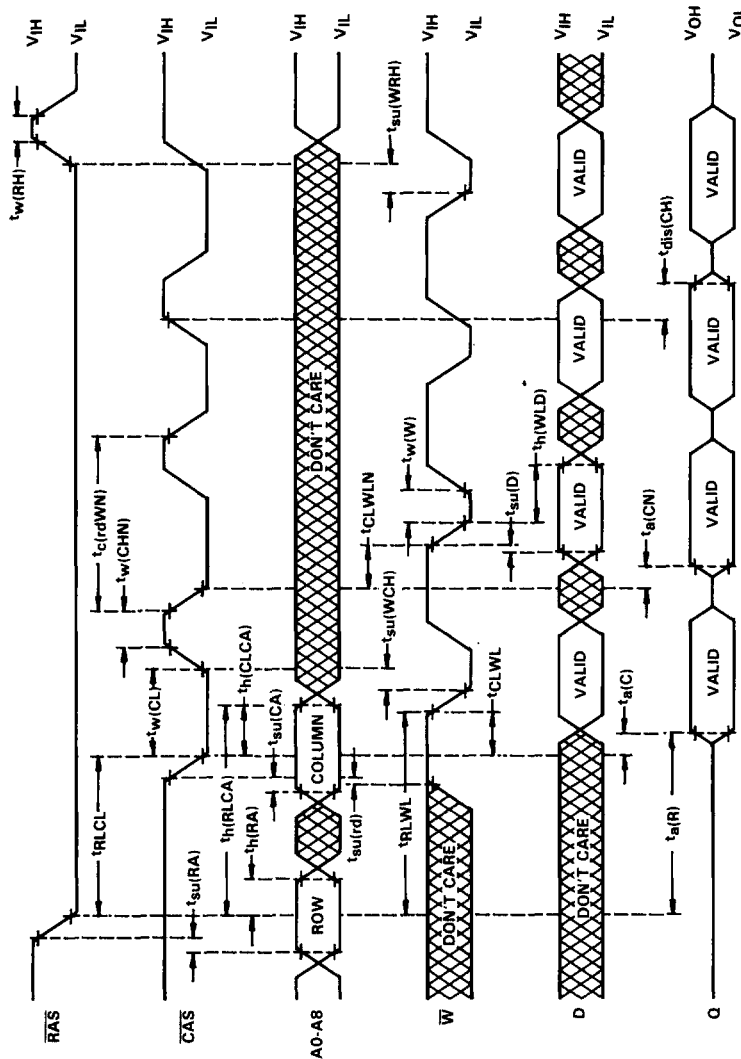


nibble-mode read cycle timing





nibble-mode read-modify-write-cycle timing

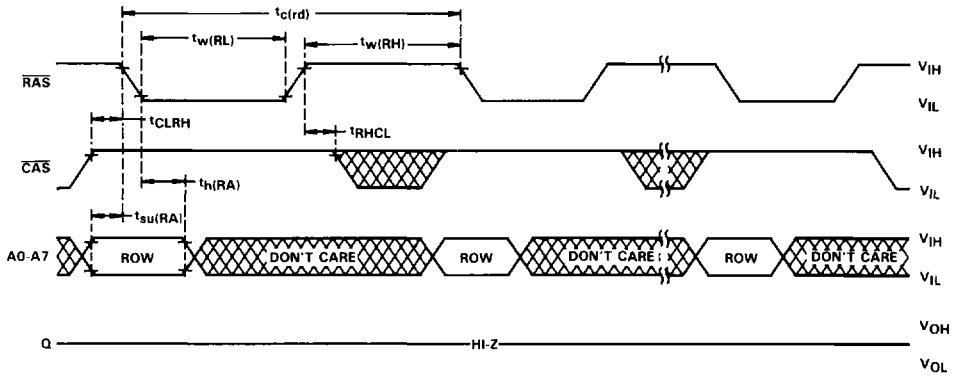


**TMS4256, TMS4257**  
**262,144-BIT DYNAMIC RANDOM-ACCESS MEMORIES**

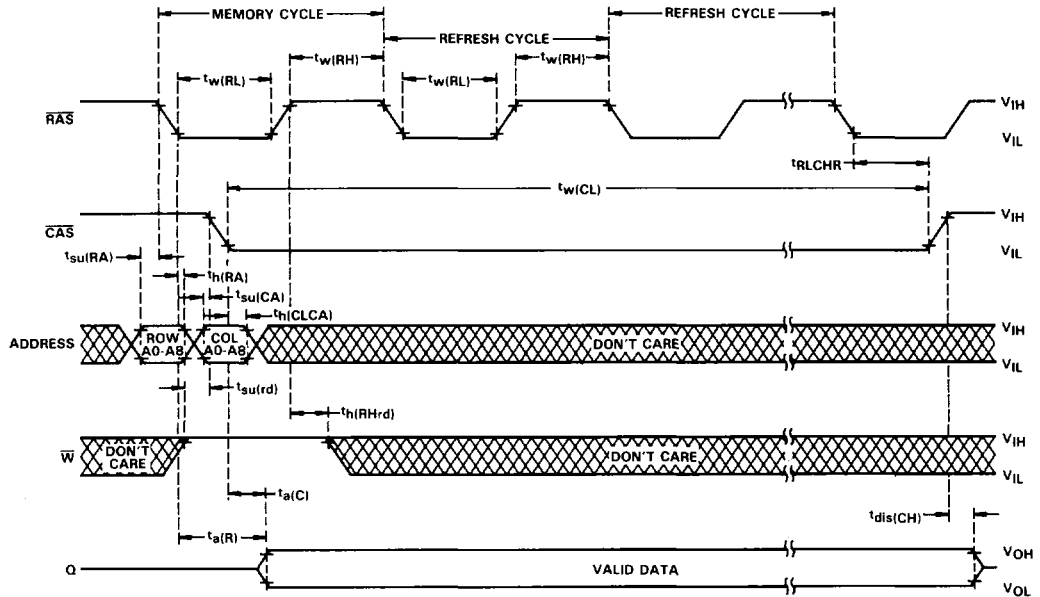
Dynamic RAMs

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**RAS-only refresh cycle timing**

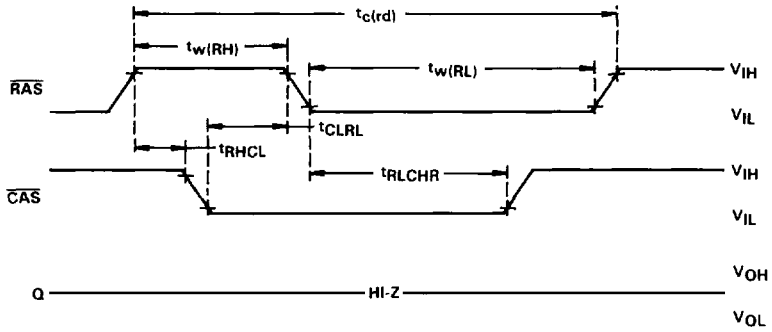


**hidden refresh cycle timing**



TMS4256, TMS4257  
262,144-BIT DYNAMIC RANDOM-ACCESS MEMORIES

automatic ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ ) refresh cycle timing



Dynamic RAMs

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