

FEATURES

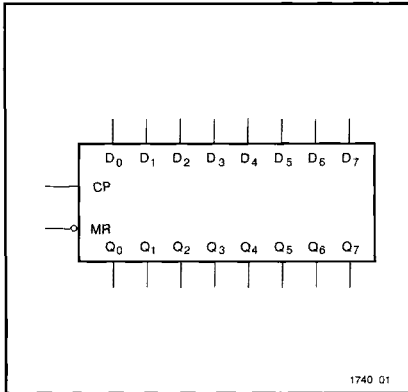
- Function, Pinout and Drive Compatible with the FCT and F Logic
- FCT-C speed at 5.8ns max. (Com'I)
FCT-A speed at 7.2ns max. (Com'I)
- Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- Power-off disable feature
- Matched Rise and Fall times
- Fully Compatible with TTL Input and Output
- Logic Levels
 - 64 mA Sink Current (Com'I), 32 mA (Mil)
 - 15 mA Source Current (Com'I), 12 mA (Mil)
 - CMOS for Low-Power Consumption — Typically 1/3 of FAST Bipolar Logic
- Edge Triggered D Flip-Flops
- Buffered Common Clock
- Buffered, Asynchronous Master Reset
- Input Clamp Diode to Limit Bus Reflections

DESCRIPTION

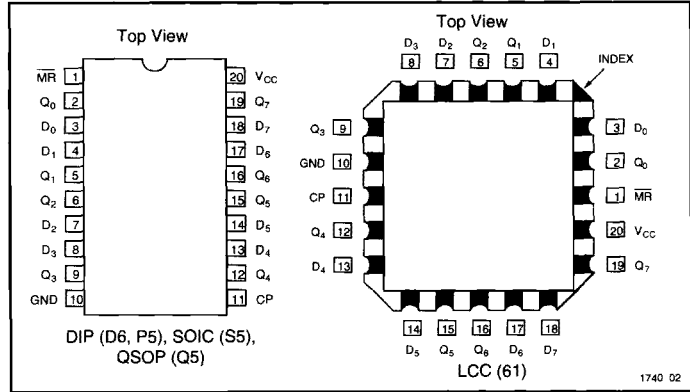
The 'FCT273T consists of eight edge triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered clock (CP) and master reset (MR) load and reset (clear) all flip-flops simultaneously. The 'FCT273T is an edge triggered register. The state of each D input (one

setup time before the low-to-high clock transition) is transferred to the corresponding flip-flop's Q output. All outputs will be forced low by a low voltage level on the MR input.

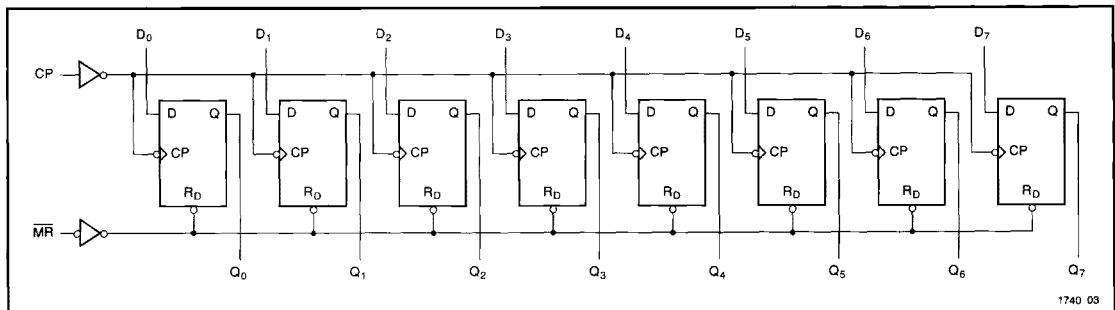
LOGIC SYMBOL



PIN CONFIGURATIONS



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS^{1,2}

| Symbol | Parameter | Value | Unit |
|-----------|--------------------------------|--------------|------|
| T_{STG} | Storage Temperature | -65 to +150 | °C |
| T_A | Ambient Temperature Under Bias | -65 to +135 | °C |
| V_{CC} | V_{CC} Potential to Ground | -0.5 to +7.0 | V |
| P_T | Power Dissipation | 0.5 | W |

1740 Tbl 01

Notes:

- Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

| Symbol | Parameter | Value | Unit |
|--------------|---------------------------|--------------|------|
| I_{OUTPUT} | Current Applied to Output | 120 | mA |
| V_{IN} | Input Voltage | -0.5 to +7.0 | V |
| V_{OUT} | Voltage Applied to Output | -0.5 to +7.0 | V |

1740 Tbl 02

- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

| Free Air Ambient Temperature | Min | Max |
|------------------------------|-------|--------|
| Military | -55°C | +125°C |
| Commercial | 0°C | +70°C |

1740 Tbl 03

| Supply Voltage (V_{CC}) | Min | Max |
|-----------------------------|--------|--------|
| Military | +4.5V | +5.5V |
| Commercial | +4.75V | +5.25V |

1740 Tbl 04

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

| Symbol | Parameter | Min | Typ ¹ | Max | Units | V_{CC} | Conditions |
|-----------|---|------------|------------------|------|-------|----------|---|
| V_{IH} | Input HIGH Voltage | 2.0 | | | V | | |
| V_{IL} | Input LOW Voltage | | | 0.8 | V | | |
| V_H | Hysteresis | | 0.2 | | V | | All inputs |
| V_{IK} | Input Clamp Diode Voltage | | -0.7 | -1.2 | V | MIN | $I_{IN} = -18mA$ |
| V_{OH} | Output HIGH Voltage | Military | 2.4 | 3.3 | V | MIN | $I_{OH} = -12mA$ |
| | | Commercial | 2.4 | 3.3 | V | MIN | $I_{OH} = -15mA$ |
| V_{OL} | Output LOW Voltage | Military | 0.3 | 0.5 | V | MIN | $I_{OL} = 32mA$ |
| | | Commercial | 0.3 | 0.5 | V | MIN | $I_{OL} = 48mA$ |
| | | Commercial | 0.3 | 0.5 | V | MIN | $I_{OL} = 64mA$ |
| I_I | Input HIGH Current | | | 20 | μA | MAX | $V_{IN} = V_{CC}$ |
| I_{IH} | Input HIGH Current | | | 5 | μA | MAX | $V_{IN} = 2.7V$ |
| I_{IL} | Input LOW Current | | | -5 | μA | MAX | $V_{IN} = 0.5V$ |
| I_{OS} | Output Short Circuit Current ² | -60 | -120 | -225 | mA | MAX | $V_{OUT} = 0.0V$ |
| I_{OFF} | Power-off Disable | | | 100 | μA | 0V | $V_{OUT} = 4.5V$ |
| C_{IN} | Input Capacitance ³ | | 5 | 10 | pF | MAX | All inputs |
| C_{OUT} | Output Capacitance ³ | | 9 | 12 | pF | MAX | All outputs |
| I_{CC} | Quiescent Power Supply Current | | 0.2 | 1.5 | mA | MAX | $V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ |

1740 Tbl 05

Notes:

- Typical values are at $V_{CC} = 5.0V$, $T_A = +25^\circ C$ ambient.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect

operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

- This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

| Symbol | Parameter | Typ ¹ | Max | Units | Conditions |
|-----------------|--|------------------|-------------------|------------|--|
| ΔI_{CC} | Quiescent Power Supply Current (TTL inputs) ² | 0.5 | 2.0 | mA | $V_{CC} = \text{MAX}$, $V_{IN} = 3.4V^2$, $f_1 = 0$, Outputs Open |
| I_{CCD} | Dynamic Power Supply Current ³ | 0.15 | 0.25 | mA/ MHz | $V_{CC} = \text{MAX}$, One Bit Toggling, 50% Duty Cycle, Outputs Open, $\overline{MR} = V_{CC}^1$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ |
| I_C | Total Power Supply Current ⁵ | 1.7 | 4.0 | mA | $V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5\text{MHz}$, $\overline{MR} = V_{CC}^1$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ |
| | | 2.2 | 6.0 | mA | $V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5\text{MHz}$, $\overline{MR} = V_{CC}^1$, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$ |
| | | 4.0 | 7.8 ⁴ | mA | $V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 2.5\text{MHz}$, $\overline{MR} = V_{CC}^1$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ |
| | | 6.2 | 16.8 ⁴ | mA | $V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 2.5\text{MHz}$, $\overline{MR} = V_{CC}^1$, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$ |

1740 Tbl 06

Notes:

- Typical values are at $V_{CC} = 5.0V$, +25°C ambient.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $$I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$$

$$I_C = I_{CC} + \Delta I_{CC} D_H N_I + I_{CCD} (f_0/2 + f_1 N_I)$$

$$I_{CC} = \text{Quiescent Current with CMOS input levels}$$

$$\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$$

- ($V_{IN} = 3.4V$)
- D_H = Duty Cycle for TTL Inputs High
 N_I = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_1 = Input Frequency
 N_I = Number of Inputs at f_1
 All currents are in milliamps and all frequencies are in megahertz.

MODE SELECT-FUNCTION TABLE

| Operating Mode | Inputs | | | Output |
|----------------|-----------------|-------------|-------|--------|
| | \overline{MR} | CP | D_n | Q_n |
| Reset (clear) | L | X | X | L |
| Load '1' | H | \lrcorner | h | H |
| Load '0' | H | \lrcorner | l | L |

- H = HIGH Voltage Level steady state
 h = HIGH Voltage Level one setup time prior to LOW-to-HIGH clock transition
 L = LOW Voltage Level steady state
 l = LOW Voltage Level one setup time prior to the LOW-to-HIGH transition
 X = Don't Care
 \lrcorner = LOW-to-HIGH clock transition

1740 Tbl 07

AC CHARACTERISTICS

| Symbol | Parameter | 'FCT273T | | | | 'FCT273AT | | | | 'FCT273CT | | | | Units | Fig. No.* |
|------------------------|--|-------------------|------|-------------------|------|-------------------|------|-------------------|------|-------------------|------|-------------------|------|-------|-----------|
| | | MIL | | COM'L | | MIL | | COM'L | | MIL | | COM'L | | | |
| | | Min. ¹ | Max. | Min. ¹ | Max. | Min. ¹ | Max. | Min. ¹ | Max. | Min. ¹ | Max. | Min. ¹ | Max. | | |
| t_{PLH} t_{PHL} | Propagation Delay Clock to Output | 2.0 | 15.0 | 2.0 | 13.0 | 2.0 | 8.3 | 2.0 | 7.2 | 2.0 | 6.5 | 2.0 | 5.8 | ns | 1, 5 |
| t_{PLH} t_{PHL} | Propagation Delay MR to Output | 2.0 | 15.0 | 2.0 | 13.0 | 2.0 | 8.3 | 2.0 | 7.2 | 2.0 | 6.8 | 2.0 | 6.1 | ns | 1, 6 |
| t_s | Set-up Time HIGH or LOW D _n to Clock | 3.5 | — | 3.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | ns | 4 |
| t_h | Hold Time HIGH or LOW D _n to Clock | 2.0 | — | 2.0 | — | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns | 4 |
| t_w | Clock Pulse Width HIGH or LOW | 7.0 | — | 7.0 | — | 6.0 | — | 6.0 | — | 6.0 | — | 6.0 | — | ns | 5 |
| t_w | MR Pulse Width LOW | 7.0 | — | 7.0 | — | 6.0 | — | 6.0 | — | 6.0 | — | 6.0 | — | ns | 6 |
| t_{rec} | Recovery Time MR to Clock | 5.0 | — | 4.0 | — | 2.5 | — | 2.0 | — | 2.5 | — | 2.0 | — | ns | 6 |

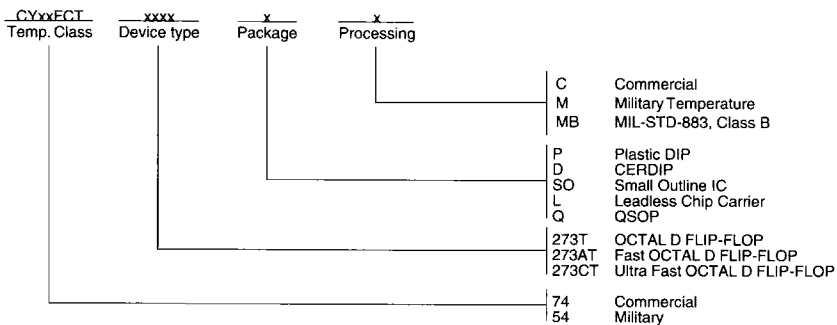
Notes:

1. Minimum limits are guaranteed but not tested on Propagation Delays.
 2. AC Characteristics guaranteed with C_i = 50pF as shown in Figure 1.
- * See "Parameter Measurement Information" in the General Information Section.

1740 Tbl 08

2

ORDERING INFORMATION



1740 04