May 1989

MBI 8289A/8289B

MULTIBUS® I iAPX 86/88/186 Bus Arbiter

Distinctive Features

- **Emulates Intel 8289 Bus Arbiter**, however, not pin for pin compatible. Please refer to pinout diagram.
- **Provides arbitration of multiple masters on MULTIBUS I.** Provides convenient arbitration for iAPX 86, 88, and 186 microprocessors in one package.
- **Supports all four modes of the Intel 8289/8289-1 Bus Arbiter** (8289A = single bus only, system/resident bus; 8289B = system/IO bus, and system/resident/IO bus).
- **Can operate with microprocessors up to 20 mHz.**
- **Capable of dirctly driving both open collector** and totem pole signals for arbitration.
- **Handles other strappable options such as ANYRQST and CRQLCK*.**

Programmable Version Available

If the MBI 8289 does not match the requirements of the design, a programmable version is available (the PLX 448) which allows the user to customize all inputs, outputs and logic. Programming is performed using industry standard tools such as ABEL™ and CUPL™ software and commonly available PLD programming hardware. Contact PLX for a data sheet on the PLX 448 and other PLX products.

Applications

* Arbitration for iAPX 86,88,186 microprocessors on the MULTIBUS I system bus.

General Description

The MBI 8289 is a CMOS bus arbiter for iAPX 86/88/186 microprocessors interfacing to the MULTIBUS I multi-master system bus. It is packaged in a compact 300 mil slimline 24 pin DIP or 28 pin J-lead PLCC/LCC. The MBI 8289 works in conjunction with the a bus controller to provide a complete interface to the multi-master MULTIBUS I system bus. The microprocessor is unaware of the MBI 8289's existence. When requesting a transfer on the MULTIBUS I system bus, the MBI 8289 prevents the bus controller, data transceivers and address latches from accessing the bus. Once the MULTIBUS I bus is obtained, the MBI 8289 signals the bus controller to continue with the access.

The MBI 8289 supports parallel arbitration resolution via the BREQ* output and BPRN* input pins. Please contact the factory if serial arbitration resolution is desired.

The MBI 8289 can support all four operating modes. These modes are selected via the RESB and IOB* input pins. The MBI 8289A supports the system bus only mode and the system/resident bus mode, while the MBI 8289B supports the IO bus/system bus and system/resident/IO bus modes. In addition, the MBI can support other strappable options, such as common bus request locking (CBRLCK*) and bus surrendering upon any request (ANYRQST).

The MBI 8289 is capable of supporting microprocessor speeds of up to 20 mHz and bus speeds up to 10 mHz.

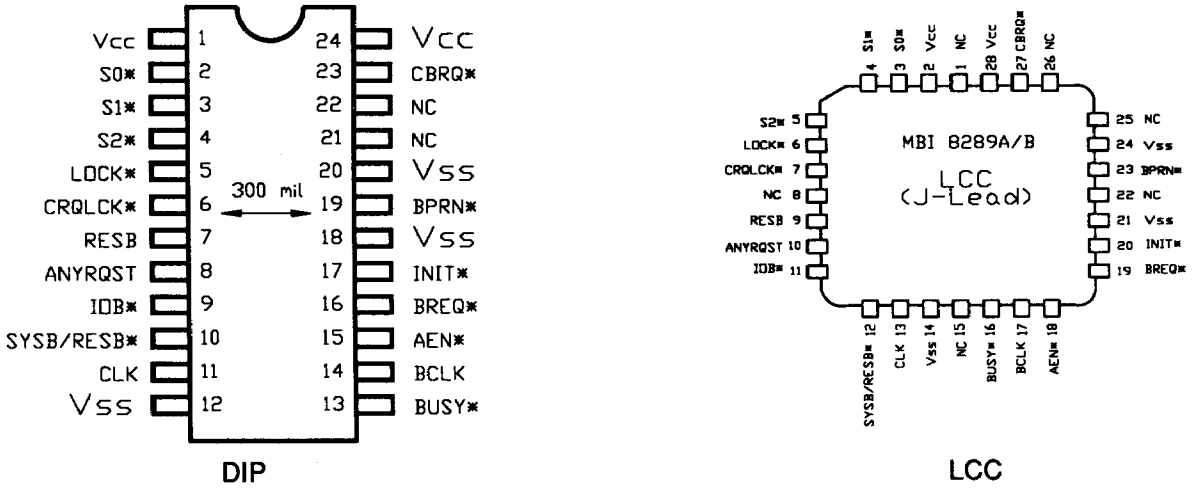

Figure 1. Pinout of MBI 8289

Patent Pending
ABEL is a trademark of Data I/O.
CUPL is a trademark of PCAD.

PLX Technology, Inc.
625 Clyde Ave., Mountain View, CA 94043

Pin Description

MBI 8289 Arbiter:

Pin # LCC	Pin # DIP	Signal	Type	Function
3	2	S0*	I	Active low; Status pin S0* from processor.
4	3	S1*	I	Active low; Status pin S1* from processor.
5	4	S2*	I	Active low; Status pin S2* from processor.
6	5	LOCK*	I	Active low; LOCK input from processor. Indicates LOCKed transaction on MULTIBUS I.
7	6	CRQLCK*	I	Active low; Input that prevents MBI 8289 from surrendering the bus to any other arbiter requesting the bus through the CBRQ* input.
9	7	RESB	I	Active high; A strappable option indicating that the MBI 8289 is operating in a system having both a multi-master system bus and a resident bus.
10	8	ANYRQST	I	Active high; A strappable option that permits the master to surrender the bus to a lower priority requesting master.
11	9	IOB*	I	Active low; A strappable option that allows the MBI 8289 to operate in a system having an I/O and multi-master system bus.
12	10	SYSB/RESB*	I	Active high; Indicates processor wishes to perform MULTIBUS I transaction when in resident bus mode (RESB strapped high). This pin is ignored if RESB is strapped low.
13	11	CLK	I	Processor CLK.
14,21, 24	12,18, 20	Vss	-	Chip Ground
16	13	BUSY*	I/O	Active low, open collector; Output indicating this master has control of the bus and is driving address and command signals. Input indicating when the multi-master bus is available.
17	14	BCLK	I	Inverted BCLK*;
18	15	AEN*	O	Active low; Output indicating this processor has control of the MULTIBUS I system bus. Used to enable address and command onto the bus.
19	16	BREQ*	O	Active low, open collector; Output used to request use of the MULTIBUS I system bus. Generally routed to system arbiter.
20	17	INIT*	I	Active low; Input causing the device to initialize to the idle state.
23	19	BPRN*	I	Active low; Input indicating this device has priority on the bus starting on the next falling BCLK* edge.
25	21	NC	O	No Connect
26	22	NC	O	No Connect
27	23	CBRQ*	I/O	Active low, open collector; Input indicating that there is a lower priority arbiter requesting use of the multi-master bus. Output from a lower priority arbiter requesting use of the multi-master bus.
2,28	1,24	Vcc	-	+5 V Chip Power
1,8, 15,22	-	NC	-	No Connect

Detailed Description

Parallel Arbitration Between Masters

The MBI 8289 supports the parallel arbitration method for resolving who controls the MULTIBUS I system bus. In this method, a each arbiter can assert its BREQ* signal indicating it wants the bus. A centralized external priority arbiter is used to determine the highest requester and that requesters BPRN* input is asserted. If a higher priority request asserts its BREQ* output to the centralized arbiter, the arbiter will negate the current arbiters BPRN* input and assert the new arbiter's BPRN* input. Depending on the straps and modes of operation, the MBI 8289 will surrender the bus to a lower priority request when CBRQ* is asserted.

In the parallel arbitration mode, any number of arbiters can be connected to the multi-master system bus, as long as the centralized prioritizing circuit can resolve who is the highest priority and assert the appropriate BPRN* output when one clock cycle.

Serial Arbitration Between Masters

The MBI 8289 is capable of supporting serial arbitration via the BREQ* output and the BPRN* input/BPRO* output daisy chain. Once BREQ* is asserted, the highest priority arbiter will assert its BPRO* output starting the daisy-chain. Once the requesting arbiter receives an asserted BPRN*, it will not assert BPRO*, thus stopping the daisy-chain grant. In order to support this, the MBI 8289 must be modified to provide the BPRO* output. This necessitates the replacement of one output pin on the device, such as AEN*. Since the device is programmable, the appropriate replacement can be made on an individual basis.

When supporting serial arbitration, the BPRN*/BPRO* daisy chain arbitration must be resolved within one bus clock cycle. This requirement would limit the MBI 8289 to only 2 arbiters using the -45 part. In order to increase this limit, the designer should use the BPRO* signal as a gating signal to an external OR gate with BPRN* as the other signal. The output of this gate would be is BPRO* for this master. This reduces the delay for BPRN*/BPRO* to one gate delay.

Modes of Operation

The MBI 8289 is capable of supporting the four Intel 8289 operating modes. The MBI 8289A supports two of the modes and the 8289B supports the other two modes. Here are the operating modes supported by the MBI 8289:

Input Pin Strapping		Mode	Part Number
RESB	IOB*		
L	H	Single Bus Only	8289A
H	H	Resident Bus/System bus	8289A
L	L	IO Bus/System bus	8289B
H	L	IO/Resident/System bus	8289B

If the MBI 8289 is strapped as a single bus only mode, then any valid request from the microprocessor (with the exception of HALT and IDLE) will cause the MBI 8289 to request the MULTIBUS I system bus. The MBI 8289 will surrender the bus if a valid request comes in while the microprocessor is in IDLE or HALTed. Note that the MBI 8289 does not surrender then bus until another valid request is received (release on request) and the microprocessor is IDLE or HALTed.

If the MBI 8289 is strapped as a resident bus/system bus, any valid request from the microprocessor (with the exception of HALT and IDLE) and the assertion of SYSB/RESB* high will cause the MBI 8289 to request the system bus. This indicates that the microprocessor is requesting an access to the system bus (SYSB/RESB* asserted high) instead of the local resident bus. The MBI 8289 will surrender the bus is a valid request comes in while SYSB/RESB* is asserted low (local resident access occurring), or the microprocessor is IDLE or HALTed.

Please refer to the Intel 8289 Bus Arbiter data sheet for a description of the other two modes.

CRQLCK* Strap

This strap can be used to prevent the MBI 8289 from surrendering the bus to any other arbiter requesting the bus through the CBRQ* input. This would occur if a lower priority master wanted the bus. This feature is activated by tying this input low.

ANYRQST Strap

This strap can be used to permit the arbiter to surrender the bus to a lower priority arbiter as if it were a higher priority arbiter. If ANYRQST is strapped low, the arbiter surrenders the bus according to the "Modes of Operation" section above. If ANYRQST is strapped high, the arbiter will surrender the bus whenever CBRQ* is asserted. Strapping ANYRQST high and CBRQ* low configures the arbiter to release the bus after each access (release when done).

MBI 8289 Clocking

The MULTIBUS I bus clocks signals on the falling edge of BCLK*. The MBI 8289 clocks signals on the rising edge of BCLK. Therefore, an inverter must be placed between the MULTIBUS I BCLK* and the BCLK input of the MBI 8289. This inverter should be fast (4-6 ns) and the output should be terminated to provide a clean clock input to the MBI 8289.

The processor clock input (CLK) clocks the processor signals on the rising edge of the clock. Please refer to the timing specifications to determine the setup times requires with respect to the processor clock speed.

Additional Information

Additional information about the modes of operation and the strappable options can be found in the Intel 8289 data sheet. Please refer to this data sheet or call PLX for more information.

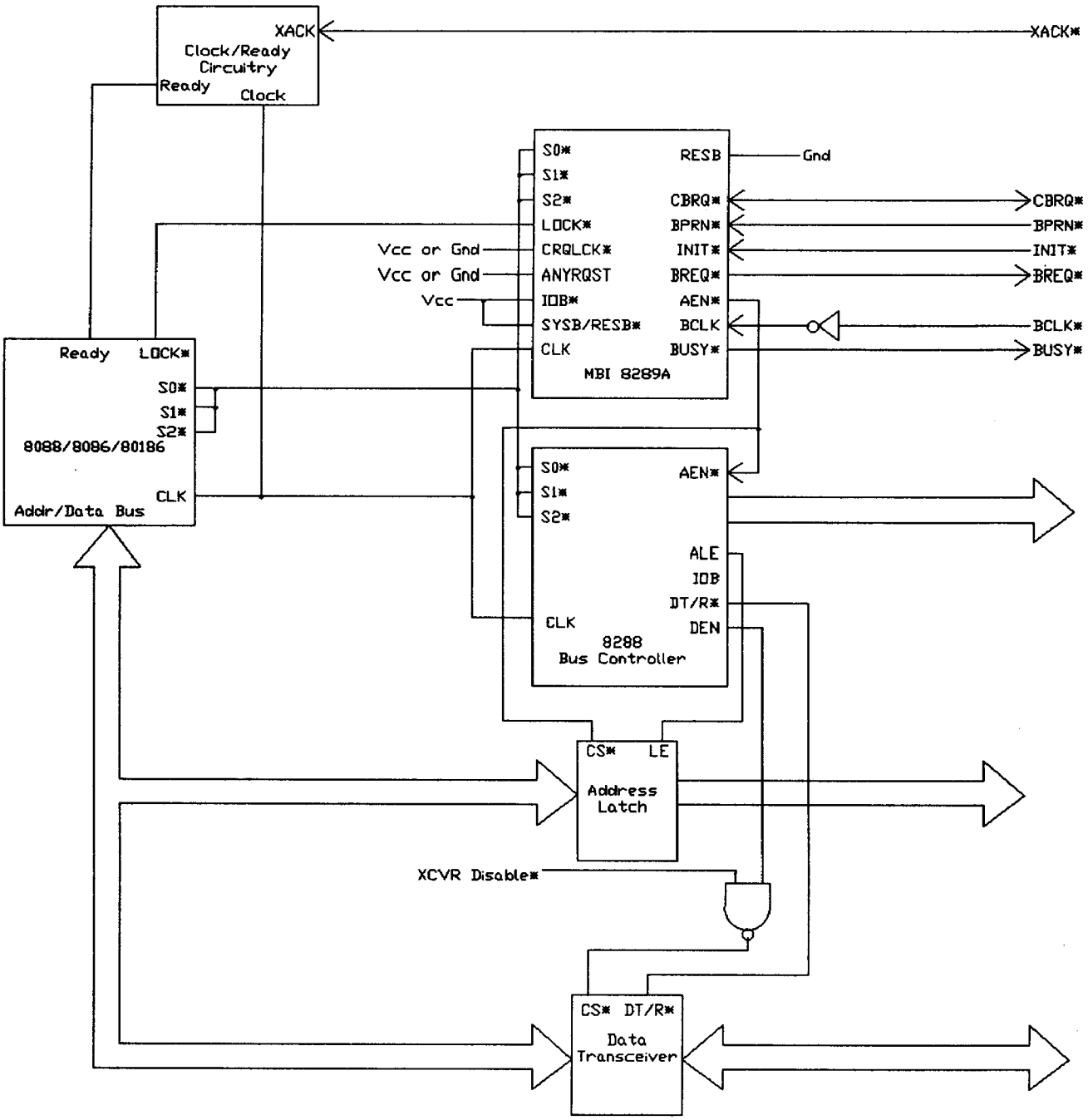

Figure 2. MBI 8289A System Configuration (Single Bus System)

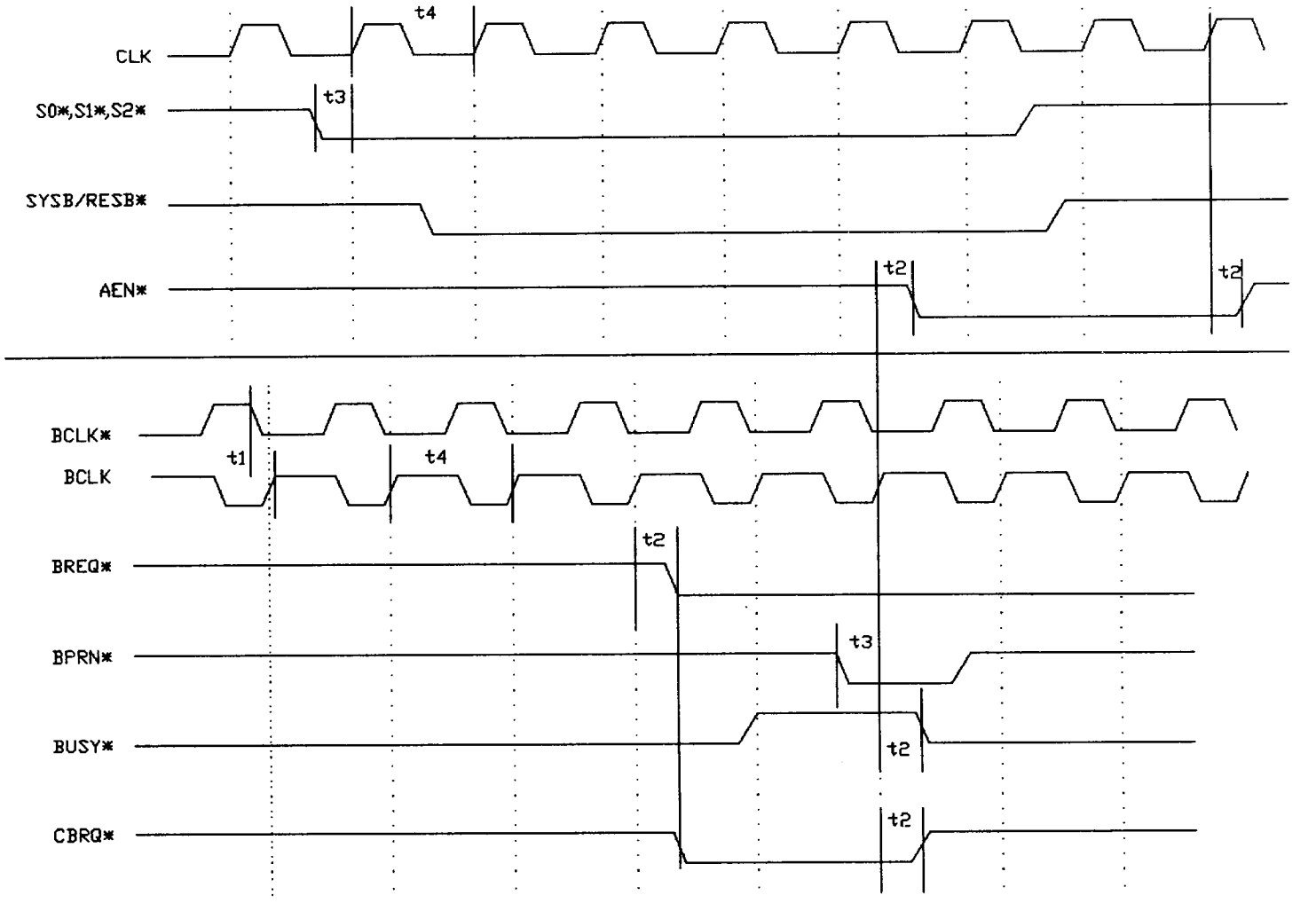

Figure 3. MBI 8289 Timing Diagram

Specifications

Timing Parameters	Signals	Max. Time(ns) -25,-35,-45 parts unless otherwise specified	Description
t1	BCLK* to BCLK	25,15,5	Inverter delay on BCLK*.
t2	Output Assertion Delay from CLK or BCLK	15,20,30	Output assertion for all signals with respect to rising BCLK edge.
t3	Input setup	20,25,30	Setup time for inputs to their respective clocks (CLK or BCLK).
t4	Maximum CLK/BCLK frequency	28.5,22,16.7 mHz	Minimum clock periods: 35, 45, 60 ns

Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground (pin 24 to pins 12, 18, & 20 DIP)	-0.5V to +7.0V
DS Voltage to Outputs in High Z State	-0.5V to +7.0V
UV Exposure	7000 Wsec/cm^2
DC Programming Voltage	14.0V

Operating Ranges

Commercial (C) Devices	
Temperature Ambient	0°C to +70°C
Supply Voltage (V_{cc})	5V ± 5%

Electrical Characteristics Tested over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
V_{OH}	Output HIGH Voltage	V_{cc}=Min, V_{IN}=V_{IH} or V_{IL}	I_{OH}=-3.0mA	2.4		V
V_{OL}	Output LOW Voltage	V_{cc}=Min, V_{IN}=V_{IH} or V_{IL}	Pins 16,17, 19,21 (DIP) I_{OL}=24mA		0.5	V
			Pins 13,15 22,23 (DIP) I_{OL}=48mA		0.5	V
V_{IH}	Input HIGH Level			2.0		V
V_{IL}	Input LOW Level				0.8	V
I_{IX}	Input Leackage Current	V_{SS} <= V_{IN} <= V_{CC}, V_{CC} = Max		-10	10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{SS} <= $V_{OU}T$ <= V_{CC}		-40	40	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_{OUT} = 0.5V		-30	-90	mA
I_{CC}	Power Supply Current	V_{CC} = Max, V_{IN} = GND Outputs Open			80	mA

Capacitance (sample tested only)

Parameter	Test Conditions	Pins (DIP)	Typ	Units
C_{IN}	V_{IN} = 2.0V @ f = 1MHz	2-11,14	5	pF
		13,15-17, 19,21-23	10	pF
C_{OUT}	V_{IN} = 2.0V @ f = 1 MHz	13,15-17, 19,21-23	10	pF

Hysteresis

Parameter	Description	Typ	Units
V_{T+}	Positive-going threshold	1.5	V
V_{T-}	Negative-going threshold	1.3	V
ΔV_T	Hysteresis (V_{T+} - V_{T-})	0.2	V

Packaging Information

The devices are available in a 24 pin slimline DIP (300 mil wide) or 28 pin LCC.

See PLX 448 or PLX 464 January 1989 data sheets for package dimensions.

Contact PLX for further packaging information.