TMC7201

040906

S-99 Only

002061

T 2061 TRW

CMOS Parallel First-In/First-Out Memory

512 x 9 bit, 65ns

The TMC7201 is a dual port FIFO memory which implements first-in, first-out sequential storage of 512 9-bit data words. The device supports asynchronous read and write operations. Full and empty flags are provided to prevent data overflow and underflow. Expansion control signals allow the FIFO to be easily cascaded, allowing multiple word widths and depths.

The dual port RAM array is addressed internally using ring counter pointers. The Write pointer addresses the location where data is to be written next, and the Read pointer addresses the location to be read next. Write Enable and Read Enable controls are provided to toggle data in and out of the device. The read pointer can be reset to its initial position with the Retransmit control.

The high performance architecture reduces costly fallthrough delays associated with shift register FIFOs. The worst case fallthrough delay associated with this dual port RAM FIFO is the time required to update the pointers, not the time required for data to propagate through the full depth of a register array. The TMC7201 is pin and function compatible with the Integrated Device Technology IDT7201 and the Mostek MK4501.

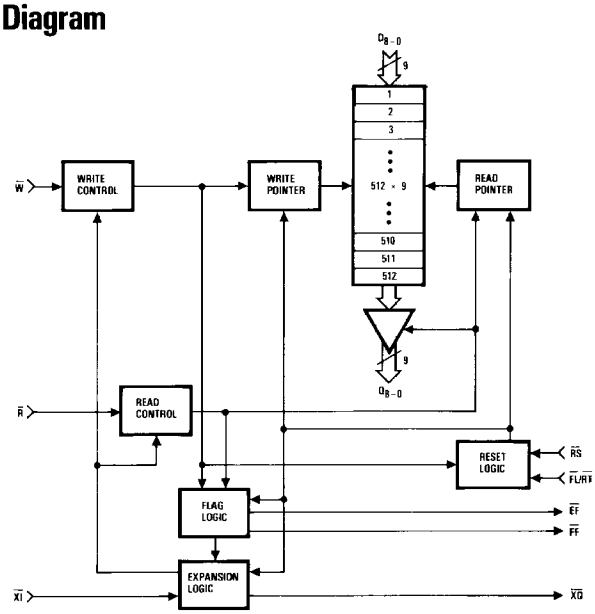
Features

- First-In, First-Out Dual Port Memory
- Lower Power Consumption Than IDT7201L And MK4501
  Active: 220mW
  Power Down: 55μW
- 512 Words By 9 Bits Organization
- 65ns Access Time: TMC7201L65
- 120ns Access Time: TMC7201L120
- Asynchronous And Simultaneous Read/Write
- Empty And Full Warning Flags
- Auto Retransmit Capability
- Readily Expandable In Word Depth And Bit Width
- TTL Compatible
- Single +5V Power Supply

Applications

- High-Speed Disk Or Tape Controller
- Local Area Networks
- Video Time Base Correction
- A/D Output Buffers
- Input/Output Formatter For Digital Filters And FFTs

Functional Block Diagram



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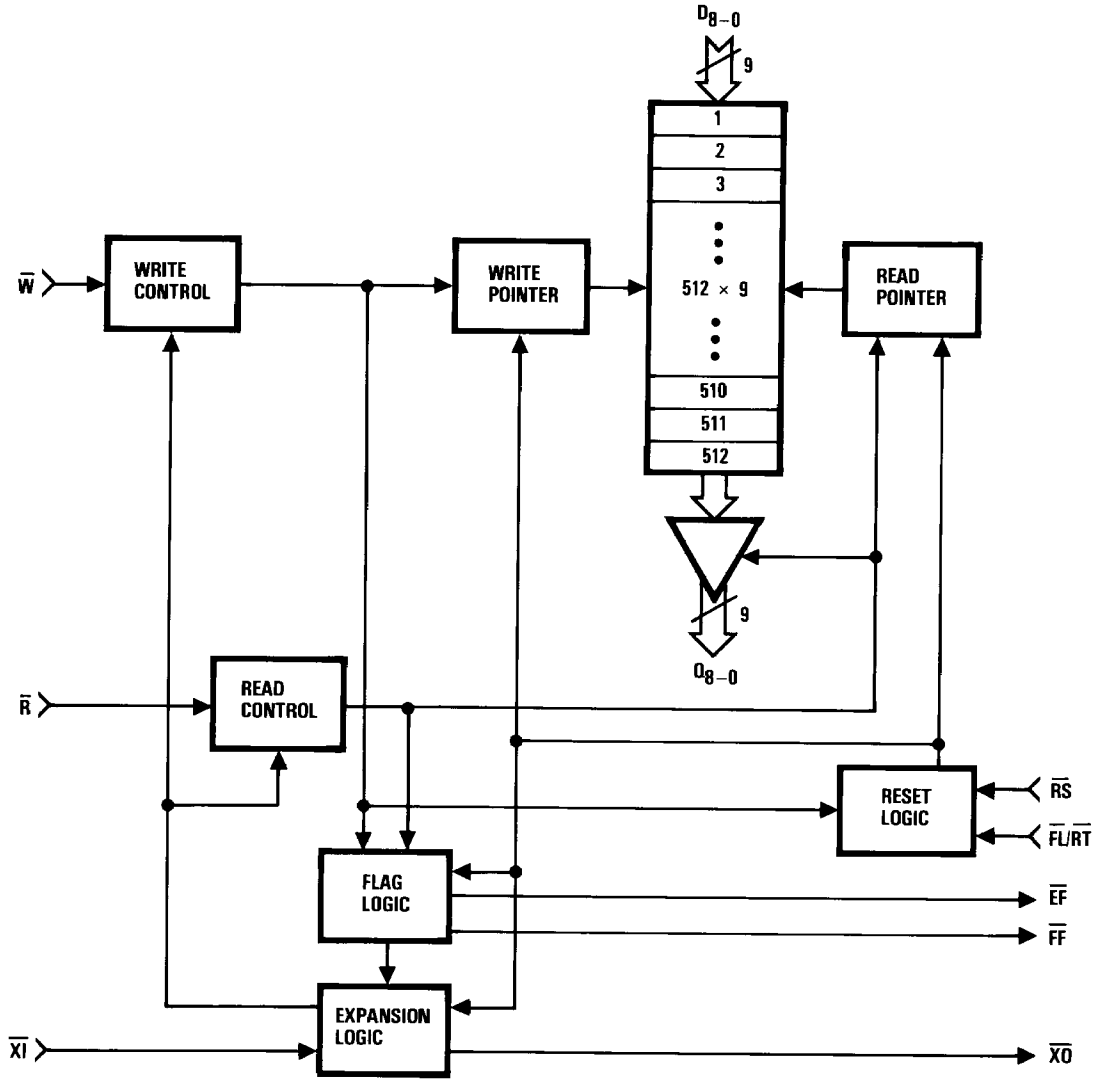
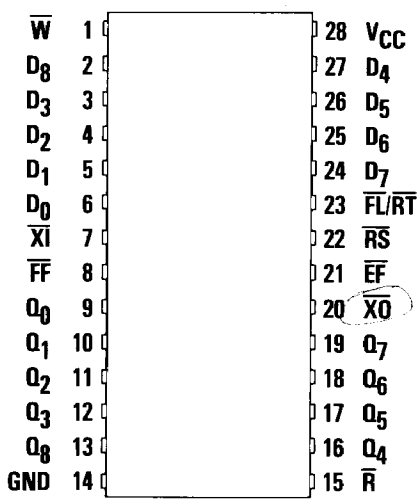
Functional Block Diagram



Pin Assignments



28 Lead DIP

Functional Description

Data Input

Following power up, the Reset control ($\overline{RS}$) must be pulsed LOW to set the internal Read and Write pointers to their initial state (the first word location). The FIFO must be reset before a write operation can occur. Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) controls must be in the HIGH state during reset.

Data present at D_{8-0} is loaded into the FIFO by the active LOW Write Enable control. The falling edge of $\overline{W}$ initiates a write cycle, as long as the Full Flag ($\overline{FF}$) is not set. Data words are stored in the RAM array sequentially. Current write addresses are generated internally by ring counter logic. Write operations are independent of read operations. Input data must satisfy setup and hold time requirements with respect to the

rising edge of $\overline{W}$. When the storage capacity has been reached, $\overline{FF}$ goes LOW to prevent data overflow. After a valid read operation, $\overline{FF}$ will go HIGH and allow for another write operation to begin.

Data Output

Data is accessed on a first-in, first-out basis from the FIFO by the active LOW Read Enable control. The falling edge of $\overline{R}$ initiates a read cycle, as long as the Empty Flag ($\overline{EF}$) is not set. Current read addresses are generated internally by ring counter logic. Read operations are independent of write operations. After $\overline{R}$ goes HIGH, the data output port (Q_{8-0}) will be in a high-impedance state until the next read operation. When all data has been read from the FIFO, $\overline{EF}$ will go LOW, and subsequent read operations are inhibited. After a valid write operation, $\overline{EF}$ will go HIGH and allow for another read operation to begin.

Signal Definitions

Power

V_{CC}, GND — The TMC7201 operates from a single +5 Volt supply.

Inputs

D_{8-0} — The 9-bit input port accepts data words for sequential storage during the write cycle.

Outputs

Q_{8-0} — The 9-bit output port is in the high-impedance state when $\overline{R}$ is HIGH.

Controls

$\overline{RS}$ — Reset is an active LOW control which sets the Read and Write pointers to the first word location.

$\overline{R}$ — Read Enable is an active LOW control which initiates a read cycle as long as $\overline{EF}$ is not set.

$\overline{W}$ — Write Enable is an active LOW control which initiates a write cycle as long as $\overline{FF}$ is not set.

$\overline{XI}$ — Expansion In indicates whether the device is being operated in single or depth expansion mode. $\overline{XI}$ is tied LOW for single device operation. For depth expansion, $\overline{XI}$ is connected to $\overline{XO}$ of the previous device.

$\overline{FL}/\overline{RT}$ — First Load/Retransmit is a control to the reset logic. $\overline{FL}/\overline{RT}$ is the active LOW, retransmit enable signal in single device mode and the first load control in depth expansion mode.

When $\overline{RT}$ is pulsed LOW, the internal read pointer is reset to the first location, but does not affect the write pointer. $\overline{R}$ and $\overline{W}$ must be HIGH during retransmit. $\overline{RT}$ cannot be used in depth expansion mode.

When used in depth expansion mode, $\overline{FL}$ of the first FIFO to be loaded is tied LOW.

Flags

$\overline{FF}$ — Full Flag goes LOW when the write pointer is one word from the read pointer. This indicates that the word capacity of the FIFO has been reached and prevents data overflow by inhibiting write operations.

$\overline{EF}$ — Empty Flag goes LOW when all of the data has been read from the FIFO. $\overline{EF}$ inhibits read operations with the data outputs remaining in a high-impedance state.

$\overline{XO}$ — Expansion Out Flag provides a signal to the next cascaded device in depth expansion mode. $\overline{XO}$ provides a pulse to access the next FIFO when the last word location has been reached. $\overline{XI}$ is connected to $\overline{XO}$ of the previous device.

Package Interconnections

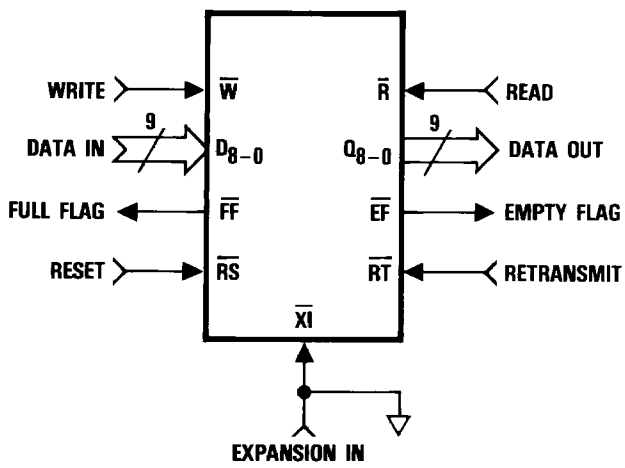
Signal Type	Signal Name	Function	Pin
Power	V_{CC}	Supply Voltage	28
	GND	Ground	14
Data Inputs	D_{8-0}	Input Word	2, 24–27, 3–6
Data Outputs	Q_{8-0}	Output Word	13, 19–16, 12–9
Controls	$\overline{RS}$	Reset	22
	$\overline{R}$	Read Enable	15
	$\overline{W}$	Write Enable	1
	$\overline{XI}$	Expansion In	7
	$\overline{FL}/\overline{RT}$	First Load/Retransmit	23
Flags	$\overline{FF}$	Full	8
	$\overline{EF}$	Empty	21
	$\overline{XO}$	Expansion Out	20

Operating Modes

Single Device Mode

For storage of 512 words or less, a single TMC7201 may be used. $\overline{XI}$ must be tied LOW for single device operation. $\overline{FL}/\overline{RT}$ is the retransmit enable signal in single device mode.

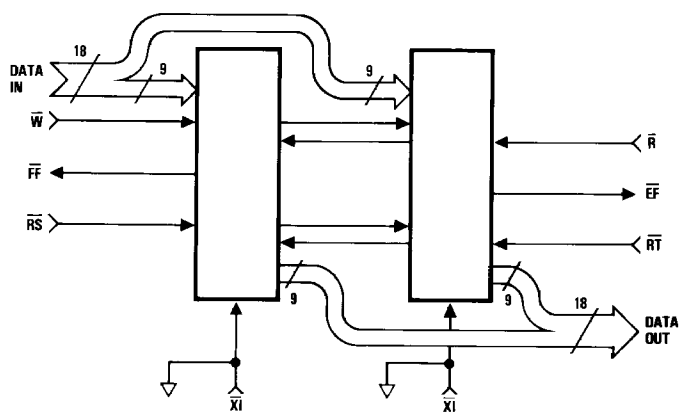
Figure 1. Single Device Mode (512 Words x 9 Bits)



Width Expansion Mode

Word size may be expanded by connecting the corresponding control signals of multiple devices. Any of the devices can be used to monitor the flags, $\overline{FF}$ and $\overline{EF}$. Do not connect output control signals together. Additional devices may be added to obtain any word width.

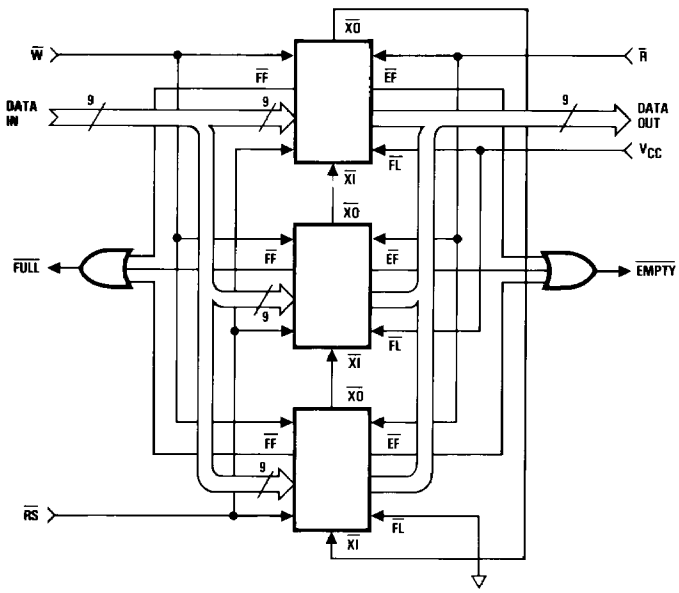
Figure 2. Width Expansion Mode (512 Words x 18 Bits)



Depth Expansion Mode

Word capacity may be expanded to any depth by adding multiple devices. $\overline{FL}$ of the first device to be loaded must be tied LOW. The remaining devices must have $\overline{FL}$ tied HIGH. $\overline{XO}$ of each device must be connected to $\overline{XI}$ of the next device. Composite full and empty flags are formed with the addition of OR logic gates. In the depth expansion mode, $\overline{RT}$ is not available.

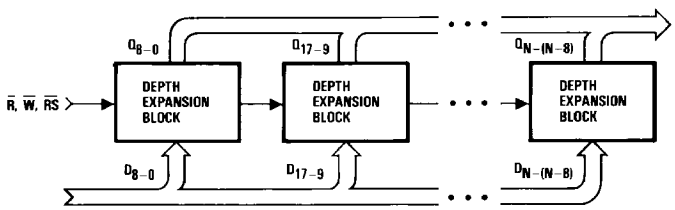
Figure 3. Depth Expansion Mode (1536 Words x 9 Bits)



Compound Expansion Mode

Both bit width and word depth may be expanded to configure large arrays.

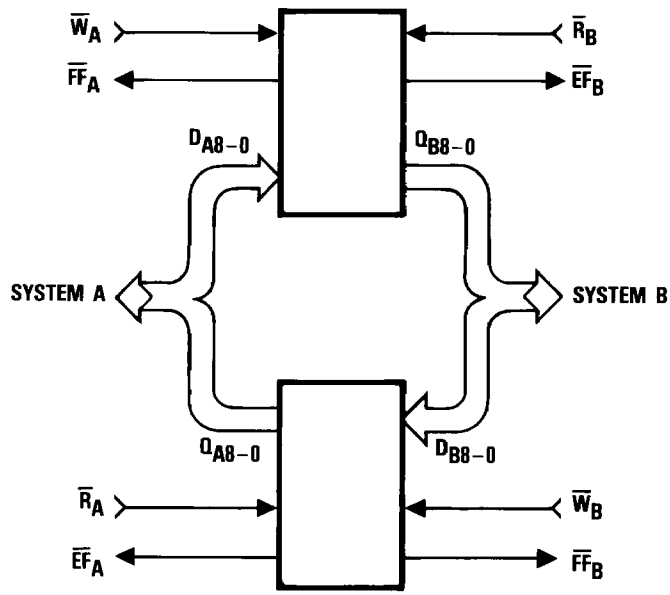
Figure 4. Compound Expansion Mode



Bidirectional Mode

Data buffering between two systems can be achieved by pairing FIFO arrays. This allows each system to read and write data. $\overline{FF}$ must be monitored on the device to which data is written and $\overline{EF}$ must be monitored on the device from which data is read. In the bidirectional mode, data may be expanded in width and depth.

Figure 5. Bidirectional Mode



Data Flow Through Mode

The read flow through mode allows a single word to be read immediately after writing one data word into an empty FIFO. The write flow through mode allows writing a single word of data immediately after reading one data word from a full FIFO.

Absolute maximum ratings (beyond which the device may be damaged) [1]

Parameter		Temperature Range: Standard	Units
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	°C
T_{STG}	Storage Temperature	−55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

Note:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.

Operating conditions

Parameter		Temperature Range: Standard Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input Voltage, Logic HIGH	2.0			V
V_{IL}	Input Voltage, Logic LOW [1]			0.8	V

Note:

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range: Standard Min	Nom	Max	Units
I_{LI}	Input Leakage Current (Any Input)	V_{IN} = 0.4V to V_{CC}	−1		1	µA
I_{LO}	Output Leakage Current	$R \geq V_{IH}$, V_{OUT} = 0.4V to V_{CC}	−10		10	µA
V_{OH}	Output Logic Voltage, HIGH	I_{OH} = −1mA	2.4			V
V_{OL}	Output Logic Voltage, LOW	I_{OL} = 4mA			0.4	V
I_{CC1}	Average V_{CC} Power Supply Current [2]			30	40	mA
I_{CC2}	Average Standby Current [2]	$\overline{R}$, $\overline{W}$, $\overline{RS}$, $\overline{FL/RT}$ = V_{IH}		3	7	mA
I_{CC3}	Power Down Current [2]	All Input = V_{CC} −0.2V			10	µA

Notes:

1. V_{CC} = 5V ± 10%.
2. Outputs open.

AC characteristics within specified operating conditions [1,2]

Parameter		7201L65 Temperature Range Standard Min	7201L65 Temperature Range Standard Max	7201L120 Temperature Range Standard Min	7201L120 Temperature Range Standard Max	Units
t_{RC}	Read Cycle Time	80		140		ns
t_A	Access Time		65		120	ns
t_{RR}	Read Recovery Time	15		20		ns
t_{RPW}	Read Pulse Width	65		120		ns
t_{RLZ}	Read Pulse LOW to Data Bus at Low-Z	10		10		ns
t_{WLZ}	Write Pulse HIGH to Data Bus at Low-Z [3]	15		20		ns
t_{DV}	Data Valid from Read Pulse HIGH	5		5		ns
t_{RHZ}	Read Pulse HIGH to Data Bus at High-Z		30		35	ns
t_{WC}	Write Cycle Time	80		140		ns
t_{WPW}	Write Pulse Width	65		120		ns
t_{WR}	Write Recovery Time	15		20		ns
t_{DS}	Data Setup Time	30		40		ns
t_{DH}	Data Hold Time	10		10		ns
t_{RSC}	Reset Cycle Time	80		140		ns
t_{RS}	Reset Pulse Width	65		120		ns
t_{RSR}	Reset Recovery Time	15		20		ns
t_{RTC}	Retransmit Cycle Time	80		140		ns
t_{RT}	Retransmit Pulse Width	65		120		ns
t_{RTR}	Retransmit Recovery Time	15		20		ns
t_{EFL}	Reset to Empty Flag LOW		80		140	ns
t_{FFH}	Reset to Full Flag HIGH		80		140	ns
t_{REF}	Read LOW to Empty Flag LOW		60		60	ns
t_{RFF}	Read HIGH to Full Flag HIGH		60		60	ns
t_{WEF}	Write HIGH to Empty Flag HIGH		60		60	ns
t_{WFF}	Write LOW to Full Flag LOW		60		60	ns

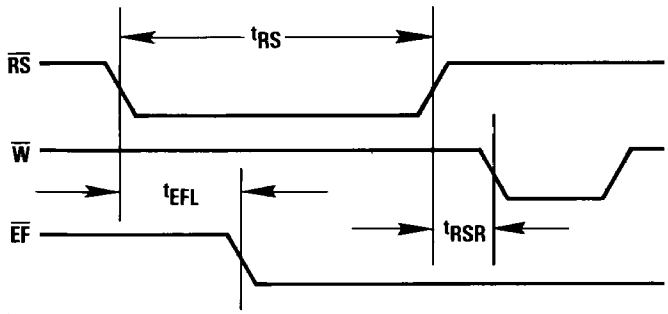
Notes:

1. V_{CC} = 5V ± 10%.
2. All transitions are measured at a 1.5V level. Input pulse levels = GND to 3.0V. Input rise and fall times = 5ns.
3. Read data flow through mode only.

Capacitance

Parameter		Test Conditions	Temperature Range Standard Nom	Units
C_{IN}	Input Capacitance	V_{IN} = 0V, T_A = 25°C, f = 1MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, T_A = 25°C, f = 1MHz	7	pF

Figure 6. Reset Timing Diagram



Notes:

1. $t_{RSC} = t_{RS} + t_{RSR}$.
2. W and R = V_{IH} during reset.

Figure 7. Write Operation Timing Diagram

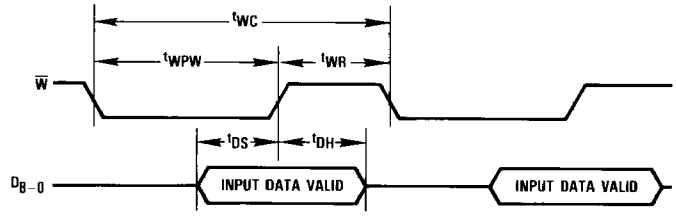


Figure 8. Read Operation Timing Diagram

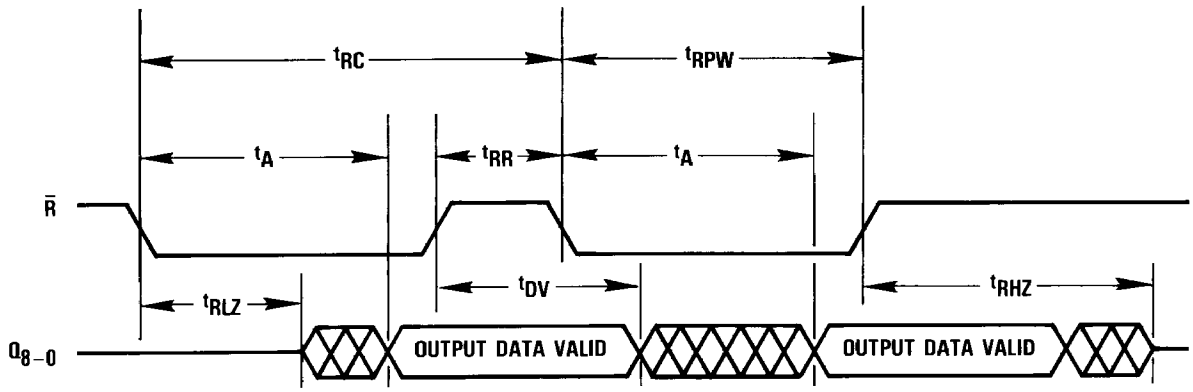


Figure 9. Full Flag from Last Write to First Read Timing Diagram

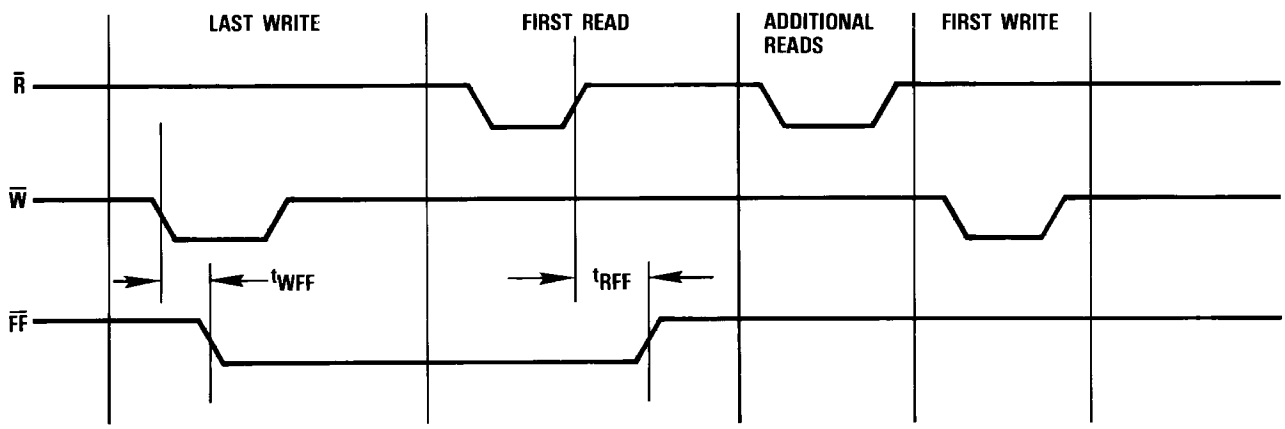


Figure 10. Empty Flag from Last Read to First Write Timing Diagram

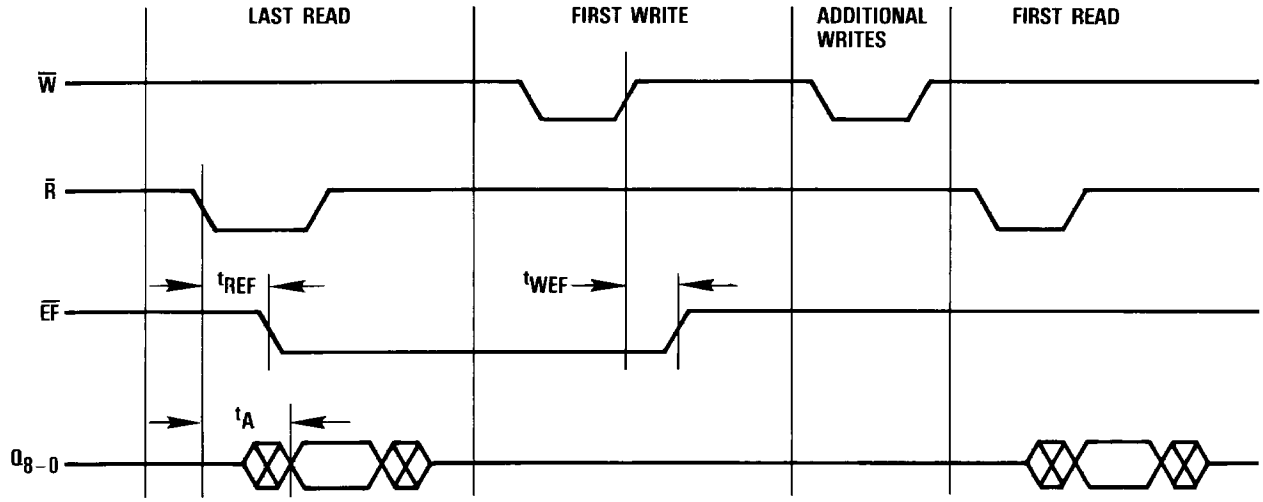
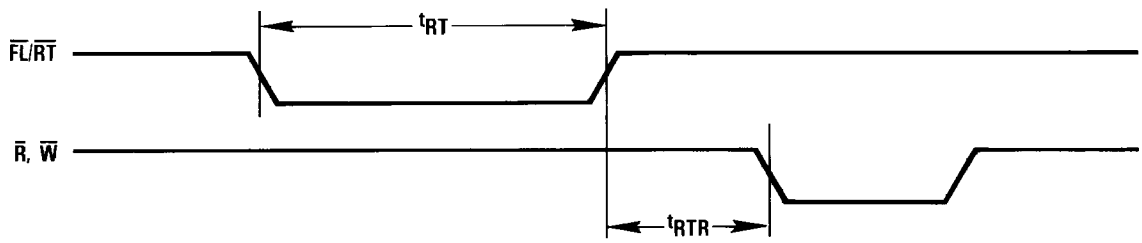


Figure 11. Retransmit Timing Diagram



Notes:

1. $t_{RTC} = t_{RT} + t_{RTR}$.
2. $\overline{EF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

Figure 12. Empty Flag Timing Diagram

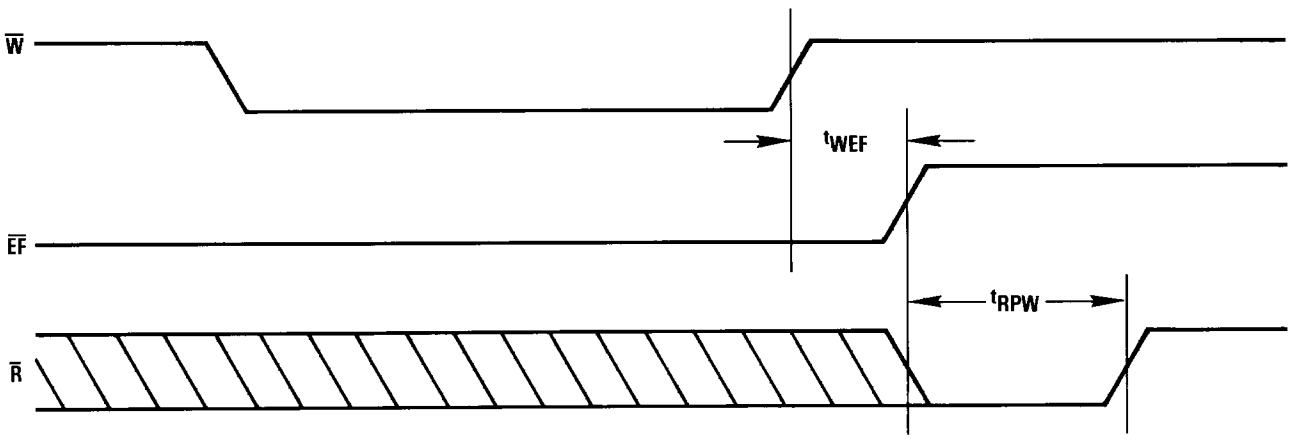


Figure 13. Full Flag Timing Diagram

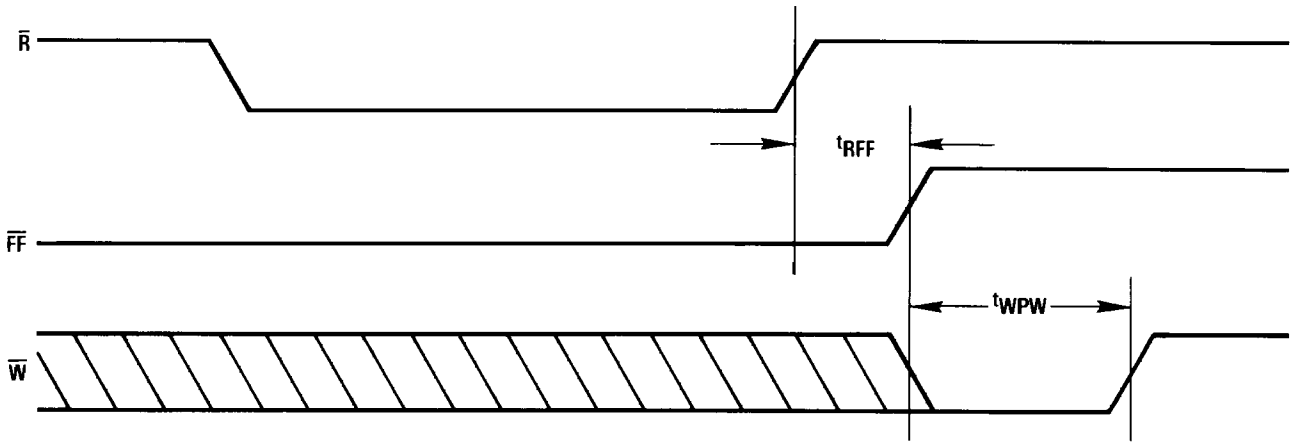


Figure 14. Read Data Flow Through Mode Timing Diagram

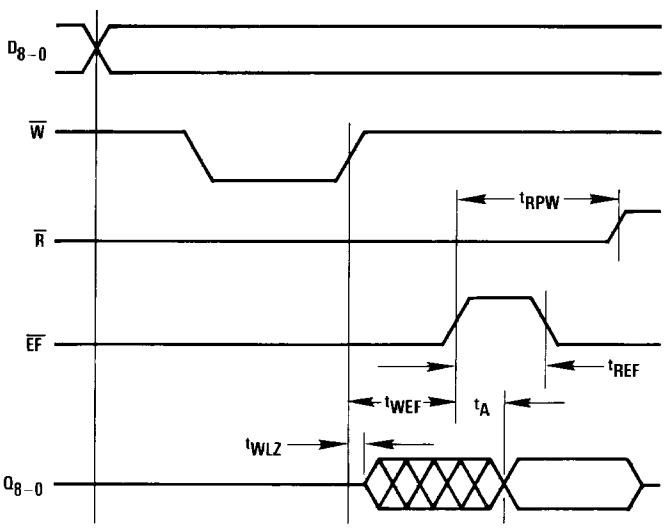


Figure 15. Write Data Flow Through Mode Timing Diagram

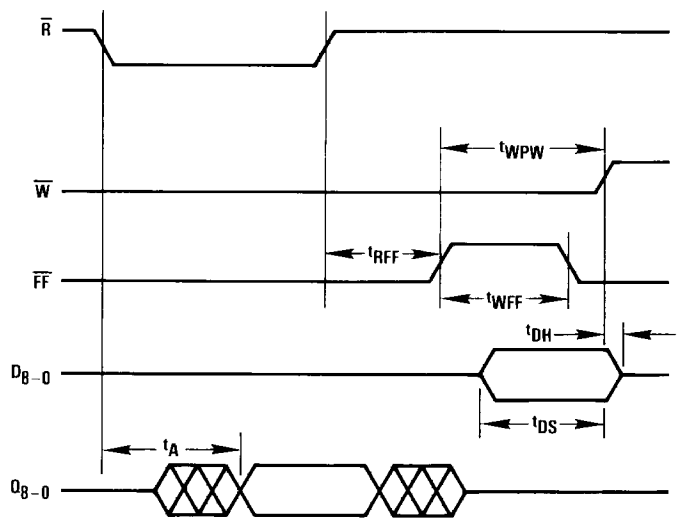
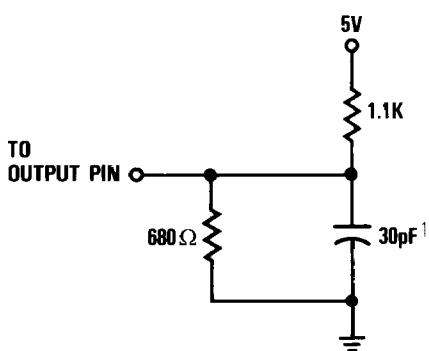


Figure 16. Output Load



Note:

1. Includes jig and scope capacitances.

Ordering Information [1]

Product Number	Temperature Range	Screening	Package	Package Marking
TMC7201L65P	STD = 0°C to 70°C	Commercial, 65ns	28 Lead Plastic DIP	7201L65P
TMC7201L120P	STD = 0°C to 70°C	Commercial, 120ns	28 Lead Plastic DIP	7201L120P

Note:

1. Contact factory for availability.

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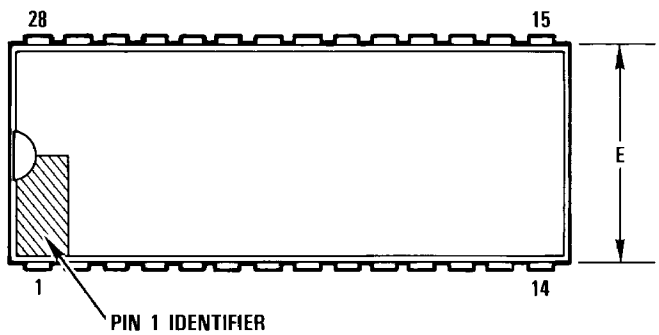
28 Lead Plastic DIP



Dimensions

	Inches (Millimeters)		
Sym	Min	Max	Nom ± Tol.
A		0.216 (5.5)	
b	0.015 (0.38)	0.021 (0.53)	
b_1	0.045 (1.14)	0.065 (1.65)	
c	0.010 (0.25)	0.015 (0.38)	
D	1.440 (36.60)	1.460 (37.08)	
E	0.540 (13.72)	0.560 (14.22)	
E_1	0.590 (14.99)	0.610 (15.49)	
e	0.090 (2.29)	0.110 (2.79)	
L	0.100 (2.50)	0.115 (2.92)	
Q	0.020 (0.51)		
S	0.065 (1.65)	0.085 (2.16)	
F	0.600 (15.24)	0.695 (17.66)	

Ref. 90X00181