SMM6312C

CMOS 128K-BIT MASK ROM

●Low Supply Current
●Access Time 250ns
●16,384 Words×8 Bits Asynchronous

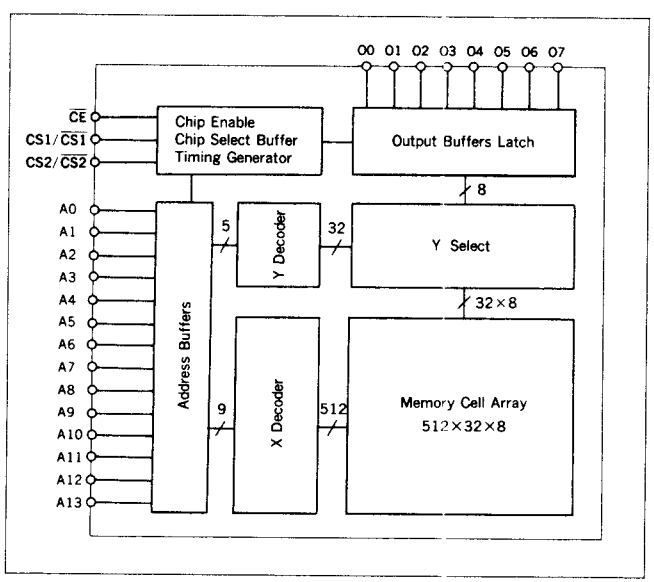
■ DESCRIPTION

The SMM6312C is a 16,384 words × 8 bits asynchronous CMOS mask programmable ROM. This device operates on a single power supply, its input and output levels are TTL compatible and the outputs are 3 state types. This device does not require clock circuit ; it has a detection circuit which detects the difference of address, CS1/$\overline{CS1}$, CS2/$\overline{CS2}$ and $\overline{CE}$ input. With the detected signal, the timing signal is generated (internal synchronous type). With such a significant performance, power dissipation is low, processing speed is high and it can be used for various applications.

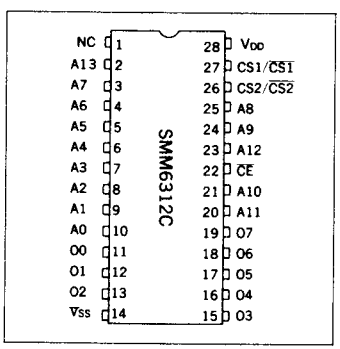
■ FEATURES

- Access time ·····250ns
- Low supply current·····standby : 0.1μA (Typ)
  operation : 16mA (Typ)
- Single power supply ·····5V±10%
- Internal synchronous type
- TTL compatible inputs and outputs
- 3-state output with wired-OR capability
- Package ·····28-pin DIP (plastic)

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

A0 to A13	Address Input
$\overline{CE}$	Chip Enable
CS1/$\overline{CS1}$, CS2/$\overline{CS2}$	Chip Select
O0 to O7	Data Output
V_{DD}	Power Supply (+5V)
V_{SS}	Power Supply (0V)
NC	No connection

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage	V_I	−0.5 to V_{DD}+0.3	V
Output voltage	V_O	−0.5 to V_{DD}+0.3	V
Power dissipation	P_D	1.0	W
DC output current	I_O	10	mA
Operating temperature	T_{opr}	−10 to 70	℃
Storage temperature	T_{stg}	−65 to 150	℃
Soldering temperature and time	T_{sol}	260℃, 10s (at lead)	—

■ ELECTRICAL CHARACTERISTICS

● DC Characteristics

(V_{DD}=+5V±10%, V_{SS}=0V, Ta=−10 to +70℃)

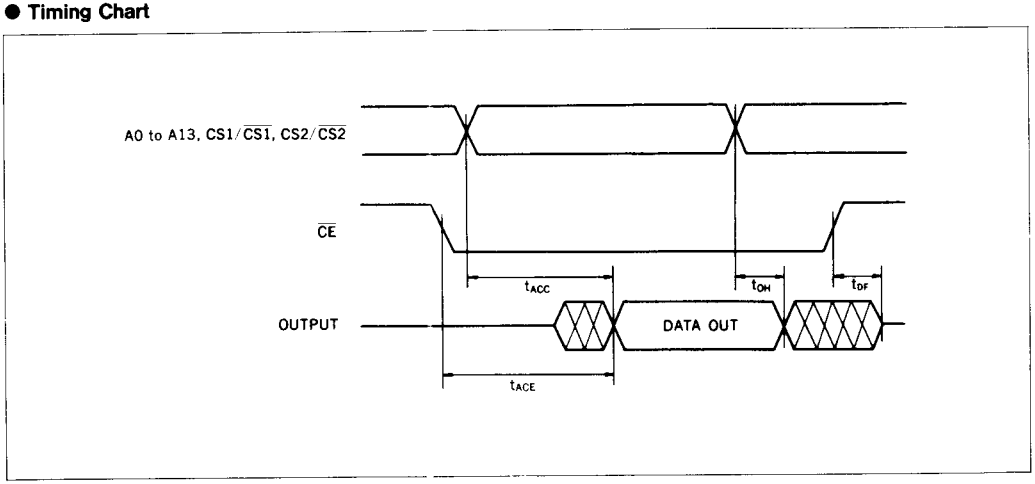
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH}		2.2	—	V_{DD}+0.3	V
Low level input voltage	V_{IL}		−0.5	—	0.8	V
Input leakage current	I_{LI}	$0 \leqq V_I \leqq V_{DD}$	−2.0	—	2.0	μA
Standby supply current	I_{DDS}	$\overline{CE}=V_{DD}-0.2V$	—	0.1	40	μA
Operating supply current	I_{DDO}	with output open	—	16	30	mA
Output leakage current	I_{LO}	$0 \leqq V_O \leqq V_{DD}$	−10.0	—	10.0	μA
High level output voltage	V_{OH}	$I_{OH}=-1.0mA$	2.4	—	—	V
Low level output voltage	V_{OL}	$I_{OL}=3.2mA$	—	—	0.4	V
Input capacitance	C_I	f=1MHz	—	—	10	pF
Output capacitance	C_O	f=1MHz	—	—	15	pF

● AC Characteristics

(V_{DD}=+5V±10%, V_{SS}=0V, Ta=−10 to +70℃)

Parameter	Symbol	Conditions	Min	Max	Unit
Read cycle time	t_{RC}	C_L=1TTL+100pF	250	—	ns
Address access time	t_{ACC}	V_{IH}=2.2V	—	250	ns
$\overline{CE}$ access time	t_{ACE}	V_{IL}=0.8V	—	250	ns
Output floating	t_{DF}	V_{OH}=1.5V	—	80	ns
Output hold time	t_{OH}	V_{OL}=1.5V tr=tf=10ns	0	—	ns

● Timing Chart



■ FUNCTIONS

● Truth Table

$\overline{CE}$	CS1/$\overline{CS1}$, CS2/$\overline{CS2}$, A0 to A13	O0 to O7	MODE
H	X	Hi-Z	Standby
L	Stable	Output data	Read

X : "H" or "L"

● Read mode

Data can be read by simply setting an address with $\overline{CE}$ held at "L", CS1/$\overline{CS1}$, CS2/$\overline{CS2}$ at each active level. At the time of power-on the initial state cannot be determined because of the operation of the internal clock circuit. If the power is on in the mode of holding $\overline{CE}$ "L" and a certain address is fixed, the data related to the address may not appear. Data should be read after the supply voltage becomes stable, and $\overline{CE}$ is set at "H" or the address input is changed in the mode of $\overline{CE}$ "L".

● Standby mode

Setting $\overline{CE}$ at "H" initiates the standby mode In this mode, the output impedance goes high and all address input is disabled.

● Specifying CS1/$\overline{CS1}$, CS2/$\overline{CS2}$

CS1/$\overline{CS1}$, CS2/$\overline{CS2}$ is mask programmable and may be selected for either active level. When ordering, specify the active level.

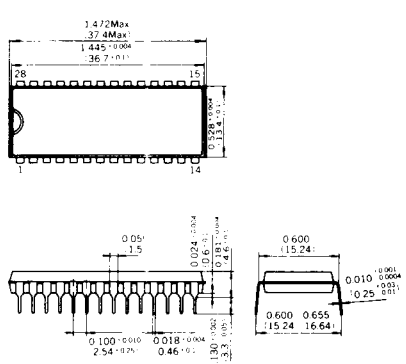
[NOTE] RECOMMENDATIONS

1. The SMM6312C is a mask programmable ROM on a CMOS chip. In the data read mode, transient current will flow in the chip at the time of transistor transition. For protection of such transients, it is recommended to connect a high-frequency capacitor and an electrolytic capacitor between the power supplies V_{DD} and V_{SS}.
2. The input and output of SMM6312C are TTL compatible. It is recommended that, when the chip is connected to TTL, pull up resistors be connected to the $\overline{CE}$, CS1/$\overline{CS1}$, CS2/$\overline{CS2}$ and address input terminal.

■ PACKAGE DIMENSIONS

C28

28-pin DIP



unit : inch
(mm)

■ CHARACTERISTICS CURVES