Chapter 12: Specifications

This chapter presents the following information for the LR3000 and LR3000A processors:

- LR3000 Electrical Specifications
- LR3000A Electrical Specifications
- Timing Diagrams
- Mechanical, Pinout, and Mounting Information
- Ordering Information

Note: All LR3000A specifications are preliminary and subject to change.

Note: Notations used in the timing diagrams are defined in the section entitled "Notations" in the preface.

12.1 LR3000 Electrical Specifications

DC Electrical Characteristics

Maximum Ratings

Operation beyond the limits set forth in this table may impair the useful life of the device. **Note:** Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

Parameter	Symbol	Test Conditions	Min	Max	Units
Supply Voltage	VCC		-0.5	+7.0	V
Input Voltage	VIN		-0.5[1]	+7.0	V
Storage Temperature	TST		-65	+150	°C
Operating Temperature	TA		0	+70	°C

Note:
(1) VIN Min. = -3.0 V for pulse width less than 15 ns.

Operating Range

Range	Ambient Temperature	VCC
Commercial	0 °C to 70 °C	5V ±5%

Operating Parameters

Parameter	Symbol	Test Conditions	16.67MHz		20 MHz		25 MHz		Units
			Min	Max	Min	Max	Min	Max	
Output High Voltage	VOH	VCC = Min IOH = -4 mA	3.5		3.5		3.5		V
Output High Voltage[1]	VOHC	VCC = Min IOH = -4 mA	4.0		4.0		4.0		V
Output Low Voltage	VOL	VCC = Min IOL = 4 mA		0.4		0.4		0.4	V
Output High Voltage[2]	VOHT	VCC = Min IOH = -8 mA	2.4		2.4		2.4		V
Output Low Voltage[2]	VOLT	VCC = Min IOL = 8 mA		0.8		0.8		0.8	V
Input High Voltage[3]	VIH		2.0		2.0		2.0		V
Input Low Voltage[4]	VIL			0.8		0.8		0.8	V
Input High Voltage[3,5]	VIHS		2.5		2.5		2.5		V
Input Low Voltage[5]	VILS			0.4		0.4		0.4	V
Input Capacitance	CIn			10		10		10	pF
Output Capacitance	COut			10		10		10	pF
Operating Current	ICC	VCC = 5.5 V		600		700		800	mA
Load Capacitance[6]	CLd			50		50		50	pF
Input High Leakage	IIH	VIH = VCC		10		10		10	µA
Input Low Leakage	IIL	VIL = Gnd	-10		-10		-10		µA
3-state Output Leakage	IOZ	VOH = 2.4 V VOL = 0.4 V	-10	10	-10	10	-10	10	µA

Note:
(1) VOHC applies to $\overline{\text{Run}}$ and $\overline{\text{Exception}}$.
(2) VOHT and VOLT apply to the bidirectional data and tag buses only. VOH and VOL also apply to these buses.
(3) Input high voltages should not be held above VCC + 0.5 volts.
(4) VIL min. = -3.0 V for pulse width less than 15 ns. VIL should not fall below -0.5 V for longer periods.
(5) VIHS and VILS apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, CpBusy, and $\overline{\text{Reset}}$.
(6) Operation above the CLd max. may impair the useful life of the device.

AC Electrical Characteristics

Tables 12.1 through 12.4 list the AC electrical specifications for the LR3000. All timings are referenced to 1.5V. All output timings assume 25pF of capacitive load. Output timings should be derated where appropriate using the values provided in Table 12.5.

Parameter	Symbol	Test Conditions	16.67MHz		20 MHz		25 MHz		Units
			Min	Max	Min	Max	Min	Max	
Input Clock High	t_{CkHigh}	Transition ≤ 5ns	12		10		8		ns
Input Clock Low	t_{CkLow}	Transition ≤ 5ns	12		10		8		ns
Input Clock Period	t_{CkP}		30	1000	25	1000	20	1000	ns
Clk2xSys to Clk2xSmp			0	$t_{Cyc}/4$	0	$t_{Cyc}/4$	0	$t_{Cyc}/4$	ns
Clk2xSmp to Clk2xRd			0	$t_{Cyc}/4$	0	$t_{Cyc}/4$	0	$t_{Cyc}/4$	ns
Clk2xSmp to Clk2xPhi			9	$t_{Cyc}/4$	7	$t_{Cyc}/4$	5	$t_{Cyc}/4$	ns

The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
t_{Cyc} is the clock cycle time.

Table 12.1 LR3000 Clock Parameters

Parameter	Symbol	Load (pF)	16.67 MHz		20 MHz		25 MHz		Units	Offset from $\overline{SysOut}$
			Min	Max	Min	Max	Min	Max		
Data/Tag Valid	t_{DVal}	25		3		3		2	ns	t_{Sys}
Data/Tag Enable	t_{DEn} [1]			-2		-2		-1.5	ns	t_{Sys}
Data/Tag Disable	t_{DDis} [1]			-1		-1		-0.5	ns	$t_{Rd} - t_{Sys}$
Write Delay	t_{WrDly}	25		5		4		3	ns	$t_{Smp} - t_{Sys}$
Data Setup	t_{DS}		9		8		6		ns	$t_{Smp} - t_{Sys}$
Data Hold	t_{DH}		-2.5		-2.5		-2.5		ns	$t_{Smp} - t_{Sys}$
CpBusy Setup	t_{CBS}		13		11		9		ns	$t_{Smp} - t_{Sys}$
CpBusy Hold	t_{CBH}		-2.5		-2.5		-2.5		ns	$t_{Smp} - t_{Sys}$
Access Type(1:0)	t_{AcTy}	25		7		7		7	ns	t_{Sys}
Access Type(2)	t_{AcTy2}	25		17		14		12	ns	t_{Sys}
Memory Write	t_{MWr}	25		27		23		18	ns	t_{Sys}
Exception	t_{Exc}	25		7		7		5	ns	t_{Sys}
Interrupt Setup	t_{IntS}		9		8		6		ns	$t_{Smp} - t_{Sys}$
Interrupt Hold	t_{IntH}		-2.5		-2.5		-2.5		ns	$t_{Smp} - t_{Sys}$

(1) Parameter guaranteed by design.

Table 12.2 LR3000 Run Operation Parameters

Parameter	Symbol	Load (pF)	16.67 MHz		20 MHz		25 MHz		Units	Offset from $\overline{SysOut}$
			Min	Max	Min	Max	Min	Max		
Address Valid	t_{SAVal}	25		30		23		20	ns	t_{Sys}
Access Type	t_{SAcTy}	25		27		23		18	ns	t_{Sys}
Memory Read Initiate	t_{MRdI}	25		27		23		18	ns	t_{Sys}
Memory Read Terminate	t_{MRdT}	25		7		7		5	ns	t_{Sys}
Run Terminate	t_{StI}	25		17		15		11	ns	t_{Sys}
Run Initiate	t_{Run}	25		7		6		4	ns	t_{Sys}
Memory Write	t_{SMwr}	25		27		23		18	ns	t_{Sys}
Exception Valid	t_{SExc}	25		20		18		15	ns	t_{Sys}

Table 12.3 LR3000 Stall Operation Parameters

Parameter	Symbol	16.67 MHz		20 MHz		25 MHz		Units
		Min	Max	Min	Max	Min	Max	
Reset Pulse Width	t_{rst}	6		6		6		TCkP
Reset Timing, Phase Lock on	t_{rstpll}[1]	3000		3000		3000		TCkP
Reset Timing, Phase Lock off	t_{rstcp}[2]	128		128		128		TCkP

(1) System configuration includes Floating-Point Unit with PLL enabled.
(2) System configuration includes Floating-Point Unit with PLL disabled.

Table 12.4 LR3000 Reset Operation

Parameter	Symbol	16.67 MHz		20 MHz		25 MHz		Units
		Min	Max	Min	Max	Min	Max	
Load Derate	CLd	0.5	2	0.5	1	0.5	1	ns/25pF

Table 12.5 LR3000 Capacitive Load Derating

12.2 LR3000A Electrical Specifications

Note: All specifications are preliminary and subject to change.

DC Electrical Characteristics

Maximum Ratings

Operation beyond the limits set forth in this table may impair the useful life of the device. **Note:** Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

Parameter	Symbol	Test Conditions	Min	Max	Units
Supply Voltage	VCC		-0.5	+7.0	V
Input Voltage	VIN		-0.5[1]	+7.0	V
Storage Temperature	TST		-65	+150	°C
Operating Temperature	TA		0	+70	°C

Note:
(1) VIN Min. = -3.0 V for pulse width less than 15 ns.

Operating Range

Range	Ambient Temperature	VCC
Commercial	0 °C to 70 °C	5V ±5%

Operating Parameters

Parameter	Symbol	Test Conditions	25 MHz		33.33 MHz		Units
			Min	Max	Min	Max	
Output High Voltage	VOH	VCC = Min IOH = -4 mA	3.5		3.5		V
Output High Voltage[1]	VOHC	VCC = Min IOH = -4 mA	4.0		4.0		V
Output Low Voltage	VOL	VCC = Min IOL = 4 mA		0.4		0.4	V
Output High Voltage[2]	VOHT	VCC = Min IOH = -8 mA	2.4		2.4		V
Output Low Voltage[2]	VOLT	VCC = Min IOL = 8 mA		0.8		0.8	V
Input High Voltage[3] Input Low Voltage[4]	VIH VIL		2.0	 0.8	2.0	 0.8	V V
Input High Voltage[3,5] Input Low Voltage[5]	VIHS VILS		2.5	 0.4	3.0	 0.4	V V
Input Capacitance Output Capacitance	CIn COut			10 10		10 10	pF pF
Operating Current	ICC	VCC = 5.5 V		600		800	mA
Load Capacitance[6]	CLd			50		50	pF
Input High Leakage Input Low Leakage	IIH IIL	VIH = VCC VIL = Gnd	 -10	10	 -10	10	µA µA
3-state Output Leakage	IOZ	VOH = 2.4 V VOL = 0.4 V	-10	10	-10	10	µA

Note:
(1) VOHC applies to $\overline{\text{Run}}$ and $\overline{\text{Exception}}$.
(2) VOHT and VOLT apply to the bidirectional data and tag buses only. VOH and VOL also apply to these buses.
(3) Input high voltages should not be held above VCC + 0.5 volts.
(4) VIL min. = -3.0 V for pulse width less than 15 ns. VIL should not fall below -0.5 V for longer periods.
(5) VIHS and VILS apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, CpBusy, and $\overline{\text{Reset}}$.
(6) Operation above the CLd max. may impair the useful life of the device.

AC Electrical Characteristics

Tables 12.6 through 12.9 list the preliminary AC electrical specifications for the LR3000A. All timings are referenced to 1.5V. All output timings assume 25pF of capacitive load. Output timings should be derated where appropriate using the values provided in Table 12.5.

Parameter	Symbol	Test Conditions	25 MHz		33.33 MHz		Units
			Min	Max	Min	Max	
Input Clock High	t_{CkHigh}	Transition ≤ 2.5ns	8		6		ns
Input Clock Low	t_{CkLow}	Transition ≤ 2.5ns	8		6		ns
Input Clock Period	t_{CkP}		20	1000	15	1000	ns
Clk2xSys to Clk2xSmp			0	$t_{Cyc}/4$	0	$t_{Cyc}/4$	ns
Clk2xSmp to Clk2xRd			0	$t_{Cyc}/4$	0	$t_{Cyc}/4$	ns
Clk2xSmp to Clk2xPhi			5	$t_{Cyc}/4$	4.5	$t_{Cyc}/4$	ns

The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi. t_{Cyc} is the clock cycle time.

Table 12.6 LR3000A Clock Parameters

Parameter	Symbol	Load (pF)	25 MHz		33.33 MHz		Units	Offset from $\overline{SysOut}$
			Min	Max	Min	Max		
Data/Tag Valid	t_{DVal}	25		3		2.5	ns	t_{Sys}
Data/Tag Enable	t_{DEn} [1]			-1.5		-1.5	ns	t_{Sys}
Data/Tag Disable	t_{DDis} [1]		0	-0.5	0	-0.5	ns	$t_{Rd} - t_{Sys}$
Write Delay	t_{WrDly}	25	0	3	0	3	ns	$t_{Smp} - t_{Sys}$
Data Setup	t_{DS}		6.5		5		ns	$t_{Smp} - t_{Sys}$
Data Hold	t_{DH}		-2.5		-2.5		ns	$t_{Smp} - t_{Sys}$
CpBusy Setup	t_{CBS}		9		7		ns	$t_{Smp} - t_{Sys}$
CpBusy Hold	t_{CBH}		-2.5		-2.5		ns	$t_{Smp} - t_{Sys}$
Access Type(1:0)	t_{AcTy}	25		5		3.5	ns	t_{Sys}
Access Type(2)	t_{AcTy2}	25		12		8.5	ns	t_{Sys}
Memory Write	t_{MWr}	25		18		13.5	ns	t_{Sys}
Address Vaild	t_{AVal}			2		1	ns	t_{Sys}
Exception	t_{Exc}	25		5		3.5	ns	t_{Sys}
Interrupt Setup	t_{IntS}		6.5		5		ns	$t_{Smp} - t_{Sys}$
Interrupt Hold	t_{IntH}		-2.5		-2.5		ns	$t_{Smp} - t_{Sys}$

(1) Parameter guaranteed by design.

Table 12.7 LR3000A Run Operation Parameters

Parameter	Symbol	Load (pF)	25 MHz		33.33 MHz		Units	Offset from SysOut
			Min	Max	Min	Max		
Address Valid	t_{SAVal}	25		20		15	ns	t_{Sys}
Access Type	t_{SAcTy}	25		18		13.5	ns	t_{Sys}
Memory Read Initiate	t_{MRdI}	25	0	18	0	13.5	ns	t_{Sys}
Memory Read Terminate	t_{MRdT}	25	0	18	0	13.5	ns	t_{Sys}
Run Terminate	t_{Stl}	25	3	11	2	7.5	ns	t_{Sys}
Run Initiate	t_{Run}	25	0	4	0	2.5	ns	t_{Sys}
Memory Write	t_{SMwr}	25	3	18	2	13.5	ns	t_{Sys}
Exception Valid	t_{SExc}	25	3	15	2	10	ns	t_{Sys}

Table 12.8 LR3000A Stall Operation Parameters

Parameter	Symbol	25 MHz		33.33 MHz		Units
		Min	Max	Min	Max	
Reset Pulse Width	t_{rst}	6		6		TCkP
Reset Timing, Phase Lock on	t_{rstpll}[1]	3000		3000		TCkP
Reset Timing, Phase Lock off	t_{rstcp}[2]	128		128		TCkP

(1) System configuration includes Floating-Point Unit with PLL enabled.
(2) System configuration includes Floating-Point Unit with PLL disabled.

Table 12.9 LR3000A Reset Operation

Parameter	Symbol	25 MHz		33.33 MHz		Units
		Min	Max	Min	Max	
Load Derate	CLd	0.5	1	0.5	1	ns/25pF

Table 12.10 LR3000A Capacitive Load Derating

12.3 Timing Diagrams

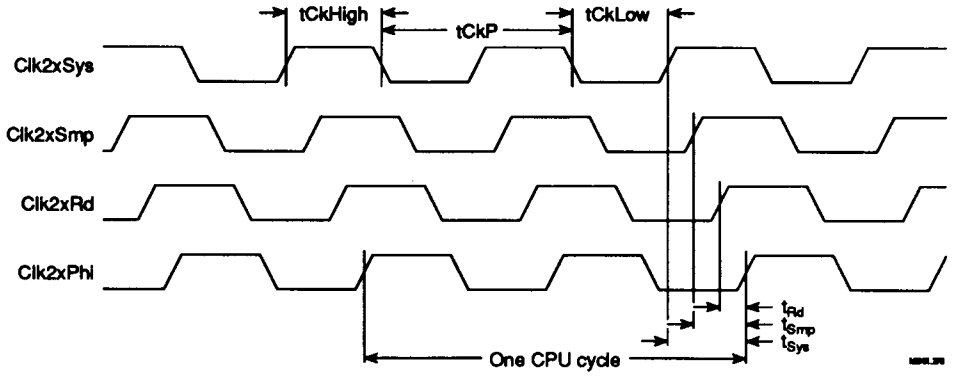


Figure 12.1 Clock Timing

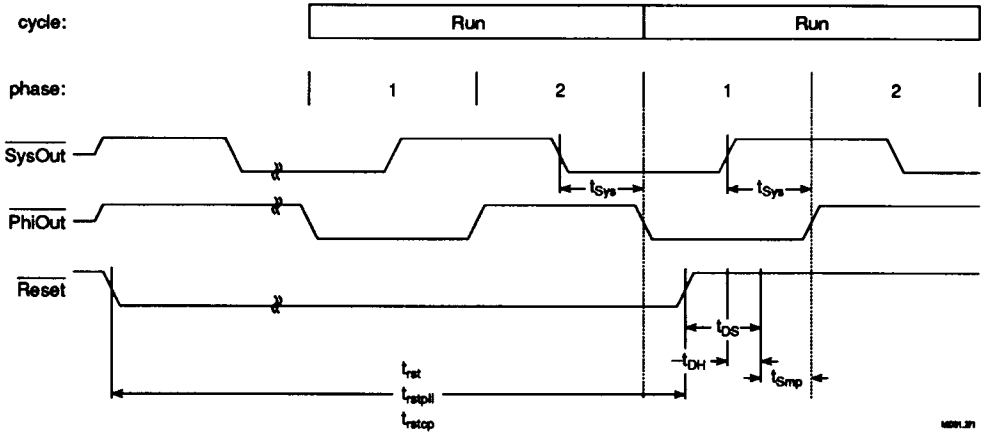


Figure 12.2 Reset Timing

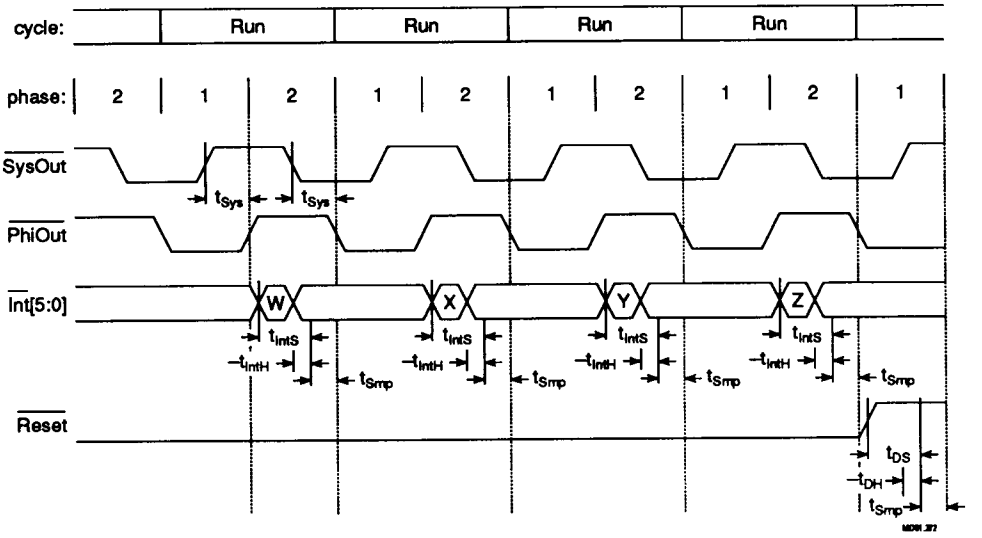


Figure 12.3 W, X, Y, and Z Mode Select Timing

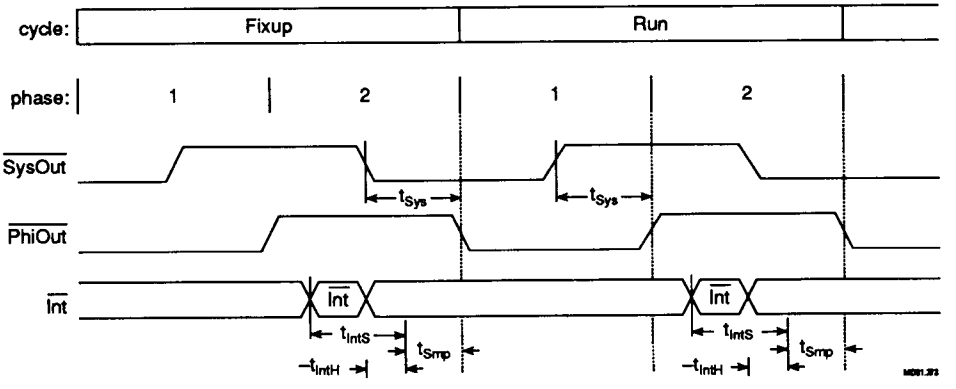


Figure 12.4 Interrupt Timing

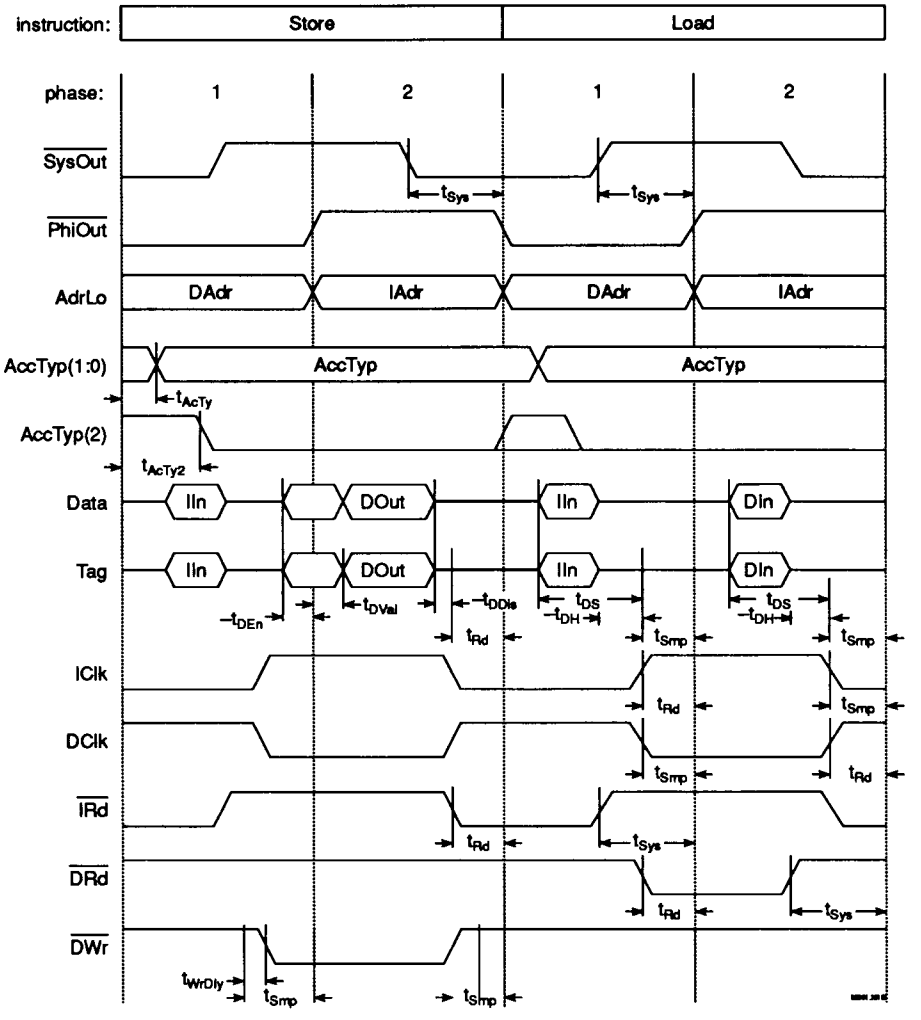


Figure 12.5 Detailed Cache Operation Timing

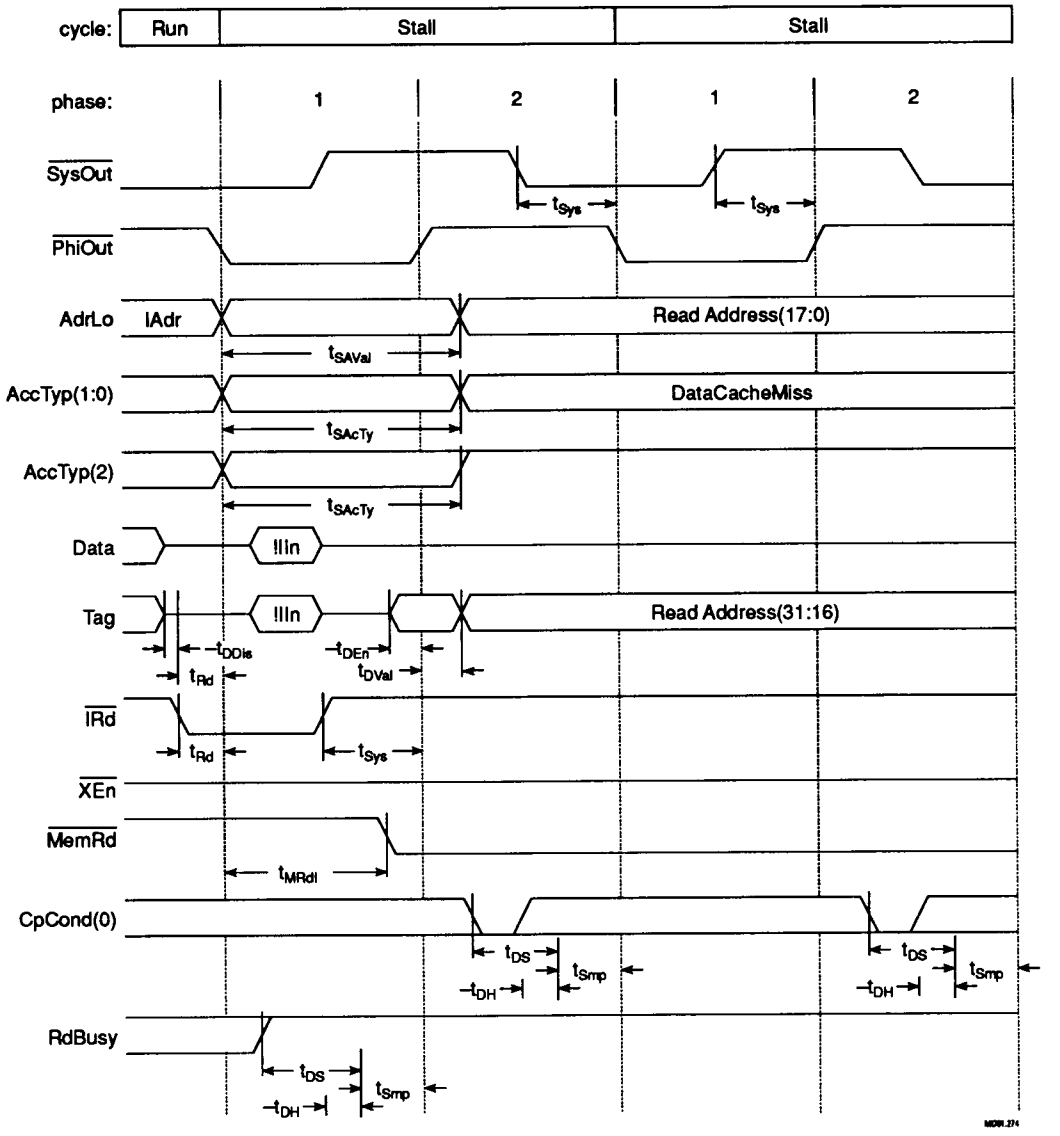


Figure 12.6 Single-Word Data Transfer—Beginning of Stall

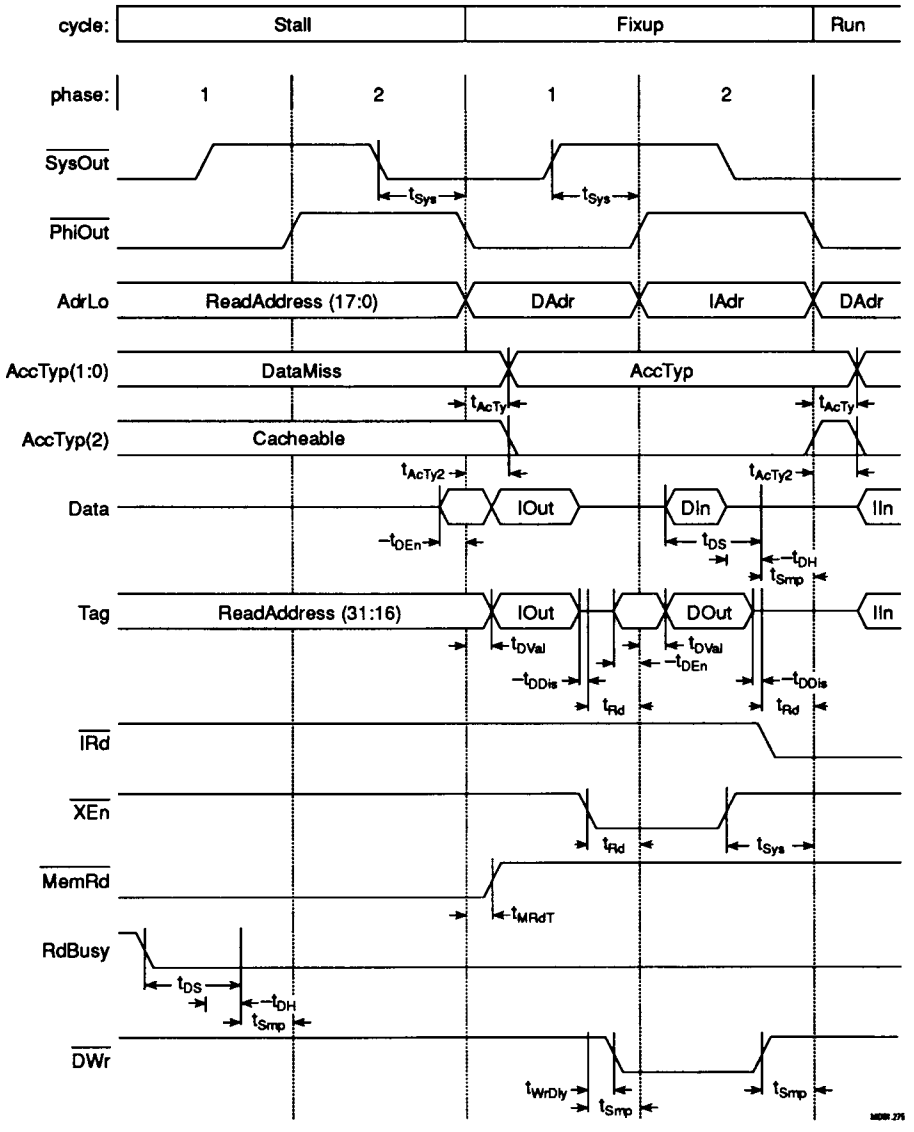


Figure 12.7 Single-Word Data Transfer—End of Stall

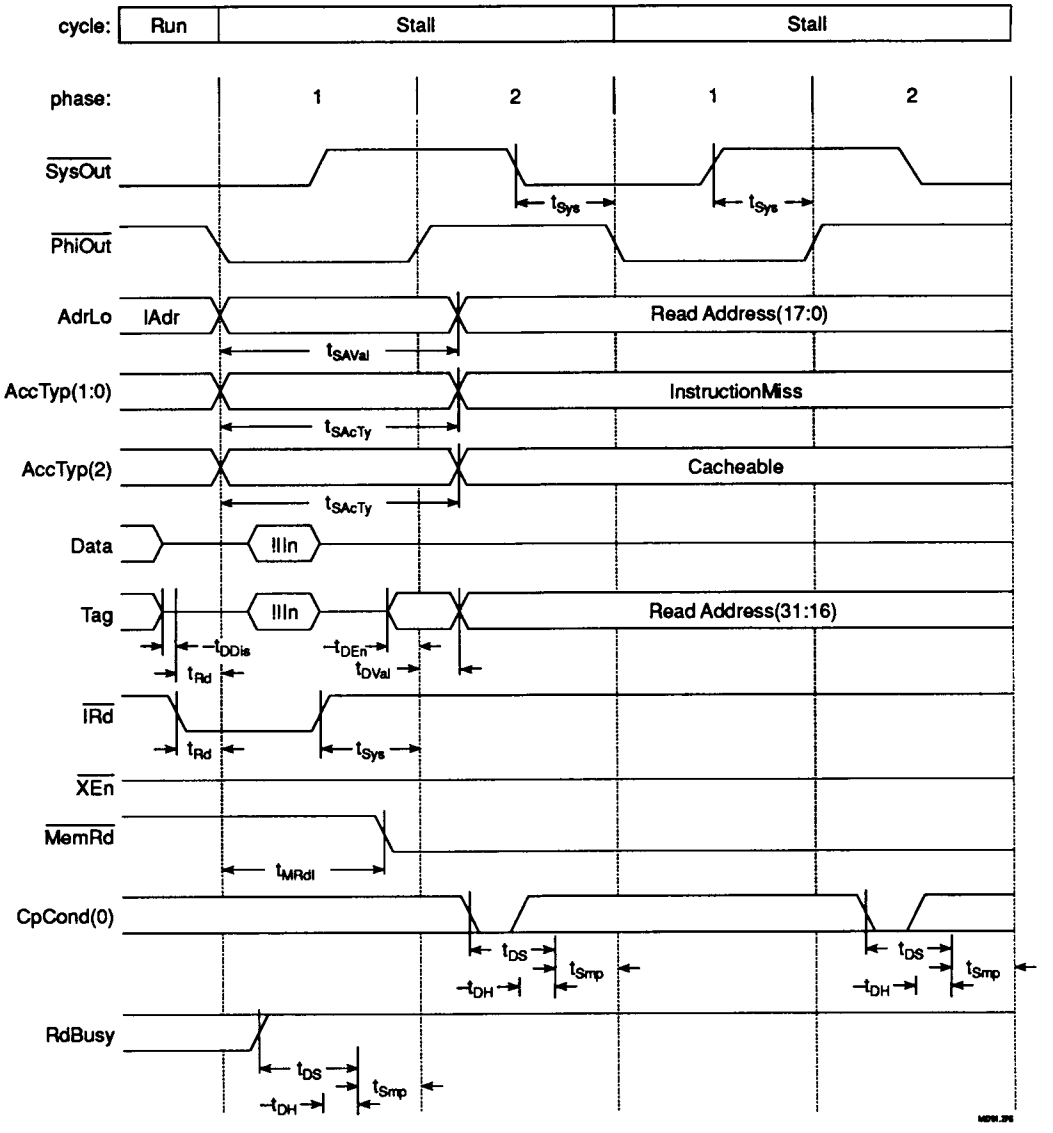


Figure 12.8 Single-Word Instruction Transfer—Beginning of Stall

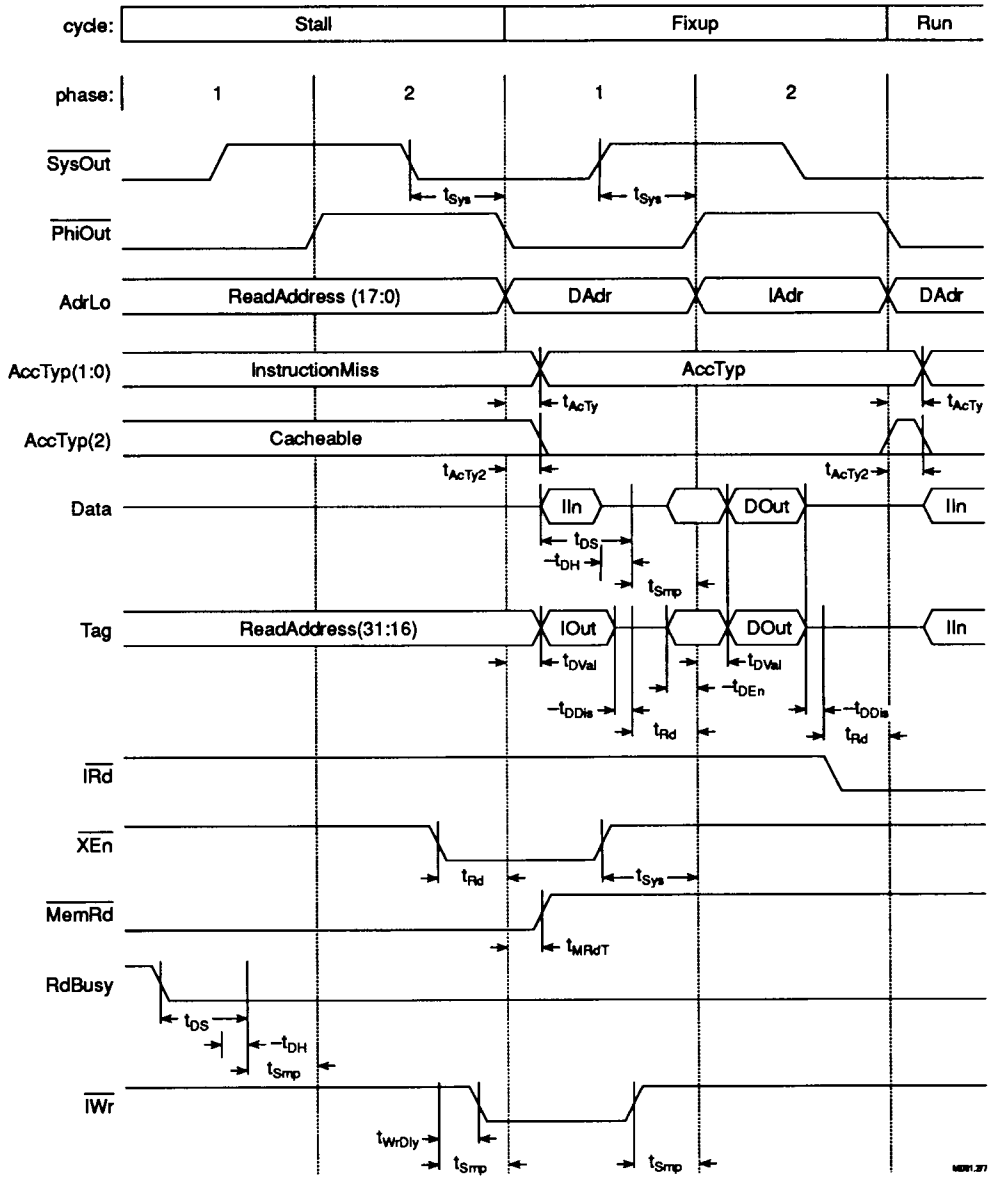


Figure 12.9 Single-Word Instruction Transfer—End of Stall

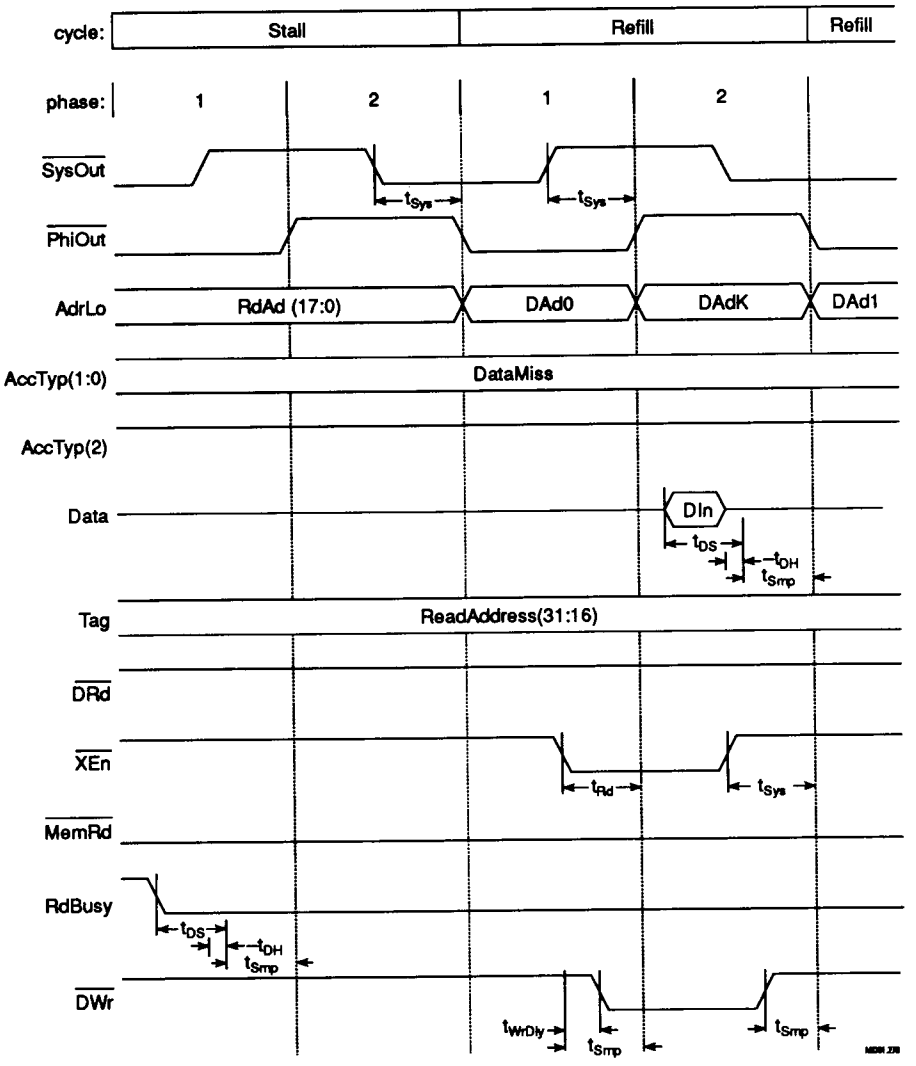


Figure 12.10 Data Block Transfer, Stall-Refill

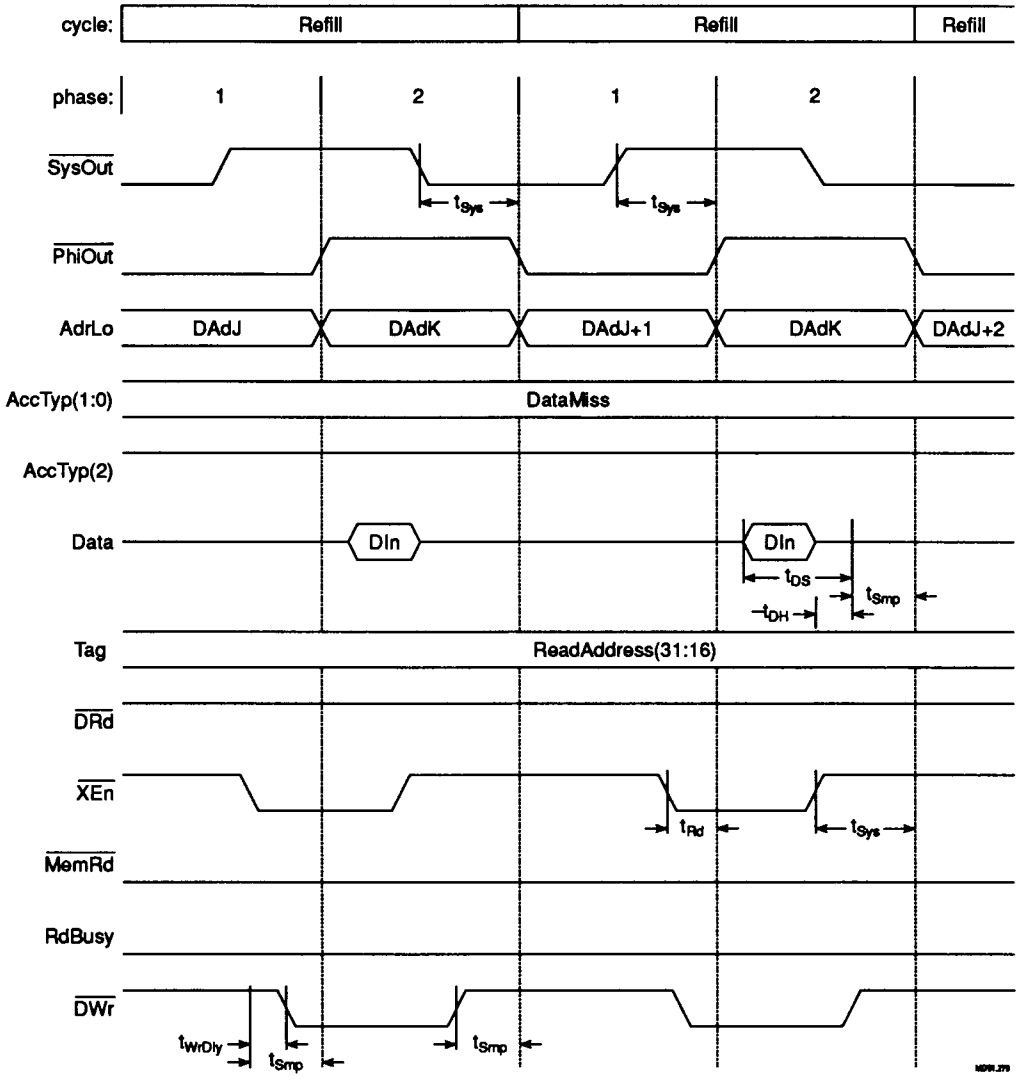


Figure 12.11 Data Block Transfer, Refill-Refill

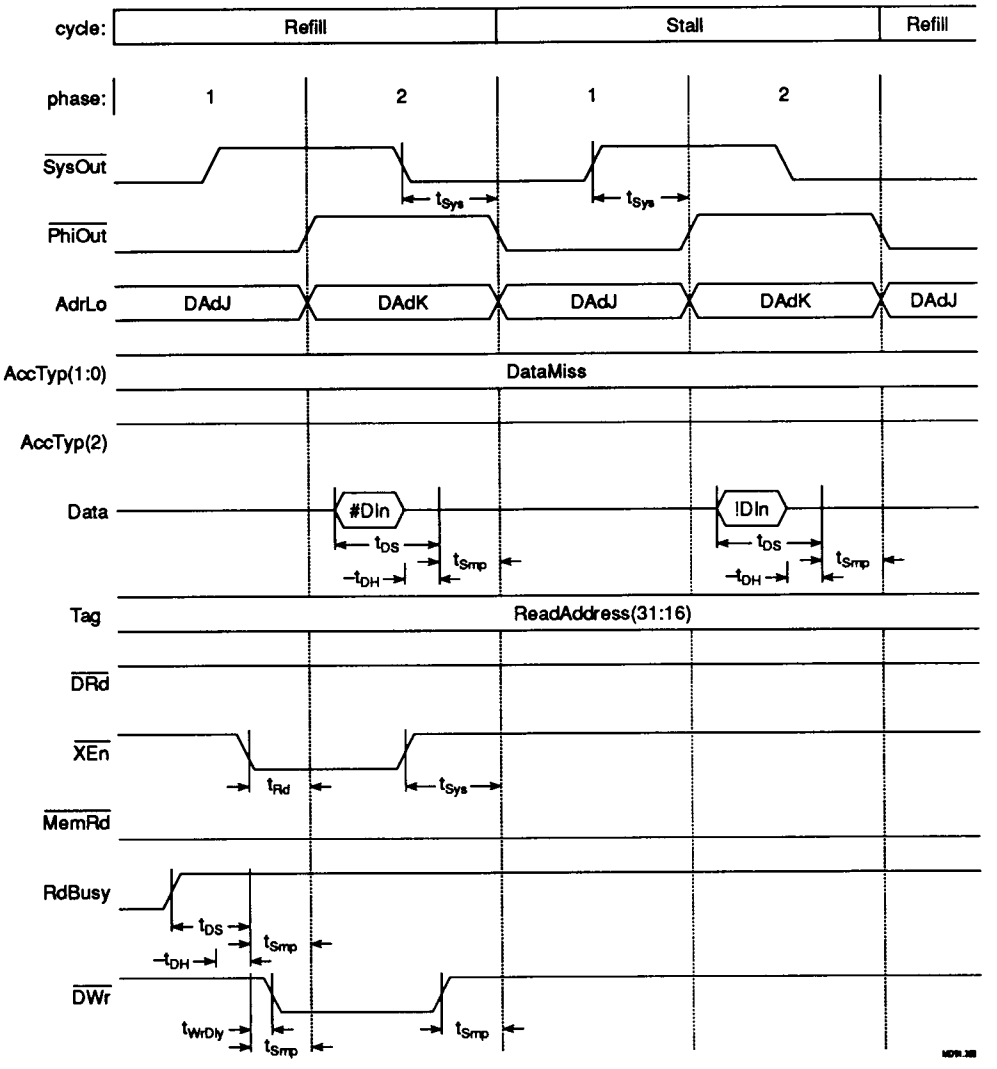


Figure 12.12 Data Block Transfer, Refill-Stall

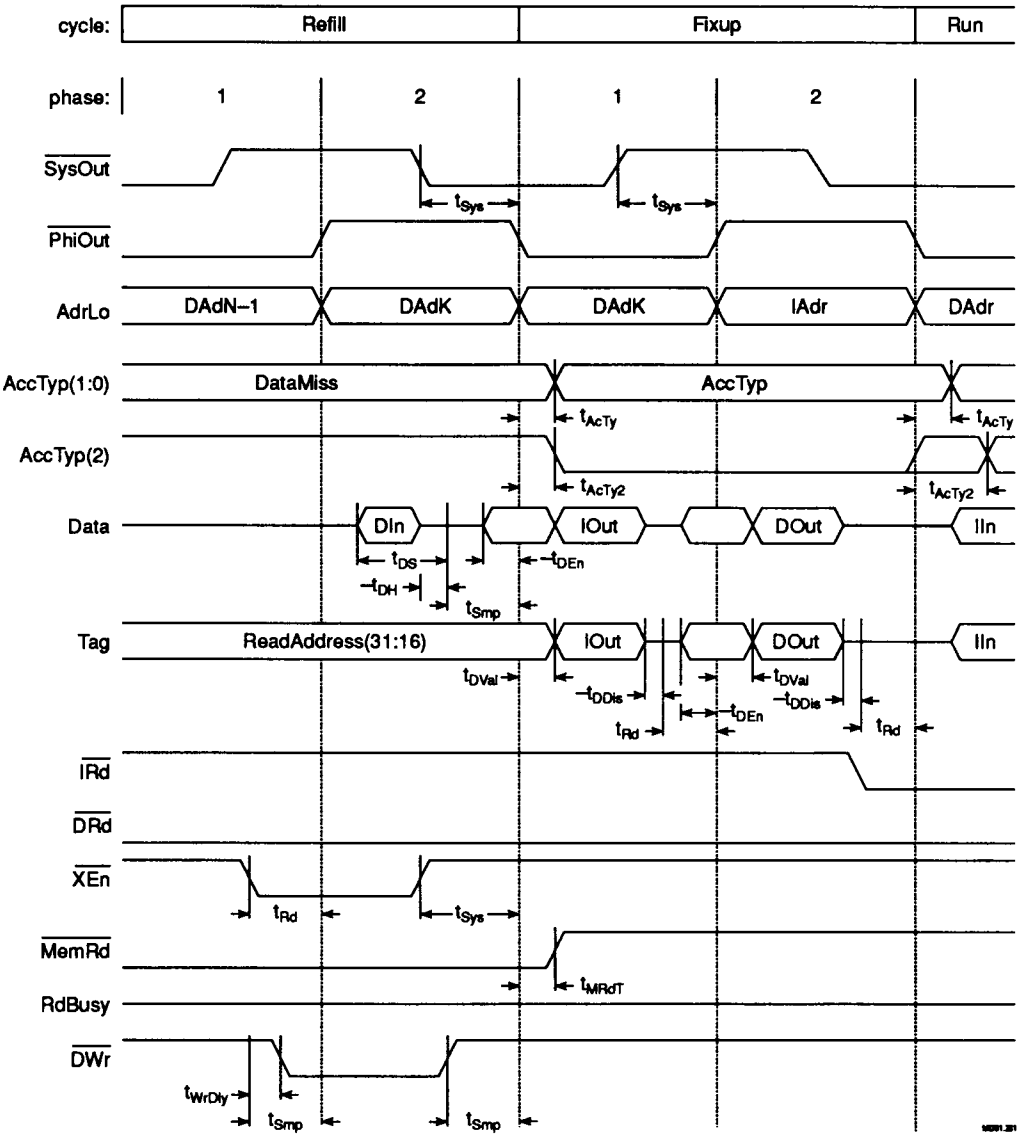


Figure 12.13 Data Block Transfer, Refill-Fixup

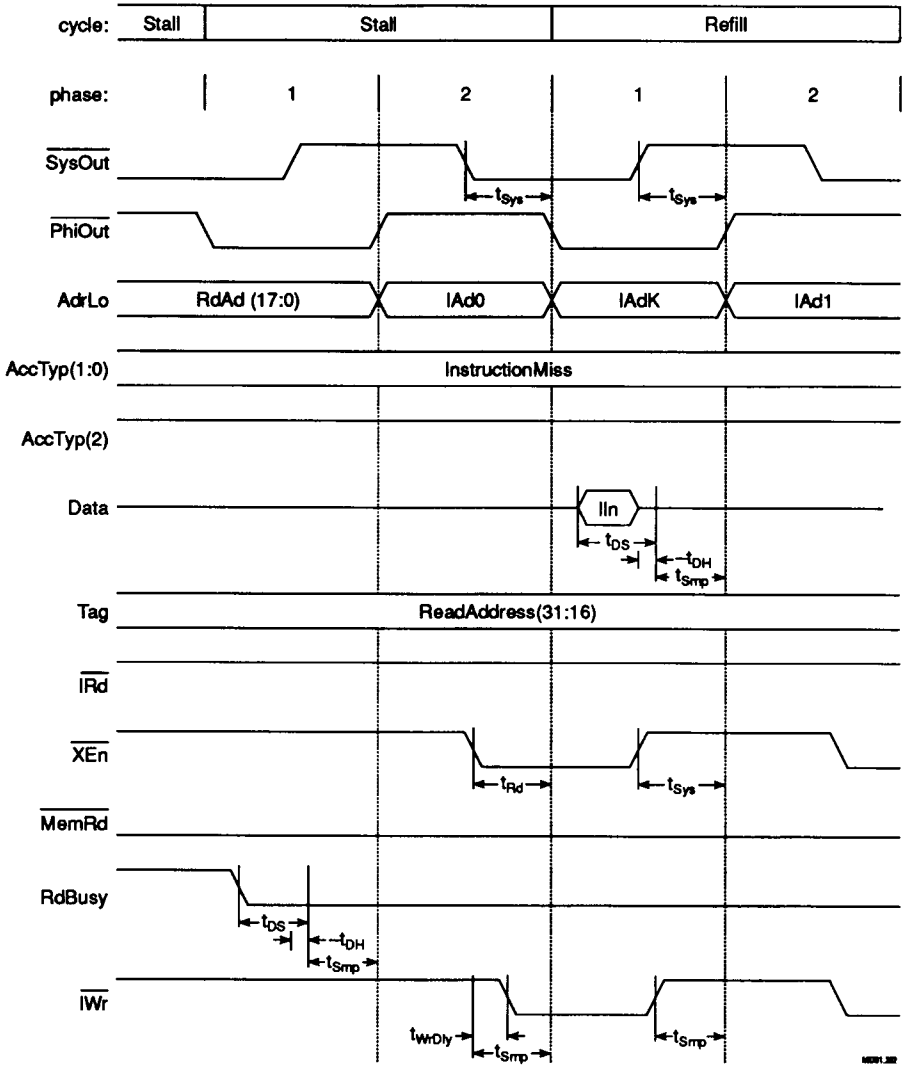


Figure 12.14 Instruction Block Transfer, Stall-Refill

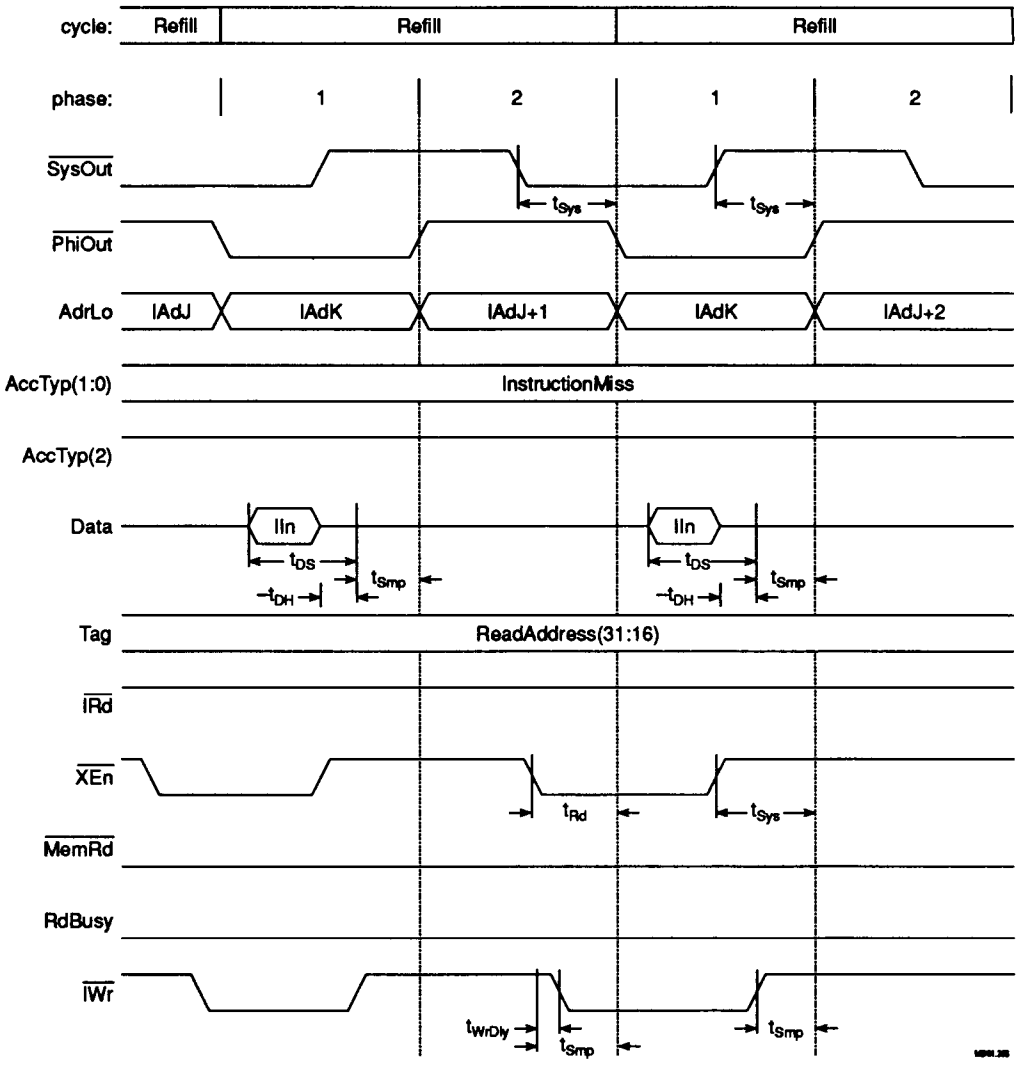


Figure 12.15 Instruction Block Transfer, Refill-Refill

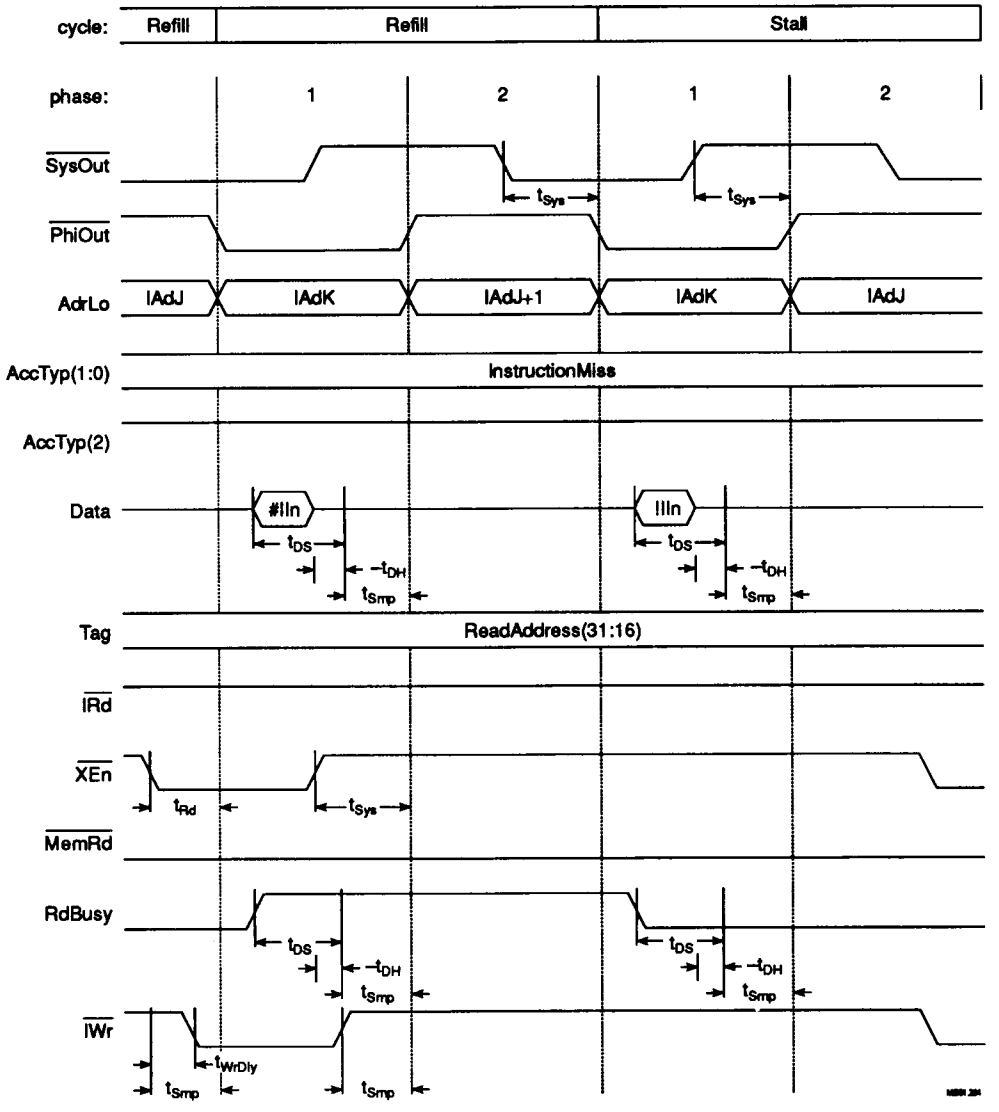


Figure 12.16 Instruction Block Transfer, Refill-Stall

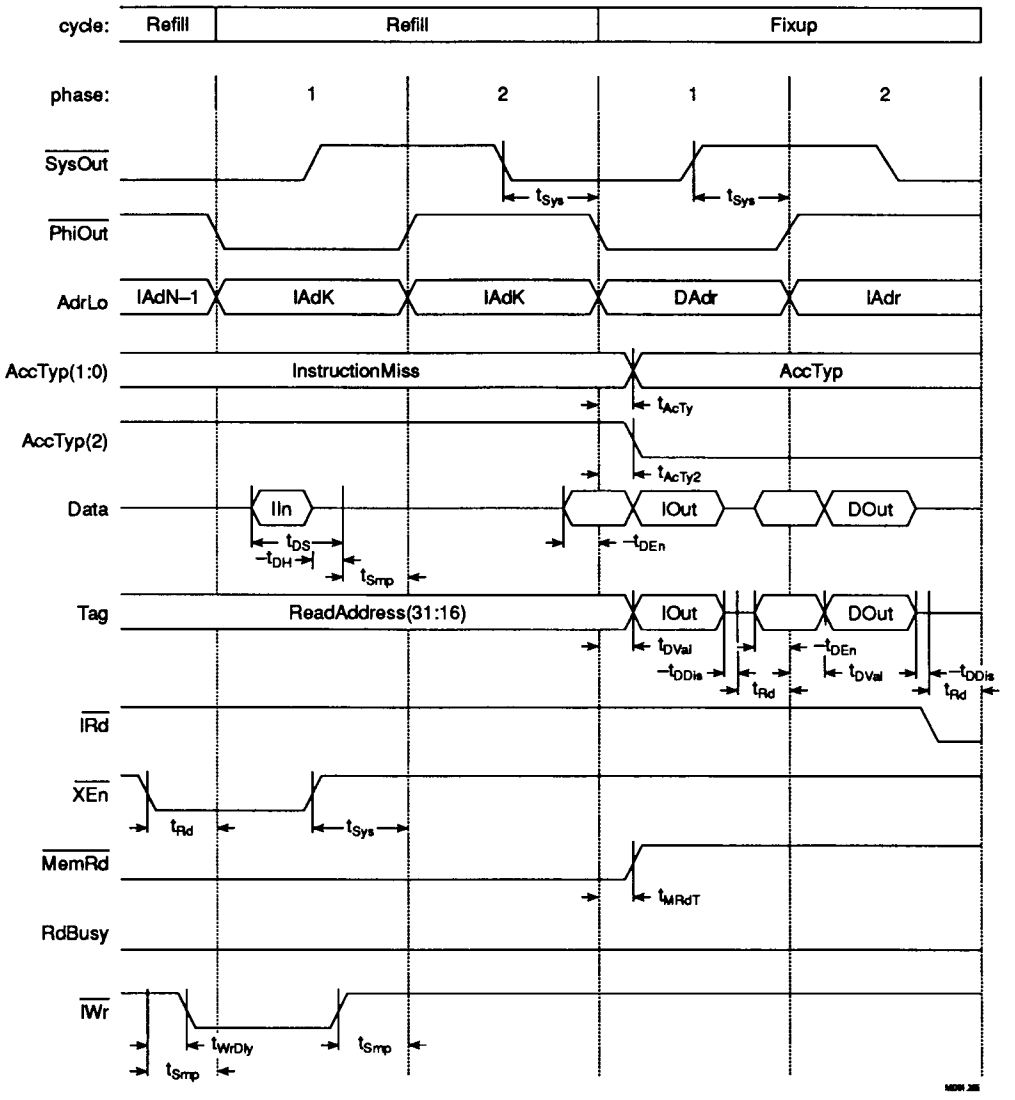


Figure 12.17 Instruction Block Transfer, Refill-Fixup

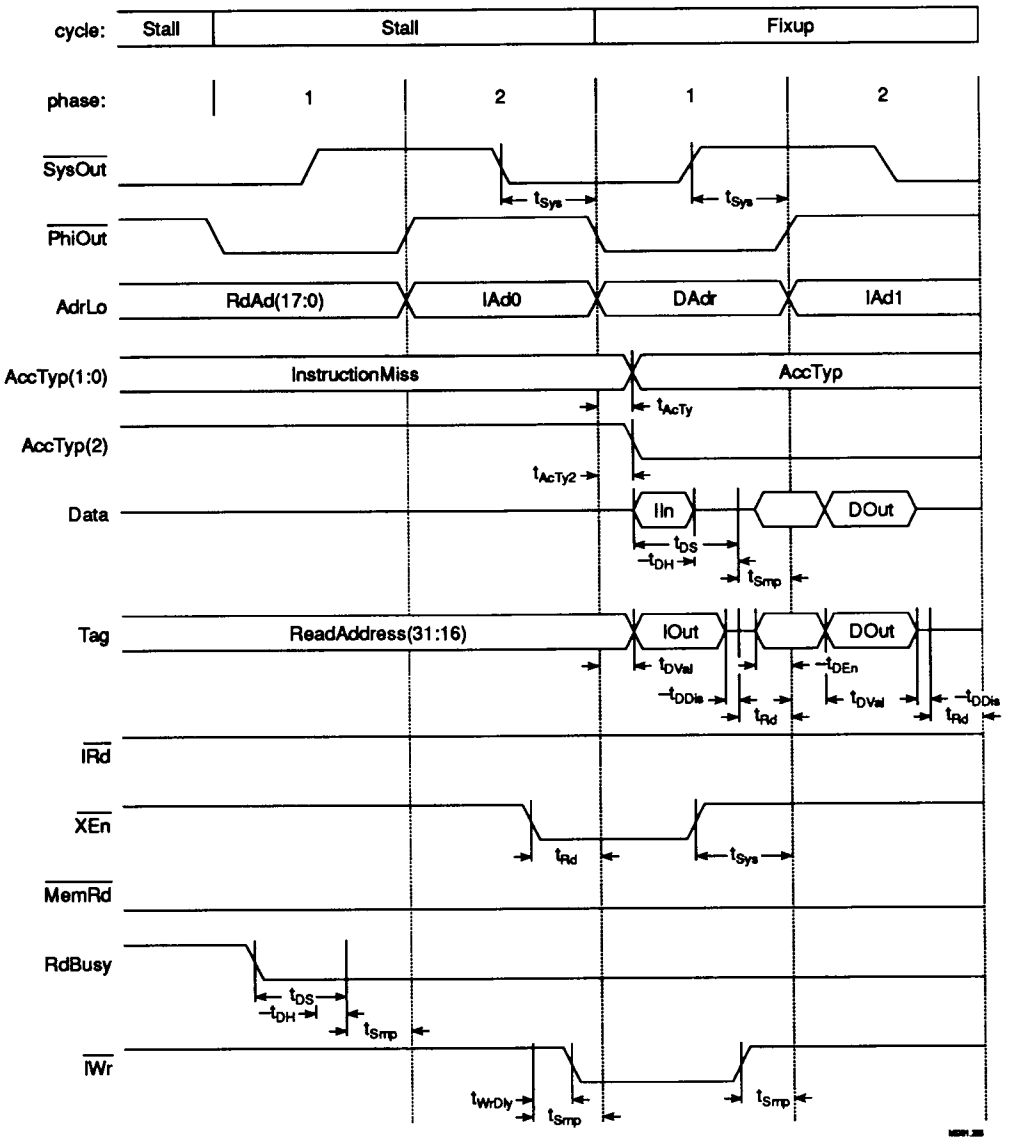


Figure 12.18 Instruction Stream, Stall-Fixup

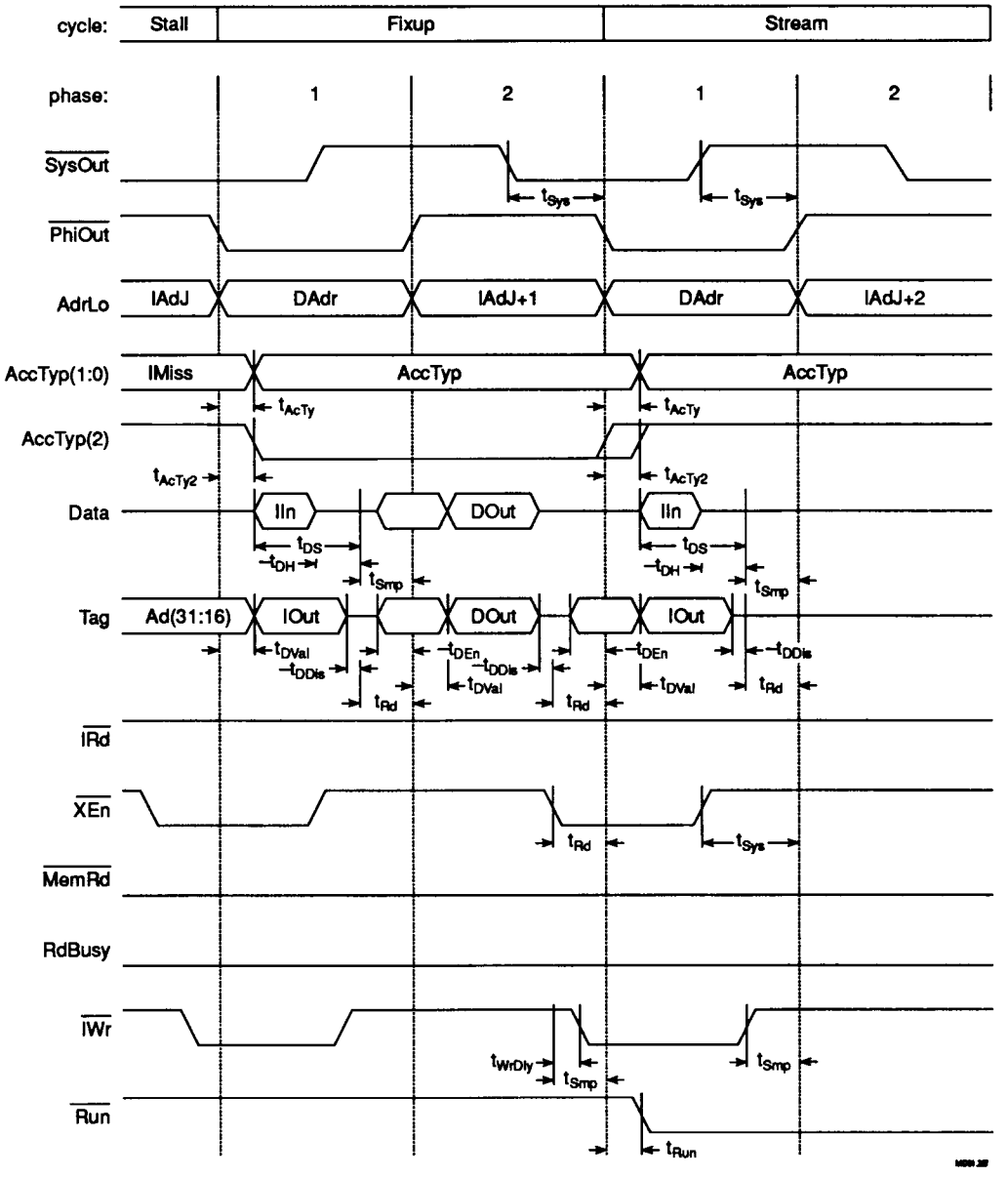


Figure 12.19 Instruction Stream, Fixup-Stream

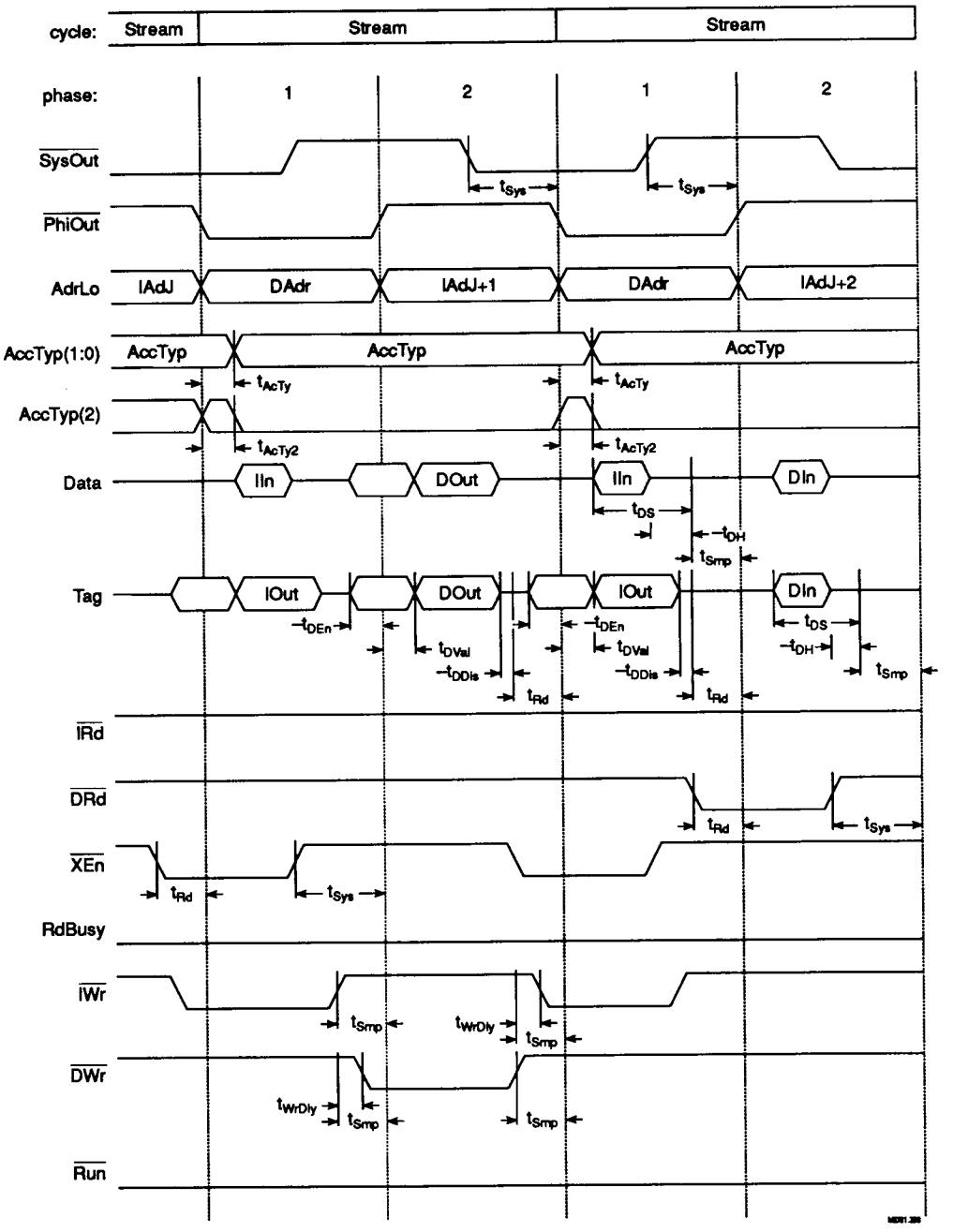


Figure 12.20 Instruction Stream, Stream-Stream

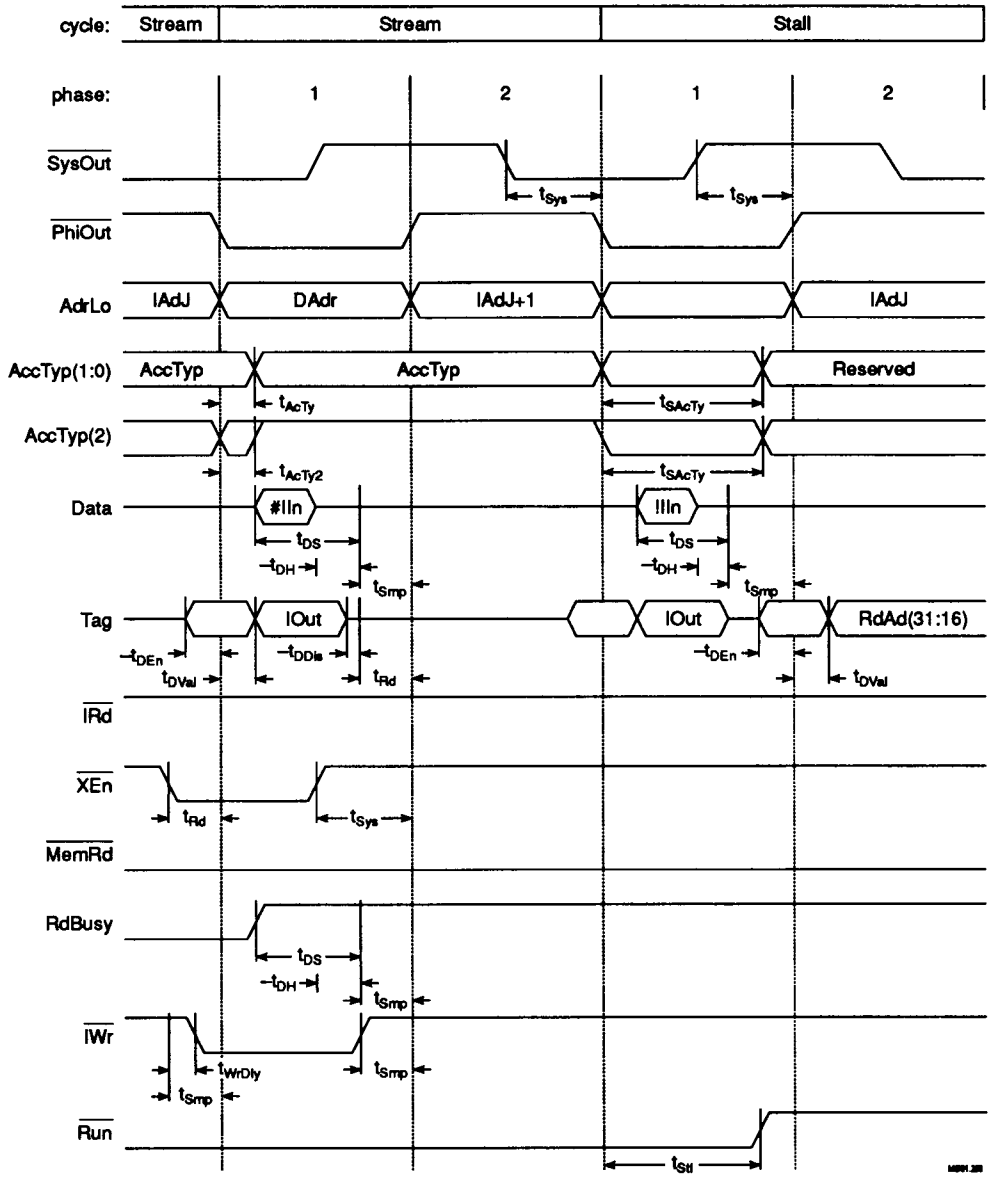


Figure 12.21 Instruction Stream, Stream-Stall

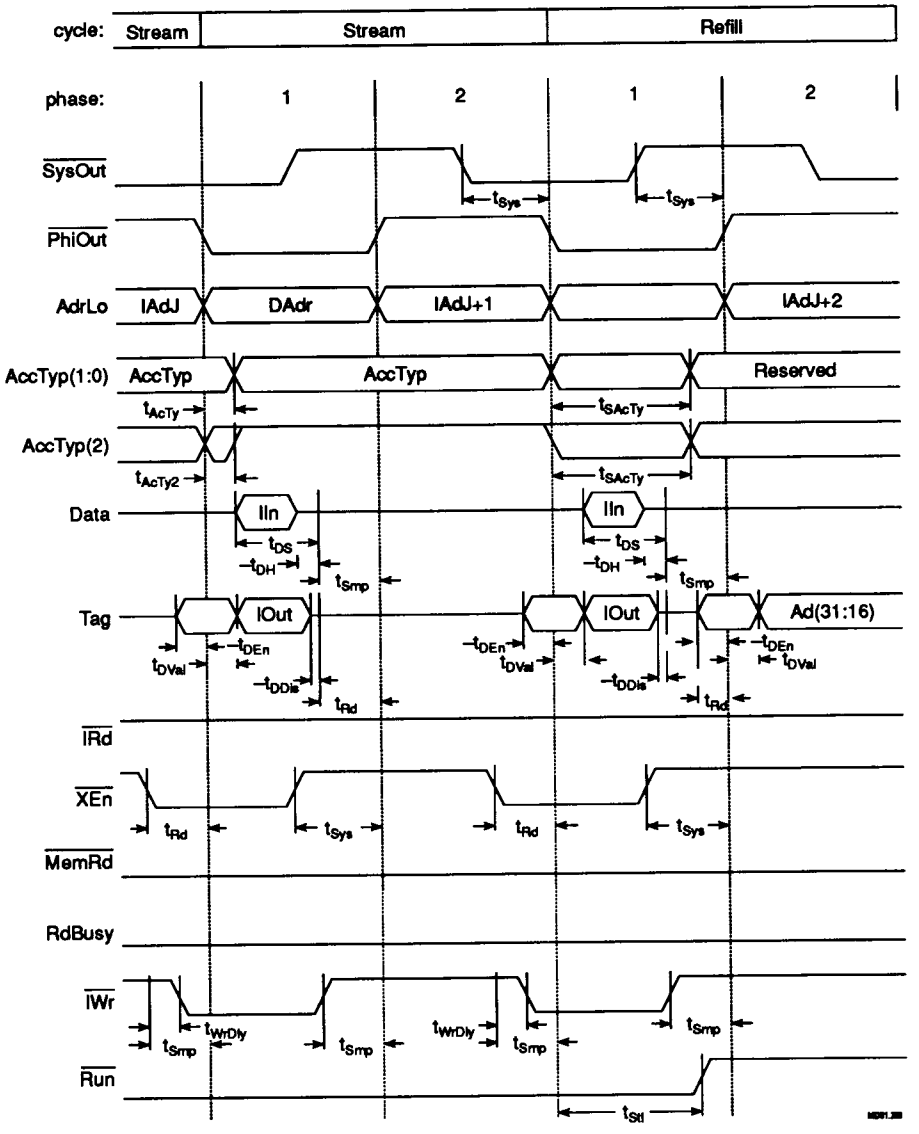


Figure 12.22 Instruction Stream, Stream-Refill

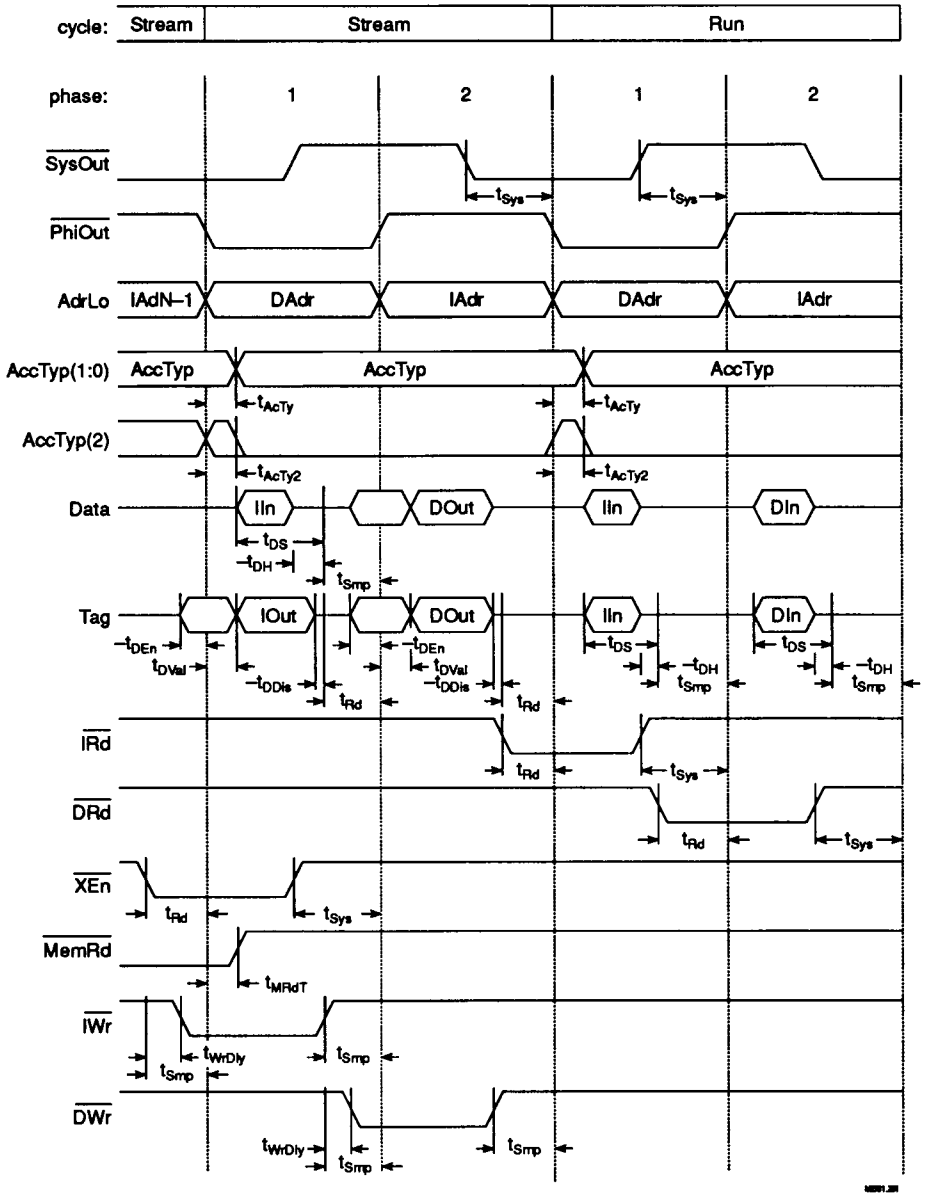


Figure 12.23 Instruction Stream, Stream-Run

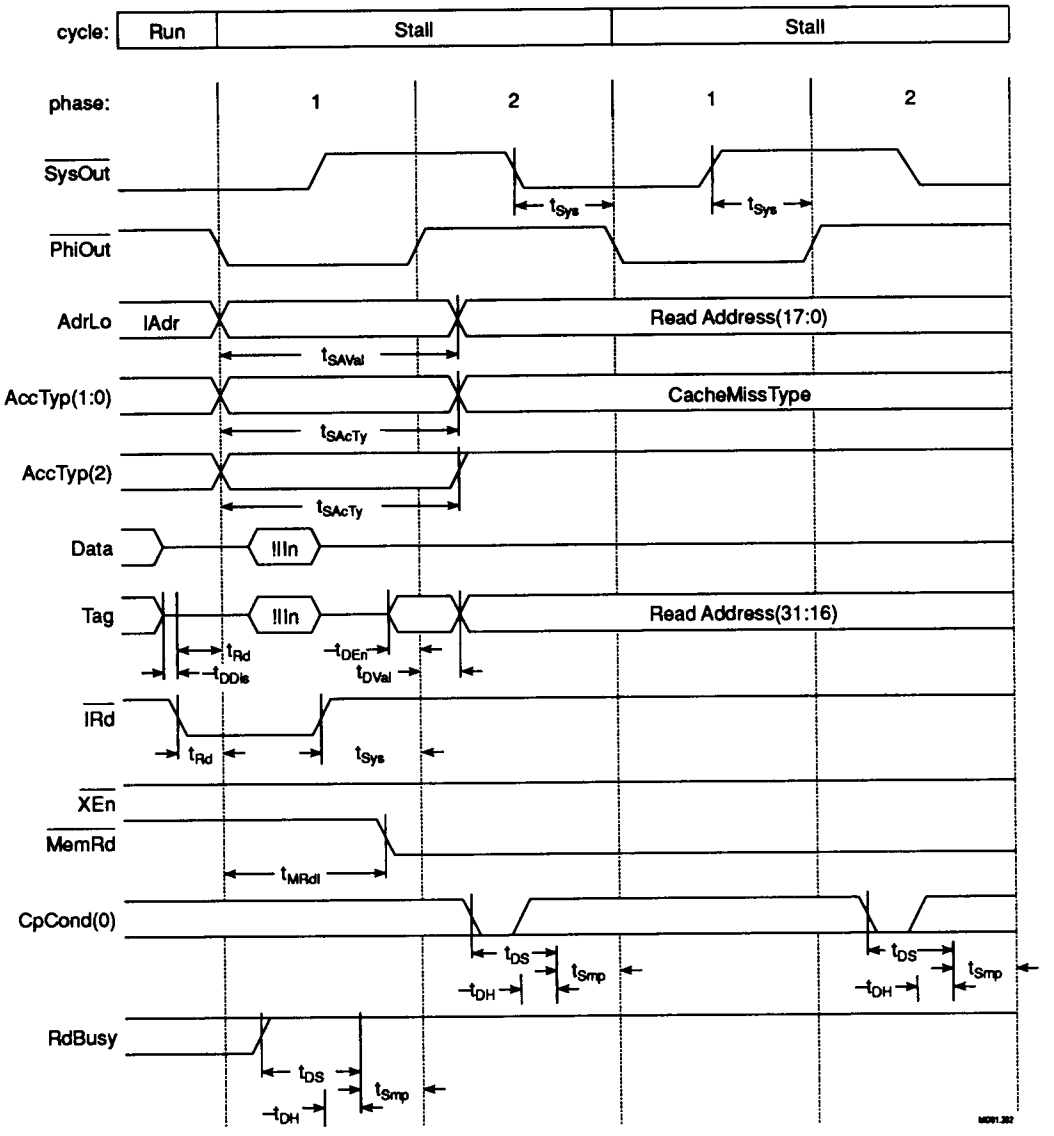


Figure 12.24 Beginning of Read Busy Stall Cycle

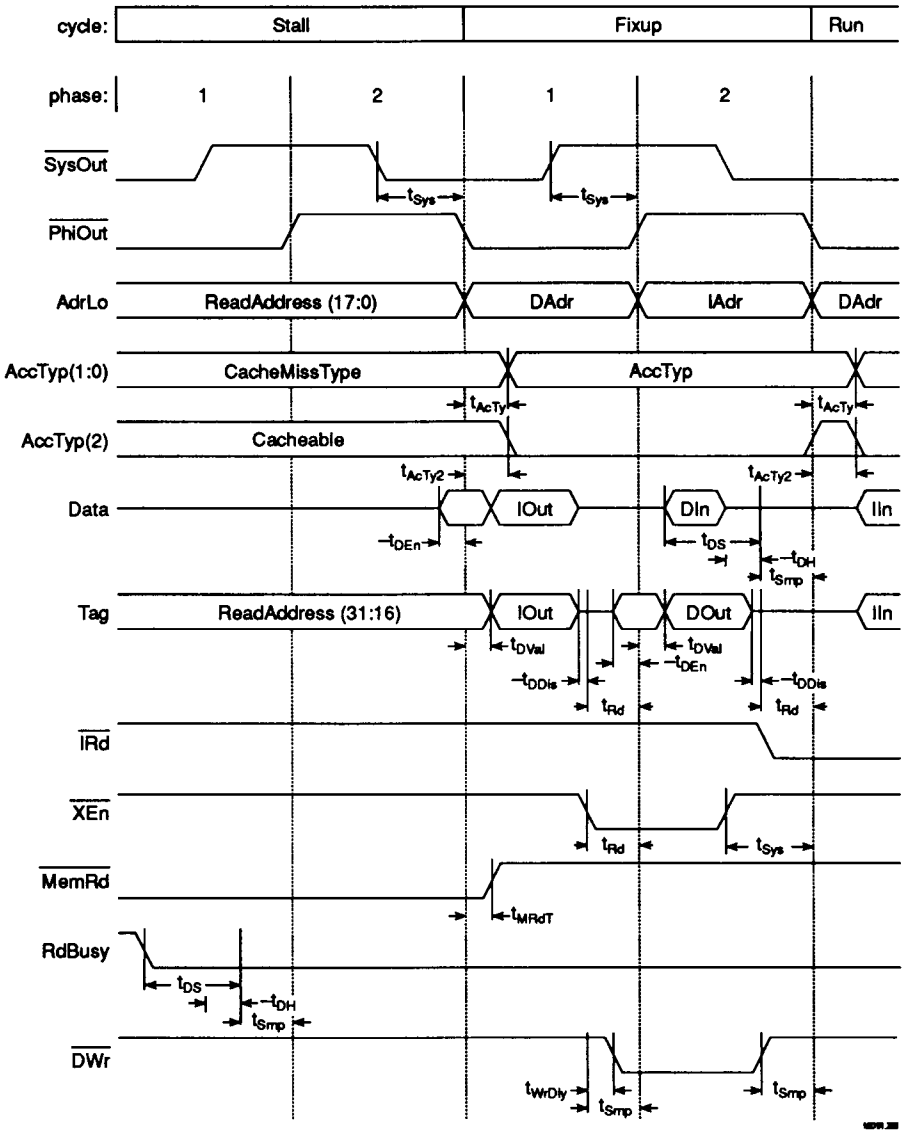


Figure 12.25 End of Read Busy Stall Cycle

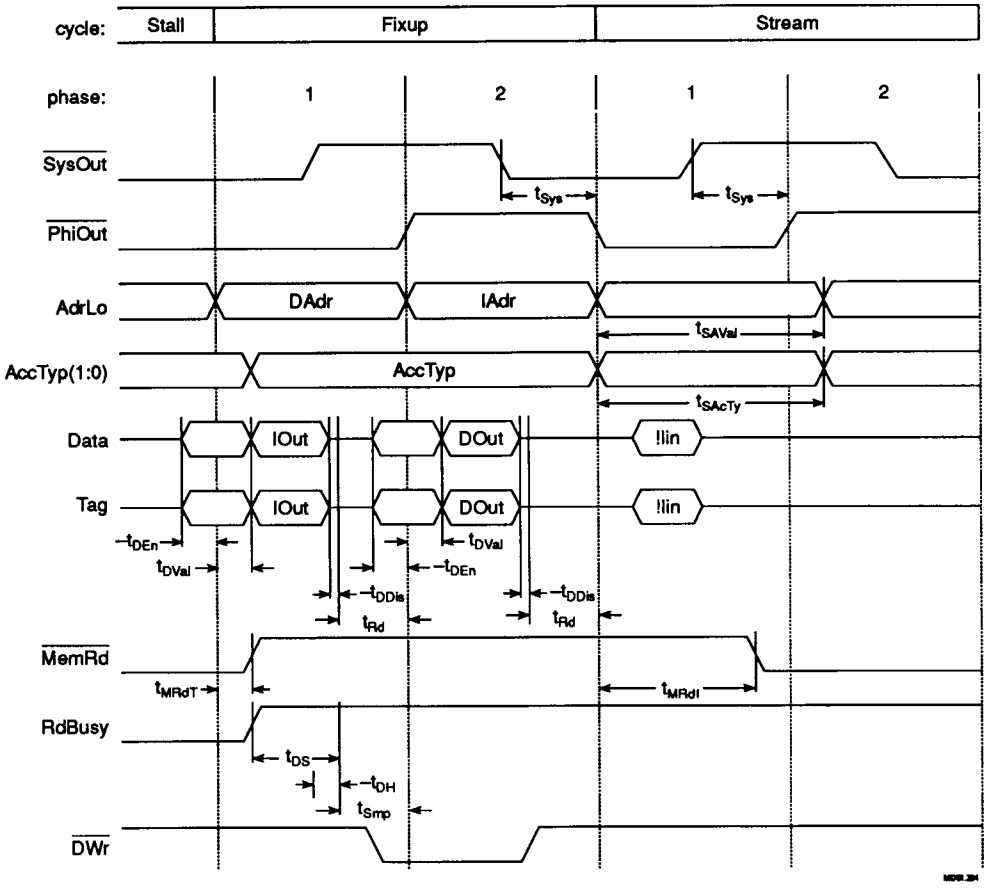


Figure 12.26 Read Busy Retry

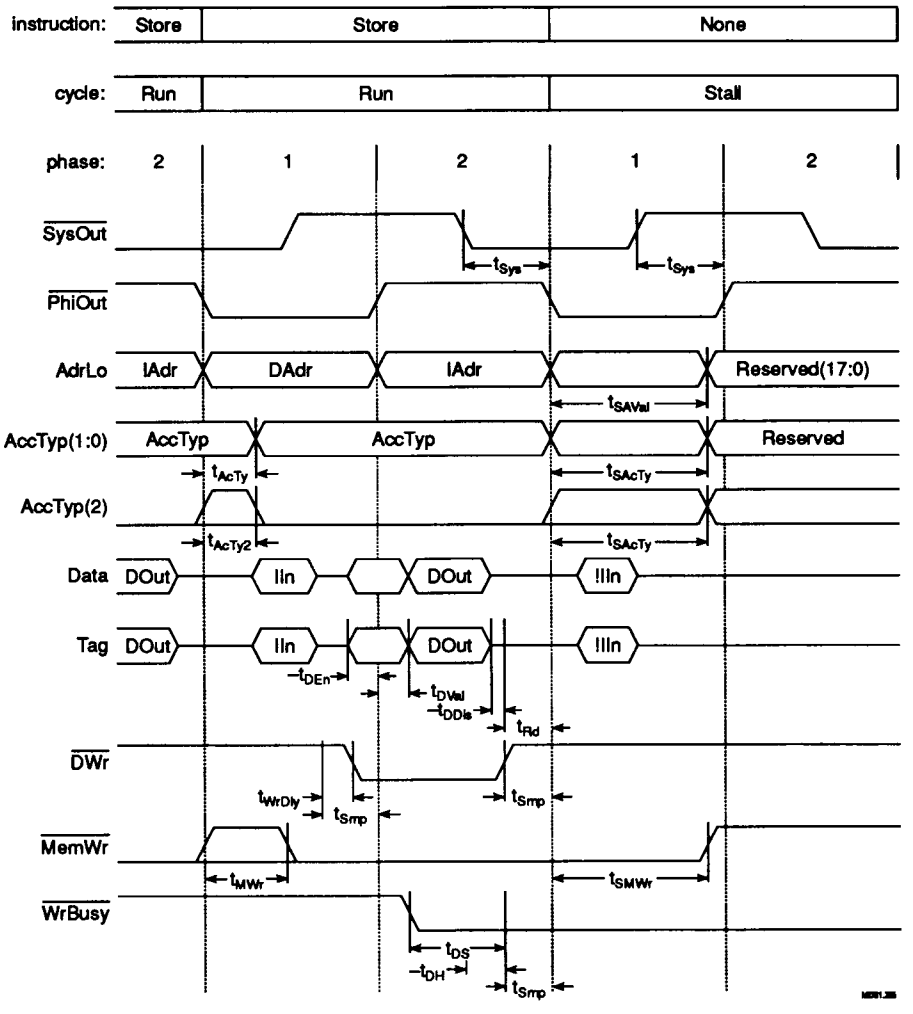


Figure 12.27 Write Busy Stall—Memory Write and Beginning of Stall

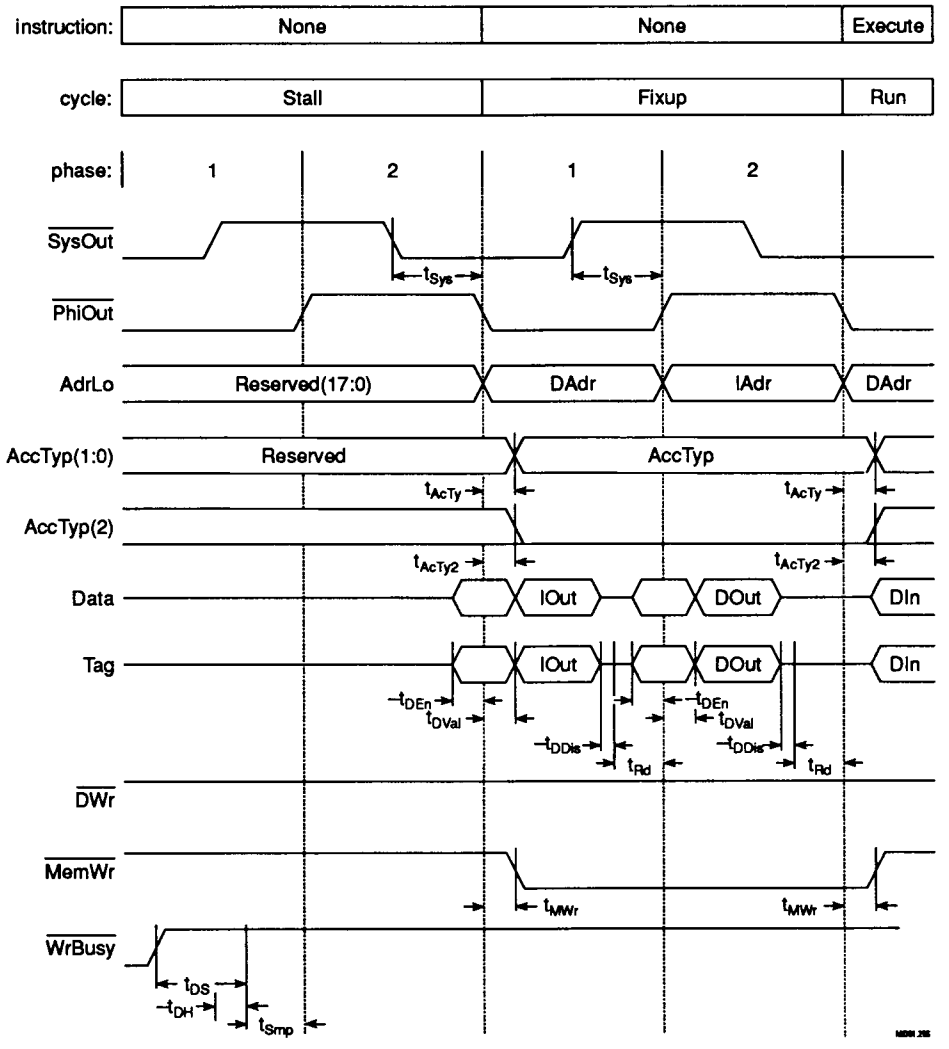


Figure 12.28 Write Busy Stall—End of Stall

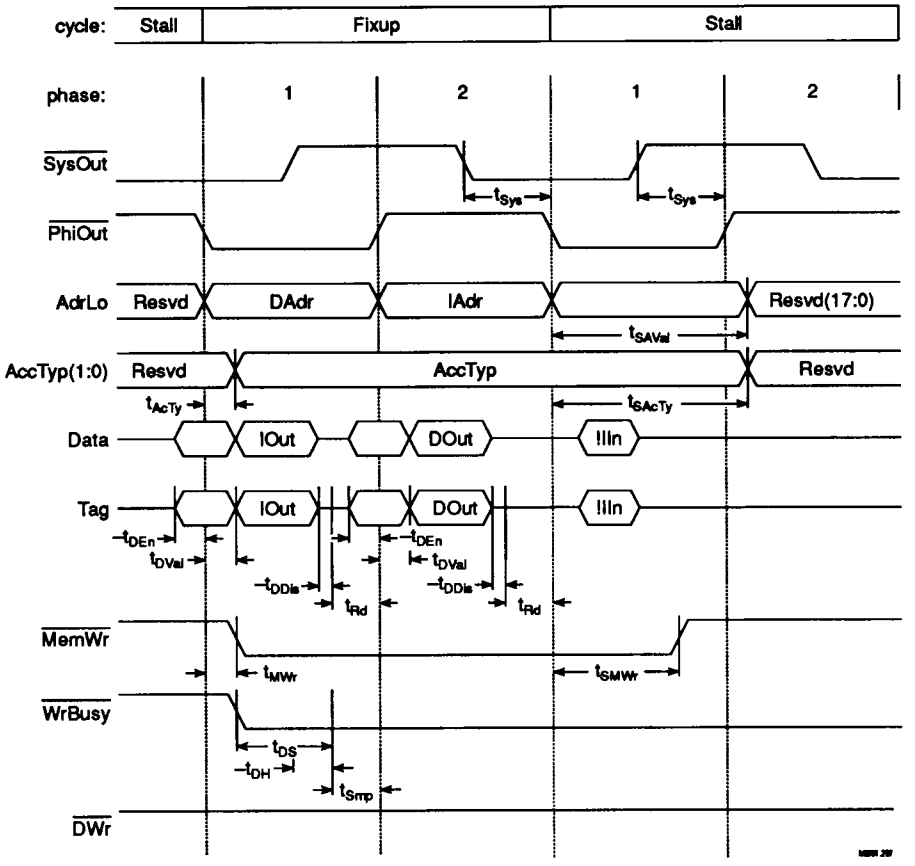


Figure 12.29 Write Busy Retry Timing

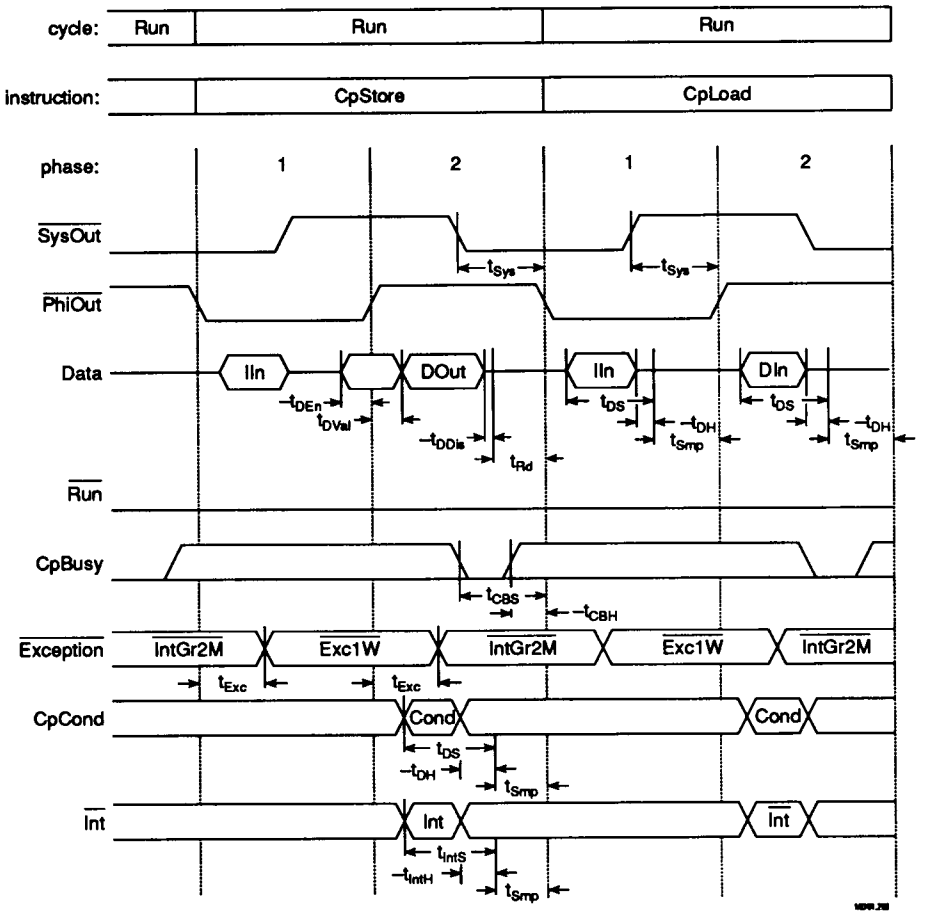


Figure 12.30 Detailed Coprocessor Run Timing

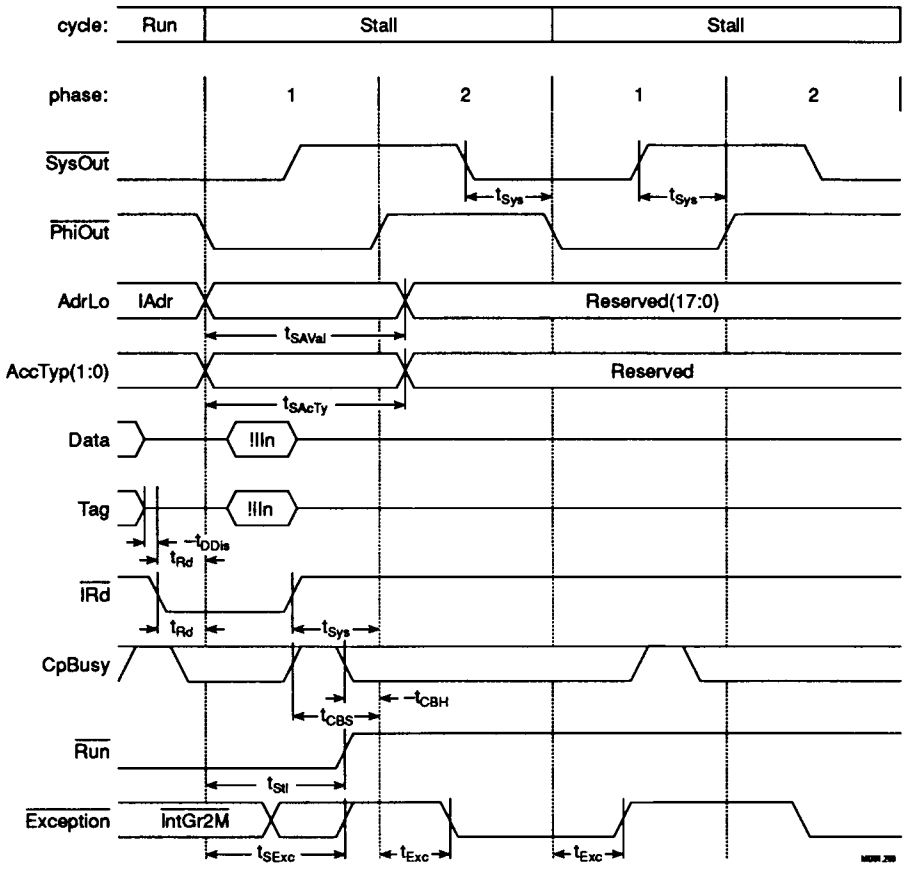


Figure 12.31 Coprocessor Busy Timing—Beginning of Stall

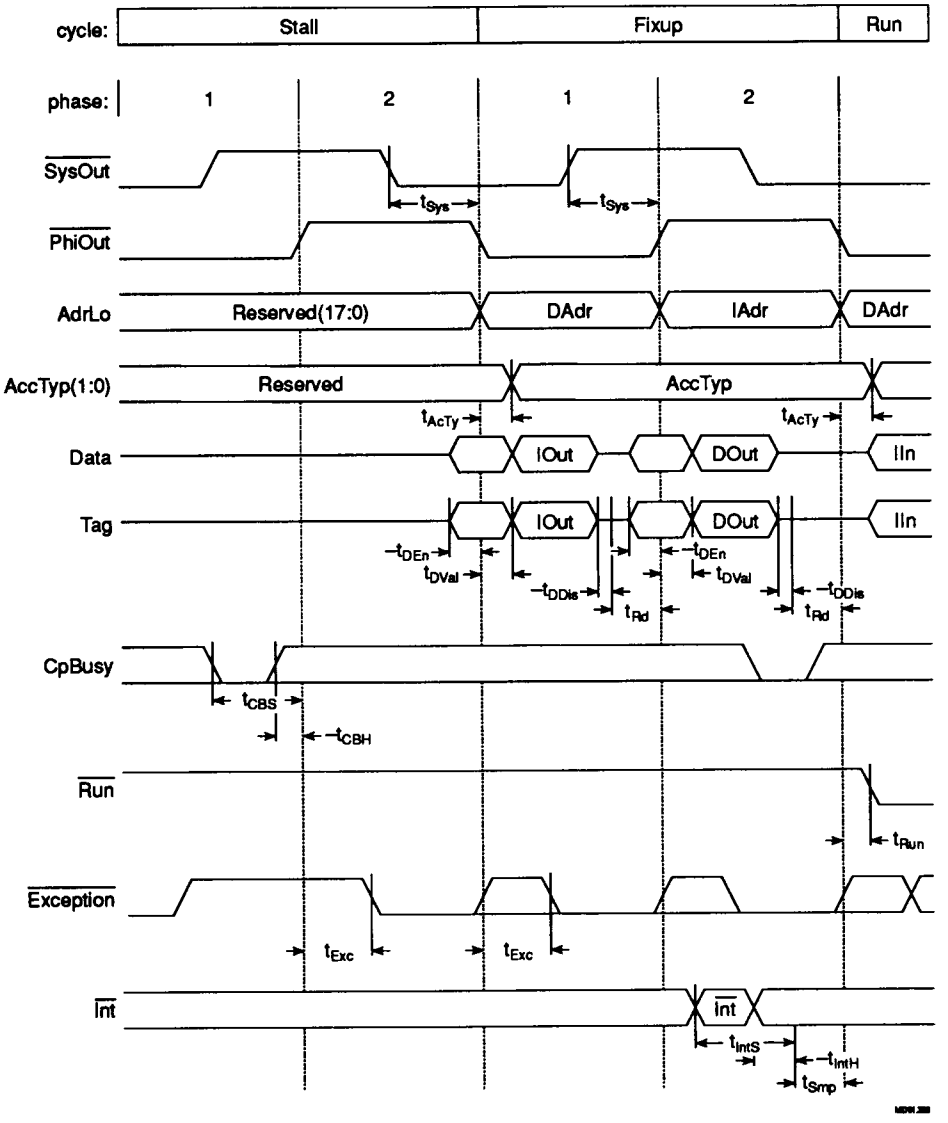


Figure 12.32 Coprocessor Busy Timing - End of Stall

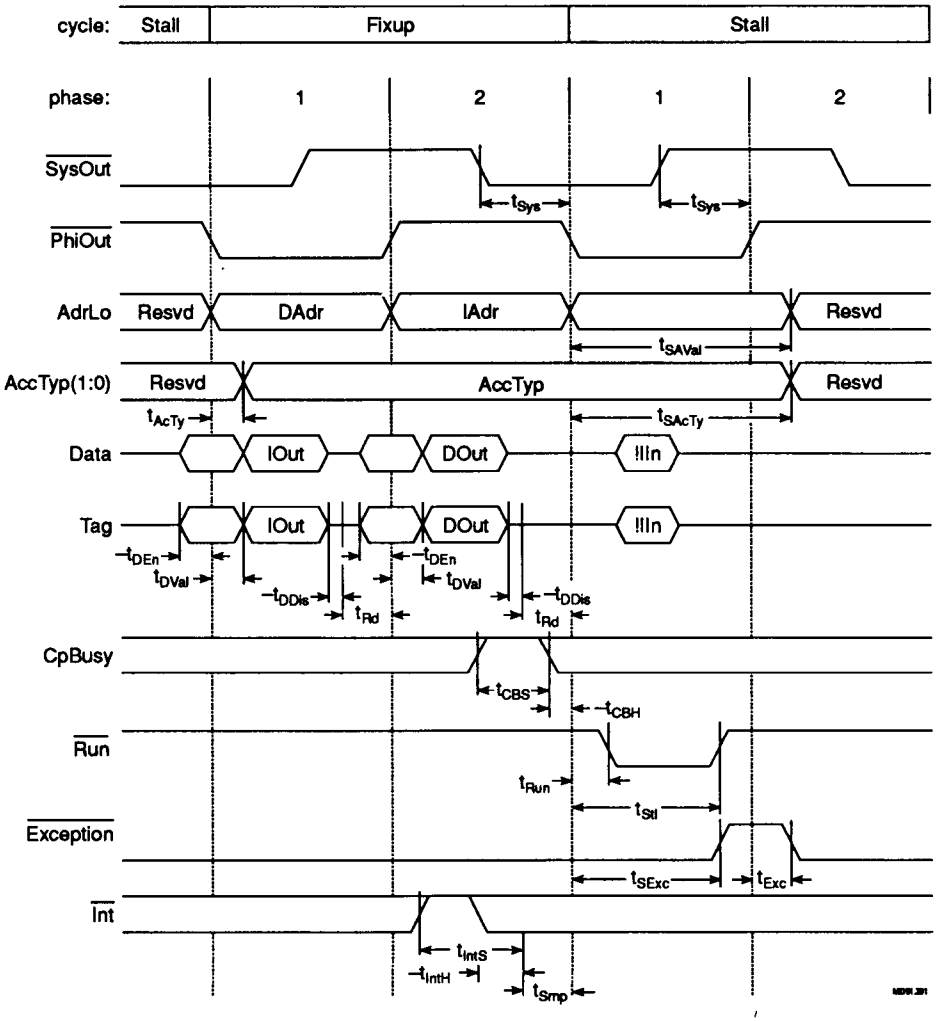


Figure 12.33 Coprocessor Busy Retry Timing

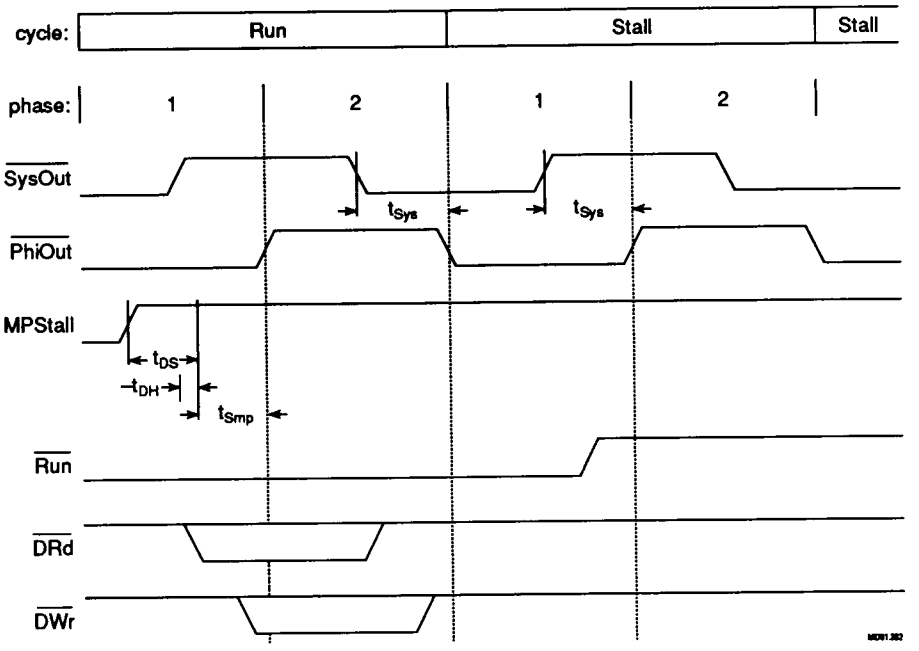


Figure 12.34 MP Stall, Entering from Run

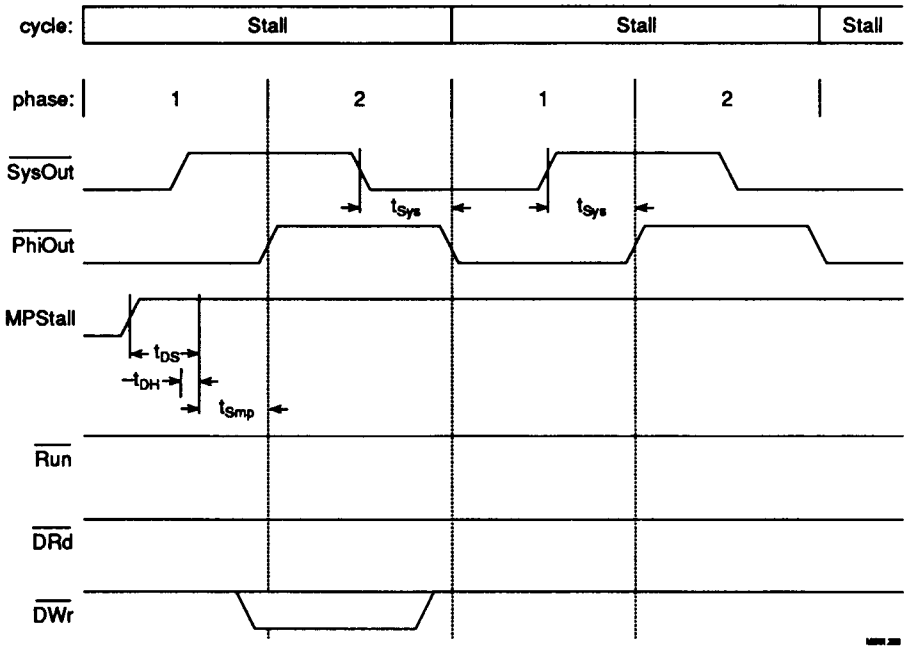


Figure 12.35 MP Stall, Entering from Stall

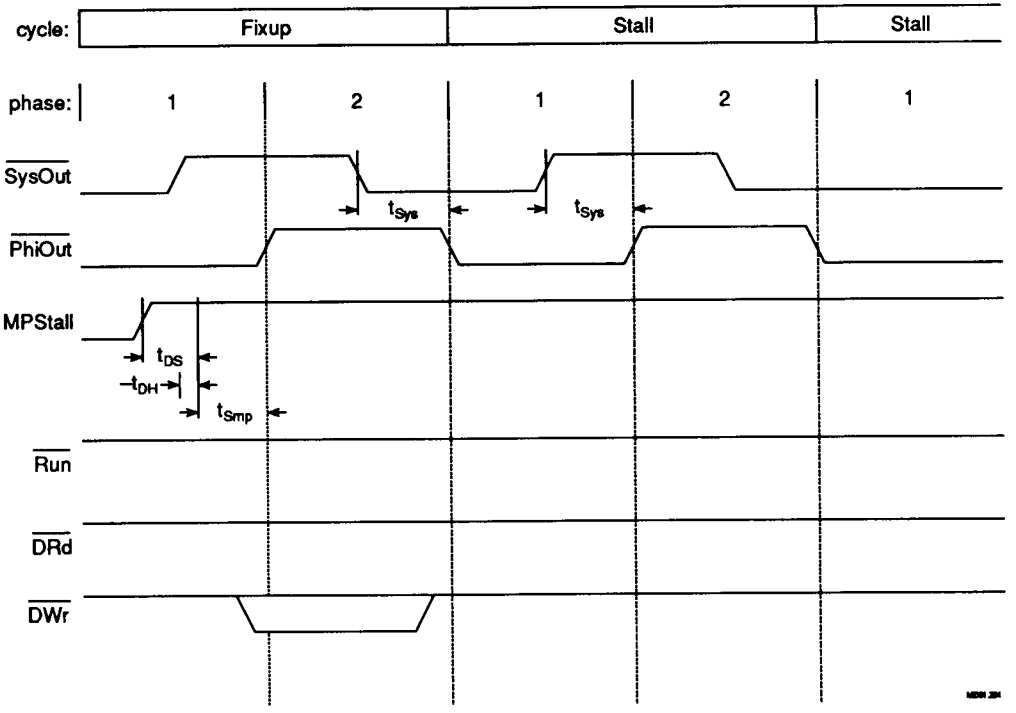


Figure 12.36 MP Stall, Entering from Fixup

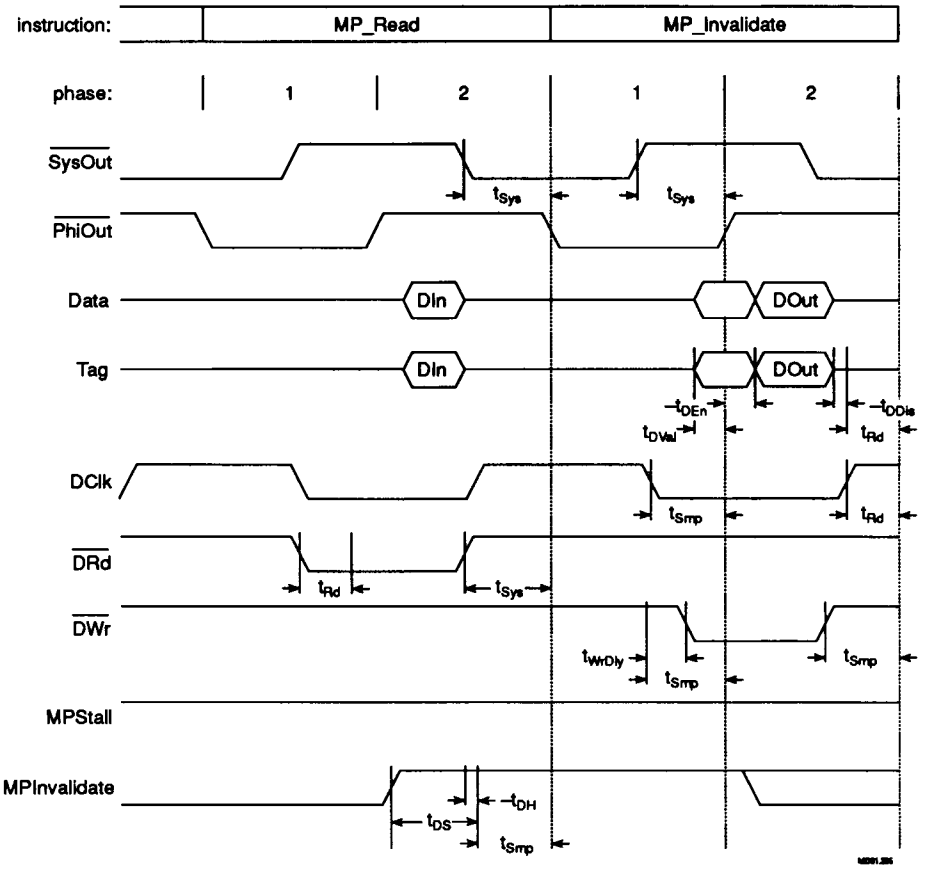


Figure 12.37 MP Stall Read and Invalidate Timing

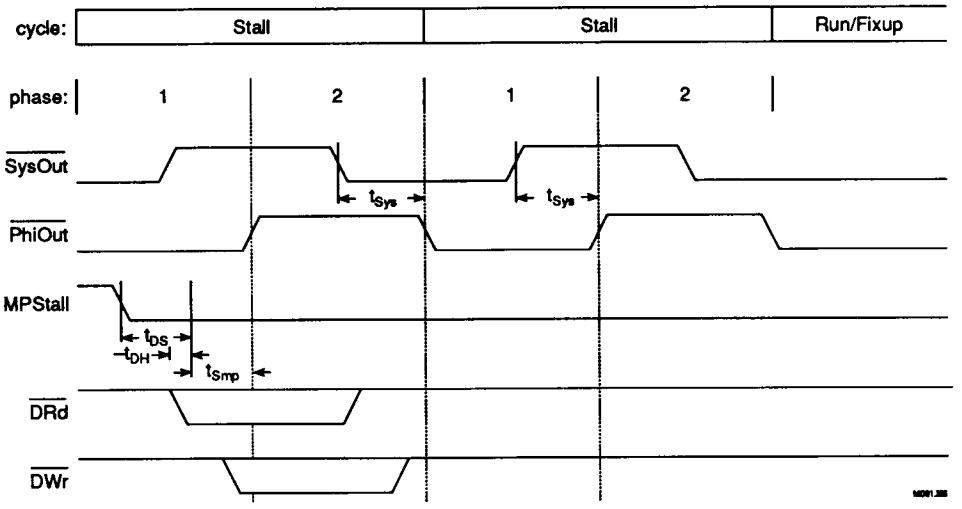


Figure 12.38 MP Stall to Run or to Another Stall via a Fixup

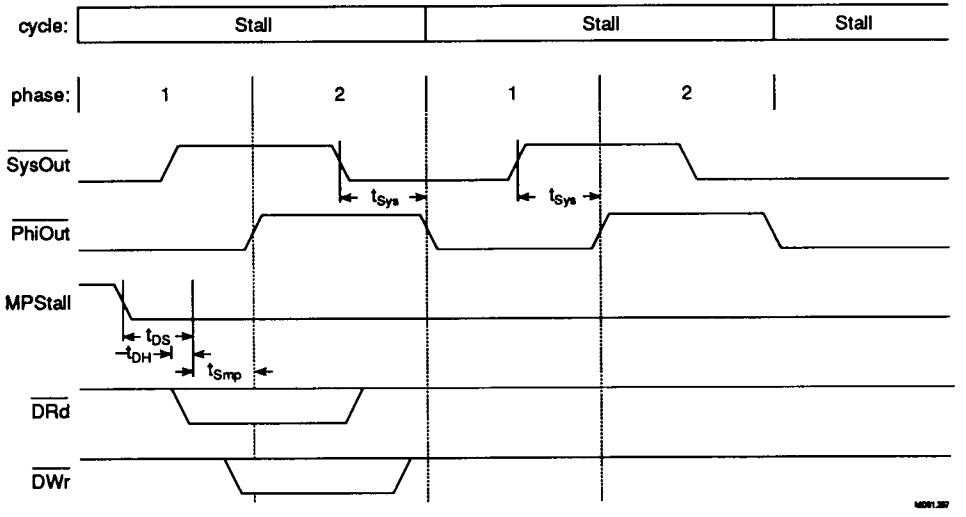


Figure 12.39 MP Stall to Old Stall

12.4 Packaging

LSI Logic provides a variety of sophisticated packages for its LR3000/LR3000A MIPS Reduced Instruction Set Computer (RISC) Family of high-performance microprocessor products. Use this information to select the appropriate packages for your system operating environment. All references

to the LR3000 family and LR3000-based systems include the LR3000A unless specifically noted. Table 12.11 summarizes the available packages.

Device	Cavity-Up CPGA	Cavity-Up CLDCC	Cavity-Down CPGA	Cavity-Down CLDCC
LR3000 CPU	available	available	—	—
LR3000A CPU	—	—	available	available

Notes:

(1) CPGA is Ceramic Pin Grid Array, CLDCC is Ceramic LeaDed Chip Carrier

(2) All CLDCCs are shipped flat. All cavity-down packages include an integral heat sink.

Table 12.11 LR3000 Family Package Options

Description

The LSI Logic packages for its LR3000 Family include both ceramic pin grid array (CPGA) and ceramic leaded chip carrier (CLDCC) packages.

LSI Logic designed many of the LR3000 Family packages specifically to support its RISC microprocessor components. These advanced packages differ from standard packages in two important ways:

1. All LR3000 Family packages are *electrically enhanced.*

   For improved high-speed operation, LSI Logic designed special packages with multiple power and ground planes for the LR3000 Family. This innovative *multiplane* technique reduces signal I/O path inductance, signal-to-signal capacitance (crosstalk), and VDD/VSS path inductance and resistance. The technique also enhances the internal decoupling capacitance of the package.

   Figure 12.40 and Figure 12.41 illustrate the advanced multiplane technology for cavity-up and cavity-down packages, respectively.

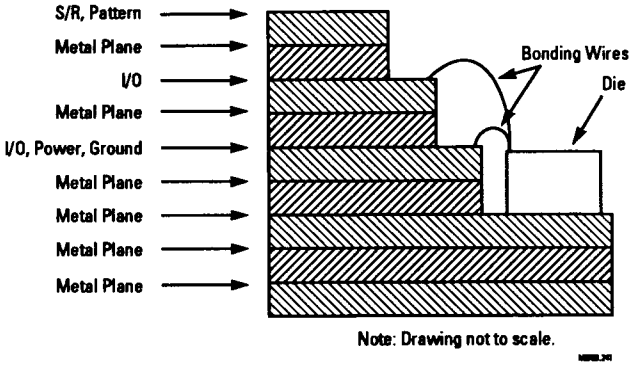


Figure 12.40 9-Layer Cavity-Up Package Cross Section

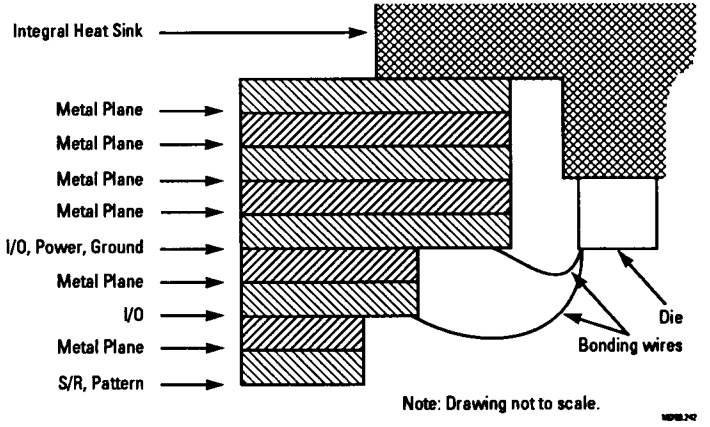


Figure 12.41 9-Layer Cavity-Down Package Cross Section

2. All LR3000 Family cavity-down packages are *thermally enhanced.*

   LSI Logic designed all LR3000 Family cavity-down packages with an integral heat sink for improved convective cooling. Refer to Appendix D, Thermal Considerations, for details on the thermal characteristics for the packages.

Mechanical, Pinout, and Mounting Information

This subsection includes the pin lists, pin diagrams, and mechanical drawings for these LR3000 Family packages, as well as mounting information:

- LR3000: 144-Pin Cavity-Up CPGA
- LR3000: 172-Pin Cavity-Up CLDCC
- LR3000A: 175-Pin Cavity-Down CPGA

- LR3000A: 172-Pin Cavity-Down CLDCC

Notice the tight tolerances on the mechanical drawings. The LSI Logic advanced manufacturing technology meets these tolerances to improve the manufacturability of your LR3000-based systems.

The LR3000 Family packages can utilize various sockets from the manufacturers listed below. Contact your local LSI Logic Sales Office or the manufacturer to check for specific compatibility. Contact the manufacturer for up-to-date socket specifications.

AMP Incorporated
P.O. Box 3608
Harrisburg, PA 17105
(800) 522-6752

Textool/3M Test and
Interconnect Products Dept.
3M Austin Center
P.O. Box 2963
Austin, TX 78769
(800) 225-5373

Yamaichi Electronics, Inc.
1425 Koll Circle, Suite 106
San Jose, CA 95112
(408) 452-0797

Wells Electronics, Inc.
1701 S. Main Street
So. Bend, IN 46613
(219) 287-5941

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
AccTyp0	P15	Data4	G1	IClk	R13	Tag31	L14
AccTyp1	M14	Data5	H2	$\overline{\text{Int0}}$	C9		
AccTyp2	L13	Data6	H1	$\overline{\text{Int1}}$	B9	TagP0	C14
		Data7	F2	$\overline{\text{Int2}}$	A11	TagP1	G15
AdrLo0	C1	Data8	H3	$\overline{\text{Int3}}$	B10	TagP2	K14
AdrLo1	E3	Data9	J3	$\overline{\text{Int4}}$	C10	TagV	N15
AdrLo2	D2	Data10	J1	$\overline{\text{Int5}}$	A12	$\overline{\text{XEn}}$	P7
AdrLo3	B1	Data11	K2			$\overline{\text{WrBusy}}$	A13
AdrLo4	C2	Data12	L2	$\overline{\text{IRd1}}$	P12		
AdrLo5	C4	Data13	M1	$\overline{\text{IRd2}}$	B6	VCC	A1
AdrLo6	A2	Data14	N1	$\overline{\text{IWr1}}$	P13	VCC	A5
AdrLo7	B3	Data15	K1	$\overline{\text{IWr2}}$	P3	VCC	A15
AdrLo8	C5	Data16	M2	$\overline{\text{MemRd}}$	N13	VCC	C3
AdrLo9	B4	Data17	L3	$\overline{\text{MemWr}}$	N12	VCC	C8
AdrLo10	A3	Data18	N2	MPInvalidate	A9[1]	VCC	E15
AdrLo11	A4	Data19	N3	MPStall	A10[1]	VCC	F1
AdrLo12	B5	Data20	P2	RdBusy	C11	VCC	H13
AdrLo13	B7	Data21	R2	$\overline{\text{Reset}}$	A14	VCC	L1
AdrLo14	A6	Data22	P4	$\overline{\text{Run}}$	N14	VCC	M15
AdrLo15	A7	Data23	P1	$\overline{\text{SysOut}}$	R11	VCC	N7
AdrLo16	A9[1]	Data24	N5			VCC	N8
AdrLo17	A10[1]	Data25	R3	Tag12	B14	VCC	R1
		Data26	P5	Tag13	C13	VCC	R12
$\overline{\text{BusError}}$	B12	Data27	P6	Tag14	D13	VCC	R15
		Data28	R5	Tag15	B15		
Clk2xPhi	R9	Data29	R7	Tag16	E13	GND	C6
Clk2xRd	P10	Data30	P8	Tag17	D14	GND	C7
Clk2xSmp	R10	Data31	R4	Tag18	C15	GND	C12
Clk2xSys	P9			Tag19	D15	GND	D3
CpBusy	B11	DataP0	E1	Tag20	E14	GND	F13
CpCond0	A8	DataP1	J2	Tag21	F14	GND	G3
CpCond1	B8	DataP2	M3	Tag22	G14	GND	G13
CpCond2	A9[1]	DataP3	N6	Tag23	F15	GND	K3
CpCond3	A10[1]			Tag24	H15	GND	K13
$\overline{\text{CpSync}}$	P14	DClk	P11	Tag25	H14	GND	M13
		$\overline{\text{DRd1}}$	N11	Tag26	J15	GND	N4
Data0	E2	$\overline{\text{DRd2}}$	B2	Tag27	K15	GND	N9
Data1	D1	$\overline{\text{DWr1}}$	R14	Tag28	J13	GND	N10
Data2	F3	$\overline{\text{DWr2}}$	B13	Tag29	J14	GND	R6
Data3	G2	$\overline{\text{Exception}}$	R8	Tag30	L15		

Note:
(1) AdrLo16 and AdrLo17 are multifunction pins controlled by mode-select programming at reset time. Signals are AdrLo16, CpCond2, or MPInvalidate, and AdrLo17, CpCond3, or MPStall.

Table 12.12 LR3000 Pin List: 144-Pin Cavity-Up CPGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	VCC	AdrLo6	AdrLo10	AdrLo11	VCC	AdrLo14	AdrLo15	CpCond0	AdrLo16[1]	AdrLo17[1]	$\overline{Int2}$	$\overline{Int5}$	$\overline{WrBusy}$	$\overline{Reset}$	VCC
B	AdrLo3	$\overline{DRd2}$	AdrLo7	AdrLo9	AdrLo12	$\overline{IRd2}$	AdrLo13	CpCond1	$\overline{Int1}$	$\overline{Int3}$	CpBusy	$\overline{BusError}$	$\overline{DWr2}$	Tag12	Tag15
C	AdrLo0	AdrLo4	VCC	AdrLo5	AdrLo8	GND	GND	VCC	$\overline{Int0}$	$\overline{Int4}$	RdBusy	GND	Tag13	TagP0	Tag18
D	Data1	AdrLo2	GND	*extra pin*									Tag14	Tag17	Tag19
E	DataP0	Data0	AdrLo1										Tag16	Tag20	VCC
F	VCC	Data7	Data2										GND	Tag21	Tag23
G	Data4	Data3	GND										GND	Tag22	TagP1
H	Data6	Data5	Data8					Top View					VCC	Tag25	Tag24
J	Data10	DataP1	Data9										Tag28	Tag29	Tag26
K	Data15	Data11	GND										GND	TagP2	Tag27
L	VCC	Data12	Data17										AccTyp2	Tag31	Tag30
M	Data13	Data16	DataP2										GND	AccTyp1	VCC
N	Data14	Data18	Data19	GND	Data24	DataP3	VCC	VCC	GND	GND	$\overline{DRdT}$	$\overline{MemWr}$	$\overline{MemRd}$	$\overline{Run}$	TagV
P	Data23	Data20	$\overline{IWr2}$	Data22	Data26	Data27	$\overline{XEn}$	Data30	Clk2xSys	Clk2xRd	DClk	$\overline{IRdT}$	$\overline{IWrT}$	$\overline{CpSync}$	AccTyp0
R	VCC	Data21	Data25	Data31	Data28	GND	Data29	$\overline{Exception}$	Clk2xPhi	Clk2xSmp	$\overline{SysOut}$	VCC	IClk	$\overline{DWrT}$	VCC

Note:
(1) AdrLo16 and AdrLo17 are multifunction pins controlled by mode-select programming at reset time. Signals are AdrLo16, CpCond2, or MPInvalidate, and AdrLo17, CpCond3, or MPStall.

Figure 12.42 LR3000 Pin Diagram: 144-Pin Cavity-Up CPGA

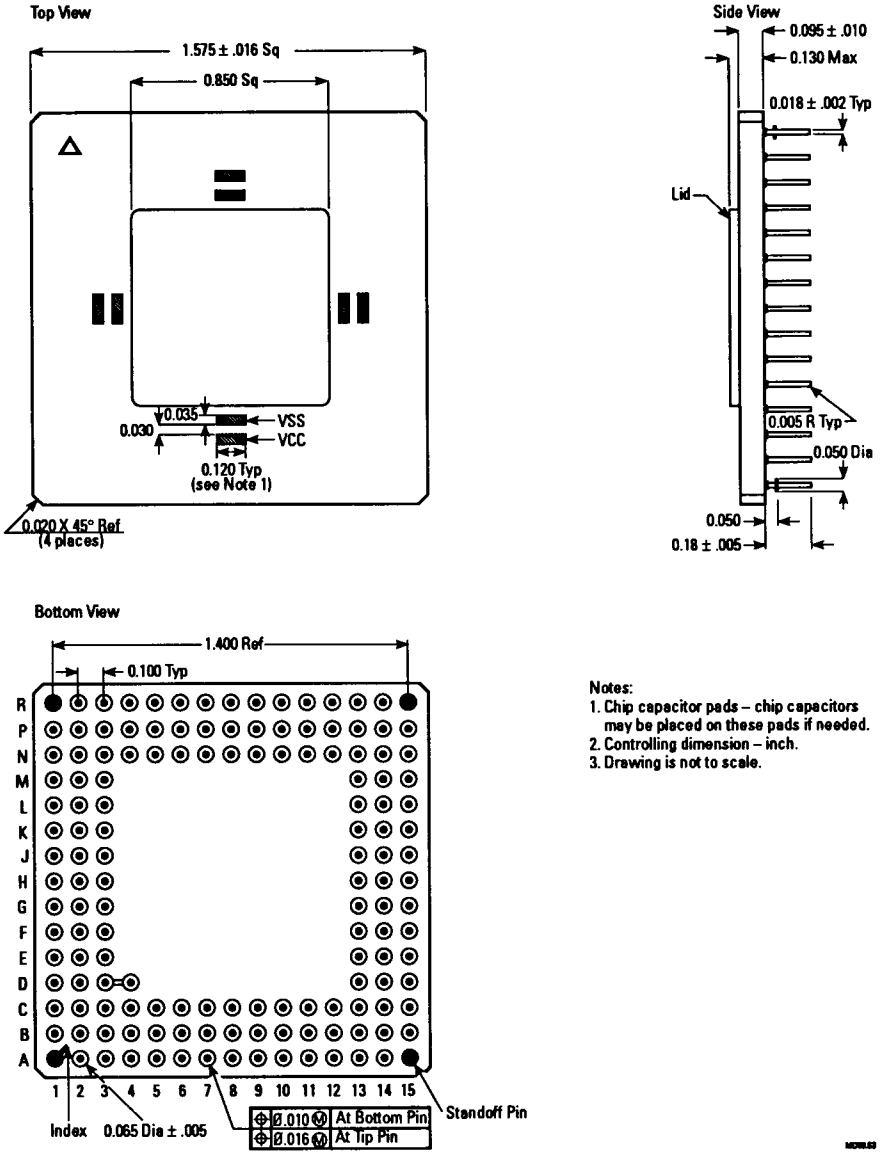


Figure 12.43 LR3000 Mechanical Drawing: 144-Pin Cavity-Up CPGA

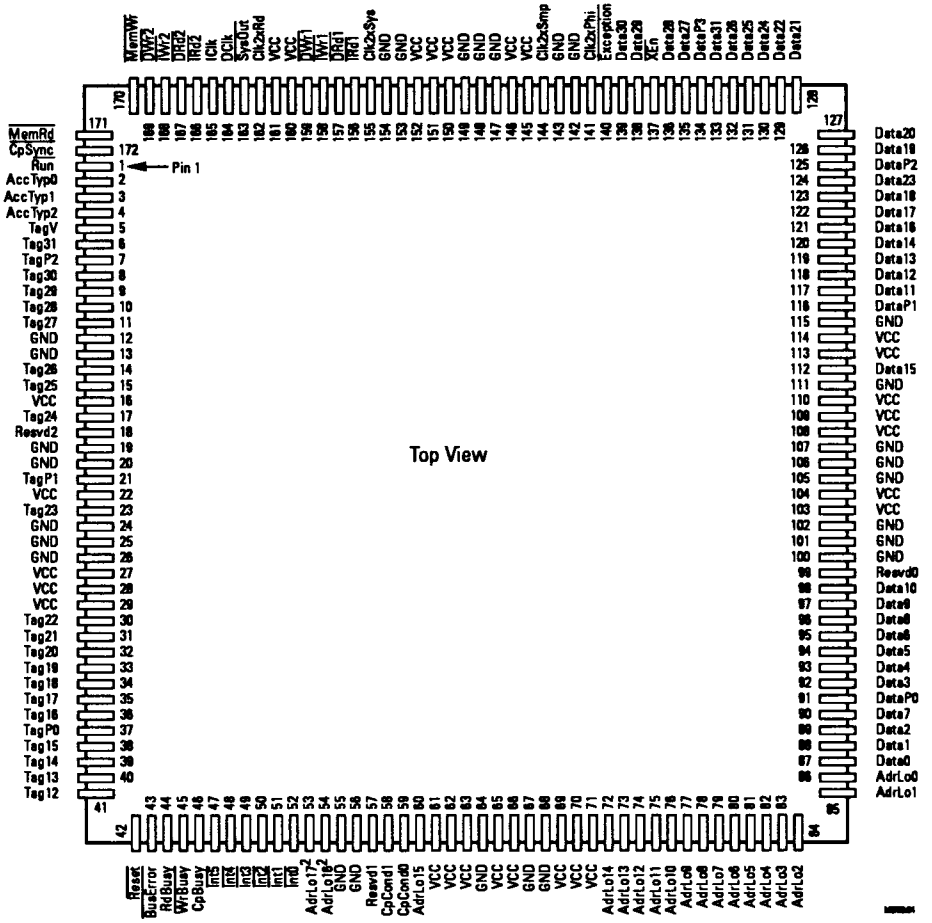
Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
AccTyp0	2	Data7	90	$\overline{\text{Int1}}$	51	Tag26	14
AccTyp1	3	Data8	96	$\overline{\text{Int2}}$	50	Tag27	11
AccTyp2	4	Data9	97	$\overline{\text{Int3}}$	49	Tag28	10
AdrLo0	86	Data10	98	$\overline{\text{Int4}}$	48	Tag29	9
AdrLo1	85	Data11	117	$\overline{\text{Int5}}$	47	Tag30	8
AdrLo2	84	Data12	118			Tag31	6
AdrLo3	83	Data13	119	$\overline{\text{IRd1}}$	156		
AdrLo4	82	Data14	120	$\overline{\text{IRd2}}$	166	TagP0	37
AdrLo5	81	Data15	112	$\overline{\text{IWr1}}$	158	TagP1	21
AdrLo6	80	Data16	121	$\overline{\text{IWr2}}$	168	TagP2	7
AdrLo7	79	Data17	122			TagV	5
AdrLo8	78	Data18	123	$\overline{\text{MemRd}}$	171		
AdrLo9	77	Data19	126	$\overline{\text{MemWr}}$	170	$\overline{\text{XEn}}$	137
AdrLo10	76	Data20	127				
AdrLo11	75	Data21	128	MPInvalidate	54[1]	$\overline{\text{WrBusy}}$	45
AdrLo12	74	Data22	129	MPStall	53[1]		
AdrLo13	73	Data23	124			VCC	16
AdrLo14	72	Data24	130	RdBusy	44	VCC	22
AdrLo15	60	Data25	131			VCC	27
AdrLo16	54[1]	Data26	132	$\overline{\text{Reset}}$	42	VCC	28
AdrLo17	53[1]	Data27	135			VCC	29
		Data28	136	Resvd0	99	VCC	61
$\overline{\text{BusError}}$	43	Data29	138	Resvd1	57	VCC	62
		Data30	139	Resvd2	18	VCC	63
Clk2xPhi	141	Data31	133			VCC	65
Clk2xRd	162			$\overline{\text{Run}}$	1	VCC	66
Clk2xSmp	144	DataP0	91			VCC	69
Clk2xSys	155	DataP1	116	$\overline{\text{SysOut}}$	163	VCC	70
		DataP2	125			VCC	71
CpBusy	46	DataP3	134	Tag12	41	VCC	103
CpCond0	59			Tag13	40	VCC	104
CpCond1	58	DClk	164	Tag14	39	VCC	108
CpCond2	54[1]			Tag15	38	VCC	109
CpCond3	53[1]	$\overline{\text{DRd1}}$	157	Tag16	36	VCC	110
$\overline{\text{CpSync}}$	172	$\overline{\text{DRd2}}$	167	Tag17	35	VCC	113
		$\overline{\text{DWr1}}$	159	Tag18	34	VCC	114
Data0	87	$\overline{\text{DWr2}}$	169	Tag19	33	VCC	145
Data1	88			Tag20	32	VCC	146
Data2	89	$\overline{\text{Exception}}$	140	Tag21	31	VCC	150
Data3	92			Tag22	30	VCC	151
Data4	93	IClk	165	Tag23	23	VCC	152
Data5	94			Tag24	17	VCC	160
Data6	95	$\overline{\text{Int0}}$	52	Tag25	15	VCC	161

Note:
(1) AdrLo16 and AdrLo17 are multifunction pins controlled by mode-select programming at reset time. Signals are AdrLo16, CpCond2, or MPInvalidate, and AdrLo17, CpCond3, or MPStall.

Table 12.13 LR3000 Pin List: 172-Pin Cavity-Up CLDCC

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
GND	12	GND	55	GND	102	GND	143
GND	13	GND	56	GND	105	GND	147
GND	19	GND	64	GND	106	GND	148
GND	20	GND	67	GND	107	GND	149
GND	24	GND	68	GND	111	GND	153
GND	25	GND	100	GND	115	GND	154
GND	26	GND	101	GND	142		

Table 12.13 LR3000 Pin List: 172-Pin Cavity-Up CLDCC, continued



Notes:
1. The physical pinout of this device matches that of the other manufacturers of the device, although the pin numbering scheme has been changed to conform with JEDEC standards.
2. AdrLo16 and AdrLo17 are multifunction pins controlled by mode-select programming at reset time. Signals are AdrLo16, CpCond2, or MPInvalidate, and AdrLo17, CpCond3, or MPStall.

Figure 12.44 LR3000 Pin Diagram: 172-Pin Cavity-Up CLDCC

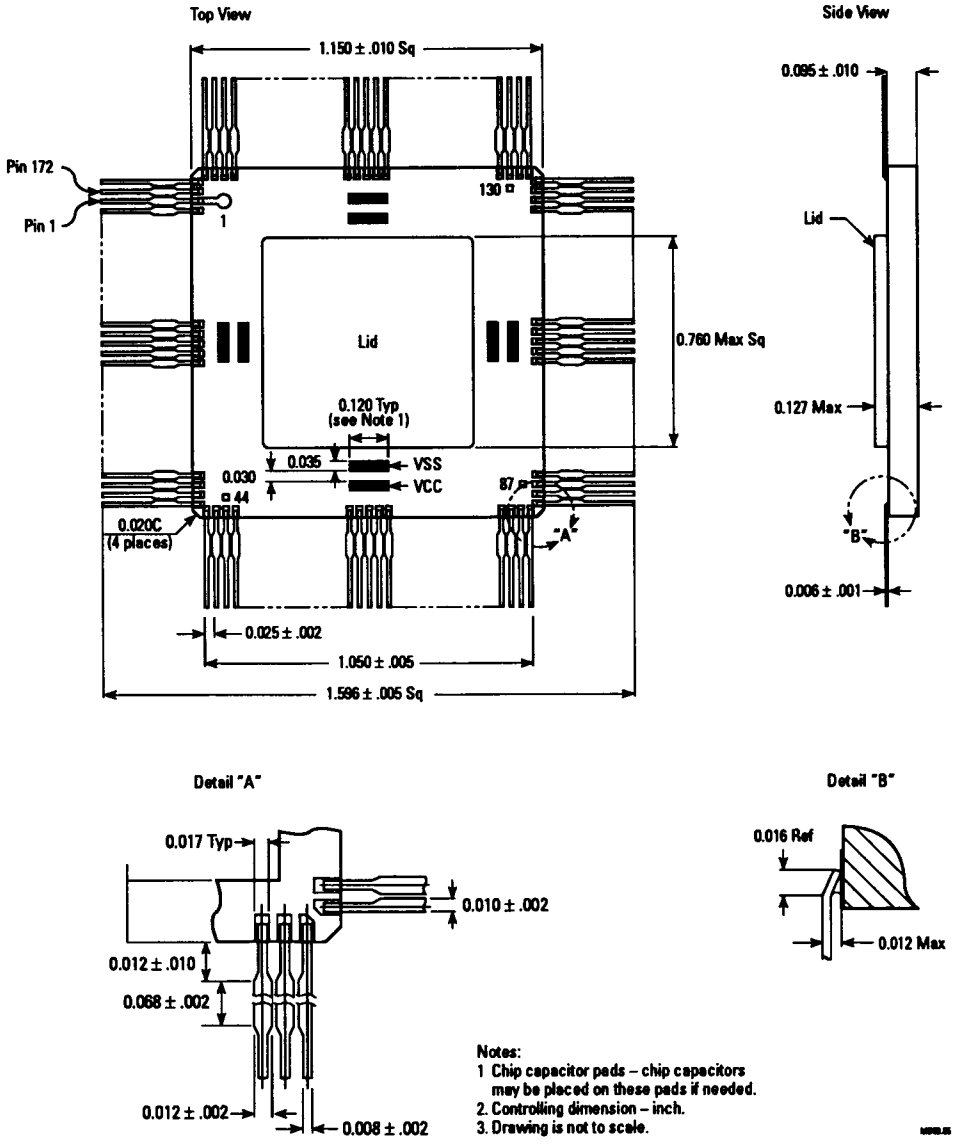


Figure 12.45 LR3000 Mechanical Drawing: 172-Pin Cavity-Up CLDCC

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
AccTyp0	P15	Data5	H2	$\overline{\text{Int0}}$	C9	TagP0	C14
AccTyp1	M14	Data6	H1	$\overline{\text{Int1}}$	B9	TagP1	G15
AccTyp2	L13	Data7	F2	$\overline{\text{Int2}}$	A11	TagP2	K14
		Data8	H3	$\overline{\text{Int3}}$	B10	TagV	N15
AdrLo0	C1	Data9	J3	$\overline{\text{Int4}}$	C10	$\overline{\text{XEn}}$	P7
AdrLo1	E3	Data10	J1	$\overline{\text{Int5}}$	A12	$\overline{\text{WrBusy}}$	A13
AdrLo2	D2	Data11	K2	$\overline{\text{IRd1}}$	P12		
AdrLo3	B1	Data12	L2	$\overline{\text{IRd2}}$	B6	VCC	A5
AdrLo4	C2	Data13	M1	$\overline{\text{IWr1}}$	P13	VCC	A15
AdrLo5	C4	Data14	N1	$\overline{\text{IWr2}}$	P3	VCC	C3
AdrLo6	A2	Data15	K1	$\overline{\text{MemRd}}$	N13	VCC	C8
AdrLo7	B3	Data16	M2	$\overline{\text{MemWr}}$	N12	VCC	D5
AdrLo8	C5	Data17	L3	MPInvalidate	A9[1]	VCC	D7
AdrLo9	B4	Data18	N2	MPStall	A10[1]	VCC	D9
AdrLo10	A3	Data19	N3	RdBusy	C11	VCC	D11
AdrLo11	A4	Data20	P2	$\overline{\text{Reset}}$	A14	VCC	E4
AdrLo12	B5	Data21	R2	$\overline{\text{Run}}$	N14	VCC	E12
AdrLo13	B7	Data22	P4	$\overline{\text{SysOut}}$	R11	VCC	E15
AdrLo14	A6	Data23	P1			VCC	F1
AdrLo15	A7	Data24	N5	Tag12	B14	VCC	G4
AdrLo16	A9[1]	Data25	R3	Tag13	C13	VCC	G12
AdrLo17	A10[1]	Data26	P5	Tag14	D13	VCC	H13
		Data27	P6	Tag15	B15	VCC	J4
$\overline{\text{BusError}}$	B12	Data28	R5	Tag16	E13	VCC	J12
Clk2xPhi	R9	Data29	R7	Tag17	D14	VCC	L1
Clk2xRd	P10	Data30	P8	Tag18	C15	VCC	L4
Clk2xSmp	R10	Data31	R4	Tag19	D15	VCC	L12
Clk2xSys	P9			Tag20	E14	VCC	M5
CpBusy	B11	DataP0	E1	Tag21	F14	VCC	M7
CpCond0	A8	DataP1	J2	Tag22	G14	VCC	M9
CpCond1	B8	DataP2	M3	Tag23	F15	VCC	M11
CpCond2	A9[1]	DataP3	N6	Tag24	H15	VCC	M15
CpCond3	A10[1]	DClk	P11	Tag25	H14	VCC	N7
$\overline{\text{CpSync}}$	P14	$\overline{\text{DRd1}}$	N11	Tag26	J15	VCC	N8
		$\overline{\text{DRd2}}$	B2	Tag27	K15	VCC	R1
Data0	E2	$\overline{\text{DWr1}}$	R14	Tag28	J13	VCC	R12
Data1	D1	$\overline{\text{DWr2}}$	B13	Tag29	J14	VCC	R15
Data2	F3	$\overline{\text{Exception}}$	R8	Tag30	L15		
Data3	G2	IClk	R13	Tag31	L14		
Data4	G1						

Note:
(1) AdrLo16 and AdrLo17 are multifunction pins controlled by mode-select programming at reset time. Signals are AdrLo16, CpCond2, or MPInvalidate, and AdrLo17, CpCond3, or MPStall.

Table 12.14 LR3000A Pin List: 175-Pin Cavity-Down CPGA

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
GND	C6	GND	D12	GND	K3	GND	M13
GND	C7	GND	F4	GND	K4	GND	N4
GND	C12	GND	F12	GND	K12	GND	N9
GND	D3	GND	F13	GND	K13	GND	N10
GND	D4	GND	G3	GND	M4	GND	R6
GND	D6	GND	G13	GND	M6		
GND	D8	GND	H4	GND	M8		
GND	D10	GND	H12	GND	M12		

Table 12.14 LR3000A Pin List: 175-Pin Cavity-Down CPGA, continued

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A		AdrLo6	AdrLo10	AdrLo11	VCC	AdrLo14	AdrLo15	CpCond0	AdrLo16	AdrLo17	$\overline{Int2}$	$\overline{Int5}$	$\overline{WrBusy}$	$\overline{Reset}$	VCC
B	AdrLo3	$\overline{DRd2}$	AdrLo7	AdrLo9	AdrLo12	$\overline{IRd2}$	AdrLo13	CpCond1	$\overline{Int1}$	$\overline{Int3}$	CpBusy	$\overline{BusError}$	$\overline{DWr2}$	Tag12	Tag15
C	AdrLo0	AdrLo4	VCC	AdrLo5	AdrLo8	GND	GND	VCC	$\overline{Int0}$	$\overline{Int4}$	RdBusy	GND	Tag13	TagP0	Tag18
D	Data1	AdrLo2	GND	GND	VCC	GND	VCC	GND	VCC	GND	VCC	GND	Tag14	Tag17	Tag19
E	DataP0	Data0	AdrLo1	VCC								VCC	Tag16	Tag20	VCC
F	VCC	Data7	Data2	GND								GND	GND	Tag21	Tag23
G	Data4	Data3	GND	VCC								VCC	GND	Tag22	TagP1
H	Data6	Data5	Data8	GND				Top View				GND	VCC	Tag25	Tag24
J	Data10	DataP1	Data9	VCC								VCC	Tag28	Tag29	Tag26
K	Data15	Data11	GND	GND								GND	GND	TagP2	Tag27
L	VCC	Data12	Data17	VCC								VCC	AccTyp2	Tag31	Tag30
M	Data13	Data16	DataP2	GND	VCC	GND	VCC	GND	VCC	GND	VCC	GND	GND	AccTyp1	VCC
N	Data14	Data18	Data19	GND	Data24	DataP3	VCC	VCC	GND	GND	$\overline{DRd1}$	$\overline{MemWr}$	MemRd	$\overline{Run}$	TagV
P	Data23	Data20	$\overline{IWr2}$	Data22	Data26	Data27	$\overline{XEn}$	Data30	Clk2xSys	Clk2xRd	DClk	$\overline{IRd1}$	$\overline{IWr1}$	$\overline{CpSync}$	AccTyp0
R	VCC	Data21	Data25	Data31	Data28	GND	Data29	$\overline{Exception}$	Clk2xPhi	Clk2xSmp	$\overline{SysOut}$	VCC	IClk	$\overline{DWr1}$	VCC

Notes:

1. The internal ring of 32 power and ground pins are added for increased electrical performance of the package. All other pins on the package are pin-for-pin compatible with the LR3000 144-pin CPGA.
2. Socket pin A1 should be tied to VCC to be compatible with the LR3000 144-pin CPGA.
3. AdrLo16 and AdrLo17 are multifunction pins controlled by mode-select programming at reset time. Signals are AdrLo16, CpCond2, or MPInvalidate, and AdrLo17, CpCond3, or MPStall.

Figure 12.46 LR3000A Pin Diagram: 175-Pin Cavity-Down CPGA

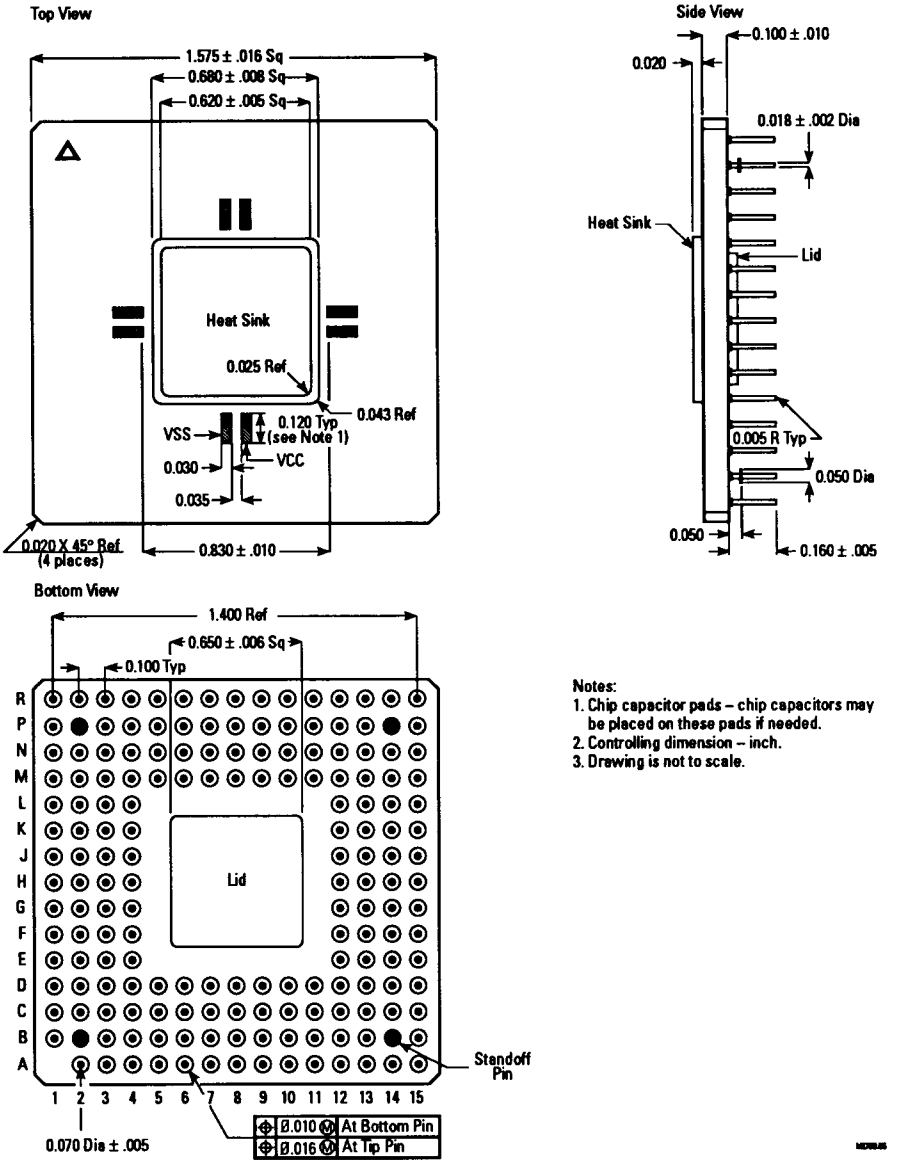


Figure 12.47 LR3000A Mechanical Drawing: 175-Pin Cavity-Down CPGA

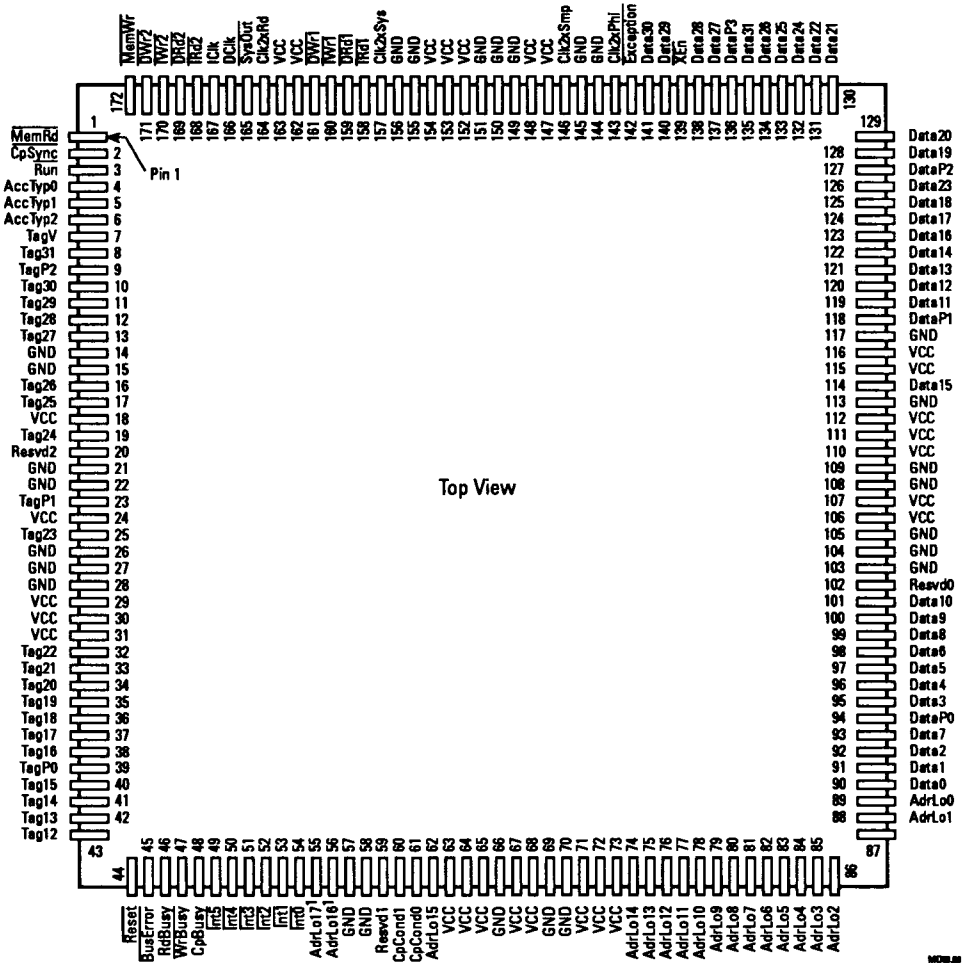
Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
AccTyp0	4	Data6	97	$\overline{\text{Int1}}$	53	Tag27	13
AccTyp1	5	Data7	92	$\overline{\text{Int2}}$	52	Tag28	12
AccTyp2	6	Data8	98	$\overline{\text{Int3}}$	51	Tag29	11
		Data9	99	$\overline{\text{Int4}}$	50	Tag30	10
AdrLo0	88	Data10	100	$\overline{\text{Int5}}$	49	Tag31	8
AdrLo1	87	Data11	119				
AdrLo2	86	Data12	120	$\overline{\text{IRd1}}$	158	TagP0	39
AdrLo3	85	Data13	121	$\overline{\text{IRd2}}$	168	TagP1	23
AdrLo4	84	Data14	122	$\overline{\text{IWr1}}$	160	TagP2	9
AdrLo5	83	Data15	114	$\overline{\text{IWr2}}$	170	TagV	7
AdrLo6	82	Data16	123				
AdrLo7	81	Data17	124	$\overline{\text{MemRd}}$	1	$\overline{\text{XEn}}$	139
AdrLo8	80	Data18	125	$\overline{\text{MemWr}}$	172		
AdrLo9	79	Data19	128	MPInvalidate	56[1]	$\overline{\text{WrBusy}}$	47
AdrLo10	78	Data20	129	MPStall	55[1]		
AdrLo11	77	Data21	130			VCC	18
AdrLo12	76	Data22	131	RdBusy	46	VCC	24
AdrLo13	75	Data23	126	$\overline{\text{Reset}}$	44	VCC	29
AdrLo14	74	Data24	132			VCC	30
AdrLo15	62	Data25	133	Resvd0	101	VCC	31
AdrLo16	56[1]	Data26	134	Resvd1	59	VCC	63
AdrLo17	55[1]	Data27	137	Resvd2	20	VCC	64
		Data28	138			VCC	65
$\overline{\text{BusError}}$	45	Data29	140	$\overline{\text{Run}}$	3	VCC	68
Clk2xPhi	143	Data30	141	$\overline{\text{SysOut}}$	165	VCC	71
Clk2xRd	164	Data31	135			VCC	72
Clk2xSmp	146			Tag12	43	VCC	73
Clk2xSys	157	DataP0	93	Tag13	42	VCC	105
CpBusy	48	DataP1	118	Tag14	41	VCC	106
CpCond0	61	DataP2	127	Tag15	40	VCC	110
CpCond1	60	DataP3	136	Tag16	38	VCC	111
CpCond2	56[1]			Tag17	37	VCC	112
CpCond3	55[1]	DClk	166	Tag18	36	VCC	115
$\overline{\text{CpSync}}$	2	$\overline{\text{DRd1}}$	159	Tag19	35	VCC	116
		$\overline{\text{DRd2}}$	169	Tag20	34	VCC	147
Data0	89	$\overline{\text{DWr1}}$	161	Tag21	33	VCC	148
Data1	90	$\overline{\text{DWr2}}$	171	Tag22	32	VCC	152
Data2	91	$\overline{\text{Exception}}$	142	Tag23	25	VCC	153
Data3	94	IClk	167	Tag24	19	VCC	154
Data4	95			Tag25	17	VCC	162
Data5	96	$\overline{\text{Int0}}$	54	Tag26	16	VCC	163

Note:
(1) AdrLo16 and AdrLo17 are multifunction pins controlled by mode-select programming at reset time. Signals are AdrLo16, CpCond2, or MPInvalidate, and AdrLo17, CpCond3, or MPStall.

Table 12.15 LR3000A Pin List: 172-Pin Cavity-Down CLDCC

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
GND	14	GND	57	GND	104	GND	145
GND	15	GND	58	GND	107	GND	149
GND	21	GND	66	GND	108	GND	150
GND	22	GND	69	GND	109	GND	151
GND	26	GND	70	GND	113	GND	155
GND	27	GND	102	GND	117	GND	156
GND	28	GND	103	GND	144		

Table 12.15 LR3000A Pin List: 172-Pin Cavity-Down CLDCC, continued



Note:
1. AdrLo16 and AdrLo17 are multifunction pins controlled by mode-select programming at reset time. Signals are AdrLo16, CpCond2, or MPInvalidate, and AdrLo17, CpCond3, or MPStall.

Figure 12.48 LR3000A Pin Diagram: 172-Pin Cavity-Down CLDCC

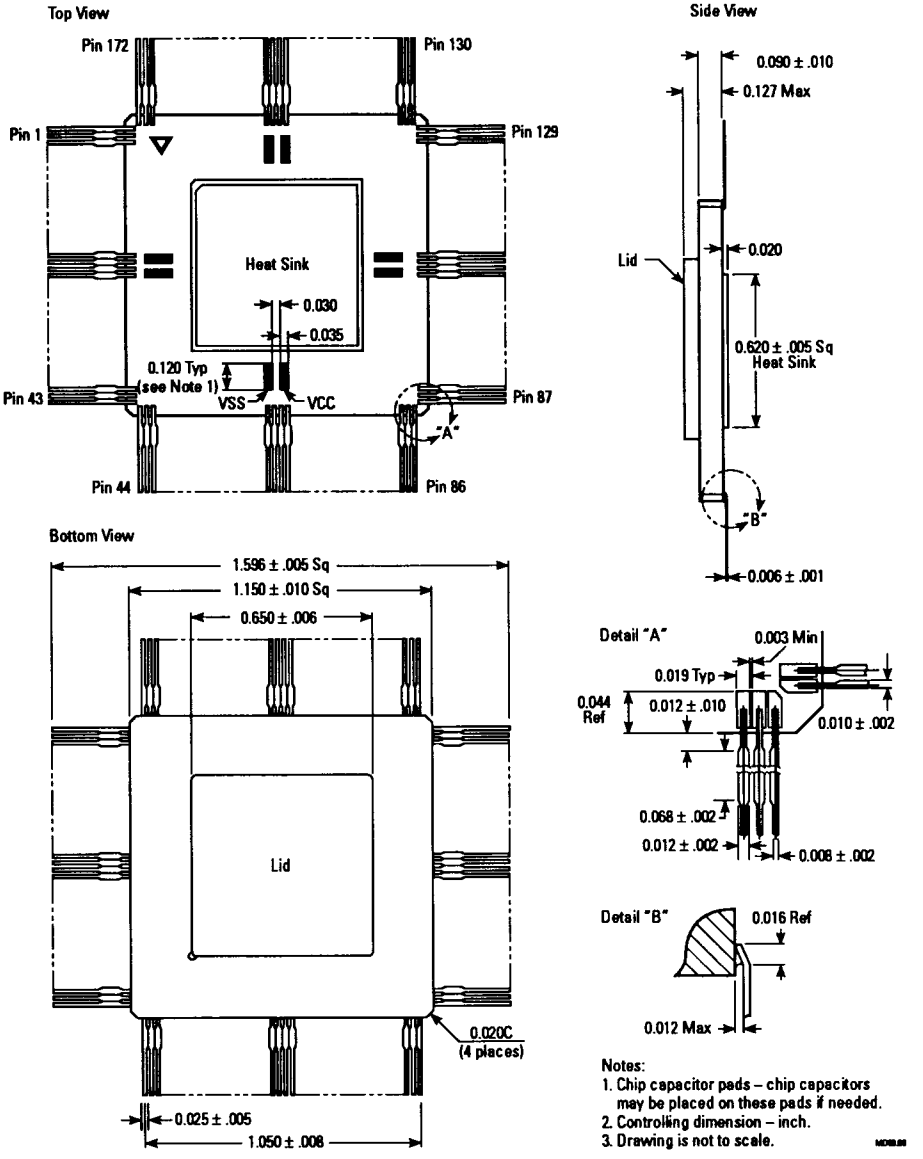


Figure 12.49 LR3000A Mechanical Drawing: 172-Pin Cavity-Down CLDCC

Ordering Information

Device Type	Frequency (MHz)	Pin Count and Package Type[1]	Temperature Range
LR3000LC-16	16.67	172-pin CLDCC	Commercial
LR3000GC-16	16.67	144-pin CPGA	Commercial
LR3000LM-16	16.67	172-pin CLDCC	Military
LR3000GM-16	16.67	144-pin CPGA	Military
LR3000LC-20	20	172-pin CLDCC	Commercial
LR3000GC-20	20	144-pin CPGA	Commercial
LR3000LC-25	25	172-pin CLDCC	Commercial
LR3000GC-25	25	144-pin CPGA	Commercial
LR3000AKM-20	20	172-pin CLDCC	Military
LR3000AHM-20	20	175-pin CPGA	Military
LR3000AKC-25	25	172-pin CLDCC	Commercial
LR3000AHC-25	25	175-pin CPGA	Commercial
LR3000AKM-25	25	172-pin CLDCC	Military
LR3000AHM-25	25	175-pin CPGA	Military
LR3000AKC-33	33.33	172-pin CLDCC	Commercial
LR3000AHC-33	33.33	175-pin CPGA	Commercial

Note:
(1) CLDCC = Ceramic LeaDed Chip Carrier; CPGA = Ceramic Pin Grid Array

Table 12.16 LR3000 Family Packages